FM01 Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA

**Session Type:** fringe Meeting  
**Date:** Monday, March 19, 2018  
**Time:** 18:00-21:00  
**Location / Room:** Saal 1

Organiser  
Cecilia Metra, University of Bologna, IT (Contact Cecilia Metra [1])

All registered conference delegates and exhibition visitors are kindly invited to join the DATE 2018 Welcome Reception & subsequent PhD Forum, which will take place on Monday, March 19, 2018, from 1800 - 2100 in “Saal 1” of the ICC Dresden.

The PhD Forum of the DATE Conference is a poster session and a buffet style dinner hosted by the European Design Automation Association (EDAA), the ACM Special Interest Group on Design Automation (SIGDA), and the IEEE Council on Electronic Design Automation (CEDA). The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work.

**Agenda**

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| 18:00 | FM01 | Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA  
Chair: Cecilia Metra, Università di Bologna, IT, Contact Cecilia Metra [1] |
| 18:00 | FM01 | An Optimization-Based Methodology for the Exploration of Cyber-Physical System Architectures  
1 Dmirti Kirov, University of Trento, IT |
| 18:00 | FM01 | Resilient Energy-Constrained Microprocessor Architectures  
2 Anteneh Gebregziorgis and Mehdi Tahoori, Karlsruhe Institute of Technology, DE |
| 18:00 | FM01 | Verified Model Refactorings for Hybrid Control Systems  
3 Sebastian Schlesinger, Technische Universität Berlin, DE |
| 18:00 | FM01 | Exact Design of Digital Microfluidic Biochips  
4 Oliver Keszeoo, University of Bremen, DE |
Nowadays, complicated devices comprising analog, digital and communications aspects are largely used in safety-critical domains, such as automotive, aerospace, health-care, industry and railway. Functional safety assessment of such devices and ensuring their dependability are becoming sophisticated and technical tasks. An effective and reliable approach which allows achieving the desired safety integrity level is needed, primarily to reduce time-to-market. The objective of this thesis is a novel methodology for the functional safety assessment for heterogeneous systems, namely Cyber-Physical Systems. The flowsheets from a mixed platform comprising digital and analog models. Automation manipulation steps transform it into an efficient homogeneous system-level description and also injects state-of-art and user-defined fault models. Then, the homogeneous description is integrated into a network infrastructure, and the communication aspects are subject to fault injection. Finally, the entire platform is used to perform an extensive fault countermeasure to evaluate different fault metrics. The proposed approach has been implemented and applied to a complete case study to evaluate its performance.

Many applications, such as image signal processing, have an inherent tolerance for insignificant inaccuracies. Adders and Multipliers are key arithmetic functions for many error-tolerant applications. Approximate computing reconsiders an efficient technique to trade off energy relative to performance and accuracy. Firstly, I proposed an approximate tree compressor (ATC) for multipliers. The proposed compressor halves the height of the partial product tree and generates a vector to recover accuracy. I also proposed a Carry-Maskable Adder (CMA). The proposed adder whose accuracy can be configured at runtime. To the best of our knowledge, this is the first work that achieves accuracy-configurable adder without multiplexers whittle select and accurate sum. Then I proposed a low-power high-speed accuracy-controllable approximations multiplier by employing the ATC and the CMA. Compared with a conventional Wallace tree multiplier, the proposed multiplier reduced power consumption by 47.3% and 56.2% and critical path delay by between 29.9% and 60.5% depending on the required accuracy. Its silicon area was also 44.6% smaller. In addition, results from an image processing application demonstrate that the quality of the processed images can be controlled by the proposed multiplier design.

The existing tools like Matlab and labview are working at algorithmic level. Then they are powerful enough to evaluate the functionality of a system and the performance. Making the gap narrow between the tools working at high-level of abstraction and the tools working at transistor level of abstraction is a novel idea to make the design exploration easier for the system designers without the need to go deep into the hardware details which is a time consuming process. As demonstrated the optimization at algorithmic level is the more efficient and practical way to achieve a maximum power efficient communication system.
Early Evaluation of Multicore Systems Soft Error Reliability Using Virtual Platforms
Felipe Rocha da Rosa, UFRGS, BR

The increasing computing capacity of multicore components like processors and graphics processing unit (GPUs) offer new opportunities for embedded and high-performance computing (HPC) domains. The progressively growing computing capacity of multicore-based systems enables to efficiently perform complex application workloads at a lower power consumption compared to traditional single-core solutions. Such efficiency and the ever-increasing complexity of application workloads encourage industry to integrate more and more computing components into the same system. The number of computing components employed in large-scale HPC systems already exceeds a million cores, while 1000 cores on-chip platforms are available in the embedded community. Beyond the massive number of cores, the increasing computing capacity, as well as the number of internal memory cells (e.g., registers, internal memory) inherent to emerging processor architectures, is making large-scale systems more vulnerable to both hard and soft errors. Moreover, to meet emerging performance and power requirements, the underlying processors usually run aggressive clock frequencies and multiple voltage domains, increasing their susceptibility to soft errors, such as the ones caused by radiation effects. The occurrence of soft errors or Single Event Effects (SEEs) may cause critical failures on system behavior, which may lead to financial or human life losses. While a rate of 280 soft errors per day has been observed during the flight of a spacecraft, electronic computing systems working at ground level are expected to experience at least one soft error per day in the near future. The increased susceptibility of multicore systems to SEEs necessitates the development of novel cost-effective tools to assess the soft error resilience of underlying multicore components with complex software stacks (operating system, drivers) early in the design phase. The primary goal addressed by this Thesis is to describe the proposal and development of a fault injection framework using a state-of-the-art virtual platform, propose novel fault injection techniques to direct the fault injection campaigns according to the software stack characteristics, and an extensive framework validation with over a million of simulation hours. The second goal of this Thesis (ongoing and future work) is to set the foundations for a new discipline in soft error reliability management for emerging manycore systems. It will identify and propose techniques that can be reused to provide different levels of reliability on the application workload and architecture level. Third and future work include software and hardware self-awareness and mitigation systems.

Spintronic memory towards Secure and Energy-Efficient Computing
Anirudh Iyengar and Swaroop Ghosh, Pennsylvania State University, US

With the advent of Internet-of-Things (IoTs), two important challenges namely: security and energy efficiency are of critical importance. Emerging memory technologies such as spintronic memory, have the potential to address both these issues. In this work, we explore low-leakage and high-entropy characteristics of spintronic memory, i.e., Domain Wall Memory (DWM) and Spin Transfer Torque-RAM (STT-RAM) for energy-efficient computing and hardware security. We propose two flavors of Physically Unclonable Functions (PUFs) using DWM and also provide solutions to address data privacy issues in STT-RAM caches. Apart from this, we have investigated various circuit and architecture-level solutions to improve robustness and reliability of STT-RAM. Additionally, two flavors of state-retentive flip-flops with an instant-ON capability have been realized using a MTJ-based solution.

Energy-Efficient and Reliable Computing in Dark Silicon Era
Mohammad-Hashem Haghbayan, University of Turku, FI

The submission contains a abstract regarding my PhD thesis. The following is an overview of this manuscript: Dark silicon denotes the phenomenon that, due to thermal and power constraints, the fraction of transistors that can operate at full frequency is decreasing in each technology generation. Furthermore, from another perspective, by increasing the number of transistors on the area of a single chip and susceptibility to internal defects alongside aging phenomena, which also is exacerbated by high chip thermal density, monitoring and managing the chip reliability before and after its activation is becoming a necessity. The proposed approaches and experimental investigations in this thesis focus on two main tracks: 1) power awareness and 2) reliability awareness in dark silicon, where later these two tracks will combine together.

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