FM01 Welcome Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA

Agenda

Time	Label	Session
18:00	FM01	**Reception & PhD Forum, hosted by EDAA, ACM SIGDA, and IEEE CEDA** **Chair:** Cecilia Metra, Università di Bologna, IT
18:00	FM01-1	**An Optimization-Based Methodology for the Exploration of Cyber-Physical System Architectures** Dmitrii Kirov, University of Trento, IT In this thesis, we address the design space exploration of cyber-physicalsystem architectures to select correct-by-construction configuration andinterconnection of system components taken from pre-defined libraries. Weformulate the exploration problem as a mapping problem and use optimization tosolve it by searching for a minimum cost architecture that meets systemrequirements. Using a graph-based representation of a system architecture, wedefine a set of generic mixed integer linear constraints over graph vertices,edges and paths, and use these constraints to instantiate a variety of designrequirements (e.g., interconnection, flow, workload, timing, reliability,routing). We implement a comprehensive toolbox that supports all steps of theproposed methodology. It provides a pattern-based formal language to facilitaterequirements specification and a set of scalable algorithms for encoding andsolving exploration problems. We prove our concepts on a set of case studiesfor different cyber-physical system domains, such as electrical powerdistribution networks, reconfigurable industrial production lines and wirelesssensor networks.
18:00	FM01-2	**Resilient Energy-Constrained Microprocessor Architectures** Anteneh Gebregiorgis and Mehdi Tahoori, Karlsruhe Institute of Technology, DE The goal of this thesis is to improve the resiliency and energy-efficiency ofenergy-constrained pipelined microprocessors by using cost effectivecross-layer solutions. This thesis presents different architectural levelsolutions for logic and memory components of a processor addressing the threemain NTC challenges, namely, increase in vulnerability to parametric variation,higher memory failure rate and performance uncertainties. Additionally, thisthesis demonstrates how to exploit emerging computing paradigms such asapproximate computing to improve the energy-efficiency of NTC designs.
18:00	FM01-3	**Verified Model Refactorings for Hybrid Control Systems** Sebastian Schlesinger, Technische Universität Berlin, DE I am Sebastian Schlesinger, PhD student in the team of Sabine Glesner,department Software and Embedded Systems Engineering, Technische UniversitätBerlin. I am in the final stage of my PhD Thesis. I plan to finish it by end ofthis year. I have uploaded one pdf containing two papers: 1) the extended abstract for myPhD Thesis at the top of the file, and 2) a published paper from the CyPhyWorkshop (http://2016.cyphy.org [1]). The paper is also publicly available at https://link.springer.com/chapter/10.1007/978-3-319-51738-4_6My [2] profile containing all information regarding my team and publication recordis available at http://www.sese.tu-berlin.de/menue/organization/team/sebastian_schlesing... [3] meter/en/The problem statement of my thesis, also to be found in the extended abstract,is as follows: The ever growing complexity in modern embedded systems requires to incorporateincreasingly many functions into a single system. Model Driven Engineering(MDE) is a well-established technique for the development of such complexembedded systems. Refactoring is a common technique to reduce the complexityand establish compliance with industrial MDE guidelines via modeltransformations. However,model refactorings are often performed manually or partially automatically viatools without guarantee of correctness. Such refactorings therefore bear therisk of introducing unwanted or even erroneous behaviour. This is critical,especially in safety-critical applications, where an error may cause enormouscosts or even endanger human lifes. To overcome this problem, I present anapproach to guarantee behavioural equivalence of graph-based hybrid controlsystems.
18:00	FM01-4	**Exact Design of Digital Microfluidic Biochips** Oliver Keszocze, University of Bremen, DE Many biological or medical experiments today are conducted manually by highly trained experts, usually requiring a large laboratory and a lot of equipment. Therefore, these experiments are expensive, do not allow for a high throughput,and are error-prone, due to humans being involved.Digital Microfluidic Biochips (DMFBs) promise to automate and miniaturize the equipment while, at the same time, reducing the consumption of materials and increasing the throughput.The thesis deals with the design problem for digital microfluidic biochips witha special focus on minimal solutions. For this, optimal solutions for individual steps in the design flow for DMFBs are developed. As even optimal solutions to these steps do not guarantee an optimal overall solutions, a holistic one-pass solution is presented that combines all individual design steps in a single approach.
18:00	FM01-5	**A Functional Safety Approach for Cyber-Physical Systems** Enrico Fraccaroli, Università degli Studi di Verona, IT Nowadays, complicated devices comprising analog, digital and communicationaspects are largely used in safety-critical domains, such as automotive,aerospace, health-care, industry and railway. Functional safety assessment ofsuch devices and ensuring their dependability are becoming sophisticated andcritical tasks. An effective and reliable approach which allows achieving thedesired safety integrity level is needed, primarily to reduce time-to-market.The objective of this thesis is a novel methodology for the functional safetyassessment for heterogeneous systems, namely Cyber-Physical Systems. The flowstarts from a mixed platform comprising digital and analog models. Automaticmanipulation steps transform it into an efficient homogeneous system-leveldescription and also injects state-of-art and user-defined fault models. Then,the homogeneous description is integrated into a network infrastructure, andthe communication aspects are subject to fault injection.Finally, the entire platform is used to perform an extensive fault champaignand to evaluate different fault metrics. The proposed approach has beenimplemented and applied to a complete case study to evaluate its performances.
18:00	FM01-6	**Research on Accuracy-Configurable Architecture for Applications and Systems** Tongxin Yang, Fukuoka University, JP Many applications, such as image signal processing, has an inherent tolerancefor insignificant inaccuracies. Adders and Multipliers are key arithmeticfunctions for many error-tolerant applications. Approximate computing isconsidered an efficient technique to trade off energy relative to performanceand accuracy.Firstly, I proposed an approximate tree compressor (ATC) for multipliers. Theproposed compressor halves the height of the partial product tree and generatesa vector to recover accuracy.I also proposed a Carry-Maskable Adder (CMA). The proposed adder whose accuracycan be configured at runtime. To the best of our knowledge, this is the firstwork that achieves accuracy-configurable adder without multiplexers whichselect approximate and accurate sums. Then I proposed a low-power high-speed accuracy-controllable approximatemultiplier by employing the ATC and the CMA. Compared with a conventionalWallace tree multiplier, the proposed multiplier reduced power consumption bybetween 47.3% and 56.2% and critical path delay by between 29.9% and 60.5%,depending on the required accuracy. Its silicon area was also 44.6% smaller. Inaddition, results from an image processing application demonstrate that thequality of the processed images can be controlled by the proposed multiplierdesign.

18:00 FM01-7 **Social Insect-inspired Adaptive Hardware Systems**
Matthew Rowlings, Andy Tyrrell and Martin Albrecht Trefzer, University of York, GB

Please find attached my extended abstract describing my PhD reasearch forsumission to the DATE PhD forum. Also attached is a paper I have had publishedin the proceedings for the IEEE CEC 2016 conference, DOI:10.1109/CEC.2016.7743887.RegardsMatthew Rowlingsmr589 🏛 york [dot] ac [dot] uk

18:00 FM01-8 **Power Modeling for Fast Power Estimation on FPGA**
Yehya Nasser, Jean-Christophe Prevotet and Maryline Helard, Institut national des sciences appliquées de Rennes (INSA) Rennes-IETR, FR

The existing tools like Matlab and labview are working at algorithmic level,then they are powerful enough to evaluate the functionality of a system thenthe performance. Making the gap narrower between the tools working athigh-level of abstraction and the tools working at transistors level toevaluate the power consumption is a novel idea to make the design explorationeasier for the system designers without the need to go deep into the hardwaredetailswhich is a time consuming processes. As demonstrated the optimization atalgorithmic level is the more efficient and practical way to achieve a maximumpower efficient communication systems.

18:00 FM01-9 **Machine Learning Approaches for Hardware Reliability Modelling and Mitigation**
Arunkumar Vijayan and Mehdi Tahoori, Karlsruhe Institute of Technology, DE

With technology scaling advancement, a host of vulnerabilitiesaffect resiliency of VLSI circuits. Each chip is born with a uniquepersonality due to process variations and grows uniquely due tooperating conditions, workload and environment. Hence, design-timesolutions and guard-bands for resilience and reliability, based ondeterministic models, are no longer sufficient for integrated circuits(ICs) fabricated at nanoscale technology nodes. There is a need forruntime analysis of the state of a system and adoption of appropriatemitigation actions to ensure resiliency.Moreover, the complexity of reliability issues makes simple resiliencymodelling and mitigation very complicated and inefficient.This complexity arises from various sources spanning from technol-ogy, device, circuit and architecture design and fabrication parameterson the one hand and the runtime workload and environment on theother hand. This is the motivation to explore machine learning andruntime methods to deal with such complexities.Modern systems incorporate a range of sensors and monitors(e.g., razor flip-flops, critical path monitors (CPM)) to trackthe impact of several reliability mechanisms on the functionality andperformance of a circuit. These reliability mechanisms include agingdue to Bias Temperature Instability (BTI), supply voltage fluctuationsetc. In addition, additional hardware is added in the form of redundantunits or error correction units in order to tackle the impact of radiation-induced soft errors. With these sensor data available online,suitable adaptation policies can be triggered on-the-fly that can help inresilient operation of a system. However, the fundamental problem ofthe above method lies in the fact that these sensors monitor the effect(e.g., path delay increase due to BTI) of a reliability phenomenonrather than its cause (nature of workload). Hence, the adaptationpolicies can only be triggered after a measurable degradation occurson the circuit.Thesis Objective: The objective of this thesis is to enable runtimepredictions on different reliability mechanisms by exploiting machinelearning techniques for workload compaction and representation.Different learning methods are used to identify low cost workloadobservables and to build prediction models that correlate the workloadobservables with reliability metrics.In this thesis, we devise machine learning techniques to model,monitor and mitigate various reliability effects spanning from imperfections indevice fabrication, design issues, and impact of runtimeworkload and environment. We target early runtime prediction ofthe impact of a workload phase on resilient operation of a circuit.This information about the impact of a workload phase can guideproper mitigation actions proactively such as relaxation of aging stressor tackling vulnerability of a circuit to soft errors. In this regard,these learning techniques can be used to correlate workload patternsto corresponding impact on system reliability under aging and softerrors. We propose a methodology to monitor hardware units onlineand predict reliability metric values on-the-fly based on predictionmodels constructed offline. Our technique involvesworkload analysis to extract hidden information that reveals relationship withreliability and vulnerability metrics such as architecturalvulnerability factor and circuit path delay increase. The workloaddata is analyzed in the logic level to maximize the informationcontent. However, this increases the complexity of analysis and hence,we deploy domain-specific feature selection and feature engineeringtechniques to capture important features of a workload segment. Inthis regard, suitable workload observables are identified offline usingcorrelation analysis and feature elimination techniques. A predictionmodel is built offline to correlate the workload observable with thereliability metric under consideration. Low cost hardware monitors areproposed to track the workload observables online and the monitoringinformation is fed to software predictors to make early predictions onthe reliability metric.

18:00 FM01-10 **Multi-formalism in Different Levels of Abstraction for Requirements Engineering and Design of Real-Time Systems**
Fabiola Ribeiro[1], Achim Rettberg[2], Carlos E. Pereira[3] and Michel dos Santos Soares[4]
[1]Universidade Federal de Uberlandia, BR; [2]Carl von Ossietzky Universität Oldenburg, DE; [3]Universidade Federal do Rio Grande do Sul, BR; [4]Federal University of Sergipe, BR

This research presents a new methodology which is grounded in the well-recognized profiles SysML and MARTE to the RTES development. Themethodology details a set of guidelines and a standardized process to theRequirement Engineering, System Design and Architectural Views in the RTESdomain through the SysML and MARTE profile adoption. The proposed methodology supports the requirements analysis, specification anddocumentation of requirements, requirements consistency check, and alsocontributes to the architectural system definition. The present research has been applied in the requirement engineering andarchitectural design study case in the real-time and embedded control systemsdomain. SysML and MARTE compose a modelling proposal which is suitable to therepresentation of functional and non-functional requirements that allows tostrengthen the activities of specification, analysis and design of systems.As contributions of this research, it can be highlighted the elaboration of amethodology able to represent not only software, but also the hardwarecomponents and their embedded controls. Furthermore, it can be also stressedthe description of a fairly simple methodology for analysis, specification andmodelling of complex systems at different levels of abstraction. Thus, systemdesigners do not need to have knowledge of different modelling tools for theRequirements Specification process. Finally, this methodology uses specificdiagrams which are suitable to requirements and design description that areenriched with stereotypes of MARTE, a profile known for the purpose ofmodelling real-time and embedded systems. In this context, our approach canimprove the description and understanding of the system by allowing the use ofdifferent abstraction levels in a specification and design process.

18:00 FM01-11 **Early Evaluation of Multicore Systems Soft Error Reliability Using Virtual Platforms**
Felipe Rocha da Rosa, UFRGS, BR

The increasing computing capacity of multicore components like processors andgraphics processing unit (GPUs) offer new opportunities for embedded andhighhyp{}performance computing (HPC) domains. The progressively growingcomputing capacity of multicore-based systems enables to efficiently performcomplex application workloads at a lower power consumption compared totraditional single-core solutions. Such efficiency and the ever-increasingcomplexity of application workloads encourage industry to integrate more andmore computing components into the same system. The number of computingcomponents employed in large-scale HPC systems already exceeds a million cores,while 1000-cores on-chip platforms are available in the embedded community.Beyond the massive number of cores, the increasing computing capacity, as wellas the number of internal memory cells (e.g., registers, internal memory)inherent to emerging processor architectures, is making large-scale systemsmore vulnerable to both hard and soft errors. Moreover, to meet emergingperformance and power requirements, the underlying processors usually run inaggressive clock frequencies and multiple voltage domains, increasing theirsusceptibility to soft errors, such as the ones caused by radiation effects.The occurrence of soft errors or Single Event Effects (SEEs) may cause criticalfailures on system behavior, which may lead to financial or human life losses.While a rate of 280 soft errors per day has been observed during the flight ofa spacecraft, electronic computing systems working at ground level are expectedto experience at least one soft error per day in near future. The increasedsusceptibility of multicore systems to SEEs necessarily calls for novelcost-effective tools to assess the soft error resilience of underlyingmulticore components with complex software stacks (operating system-OS,drivers) early in the design phase.The primary goal addressed by this Thesis is to describe the proposal anddevelopment of a fault injection framework using a state-of-the-art virtualplatform, propose set of novel fault injection techniques to direct the faultcampaigns according to with the software stack characteristics, and anextensive framework validation with over a million of simulation hours. Thesecond goal of this Thesis (ongoing and future work) is to set the foundationsfor a new discipline in soft error reliability management for emergingmulti/manycore systems. It will identify and propose techniques that can beused to provide different levels of reliability on the application workload andcriticality. Third and future work include software and hardware self-awaremitigation system.

18:00 FM01-12 **Spintronic memory towards Secure and Energy-Efficient Computing**
Anirudh Iyengar and Swaroop Ghosh, Pennsylvania State University, US

With the advent of Internet-of-Things (IoTs) two important challenges namely:security and energy efficiency are of critical importance. Emerging memorytechnologies such as spintronic memory, have the potential to address boththese issues. In this work we exploit low-leakage and high-entropycharacteristics of spintronic memory i.e. Domain Wall Memory (DWM) and SpinTransfer Torque-RAM (STT-RAM) for energy efficient computing and hardwaresecurity. We propose two flavors of Physically Unclonable Functions (PUFs)using DWM and also provide solutions to address data privacy issues in STTRAMcaches. Apart from this, we have investigated various circuit and architecturelevel solutions to improve robustness and reliability of STTRAM. Additionally,two flavors of state retentive flip flops with an instant-ON (ION) capabilityhave been realized using a MTJ-based solution.

18:00 FM01-13 **Energy-Efficient and Reliable Computing in Dark Silicon Era**
Mohammad-Hashem Haghbayan, University of Turku, FI

The submission contains a abstract regarding my PhD thesis. The following is anoverview of this manuscript: Dark silicon denotes the phenomenon that, due to thermal and power constraints,the fraction of transistors that can operate at full frequency is decreasing ineach technology generation. Furthermore, from another perspective, byincreasing the number of transistors on the area of a single chip andsusceptibility to internal defects alongside aging phenomena, which also isexacerbated by high chip thermal density, monitoring and managing the chipreliability before and after its activation is becoming a necessity. Theproposed approaches and experimental investigations in this thesis focus on twomain tracks: 1) power awareness and 2) reliability awareness in dark siliconera, where later these two tracks will combine together.

Links:
[1] http://2016.cyphy.org
[2] https://link.springer.com/chapter/10.1007/978-3-319-51738-4_6My
[3] http://www.sese.tu-berlin.de/menue/organization/team/sebastian_schlesinger/para