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## UB09 Session 9

**Date:** Thursday 28 March 2019

**Time:** 10:00 - 12:00

**Location / Room:**

Label	Presentation Title Authors
UB09.1	<b>TINYWIDS: A INTRUSION DETECTION SYSTEM FOR WIRELESS SENSOR NETWORKS</b> <b>Authors:</b> Walter Tiberti <sup>1</sup> and Luigi Pomante <sup>2</sup> <sup>1</sup> University of L'Aquila, IT; <sup>2</sup> DEWS, IT <b>Abstract</b> <i>In the domain of Wireless Sensor Networks (WSN), providing an effective security solution to protect the motes and their communications is challenging. Due to the hard constraints on performance, storage and energy consumption, normal network-security related techniques cannot be applied. Focusing on the "Intrusion Detection" problem, we propose a real-world application of our WSN Intrusion Detection System (WIDS). WIDS exploits the Weak Process Models to classify potential security issues in the WSN and to notify the operators when an attack tentative is detected. In this demonstration, we show how our IDS works, how it detects some basic attacks and how the IDS can evolve to fulfill the needs of secure WSN deployments.</i> <a href="#">Download Paper (PDF)</a>
UB09.2	<b>RESCUE: EDA TOOLSET FOR INTERDEPENDENT ASPECTS OF RELIABILITY, SECURITY AND QUALITY IN NANO-ELECTRONIC SYSTEMS DESIGN</b> <b>Authors:</b> Cemil Cem Gürsoy <sup>1</sup> , Guilherme Cardoso Medeiros <sup>2</sup> , Junchao Chen <sup>3</sup> , Nevin George <sup>4</sup> , Josie Esteban Rodriguez Condia <sup>5</sup> , Thomas Lange <sup>6</sup> , Aleksa Damjanovic <sup>5</sup> , Raphael Segabinazzi Ferreira <sup>4</sup> , Aneesh Balakrishnan <sup>6</sup> , Xinhui Anna Lai <sup>1</sup> , Shayesteh Masoumian <sup>7</sup> , Dmytro Petryk <sup>3</sup> , Troya Cagil Koylu <sup>2</sup> , Felipe Augusto da Silva <sup>8</sup> , Ahmet Cagri Bagbaba <sup>8</sup> and Maksim Jenihhin <sup>1</sup> <sup>1</sup> Tallinn University of Technology, EE; <sup>2</sup> Delft University of Technology, NL; <sup>3</sup> IHP, DE; <sup>4</sup> BTU Cottbus-Senftenberg, DE; <sup>5</sup> Politecnico di Torino, IT; <sup>6</sup> IROC Technologies, FR; <sup>7</sup> Intrinsic ID B.V., NL; <sup>8</sup> Cadence Design Systems GmbH, DE <b>Abstract</b> <i>The demonstrator will introduce an EDA toolset developed by a team of PhD students in the H2020-MSCA-ITN RESCUE project. The recent trends for the computing systems include machine intelligence in the era of IoT, complex safety-critical applications, extreme miniaturization of technologies and intensive interaction with the physical world. These trends set tough requirements on mutually dependent extra-functional design aspects. RESCUE is focused on the key challenges for reliability (functional safety, ageing, soft errors), security (tamper-resistance, PUF technology, intelligent security) and quality (novel fault models, functional test, FMEA/FMECA, verification/debug) and related EDA methodologies. The objective of the interdisciplinary cross-sectoral team from Tallinn UT, TU Delft, BTU Cottbus, POLITO, IHP, IROC, Intrinsic-ID, Cadence and Bosch is to develop in collaboration a holistic EDA toolset for modelling, assessment and enhancement of these extra-functional design aspects.</i> <a href="#">Download Paper (PDF)</a>
UB09.3	<b>ASAM: AUTOMATIC SYNTHESIS OF ALGORITHMS ON MULTI CHIP/FPGA WITH COMMUNICATION CONSTRAINTS</b> <b>Authors:</b> Amir Masoud Gharehbaghi, Tomohiro Maruoka, Yukio Miyasaka, Akihiro Goda, Amir Masoud Gharehbaghi and Masahiro Fujita, The University of Tokyo, JP <b>Abstract</b> <i>Mapping of large systems/computations on multiple chips/multiple cores needs sophisticated compilation methods. In this demonstration, we present our compiler tools for multi-chip and multi-core systems that considers communication architecture and the related constraints for optimal mapping. Specifically, we demonstrate compilation methods for multi-chip connected with ring topology, and multi-core connected with mesh topology, assuming fine-grained reconfigurable cores, as well as generalization techniques for large problems size as convolutional neural networks. We will demonstrate our mappings methods starting from data-flow graphs (DFGs) and equations, specifically with applications to convolutional neural networks (CNNs) for convolution layers as well as fully connected layers.</i> <a href="#">Download Paper (PDF)</a>
UB09.4	<b>HEPSYCODE-MC: ELECTRONIC SYSTEM-LEVEL METHODOLOGY FOR HW/SW CO-DESIGN OF MIXED-CRITICALITY EMBEDDED SYSTEMS</b> <b>Authors:</b> Luigi Pomante <sup>1</sup> , Vittorio Muttillio <sup>1</sup> , Marco Santic <sup>1</sup> and Emilio Incerto <sup>2</sup> <sup>1</sup> Università degli Studi dell'Aquila - DEWS, IT; <sup>2</sup> IMT Lucca, IT <b>Abstract</b> <i>Heterogeneous parallel architectures have been recently exploited for a wide range of embedded application domains. Embedded systems based on such kind of architectures can include different processor cores, memories, dedicated ICs and a set of connections among them. Moreover, especially in automotive and aerospace application domains, they are even more subjected to mixed-criticality constraints. So, this demo addresses the problem of the ESL HW/SW co-design of mixed-criticality embedded systems that exploit hypervisor (HPV) technologies. In particular, it shows an enhanced CSP/SystemC-based design space exploration step, in the context of an existing HW/SW co-design flow that, given the system specification is able to (semi)automatically propose to the designer: - a custom heterogeneous parallel HPV-based architecture; - an HW/SW partitioning of the application; - a mapping of the partitioned entities onto the proposed architecture.</i> <a href="#">Download Paper (PDF)</a>
UB09.5	<b>CS: CRAZYSQUARE</b> <b>Authors:</b> Federica Caruso <sup>1</sup> , Federica Caruso <sup>1</sup> , Tania Di Mascio <sup>1</sup> , Alessandro D'Errico <sup>1</sup> , Marco Pennese <sup>2</sup> , Luigi Pomante <sup>1</sup> , Claudia Rinaldi <sup>1</sup> and Marco Santic <sup>1</sup> <sup>1</sup> University of L'Aquila, IT; <sup>2</sup> Ministry of Education, IT <b>Abstract</b> <i>CrazySquare (CS) is an adaptive learning system, developed as a serious game for music education, specifically indicated for young teenager approaching music for the first time. CS is based on recent educative directions which consist of using a more direct approach to sound instead of the musical notation alone. It has been inspired by a paper-based procedure that is currently used in an Italian middle school. CS represents a support for such teachers who prefer involving their students in a playful dimension of learning rhythmic notation and pitch, and, at the same time, teaching playing a musical instrument. To reach such goals in a cost-effective way, CS fully exploits all the recent advances in the EDA domain. In fact, it is based on a framework composed of mobile applications that will be integrated with augmented reality HW/SW tools to provide virtual/augmented musical instruments. The proposed demo will show the main features of the current CS framework implementation.</i> <a href="#">Download Paper (PDF)</a>

- UB09.6 **LABSMILING: A SAAS FRAMEWORK, COMPOSED OF A NUMBER OF REMOTELY ACCESSIBLE TESTBEDS AND RELATED SW TOOLS, FOR ANALYSIS, DESIGN AND MANAGEMENT OF LOW DATA-RATE WIRELESS PERSONAL AREA NETWORKS BASED ON IEEE 802.15.4**  
**Authors:**  
Carlo Centofanti, Luigi Pomante, Marco Santic and Walter Tiberti, University of L'Aquila, IT  
**Abstract**  
*Low data-rate wireless personal area networks (LR-WPANs) are constantly increasing their presence in the fields of IoT, wearable, home automation, health monitoring. The development, deployment and testing of SW based on IEEE 802.15.4 standard (and derivations, e.g. 15.4e), require the exploitation of a testbed as the network grows in complexity and heterogeneity. This demo shows LabSmiling: a SaaS framework which connects testbeds deployed in a real-world-environment and the related SW tools that make available a meaningful (but still scalable) number of physical devices (sensor nodes) to developers. It provides a comfortable out-of-the-box service designed to fulfill developer needs giving them full control on single motes (program, reset, physical power on/off, up/down links, commands/messages/packets in/from the network). Advanced services are: full-customizable testing scenario, validation/testing protocol compliances/extensions, run low level packet sniffers with QoS metrics.*  
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- UB09.7 **SETA-RAY: A NEW IDE TOOL FOR PREDICTING, ANALYZING AND MITIGATING RADIATION-INDUCED SOFT ERRORS ON FPGAS**  
**Authors:**  
Luca Sterpone, Boyang Du and Sarah Azimi, Politecnico di Torino, IT  
**Abstract**  
*One of the main concern for FPGA adopted in mission critical application such as space and avionic fields is radiation-induced soft errors. Therefore, we propose an IDE including two software tools compatible with commercial EDA tools. RAD-RAY as the first and only developed tool capable to predict the source of the SET phenomena by taking in to account the features of the radiation environment such as the type, LET and interaction angle of the particles, the material and physical layout of the device exposed to the radiation. The predicted source SET pulse is provided to the SETA tool as the second developed tool integrated with the commercial FPGA design tool for evaluating the sensitivity of the industrial circuit implemented on Flash-based FPGA and mitigate the original netlist based on the performed analysis. This IDE is supported by ESA and Thales Alenia Space. It has been applied to the EUCLID space mission project that will be launched in 2021.*  
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- UB09.8 **REQV: A TOOL FOR REQUIREMENTS FORMAL CONSISTENCY CHECKING**  
**Authors:**  
Luca Pulina<sup>1</sup>, Massimo Narizzano<sup>2</sup>, Armando Tacchella<sup>2</sup> and Simone Vuotto<sup>1</sup>  
<sup>1</sup>University of Sassari, IT; <sup>2</sup>University of Genoa, IT  
**Abstract**  
*In the demo we will present ReqV, a tool for requirements formal consistency checking developed in the context of the H2020 EU project CERBERO (<http://www.cerbero-h2020.eu/tools-and-tutorials/>). ReqV takes as input a set of requirements expressed in natural language, so it does not require any background knowledge of formal methods and logical languages. A video tutorial is currently available at [http://www.cluster-prossimo.it/docs/ReqV\\_video.mp4](http://www.cluster-prossimo.it/docs/ReqV_video.mp4). The basic technologies used in ReqV are an extension of Property Specification Patterns to constrained numerical signals -- which enables to write useful requirements specifications in the context of Cyber-Physical Systems -- and Linear Temporal Logic satisfiability solvers for the formal consistency checking part. In the case of inconsistency of the set of input requirements, ReqV can also extract the minimal set of conflicting requirements, in order to help the designer to correct a wrong specification.*  
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- UB09.9 **MECO: AN AUTONOMIC MANAGER FOR EDGE-COMPUTING PLATFORMS**  
**Authors:**  
Gabriella D'Andrea, Tania Di Mascio, Luigi Pomante and Giacomo Valente, University of L'Aquila, IT  
**Abstract**  
*In the Cyber-Physical-Systems word, the need for hardware platforms able to satisfy increasing requirements in computing performance, while keeping the adaptability imposed by the interactions with the physical world is leading on the use FPGAs, due to their inherent run-time reconfigurability. So, this demo presents an implementation of a self-adaptive loop for edge- computing devices targeting FPGAs. An adaptive run-time manager, together with a smart monitoring system, evaluates the quality of service and determines whether is convenient to perform a dynamic partial reconfiguration. The whole development flow, that exploits a library of elements to compose the monitoring system and then selects the appropriate manager, will be shown by means of a reference use case implemented on a Zynq Ultrascale+ SoC. Finally, a comparison among different functionalities will be illustrated as well.*  
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- UB09.10 **DESIGN SPACE EXPLORATION FRAMEWORKS FOR APPROXIMATE COMPUTING**  
**Authors:**  
Alberto Bosio<sup>1</sup>, Olivier Sentieys<sup>2</sup> and Daniel Ménard<sup>3</sup>  
<sup>1</sup>University of Lyon, FR; <sup>2</sup>University of Rennes, INRIA/IRISA, FR; <sup>3</sup>INSA Rennes - IETR, FR  
**Abstract**  
*Approximate Computing (AxC) investigates how to design energy efficient, faster, and less complex computing systems. Instead of performing exact computation and, consequently, requiring a high amount of resources, AxC aims to selectively relax the specifications, trading accuracy off for efficiency. The goal of this demonstrator, is to present a Design Space Exploration framework able to automatically explore the impact of different approximate operators on a given application accordingly to the required level of accuracy and the available HW architecture. The first demonstration relates to the word-length optimization of variables in a software or hardware system to explore cost (e.g., energy) and quality trade-off solution. The tool is scalable and targets both customized fixed-point and floating-point arithmetic. The second demonstration is about the use of other approximate techniques. The proposed demonstrator is linked with the DATE19 Monday tutorial M03.*  
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- 12:00 End of session

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