HEPSYCODE-MC

Electronic System-Level Methodology for
HW/SW Co-Design of Mixed-Criticality Embedded Systems

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Introduction

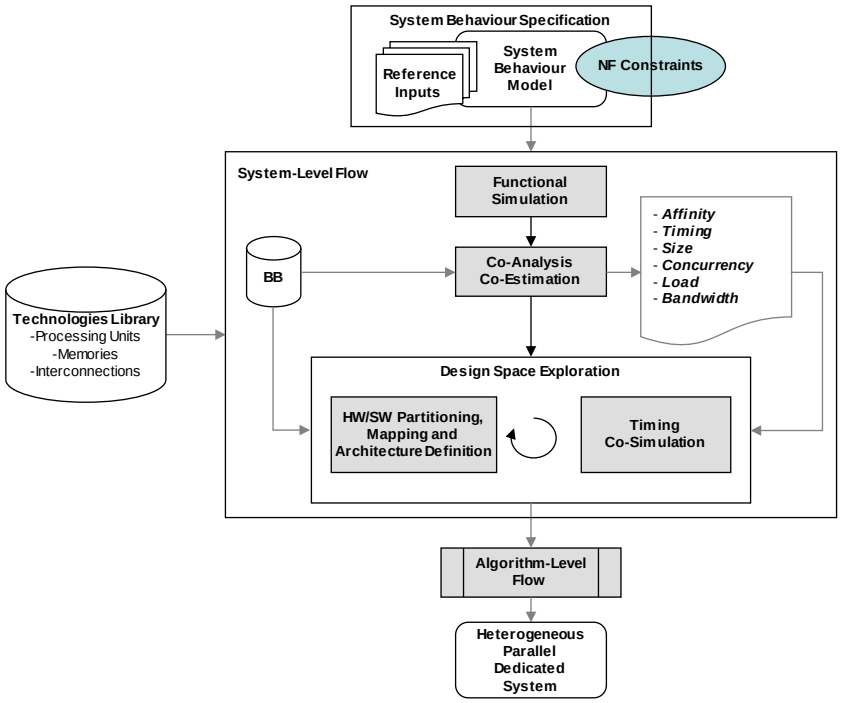
Heterogeneous parallel architectures have been recently exploited for a wide range of embedded application domains. Embedded systems based on such kind of architectures can include different processor cores, memories, dedicated ICs and a set of connections among them. Moreover, especially in automotive and aerospace application domains, they are even more subjected to mixed-criticality constraints.

Goals

The main goals of this demo are to describe the proposed *Electronic System-Level Methodology for HW/SW Co-Design of Mixed-Criticality Embedded Systems* and to show its application to some basic examples.

Demo description

So, this demo addresses the problem of the ESL HW/SW co-design of mixed-criticality embedded systems that exploit hypervisor (HPV) technologies. In particular, it shows an enhanced CSP/SystemC-based design space exploration step, in the context of an existing HW/SW co-design flow that, given the system specification is able to (semi)automatically propose to the designer:
- a custom heterogeneous parallel HPV-based architecture;
- an HW/SW partitioning of the application;
- a mapping of the partitioned entities onto the proposed architecture.



HEPSYCODE-MC HW/SW Co-Design Flow

The focus is on the tools that compose the DSE step:
- HW/SW Partitioning, Mapping and Architecture Definition
- HW/SW Timing Co-Simulation

Some basic examples will show the possible support to designers during the system development.

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