SETA-RAY: A New IDE tool for Predicting, Analyzing and Mitigating Radiation-induced Soft Errors on FPGAs

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***Abstract*—One of the main concern for FPGA adopted in mission critical application such as space and avionic fields is radiation-induced soft errors. Therefore, we propose an IDE including two software tools compatible with commercial EDA tools. Rad-Ray as the first and only developed tool capable to predict the source of the SET phenomena by taking in to account the features of the radiation environment such as the type, LET and interaction angle of the particles, the material and physical layout of the device exposed to the radiation. The predicted source SET pulse in provided to the SETA tool as the second developed tool integrated with the commercial FPGA design tool for evaluating the sensitivity of the industrial circuit implemented on Flash-based FPGA and mitigate the original netlist based on the performed analysis. This IDE is supported by ESA and Thales Alenia Space. It has been applied to the EUCLID space mission project that will be launched in 2021.**

Keywords—Radiation-effects, EDA tools, Linear Energy Transfer (LET), Flash-based FPGA.

I. INTRODUCTION

Nowadays digital circuits are going towards technology below 7nm and with 3DVLSI processes where gates can be implemented on multiple tiers by means of TSV process that were able to shorten the interconnections and increase the performances. However, 3D VLSI is an emerging technology process and in the near future, when face-2-back or face-2-face implementation process will be consolidated [1] the methods to calculate the sensitivity to soft-errors will need EDA tools able to manage the three-dimensional nanowires as well as ultra-thin gate layers. In this work, we propose SETA-RAY, a Single Event Transient Analyzer (SETA) EDA tool for Radiation particle rays (RAY). The tool is compatible with different commercial tool chains of FPGA manufacturers such as Microchip, Xilinx and Altera.

II. THE SETA-RAY TOOL

The SETA-RAY tool flow is illustrated in Figure 1. The tool elaborates a post-layout netlist and the physical design information generated by a commercial tool chain. Besides, it allows the elaboration of the netlist layout cells in the form of a GDS layout files. The tool simulates the effect of a highly charged particle traversing the silicon junction of the device. The produced free mobile carriers are concentrated within the depletion region of a p-n junction in the transistor sensitive parts individuated by the Rad-Ray algorithm. The eV transmitted by the particle, depending on the traversed section of the cell, can cause a voltage glitch that is propagated at the output of the transistor and finally, to the output of the affected cell generating a Single Event Transient (SET) effect into the circuit [2][3]. The generated SET pulse propagates through several paths of the implemented circuits, creating several SET pulses simulated by the SETA tool [4]. The propagated SETs may reach to multiple primary outputs of the circuit thus provoking a circuit functional interruption. The tool provides the feature to include different mitigation strategies ranging from Duplication With Comparison (DWC), Triple Modular Redundancy (TMR) and Guard-gate insertion (GG) [5].

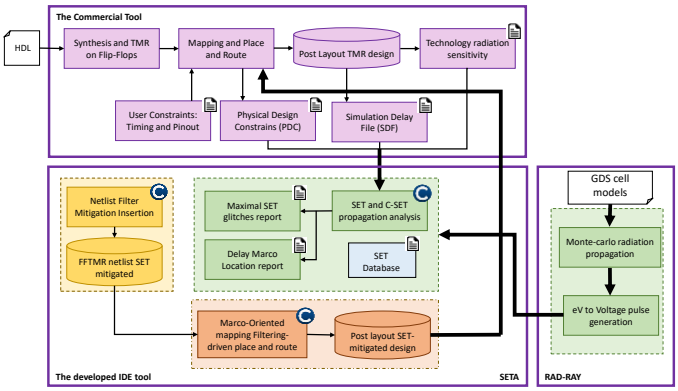
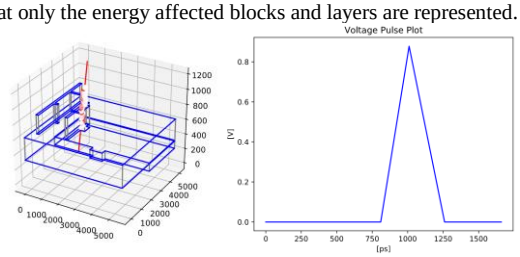


Fig. 1. A rendering of an Ion particle traversing a single SRAM cell (left), the linear plot of the voltage pulse generated by the particle trajectory. Please note that only the energy affected blocks and layers are represented.



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