Scheduled Poster Presentations

1. Agathoklis Papadopoulos (University of Cyprus, CY): Accelerating Bioinformatics and Biomedical Applications via Massively Parallel Reconfigurable Systems
4. Anup Das (National University of Singapore, SG): Design Methodology for Reliable and Energy Efficient Multicore Systems
5. Amaldo Cruz (Kyushu University, JP): Compiler optimization space exploration using machine learning techniques
7. Daniele Bertolotti (University of Bologna, I): A Process and Environmental Variation Tolerance Scheme for ULP Shared-memory Processor Cluster
9. Domitian Tamas-Selicean (Technical University of Denmark, DK): Design of Mixed-Critically Applications on Distributed Real-Time Systems
10. Emad Ebeid (University of Verona, I): Modeling and Synthesis of the Network in Distributed Embedded Systems
11. Fabian Oboiř (Karlsruhe Institute of Technology, D): Cross-Layer Approaches for Aging-Aware Design of Nanoscale Microprocessors
12. Fatemeh Negin Javaheri (TUM Lab, F): Designing from Assertions: from PSL Properties to a Compliant Hardware Prototype
13. Fazal Hameed (Karlsruhe Institute of Technology, D): DRAM Aware Last Level Cache Policies for Multi-Core Systems
15. Karthik Chandrasekhar (Delft University of Technology, NL): High-Level Power Estimation of DRAMs
16. Lars Middendorf (University of Rostock, D): Dynamic Task Mapping on Multi-Core Architectures using Stream Rewriting
17. Leonidas Kosmidis (Barcelona Supercomputing Center, ES): Enabling Caches in Probabilistic Timing Analysis
18. Luca Cassano (University of Pisa, I): Analysis and Test of the Effects of Single Event Upsets Affecting the Configuration Memory of SRAM-based FPGAs
19. Marco Indaco (Politecnico di Torino, I): Service Oriented Non Volatile Memories
20. Mathew Moreira (Pontifical Catholic University of Rio Grande do Sul, BR): Quasi-Delay-Insensitive Return-to-One Design
22. Milan Pavić (Barcelona Supercomputing Center, ES): Data Placement in HPC Architectures with Heterogeneous Off-chip Memory
23. Mira Salazar (Technical University of Denmark, DK): Compilation and Synthesis for Fault-Tolerant Digital Microfluidic Biochips
24. Miroslav Valla (University of Montpellier II, F): Power Aware Test and Test of Low Power Devices
25. Mohamed Barmakshama (Leiden University, NL): On Hard Real-Time Scheduling of Cyclo-Static Dataflow and its Application in System-Level Design
26. Namita Sharma (Indian Institute of Technology Delhi, IN): Data Memory Optimizations for SPM based Baseband Processor Architectures
27. Nikita Rapojev (Barcelona Supercomputing Center, ES): High Performance Computing with Mobile SoCs: Opportunities and Challenges
28. Norica Montallegro (Heinz Nixdorf Institute, Paderborn, D): Immuno-repating of Hardware Systems
29. Ogun Turkylmaz (CEA-LETI, Grenoble, F): Using 3D technologies to reduce power consumption of FPGAs
30. Oliver Arnold (TU Dresden, D): Dynamic Task Scheduling for heterogeneous MPSoCs
31. Piyd Bahulabadrudini (University of Porto, PT): Analog/Mixed – Signal Circuits using a GUIO TFTs
32. Robert Reichert (Technische Universität Berlin, D): Formal Verification of Discrete-Time MATLAB/Simulink Models using Boogie
33. Sasan Kiamnezh (Karlsruhe Institute of Technology, D): Cross-layer resiliency modeling and optimization: A device to circuit approach
34. Samaneh Ghandali (University of Tehran, IR): High-level Synthesis and Optimization of Datapath-intensive Embedded System Designs
35. Sudip Roy (Indian Institute of Technology Kharagpur, IN): Algorithms for Design Automation of Sample Preparation on Digital Microfluidic Biochips
36. Turbo Majumder (Indian Institute of Technology Delhi, IN): On-Chip Network-Enabled Many-Core Architectures for Computational Biology Applications
37. Vito Giovanni Castellana (Politecnico di Milano, I): C-Based High Level Synthesis of Adaptive Hardware Components

Source URL: https://past.date-conference.com/date14/conference/tutorial-fm1

Links:
[1] https://past.date-conference.com/date14/user/903/contact_form