UB11 Session 11

Date: Thursday 30 March 2017
Time: 14:30 - 16:30
Location / Room: Booth 1, Exhibition Area

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<td>UB11.1</td>
<td>TGV: TESTER GENERIC AND VERSATILE FOR RADIATION EFFECTS ON ADVANCED VLSI CIRCUITS</td>
<td>Miguel Solinas, TIMA, FR; Alexandre Coelho Coelho, Juan Fraire, Nacer Eddine Zergainoh and Raoul Velazco, Univ. Grenoble Alpes, CNRS, Grenoble INP, FR</td>
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**Abstract**

The purpose of this work is to describe a novel tester for radiation effects experiments, called TGV (Tester Generic and Versatile) based on a commercial development board ZEDBOARD. The main idea is to implement the whole DUT (Device Under Test) board architecture controlled by an FPGA, whose configuration is obtained from compiling the description of key features of the DUT in a high-level language such as C. This tester constitutes a powerful tool with generic capabilities for the functional validation and test under radiation of any digital circuit, with a particular focus on processor-like circuits. In this way, there is only a minor hardware development, limited to wiring the DUT pins to the ones of the tester connector. During the demonstration will be shown details of TGV platform, its use being illustrated be means of fault injection experiments which reproduces in a realistic way the random occurrence in time and location of SEUs in sensitive targets of the considered circuit.

More information ...

| UB11.2 | NETFI-2: AN AUTOMATIC METHOD FOR FAULT INJECTION ON HDL-BASED DESIGNS | Alexandre Coelho, Université Grenoble Alpe, FR; Miguel Solinas, Juan Fraire, Nacer-Eddine Zergainoh, Pablo Ferreyra and Raoul Velazco, TIMA, FR |

**Abstract**

Fault injection tools, which include fault simulation and emulation, are a well-known technique to evaluate the susceptibility of integrated circuits to the effects of radiation. This work presents a methodology to emulate Single Event Upsets (SEUs) and Single Event Transients (SETs) in a Field Programmable Gate Array (FPGA). The method proposed combines the flexibility of FPGA with the controllability provided by the MicroBlaze, to emulate HDL circuit and control the fault injection campaign. This approach has been integrated into a fault-injection platform, named NETFI (NETlist Fault Injection), developed by our research group, and received the name of NETFI-2. To validate this methodology fault injection campaign have been performed in Leon3 and Stochastic Bayesian Machine. Results on an Artix-7 FPGA show that NETFI-2 provides accurate measurements while improving the execution time of the experiment by more than 300% compared with analogous simulation-based campaigns.

More information ...

| UB11.4 | AF3-MC: DEVELOPMENT OF MIXED CRITICALITY SYSTEMS USING MBSE | Thomas Boehm, fortiss, DE; Johannes Eder and Sebastian Voss, fortiss, DE |

**Abstract**

AutoFOCUS3 (https://af3.fortiss.org/) is an open-source model-based development tool, including a number of different analysis- and verification tools as well as design space exploration functionality, task scheduling dependent on a number of system requirements (timing, resource, energy, etc.), and code generators targeting C-code or VHDL. The presented demonstrator illustrates both a SW tool demonstrator and a corresponding HW demonstrator setup to show how a seamless model-based system approach could look like, w.r.t. to mixed-critical applications integrated on a (COTS) MC-platform. A floating ball can be controlled by an person by moving his hand over an US sensor, providing input to the control loop implemented in the high criticality part of the system. The low criticality part of the system which is running on the same CPU consists of the computation of the digits of PI and of the Fibonacci sequence, providing computationally intensive neighbors to the control loop.

More information ...

| UB11.5 | A VOLTAGE-SCALABLE FULLY DIGITAL ON-CHIP MEMORY FOR ULTRA-LOW-POWER IOT PROCESSORS | Jun Shiom, Kyoto University, JP; Tohru Ishihara and Hidetoshi Ondera, Kyoto University, JP |

**Abstract**

A voltage-scalable RISC processor integrating standard-cell based memory (SCM) is demonstrated. Unlike conventional processors, the processor has Standard-Cell based Memories (SCMs) as an alternative to conventional SRAM macros, enabling it to operate at a 0.4 V single-supply voltage. The processor is implemented with the fully automated cell-based design, which leads to low design costs. By scaling the supply voltage and applying the back-gate biasing techniques, the power dissipation of the SCMs is less than 20 uW, enabling the SCMs to operate with ambient energy source only. In this demonstration, the SCMs of the processor operates with a lemon battery as the ambient energy source.

More information ...
UB11.6 GNoCS: AN ULTRA-FAST, HIGHLY EXTENSIBLE, CYCLE-ACCURATE GPU-BASED PARALLEL NETWORK-ON-CHIP SIMULATOR

Presenter:
Amir CHARIF, TIMA, FR

Authors:
Nacer-Eddine Zergainoh and Michael Nicolaidis, TIMA, FR

Abstract
With the continuous decrease in feature sizes and the recent emergence of 3D stacking, chips comprising thousands of nodes are becoming increasingly relevant, and state-of-the-art NoC simulators are unable to simulate such a high number of nodes in reasonable times. In this demo, we showcase GNoCS, the first detailed, modular and scalable parallel NoC simulator running fully on GPU (Graphics Processing Unit). Based on a unique design specifically tailored for GPU parallelism, GNoCS is able to achieve unprecedented speedups with no loss of accuracy. To enable quick and easy validation of novel ideas, the programming model was designed with high extensibility in mind. Currently, GNoCS accurately models a VC-based microarchitecture. It supports 2D and 3D mesh topologies with full or partial vertical connections. A variety of routing algorithms and synthetic traffic patterns, as well as dependency-driven trace-based simulation (Nettrace), are implemented and will be demonstrated.

More information ...

UB11.7 EMU: RAPID FPGA PROTOTYPING OF NETWORK SERVICES IN C#

Presenter:
Salvator Galea, University of Cambridge, GB

Authors:
Nik Sultana1, Pietro Bressana2, David Greaves1, Robert Soulé2, Andrew W Moore1 and Noa Zilberman 1
1University of Cambridge, GB; 2Università della Svizzera italiana, CH

Abstract
General-purpose CPUs and OS abstractions impose overheads that make it challenging to implement network functions and services in software. On the other hand, programmable hardware such as FPGAs suffer from low-level programming models, which make the rapid development of network services cumbersome. We demonstrate Emu, a framework that makes use of an HLS tool (Kiwi) and enables the execution of high-level descriptions of network services, written in C#, on both x86 and Xilinx FPGA. Emu therefore opens up new opportunities for improved performance and power usage, and enables developers to more easily write network services and functions. We demonstrate C# implementations of network functions, such as Memcached and DNS Server, using Emu running on both x86 and NetFPGA-SUME platform and show that they are competitive to natively written hardware counterparts while providing a superior development and debug environment.

More information ...

UB11.9 HEPSYCODE: A SYSTEM-LEVEL METHODOLOGY FOR HW/SW CO-DESIGN OF HETEROGENEOUS PARALLEL DEDICATED SYSTEMS

Presenter:
Luigi Pomante, University of L’Aquila, IT

Authors:
Giacomo Valente1, Vittoriano Muttillo1, Daniele Di Pompeo1, Emilio Incerto2 and Daniele Ciambrone1
1University of L’Aquila, IT; 2Gran Sasso Science Institute, IT

Abstract
Heterogeneous parallel systems have been recently exploited for a wide range of application domains, for both the dedicated (e.g. embedded) and the general purpose products. Such systems can include different processor cores, memories, dedicated ICs and a set of connections between them. They are so complex that the design methodology plays a major role in determining the success of the products. So, this demo addresses the problem of the electronic system-level hw/sw co-design of heterogeneous parallel dedicated systems. In particular, it shows an enhanced CSP/SystemC-based design space exploration step (and related ESL-EDA prototype tools), in the context of an existing hw/sw co-design flow that, given the system specification and related F/NF requirements, is able to (semi)automatically propose to the designer: - a custom heterogeneous parallel architecture; - an HW/SW partitioning of the application; - a mapping of the partitioned entities onto the proposed architecture.

More information ...

16:30 End of session

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