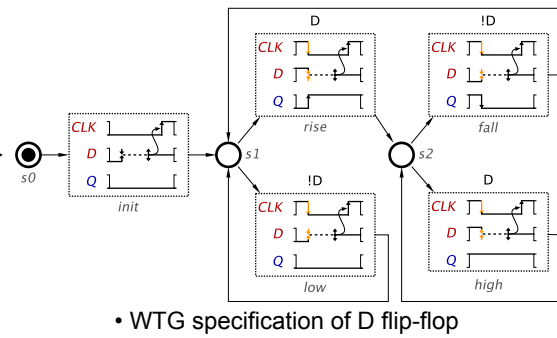
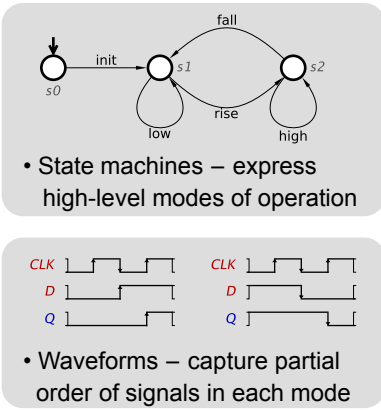


# Waveform Transition Graphs: A designer-friendly formalism for asynchronous circuits

## Overview

- Existing specification methods for asynchronous circuits are either insufficiently expressive (e.g. extended burst mode automata), or unfamiliar to electronic engineers (e.g. labelled Petri nets).
- We propose a designer-friendly Waveform Transition Graphs (WTGs): a symbioses of state machines and waveform diagrams.
- Translation of WTGs semantics into Signal Transition Graphs (STGs) to reuse the existing body of research and tools for verification and logic synthesis of speed-independent asynchronous circuits.
- Design automation in the **Workcraft** toolkit (<https://workcraft.org>)

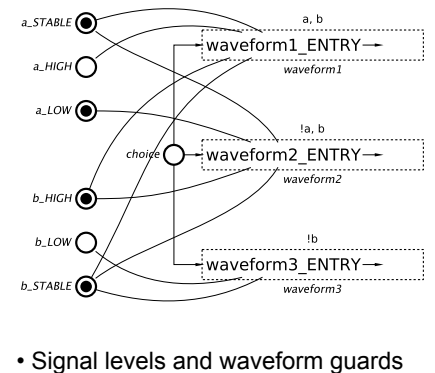
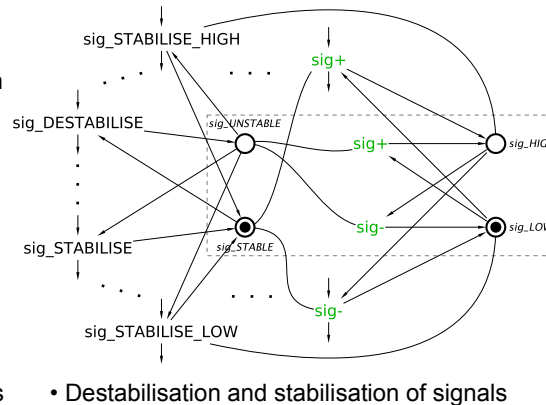
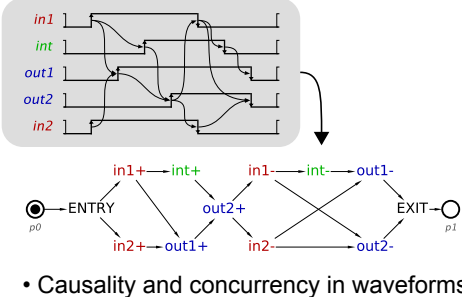
## State machines + Waveforms = WTGs



- Explicit differentiation of *concurrency* and *choice* aspects:
- Concurrency is localised in *waveforms*
  - Choice is restricted to the *nodal states*
- Reach support for modelling of signals:
- Transitions and levels of signals
  - Stable and unstable signal states
- Expressiveness of the model:
- Guards for waveform activation
  - True concurrency (as opposed to bursts) between inputs and outputs

## Translation of WTGs to STGs

- Enables reuse of methods and tools for:
- Formal verification of specification
  - Logic synthesis of circuit implementation



## Design automation in Workcraft

