# An Optimization-Based Design Methodology for Ultra-Low Voltage Analog Integrated Circuits

Lucas C. Severo[12] and Wilhemus A. M. V. Noije[2]
lucassevero@unipampa.edu.br and noije@lsi.usp.br
[1]Federal University of Pampa - Brazil
[2]University of São Paulo – Brazil

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This work presents an Ultra-Low Voltage (ULV) analog integrated circuit design methodology. This methodology is able to sizing analog circuits using an exploration in design space with Simulated Annealing optimization heuristic and an electrical simulator for the specifications estimation [1,2]. This exploration includes the analysis of Process, Voltage and Temperature variations in order to reduce the effect of these variations in the circuit specifications [3]. The methodology implementation is optimized to ULV circuits and has several testbenches, making possible to design a large number of circuit topologies. To reduce the execution time, parallel simulations are used. Fig. 1 shows the methodology design flow.

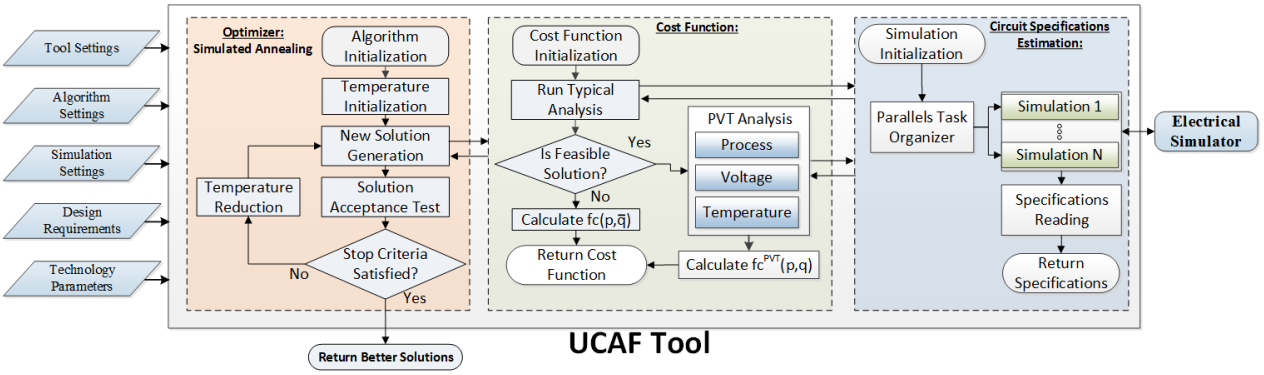
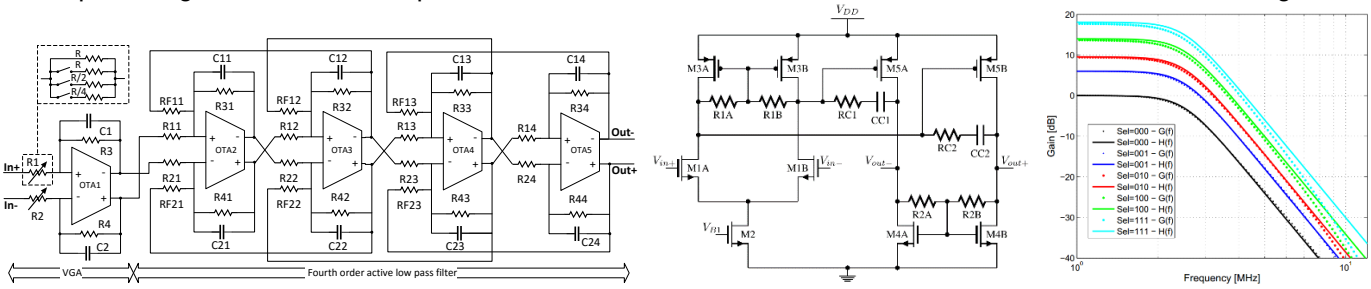



**Figure 1 – Complete design flow of the proposed methodology.**

The methodology was implemented in Matlab and named as UCAF [3]. The UCAF tool has script and graphical interfaces to setting and to execute the tool. All the implemented functions can be reconfigured according to the application. The UCAF output has an environmental to analyze the obtained solutions and to make the circuit design variables tuning.

As an application of this methodology a 0.6 V active Leapfrog low-pass filter with 2.5 MHz cutoff was designed [4]. For this design a fully differential Operational Transconductance Amplifier (OTA) was first designed. In a second time, using a bottom-up approach, an active low-pass filter is designed using the previously designed OTA. The filter results is in according with the IEEE 802.15.4 standard requirements as the baseband filter of a 2.4 GHz radio with power dissipation of 924 µW and gate area of 85,400 µm². The circuits and the simulated transference function are shown in Fig. 2.




**(a)** **(b)** **(c)**

**Figure 2 – Application circuit: (a) VGA with Active Low-Pass Filter, (b) OTA and (c) simulated transference function (Vout/Vin).**

As future works we intend to improve the efficiency of the process parameter analysis in order to reduce the simulation time of this analysis and to insert some layout strategies to make more easy the circuit to physical level translation. Also is intended to design others ULV low power basic building blocks like LNAs, PAs and Mixers as the application of the implemented tool.

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