PFPSim: A Programmable Forwarding Plane Simulator

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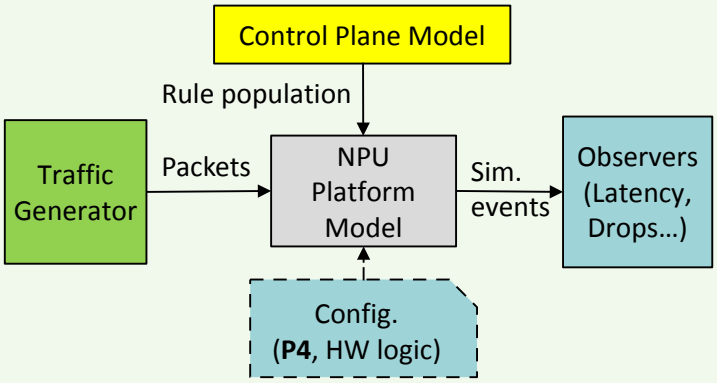
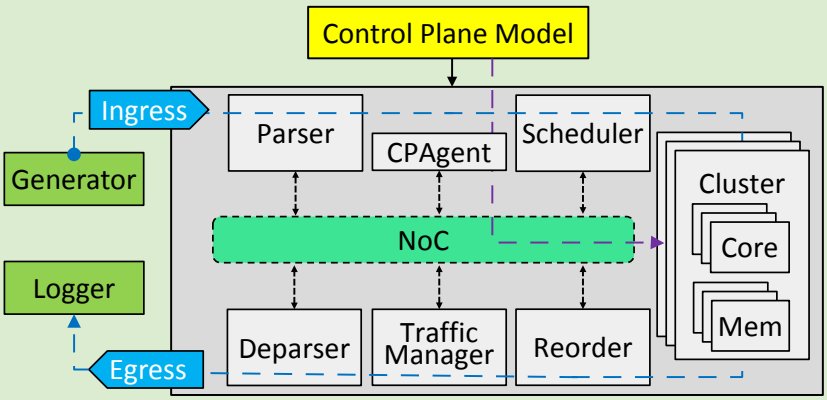
PFPSim Simulation Environment



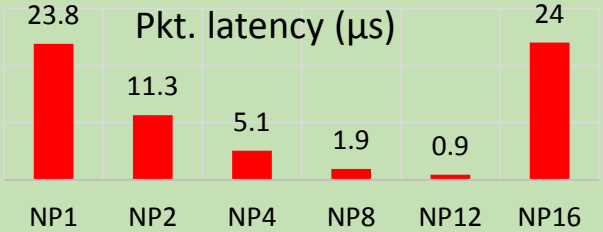
- System-level simulation of forwarding arch.
- High simulation speed for validation
- Cycle-approximate timing estimation
- Easy modification of arch. parameters
- Reliable evaluation of design decisions
- Easy debug of a P4/C application

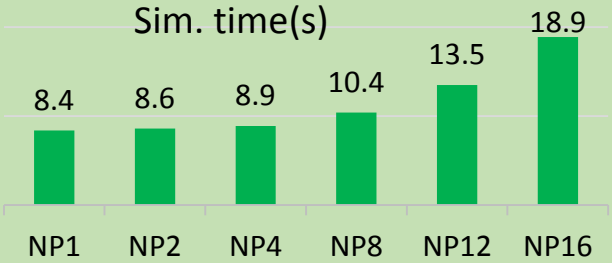
SystemC Programmable Forwarding Plane Model Semantics



- Generic NPU architecture
  - Inspired by Ericsson SNP4000
- Hierarchy of SC_MODULEs
  - Models HW structure
- SC_MODULEs contain SC_THREADs
  - model logic on PE
- Run-to-complete threads on cores
- Memories
  - Transaction-level SC_MODULE
- On-chip routers and switches
  - Special Router SC_MODULE

Experimental Results





Design	NP1	NP2	NP4	NP8	NP12	NP16
#cores	4	8	16	32	48	64
eDRAM	64K	32K	16K	8K	6K	4K

- 2.7 GHz, 8GB RAM simulation host
- Sample P4 application with 5 MATs
- Table size = 2048, 5K packets simulated
- NPUs with 1-16 clusters simulated
- 4 cores/cluster, eDRAM distributed uniformly
- NP16 tries spill over to off-chip memory
- Simulation time 17X – 40X of soft-switch

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