A DAC Stage Analog Circuit Generator for UDSM and FD-SOI Technologies

Benjamin Prautsch, Sunil Rao, Uwe Eichler, Ajith Puppala, Torsten Reich
Fraunhofer Institute for Integrated Circuits,
Design Automation Division, Dresden, Germany
{Benjamin.Prautsch, Sunil.Rao, Uwe.Eichler, Ajith.Puppala, Torsten.Reich}@eas.iis.fraunhofer.de

***Abstract*—The design of analog integrated circuits requires extensive manual work which is error-prone and inefficient. With advanced ultra-deep sub-micron (UDSM) technologies, the manual design effort increases further dramatically. This work presents the application of a rethought generator approach for the efficient reusable design of a 12-bit current steering DAC. The current mirror stage of the DAC, which is arranged in the complex Q² random walk scheme for high intrinsic matching [1], is realized by a circuit generator which automatically creates schematic, symbol, and layout of the required cells within few minutes. Originally focused on a 28 nm bulk technology, the generator code was also executed in a 28 nm FD-SOI technology with minor migration effort due to the generic nature of our tool. In addition, the fast circuit generation enables an efficient layout optimization showcasing the benefit of analog circuit generators for "bottom-up" design [2] in advanced technology nodes.**

Keywords—Analog IC Design; Analog Design Automation; Analog Generators; Reuse; 28 nm FD-SOI

I. Introduction

While digital circuit design benefits from complete automatic flows from a hardware description language towards the physical layout, analog design suffers from its manual design fashion. A conventionally designed analog block can hardly be reused due to its static nature. In contrast, analog circuit generators are holding expert knowledge in the form of source code. They are reconfigurable and allow the complete regeneration of analog blocks (schematic, symbol, and layout views) including their testbenches within seconds to minutes.

In this work, a generator was developed to improve both reuse and design efficiency of the complex current mirror array of a current steering DAC consisting of over 8000 transistors.

II. The DAC Stage Generator

Each digital system which communicates with the "real world" requires a mixed signal circuit interface containing ADCs and DACs. A frequently-used digital-to-analog converter is the current steering DAC [3]. In order to improve the intrinsic matching of the current mirror array of such DACs, the Q² random walk scheme was introduced [1]. The manual layout design of this structure is very time-consuming, since hierarchical decomposition and signal abutment is not entirely possible. Moreover, in the employed 28 nm technologies parasitic parameters greatly depend on the layout context which causes faulty parasitic estimations. Therefore, we decided to implement a generic and abstract generator using our TAL syntax presented in [4] which allows the generation of this DAC stage for a wide range of technologies and parameters. The placement of all layout elements is determined by the definition of their placement relations down to the lowest hierarchy level. Subsequently, technology-specific layout-dependent design rules are evaluated and applied to this abstract placement description in order to achieve DRC-correct layouts. With our parameterizable generator implementation we have generated different versions of the DAC stage followed by parasitic extraction and simulation. We optimized the layout of the analog block especially regarding the crucial wire width and wire spacing in an efficient way (see Table I).

TABLE I. Comparison of the effort of manual (estimated) and generator-based layout design of the DAC stage.

	Design	Porting	Resizing
Manual	2 weeks	1-2 weeks	1-2 weeks
Generator	3-4 weeks	< 1 day	< 10 min

III. Conclusion and Outlook

Analog circuit generators are an effective tool to facilitate the work of designers. Rethinking this principle enables DRC-clean and LVS-clean analog circuit generation through abstract generator descriptions even in advanced UDSM technologies. The huge amount of layout-dependent design rules to be considered and the dependency of sheet resistances and other parasitic parameters on the layout context complicate manual analog design dramatically. Our generators are a beneficial tool to overcome these challenges by means of correct and very fast generation of circuit varieties. In this work, the iteration of parasitic extraction and simulation is still done manually and will be further automated in the future. In addition, a qualified measure of the "efficiency" of analog generators is required.

Acknowledgements

The presented work was partly supported by the European Union and the Free State of Saxony within the project THINGS2DO (Ref. No. 16ES0240).

References

[1] G. A. Van der Plas, J. Vandenbussche, W. Sansen, M. S. Steyaert and G. G. Gielen, "A 14-bit intrinsic accuracy Q² random walk CMOS DAC," *IEEE Journal of Solid-State Circuits,* pp. 1708-1718, 1999.

[2] J. Scheible and J. Lienig, "Automation of Analog IC Layout–Challenges and Solutions," *Proceedings of the 2015 International Symposium on Physical Design,* pp. 33-40, 2015.

[3] P. Harpe, A. Baschirotto and K. A. Makinwa (Eds.), *High-performance AD and DA Converters, IC Design in Scaled Technologies, and Time-domain Signal Processing: Advances in Analog Circuit Design 2014*, Springer, 2014.

[4] B. Prautsch, U. Eichler, T. Reich, A. Puppala and J. Lienig, "Abstract Technology Handling for Generator-Based Analog Circuit Design," *Proceedings of ZuE 2015; 8. GMM/ITG/GI-Symposium Reliability by Design,* pp. 1-6, 2015.