## Automated Refinement of Analog/Mixed-Signal SystemC Models to Include Non-Functional Effects

Georg Gläser<sup>1</sup>, Hyun-Sek Lukas Lee<sup>2</sup>, Eckhard Hennig<sup>3</sup>, Markus Olbrich<sup>2</sup>, and Erich Barke<sup>2</sup>

<sup>1</sup>IMMS Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH Ilmenau, Germany <sup>2</sup>Institute of Microelectronic Systems, Leibniz Universität Hannover, Germany <sup>3</sup>Reutlingen University, Germany

*Abstract*—Virtual prototyping of analog/mixed-signal (A/MS) systems is a key concern in a modern design process. The main challenge to performing the verification of functional properties and to include non-functional effects, e.g. signal and power integrity. System architects are challenged by identifying critical scenarios in which these effects possibly degrade or even destroy the system's functionality. We demonstrate a method to automatically extend an existing functional model by non-functional effects. Combined with an accelerated, piecewise-linear (PWL) simulation scheme (PRAISE), we explore the resulting system acceptance regions and identify critical scenarios.

## I. DEMONSTRATION SCENARIO

As an example, we use a hysteretic current-mode buck converter system shown in Figure 1. This system poses several challenges during the design process. Here, we take the designer's point of view: Starting from purely functional models (Step 1), here described in SystemC, critical (non-functional) parameters have to be examined. This is done by refining the block models by automatically analyzing the given SystemC code and extending it to account for non-functional effects (Step 2). The affected functions (yellow boxes) are wrapped by additional SystemC code describing the non-functional effects (blue boxes). Sweeping the parameters of the refined models in simulation yields the estimated system acceptance regions shown in Step 3. For evaluating these regions, many simulations need to be executed. Obviously, the simulation performance is crucial for efficiently exploring these regions. To speed up the simulation, we use an accelerated analog simulation approach for simulating the buck converter circuit [1]. This approach uses PWL models to avoid numerical integration and nonlinear solving.

Using this combination of accelerated analog simulation and automated refinements for non-functional properties, the critical scenarios in a design can be identified in a very early design stage. The identified regions can be used for evaluations of different implementations of system components to include non-functional influences and to generate new specification parameters with their corresponding test cases.

## REFERENCES

 S. Hoelldampf, D. Zaum, M. Olbrich, and E. Barke, "Using analog circuit behavior to generate SystemC events for an acceleration of mixedsignal simulation," in *IEEE International Conference on Computer Design* (*ICCD*), Oct. 2011, pp. 108–112.

This work has been carried out in the project ANCONA, funded by the German Federal Ministry of Education and Research (BMBF) in the ICT2020 program under grant no. 16ES021.



Fig. 1. Concept of system acceptance region exploration: After analyzing the model (Step 1), the systems non-functional effects (blue boxes) are automatically refined (Step 2). Finally, a simulation can be executed to evaluate points in the parameter space and observe the corresponding system behavior (Step 3).