Demonstration of a Digitally Driven Top-Down Methodology for Mixed Signal Circuit Design

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Methodologies in analog and digital circuit design are still very incoherent today. Whereas the design approach for digital logic is usually a top-down process in a hardware description language (HDL), followed by a massively automated synthesis and implementation flow, analog circuits are often implemented in a bottom-up block oriented design process which is very manually driven.

Yet, the integration into large system-on chip (SoC) designs brings digital and analog blocks closer together. The increasing number of today's mixed-signal designs therefore leads to challenges for both design and verification, especially when it comes to the interface of semi- and full custom blocks.

Additionally, advanced node technologies favor the use of digital, standard cell based circuits, which scale with the technology, whereas analog circuit performance usually suffers from increasing process variations and less favorable transistor properties. A robust, portable and flexible design should therefore make use of digital logic wherever possible in order to profit from technology scaling.

To verify the behavior of complex SoC designs system level simulations are required, which naturally also include the full custom blocks. Because transistor level SPICE simulations are absolutely impossible at this design scope, more abstract, but faster models are necessary. This in turn leads to the challenge of maintaining consistency between component specifications, testbenches, models as well as the actual implementation.

To address all of the above, a digital centric design methodology has been developed and applied to a high speed Serializer/Deserializer (SerDes) macro. The digital centric SerDes design itself leverages digital filters and calibration loops in order to yield robust performance in advanced node processes and achieve good portability. Key concepts of the demonstrated methodology are listed below:

- The complete system consisting of parametrized synthesizable modules and full custom blocks, is modelled in a top-down approach using Verilog HDL
- First VerilogAMS is used to develop real number based models exhibiting analog metrics of importance to system scope and cell performance
- Connectivity between full custom cells is described by "structural" Verilog, which allows automatic schematic generation for use in full custom tool chain and ensures consistency with the modelled system
- Schematic templates are generated for full custom cells, exhibiting correct port names, widths and serving as specification for transistor level implementation
- The implemented cells as well as the complete system are checked against the VerilogAMS models as a golden sample

Once the complete mixed signal macro is described, the SerDes model can already be used at the SoC level for further integration and verification while the mixed signal macro development is still ongoing.

All early design space exploration is faster and more efficient in this top-down design flow. Cells which can be reused at different places in the design are identified easier and problems arising from interactions on the system level are found early in the design phase. This increases the chance of avoiding fundamental problems during the implementation phase which are costly and can ruin the complete tapeout schedule. The verification environment can be developed in parallel. The real number models are used during development phase of the testbenches and can later be replaced with the actual spice netlists, where required.

This methodology accelerates the design process significantly, avoids errors and provides higher flexibility for design changes. The digital centric design flow from HDL to schematic netlist at the example of the SerDes IP is demonstrated.