A Fast Prototyping Methodology with Constrained Floorplaning on Analog Layout Generation

Dr. Po-Cheng Pan*, Prof. Hung-Ming Chen* and Hung-Wen Huang*
*Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan
Email: pocheng.pan@g2.nctu.edu.tw; hmchen@mail.nctu.edu.tw; reimu5492@gmail.com

***Abstract*—Layout generation in the recent analog design is challenging by its critical layout dependent effect (LDE). Based on the same netlist design, different layouts lead distinct performances. Therefore, it is necessary to observe and avoid the LDE during generation. Traditionally, the strategies of analog layout generation mostly count on experienced designers. However, the experience is based on time-consuming manually try-run, which is inefficient and unreliable.**

In this work, we develop a fast prototyping for analog layout generation. In our approach, we apply a fast floorplanning algorithm, for multi-layout generation and select the feasible results w.r.t. the analog constraints pre-decided. For practical usage, we implement this approach embedded on the EDA-tool so that layout designers are able to design with such prototypes for efficiency. The demonstration includes layout prototyping generation, the integration between our program and EDA-tool and the resulting layout prototypes.

I. Background and Related Work

The application of analog layout generation is widely developed in academia and industry. Commercial tools like Cadence Virtuoso ADE, Synopsys Laker have provided template-based schematic-driven analog layout generator. However, the generated layout mostly keeps the original topology. Our Previous Approach integrates mechanisms from [1], [2], [3]. The device sizes of targeting technology is generated from [2]. In [1], it provides multiple placement results withholding analog layout constraints. For routing generation, [3] preserves the behavior of routing from the reference layout and fast generates routing on the targeting layout.

II. Flow of Our Framework

Although previous approach provides methodologies to preserve existing design for layout migration, the solution space is restricted to the extraction. In order to provide fast prototyping for layout migration without existing layout, this software performs a constrained floorplanning. The multiple floorplanned layouts are generated according to the constraints which are defined with netlist. Later, these prototypes transform into results in Candence Layout View. These prototypes contribute layout designers to implement layouts without manual placement. Fig. 1 shows the overall flow diagram of our methodology. The flow is mainly separated into three stages:

1) **Netlist Extraction and Constraints Definition**
2) **Fast prototyping based on Slicing Tree Generation**
3) **Abstract Prototypes into Industrial Layout Transformation**

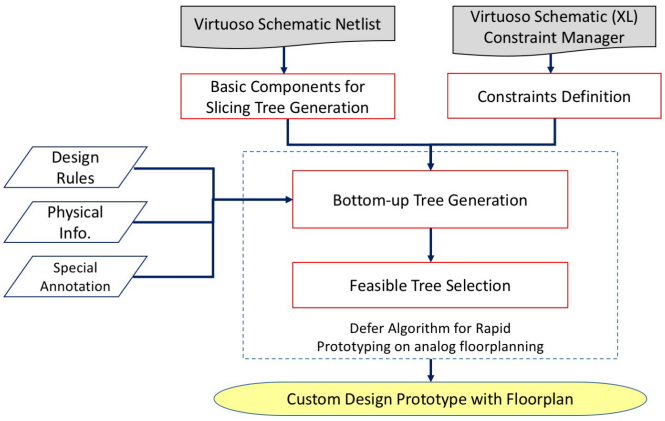

Fig. 1. Overall flow of the proposed layout migration framework.

In the end, a set of layouts with floorplanning are obtained, which provides designers a quick look of possible solutions that can be used. Other than extracting fixed templates as [3], this work generates analog layout prototypes independently. Furthermore, we integrate the methodologies with Candence Virtuoso Design Environment for design efficiency.

III. Program Setting and Results

Our Software is developed with g++ 4.4.7 for methodology, Cadence® Virtuoso® 6.1.5 with its Schematic Editor, Constraint Manager and Layout Suite for layout realization. The prototypes of a folded-cascode operational amplifier (OpAmp) will be demonstrated step-by-step as applications to show the feasibility of our Software.

References

[1] Y.-P. Weng, H.-M. Chen, T.-C. Chen, P.-C. Pan, C.-H. Chen, and W.-Z. Chen, "Fast analog layout prototyping for nanometer design migration," in *International Conference on Computer-Aided Design*, 2011, pp. 517 – 522.

[2] P.-C. Pan, H.-M. Chen, and C.-C. Lin, "Page: Parallel agile genetic exploration towards utmost performance for analog circuit design," in *Design, Automation and Testing in Europe*, 2013, pp. 1849—1854.

[3] P.-C. Pan, C.-Y. Chin, H.-M. Chen, T.-C. Chen, C.-C. Lee, and J.-C. Lin, "A fast prototyping framework for analog layout migration with planar preservation," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 34, no. 9, pp. 1373–1386, Sep. 2015.