VisualNoC: Visualization Network-on-Chip Design Framework

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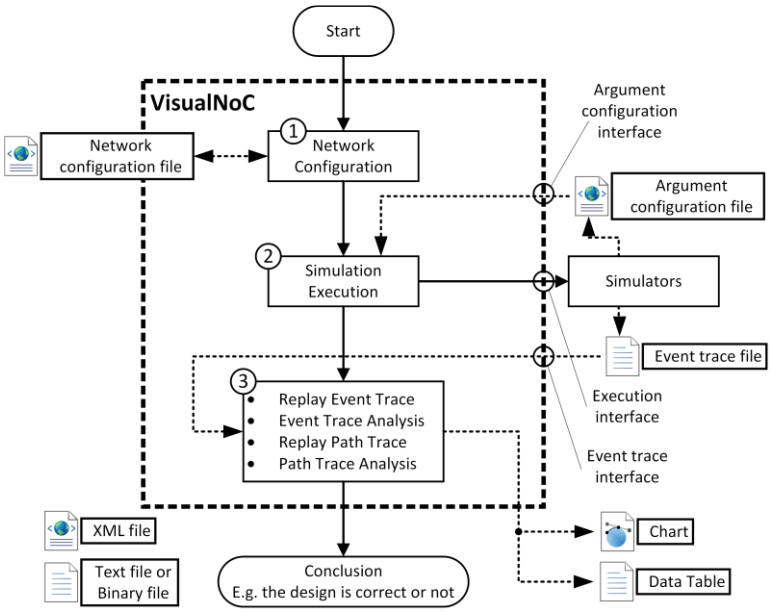
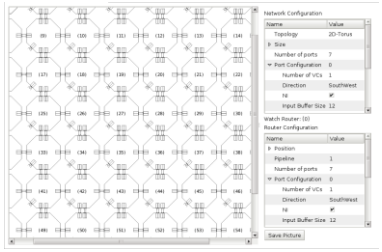
Abstract - Simulation is the most common approach to evaluating Network-on-Chip (NoC) designs and developers spend a lot of time and energy on implementation, debugging, execution and analysis. Visualization of simulation is sensible to make the evaluation flow more effective. The **Visualization Network-on-Chip Design Framework** (**VisualNoC**) can visualize the entire flow of simulation to support the designer in understanding the NoC behavior.

Features

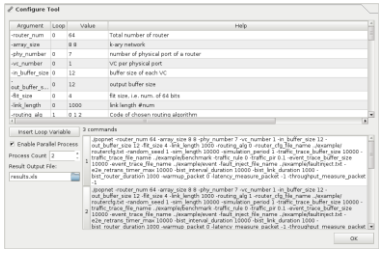
- *Open Architecture.* With defined function calls and data interfaces, any simulator and auxiliary tool can be linked to VisualNoC.
- *Event-based Behavior Recorder.* A simple but extensible event-based behavior model is used to record the operations in routers and flits.
- *Debugging.* By reproducing the operations of routers and movements of packets forward and backward in an animation, design flaws and implementation bugs are made apparent.
- *Statistics.* The simulation results are analyzed and presented in small granularity and rich in aspects and views.
- *MapReduce Parallelism Execution.* Groups of simulations can run in parallel to utilize the computation capacity of computers.
- *Open Source and Cross-platform.* The program is fully open source. It supports different OS platforms (Windows, Linux).



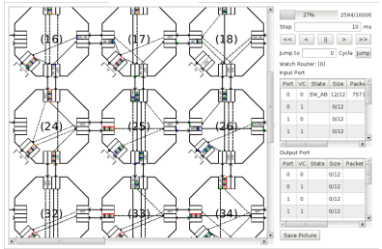
Functions and Panels



← *Network Configuration.* Contains network configurations available for all routers or individual configurations for one specific router. Supports regular and irregular topology as well.

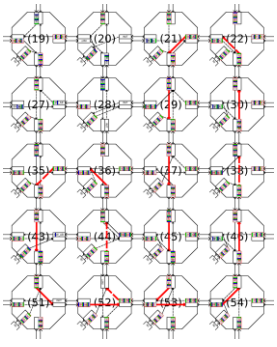


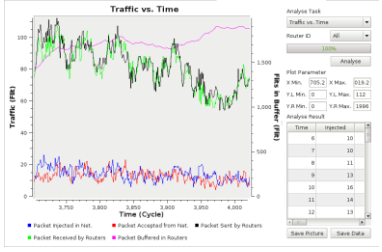
→ *Simulation Execution.* Configures the simulators and calls a group of simulations in parallel. Watch simulation progress and collect simulation results.



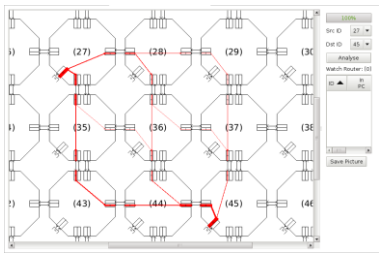
← *Simulation Reproduction.* During the retrace of the event trace file, the packets move in the NoC on the screen. (Fast) forward/backward with configurable speed are supported as well as jumping to specific time instances.

→ *Deadlock Detection.* On-time deadlock detection during simulation reproduction marking the cause of deadlock.





← *Event Trace Analysis.* Shows statistics results based on event trace files in rich charts. The analysis tasks include: traffic temporal distribution, distance distribution, latency distribution, and traffic spatial distribution.



→ *Path Trace Analysis.* Shows the paths of packets and distribution of traffic between certain source and destination. The width of lines shows the number of traffic.