

VisualNoC: Visualization Network-on-Chip Design Framework

VisualNoC

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Abstract - Simulation is the most common approach to evaluating Network-on-Chip (NoC) designs and developers spend a lot of time and energy on implementation, debugging, execution and analysis. Visualization of simulation is sensible to make the evaluation flow more effective. The **Visualization Network-on-Chip Design Framework** (**VisualNoC**) can visualize the entire flow of simulation to support the designer in understanding the NoC behavior.

Networ

configuration file

Features

- <u>Open Architecture</u>. With defined function calls and data interfaces, any simulator and auxiliary tool can be linked to VisualNoC.
- <u>Event-based Behavior Recorder</u>. A simple but extensible event-based behavior model is used to record the operations in routers and flits.
- <u>Debugging</u>. By reproducing the operations of routers and movements of packets forward and backward in an animation, design flaws and implementation bugs are made apparent.
- <u>Statistics.</u> The simulation results are analyzed and presented in small granularity and rich in aspects and views.
- <u>MapReduce Parallelism Execution</u>. Groups of simulations can run in parallel to utilize the computation capacity of computers.
- <u>Open Source and Cross-platform.</u> The program is fully open source. It supports different OS platforms (Windows, Linux).

Argument configuration file Simulation Simulators Execution Event trace file Execution Replay Event Trace interface **Event Trace Analysis** Replay Path Trace Event trace Path Trace Analysis interface XML file Chart Conclusion Text file o Data Table Binary file E.g. the design is correct or not

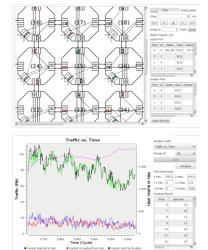
Start

Network

Configuration

Functions and Panels

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 \leftarrow <u>Network</u> <u>Configuration</u>. Contains network configurations available for all routers or individual configurations for one specific router. Supports regular and irregular topology as well.

 \rightarrow <u>Simulation Execution.</u> Configures the simulators and calls a group of simulations in parallel. Watch simulation progress and collect simulation results.

 \leftarrow <u>Simulation Reproduction.</u> During the retrace of the event trace file, the packets move in the NoC on the screen. (Fast) forward/backward with configurable speed are supported as well as jumping to specific time instances.

 \rightarrow <u>Deadlock Detection</u>. On-time deadlock detection during simulation reproduction marking the cause of deadlock.

 \leftarrow <u>Event Trace Analysis.</u> Shows statistics results based on event trace files in rich charts. The analysis tasks include: traffic temporal distribution, distance distribution, latency distribution, and traffic spatial distribution.

 \rightarrow <u>Path Trace Analysis.</u> Shows the paths of packets and distribution of traffic between certain source and destination. The width of lines shows the number of traffic.



Argument

configuration

interface

