Voltage Propagation Method for 3-D Power Grid Analysis

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Abstract— **Power grid analysis is a challenging problem for modern integrated circuits. For 3-D systems fabricated using stacked tiers with TSVs, traditional power grid analysis methods for planar (2-D) circuits do not demonstrate the same performance. An efficient *IR* drop analysis method for 3-D large-scale circuits, called 3-D voltage propagation method, is proposed in this paper. This method is compared with another widely used power grid analysis method, with preconditioned conjugated gradients. Simulation results demonstrate that the proposed method is more efficient for the *IR* drop analysis of large size 3-D power grids. Speedups between 10× to 20× over the preconditioned conjugated gradients method are shown.**

Keywords – 3-D integrated circuits; Through-silicon vias; Power grid analysis

I. INTRODUCTION

Three-dimensional (3-D) system integration, using *Through-Silicon-Vias* (TSV) to connect several tiers, has emerged as a promising technology to mitigate interconnect issues related to modern ICs [1]. Since this technology greatly reduces the interconnection length between vertically stacked integrated circuits, TSV-based 3-D ICs have become a potent solution for the design of high-speed IC systems with smaller form factors and enhanced performance.
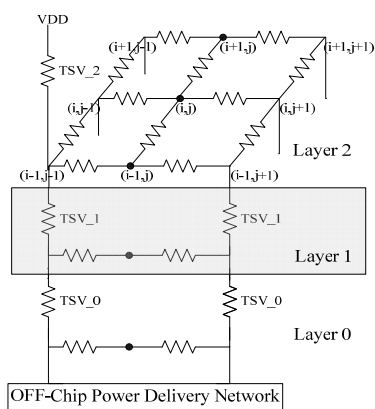

Fig. 1. Schematic of a typical on-chip 3-D power distribution network.

Meanwhile, the increase in the complexity of VLSI circuits has accentuated the requirement for fast and accurate power grid analysis techniques. Consider, for example, the power grid of a three-plane 3-D circuit as depicted in Fig. 1. This model of the 3-D power distribution network includes a resistive network, where the tiers are connected by TSVs at specific nodes, power and ground pads in one of the layers, and devices modeled as current sources.

Traditionally, such a power grid network is represented as a large-scale linear system

$$\mathbf{Gx = I,} \tag{1}$$

where $\mathbf{G}$ is the conductance matrix of the interconnected network, $\mathbf{x}$ is the vector of node voltages and $\mathbf{I}$ is the vector of independent current sources. However, for modern SoC designs, the network can have tens of millions of nodes [2], which results in over one trillion elements for matrix $\mathbf{G}$. Solving this linear system can become prohibitively expensive due to the limited computational resources.

Several simulation techniques have been developed for analyzing 2-D power grids. These methods include, the *grid-reduction* (GR) scheme [3], the *hierarchical analysis* method (HA), the *random walk* (RW) method [4], the *row-based* (RB) method [5] and the multi-grid *preconditioned conjugated gradients* (PCG) algorithm [6]. Some of these techniques are related to the proposed technique and are discussed in the background section.

All these methods are suitable for 2-D ICs, but cannot be directly used into a 3-D system due to several reasons. A primary reason is the analysis implications due to the TSVs, which provide power and ground to all but one of the planes of a 3-D stack. For instance, in 3-D ICs with TSVs, distinguishing between global and local grids is more difficult than in 2-D circuits, since the power grids form a vertical stack [7]. Additionally, the TSV resistance plays an important role in connecting two different planes, such that ignoring this resistance can produce unpredictable errors. Since the resistance of a TSV is considerably lower as compared to the resistance of the horizontal wire segments of the power grid, if the TSVs are considered, methods, such as the RW technique can be trapped in the TSVs infinitely, while searching a path to a power pad [8]. Alternatively, other iterative methods, such as RB can require an excessive number of iterations delaying convergence to the precise node voltages.

A 3-D power grid analysis method, which considers the structure of the power grid and circuit analysis techniques, is presented to estimate node voltages accurately and fast. This 3-D *voltage propagation* (VP) method exhibits both higher accuracy and lower runtime over the multi-grid PCG algorithm [6].

The remainder of this paper is organized as follows. A brief overview of well-known power grid analysis methods is pro-

vided in Section II. The proposed 3-D VP method is presented in Section III. Simulation results on some industrial test benchmarks with Spice, the PCG, and the new method are given in Section IV. Some conclusions are drawn in Section V.

II. BACKGROUND

In this section, three 2-D power grid analysis methods are discussed. The RW algorithm is briefly described in Section II-A and another two iterative methods, RB and PCG are overviewed in Sections II-B and II-C, respectively.

A. Random Walk Algorithm

The RW algorithm is a broadly used method to analyze power grids. The analytic expressions describing a random walk model have a similar form to (1). The basic principle of the RW technique exploits this similarity to determine the *IR* drop across a power grid [4]. Some limitations of this method relate to the required large number of iterations, although a large error margin is allowed. For a small network discussed in [4], 5,000 iterations are required such that the error margin decreases to less than 5 mV. This error is ten times larger than the allowed error in the proposed 3-D power grid analysis method. Additionally, the required iterations are expected to further grow for 3-D circuits.

B. Row-Based Algorithm

The RB iterative scheme presented in [5] has exhibited good convergence properties. Since a power grid consists of horizontal rows and vertical columns, the row-based method treats each row of nodes as one group depending on the boundary conditions of adjacent rows. Assuming all nodes are initialized to a specific voltage and the node voltages of the adjacent rows have already been computed, the problem of determining the node voltages of the present row is equivalent to a block-iterative Gauss-Seidel (GS) relaxation technique [9], which is a linear-time special case of Gaussian elimination. Since the matrix $\mathbf{G}$ is symmetric and positive-definite, the GS method can converge with any initial solution [10]. The required number of iterations increases with the number of grid nodes proportionally to N^2 [5]. Moreover, using *successive over-relaxation* (SOR), the convergence of the RB method can be further sped up, and the convergence rate becomes proportional to N [11].

C. Preconditioned Conjugate Gradient Algorithm

The PCG algorithm is another algebraic iterative technique for solving sparse linear systems. Intuitively, this PCG method is a realization of an orthogonal projection technique onto the Krylov subspace [6] and the use of preconditioning results in faster convergence. The preconditioner $\mathbf{M}$ used in PCG should satisfy $\mathbf{M^{-1}(Gx\text{-}I)} = \mathbf{0}$ [12].

III. VOLTAGE PROPAGATION METHOD

In this section, a new method to analyze 3-D power distribution networks is presented. In Section III-A, the rationale for which RB is chosen as the basic method extended to 3-D is provided. The general idea of the technique that determines the *IR* drop within a 3-D power grid is presented in Section III-B. In Section III-C, the VP algorithm is described.

A. Extending 2-D methods to 3-D

Among the existing methods, the RB algorithm exhibits some attractive features. For large power grids, the matrix $\mathbf{G}$ in (1), which contains all the information of the nodes, is excessively large and sparse. Since the RB algorithm does not need to simultaneously consider the entire power grid structure and is executed row by row, the new iterative solution can be generated by the previous row. This situation leads to more efficient memory utilization. Furthermore, for each row, the time used in RB depends only on the number of the nodes, which means that the time and memory usage are linear in the number of nodes. Therefore, the 3-D power grid analysis method is based on the 2-D RB algorithm.

Alternatively, the Gauss-Seidel method converges where the coefficient matrix $\mathbf{G}$ is diagonally dominated or symmetric positive-definite. The convergence rate increases if the diagonal elements are much bigger than the sum of the rest elements of the same line [13]. In 2-D grids, this condition is typically met and the theoretical convergence rate is proportional to N. However, in 3-D grids, the resistance of a TSV is considerably lower as compared to the resistance of the horizontal wire segments of the power grid. This reduces the diagonal dominance of matrix $\mathbf{G}$ and, consequently, the convergence ratio.

Consequently, specific rows of matrix $\mathbf{G}$ in (1) are dominated by the large conductance of the TSVs which can increase the number of iterations. This behavior limits the applicability of the RB method to 3-D grids. By separately treating the TSV conductance (since these terms exhibit high sensitivity), faster convergence can be achieved. The 3-D VP algorithm modifies the 2-D RB method to consider the different characteristics of the TSVs to improve accuracy and convergence rate.

B. IR Drop Analysis for 3-D Power Network

In this section, two aspects of the method for *IR* drop analysis in 3-D ICs are described. In subsection III-B-1, the general idea of how to treat TSVs is presented. The 3-D benchmark circuits analyzed by the proposed technique are discussed in subsection III-B-2.

1) Coping with the Through-Silicon-Vias

The basic idea can be described as follows. The VP method treats each TSV as a resistive pillar that connects the nodes of adjacent tiers. Without loss of generality, three stacked circuits are used to demonstrate the 3-D VP method. Typically, power is delivered to the circuit through TSVs. For a 3-D power grid, assuming that the package pins are connected to the topmost tier, the current flows through TSVs from the upper tiers to the bottommost tier. Due to the stacked structure, each TSV supplies current to the layer that contains this TSV as well as to the remaining layers of the stack farther from the package pins. This current distribution can not be determined in the beginning by applying (1) to the first layer (the tier closest to the package pins). The VP method, therefore, should be applied starting from the bottommost tier.

To address this issue, specific modifications are needed. Although the current flows through the TSVs from top to bottom, the VP method progresses in an opposite direction. With this approach, the 3-D VP method is divided in three phases, 1)

intra-plane voltage calculation, 2) TSV current computation, and 3) voltage propagation. The effect of TSVs is considered within the propagation phase. Since a resistance should not be processed twice, during the first stage, the resistance of the TSVs is not considered.

2)   3-D Benchmark Circuits

To the best of author's knowledge, there are no 3-D benchmark circuits (*i.e.*, extracted 3-D power distribution networks) where the VP technique can be applied. Different 3-D power grids are produced based on planar circuits. The basic planar benchmark circuits used are provided by the IBM TAU 2011 Power Grid Simulation Contest [14]. Single tiers are replicated thrice to produce three-plane 3-D circuits connected by TSVs at specific nodes. For the placement of the TSVs, without loss of generality a uniform distribution across the plane is assumed and the resistance of the TSVs is fixed to 0.05 Ω [14]. The proposed method is equally applicable to any TSV distribution, in other words, the technique is oblivious to the TSV distribution.

In the employed 3-D benchmark circuits, there is one TSV node for every four nodes. For the nodes, which are not TSVs, an independent current source is connected to simulate a device or a group of devices in the vicinity of the node. Note that due to the necessary keep-out zones for the TSVs, a current source (*i.e.,* a device) cannot be connected to a TSV node.

C.   Voltage Propagation Algorithm

The pseudocode of the VP algorithm is illustrated in Fig. 2. The VP algorithm is initially applied to the bottommost physical tier (layer 0). The voltage of all nodes is initialized. Since the voltage of the nodes, which connect to a power pad with TSVs, should not considerably depart from VDD, to speed up the analysis, the initial voltage for these nodes can be chosen as VDD. Keeping the voltage of the nodes, which correspond to TSVs, fixed, the voltage of all other nodes is determined by using the RB iterative method. Applying Kirchhoff's current and voltage laws, respectively, to each TSV node, the current flowing through each TSV is determined.

Based on the resulting current and the resistance of each TSV, the voltage drop across these interconnects is determined. This voltage drop is added to the initially assigned node voltage of the TSVs in layer 0, to obtain the voltage node of the TSVs in layer 1. Applying the RB method to the nodes in layer 1, every node (excluding the TSVs) voltage can be obtained. This process is repeated until the topmost tier is reached as succinctly depicted in Fig. 3.

Note that the "propagated source voltage" is not the nominal VDD but corresponds to a computed voltage from the initial voltage assumed for the power TSVs in layer 0. Consequently, there can be a voltage difference between the nominal voltage and the "propagated source voltage". In Fig. 3, the assumed voltage at a TSV node in layer 0 is V_0 and the "propagated source voltage" to the TSV in the topmost layer is $V_0 + \sum_{k=0}^{2} I^k * R_{TSV}$, which is different than VDD.

Intuitively, if a "propagated voltage" is higher than VDD, the initial voltage assumed in layer 0 should be slightly lower

according to the voltage difference and *vice versa*. There is only one principle that should be considered, such that the "propagated voltage" converges to VDD (GND) at a power (ground) node, the voltage difference of the new state should be smaller than the previous iteration.

Voltage Propagation Method

1. Calculating Voltage of Nodes (CVN)
2.   Row-Based Iterative;
3.   Calculating Current of TSV;
4. Voltage Difference Adjustment (VDA)
5. $V_{diff}(j) \rightarrow V_{diff}'(j)$
6. Main
7. $V_0(j)$ = initial guess for layer-0
8.   set $\varepsilon \ll 1$
9.   if $\left| V_{diff}(j) \right| < \varepsilon$, return
10.   for layer-*l*, *l*=0,1,2
11. $V_l(j) = V_{l-1}(j) + \sum_{N=0}^{l-1} iTSV_N(j) \times rTSV(j)$;
12.   CVN;
13. $V_{DD}'(j) = V_2(j) + \sum_{N=0}^{2} iTSV_N(j) \times rTSV(j)$;
14. $V_{diff}(j) = V_{DD} - V_{DD}'(j)$;
15.   VDA;
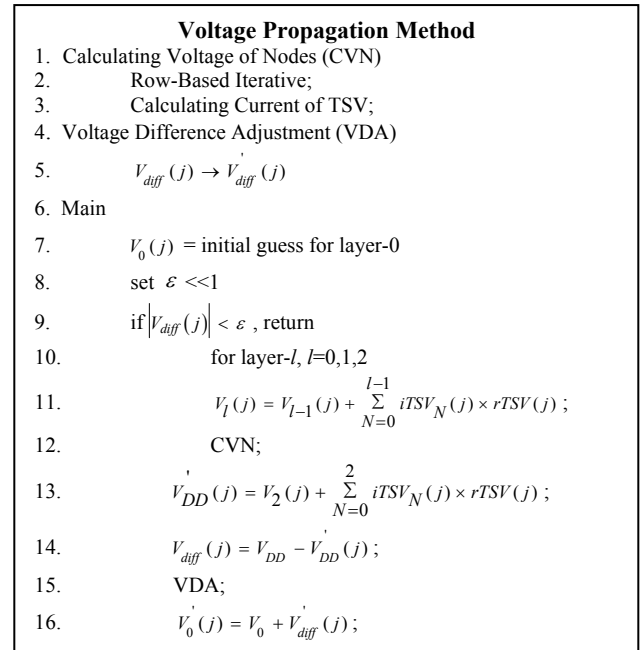16. $V_0'(j) = V_0 + V_{diff}'(j)$;

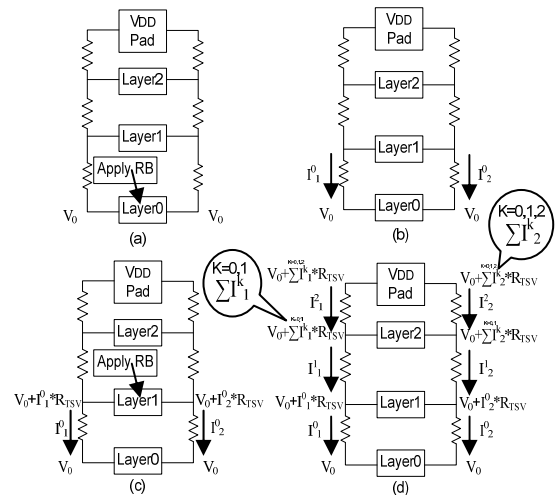Fig. 2. The pseudo-code of the algorithm for the voltage propagation method.

Fig. 3. The procedure of the voltage propagation method, (a) apply the row-based method in layer 0, (b) obtain the current flowing through TSVs, (c) determine the voltage of the TSV terminal on layer 1, and (d) obtain the "propagated source voltage".

There are two employed sub-functions in the VP method, the role of which is briefly discussed due to space limitations. "Calculating Voltage of Nodes (CVN)" is used to determine the voltages and currents of the power grid nodes. Exploiting the traits of the power grid, processing the nodes of a row within a grid requires 5*N*-4 multiplications and 3(*N*-1) additions [5], where *N* is the number of the nodes in this row.

Another sub-function called "Voltage Difference Adjustment (VDA)" is used to control convergence for a 3-D power distribution network. In each iteration, the procedure updates the voltage of the nodes within each layer by distributing the resulting voltage difference at the power/ground pads produced during the previous state.

IV. EXPERIMENTAL RESULTS

The 3-D VP power grid analysis technique is implemented with C/C++. A set of benchmark circuits is used to evaluate the accuracy of the proposed method. The largest problem that SPICE can handle with the available resources is up to 230K nodes. The simulations are carried out on a Linux workstation with 2.67 GHz CPU and a memory size of 3 GB.

To compare the runtime of the VP method with other power grid analysis methods, the PCG algorithm is applied to the synthesized set of benchmark circuits. The related results are reported in Table I. The maximum error for the applied methods is set to 0.5 mV according to [12].

In column 1, there are six 3-D test circuits extended from the example benchmark circuits in [11], which have the same TSV distribution but different size. The number of nodes in these test circuits is listed in column 2. The columns 3 and 4, 5 and 6, 7 and 8 report the memory and time used by the VP method, the PCG method, and SPICE, respectively. SPICE runs out of memory for circuits C3 to C5.

Simulation results show that the 3-D VP method outperforms the PCG algorithm. Consider circuit C5 for example, the runtime of the PCG algorithm is almost 1.5 hours, while the VP method requires only 3.5 minutes. As the number of nodes increases, the memory used in PCG is almost three times larger than that of the VP method. Additionally, the improvement in computational time increases for larger circuits. When the number of nodes in a 3-D circuit is just *30K*, the speedup achieved by the VP method is 10× over the PCG technique. For larger benchmark circuits, such as *12M* nodes in circuit C5, the speedup increases to 20×. Consequently, more complex 3-D power distribution networks, due to an increasing number of tiers, for example, are expected to benefit more from the VP method.

V. CONCLUSIONS

An efficient method for *IR* drop analysis of 3-D power distribution networks, based on the 2-D RB algorithm, is presented. The experimental results demonstrate that this method, called 3-D VP, extends the power grid analysis to a 3-D system with considerable improvements in accuracy, memory, and runtime as compared to other 2-D techniques adapted for 3-D circuits.

The 3-D VP method requires one third of the memory size used by the PCG technique, while achieving a 10× to 20× speedup. These improvements are expected to increase for larger circuits.

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TABLE I. MEMORY AND RUNTIME COMPARISON.

Circuit	# of nodes	Voltage Propagation		PCG [12]		SPICE	
		Memory (MB)	Time (sec)	Memory (MB)	Time (sec)	Memory (MB)	Time (sec)
C0	30K	1.5	0.516	3.1	6.063	330	512.7
C1	90K	3.2	1.453	7.8	22.47	1100	2905
C2	230K	6.9	3.625	18.5	50.71	3000	22394
C3	1M	27	15.75	77	264.8		
C4	3M	80	49.29	230	877.5		
C5	12M	322	219.7	880	4843		