

Design of an intrinsically-linear double-VCO-based ADC with 2nd-order noise shaping

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Abstract—This paper presents the modeling and design consideration of a time-based ADC architecture that uses VCOs in a high-linearity, 2nd-order noise-shaping delta-sigma ADC. Instead of driving the VCO by a continuous analog signal, which suffers from the nonlinearity problem of the VCO gain, the VCO is driven in an intrinsically linear way, by a time-domain PWM signal. The two discrete levels of the PWM waveform define only two operating points of the VCO, therefore guaranteeing linearity. In addition, the phase quantization error between two consecutive samples is generated by a phase detector and processed by a second VCO. Together with the output of the first VCO, a MASH 1-1 2nd-order noise-shaping VCO-based time-domain delta-sigma converter is obtained. Fabricated in 90nm CMOS technology, the SFDR is larger than 67dB without any calibration for a 20MHz bandwidth.

Index Terms—ADC, Gate-ring VCO, time-domain, Delta-sigma, Asynchronous Delta-sigma Modulator.

I. INTRODUCTION

With the continuous scaling of the CMOS technology according to Moore's law, digital integrated circuits benefit simultaneously from double the speed and half the area (cost) every two years. But the impact of Moore's law is different on analog integrated circuits, since their performances are fundamentally limited by the trade-off between speed, accuracy and power. The scaling boosts the transistor speed which may enable more high frequency applications, but for existing applications the scaling worsens the accuracy due to the increasing variability and shrinks the dynamic range due to the decreasing supply voltage, thus increases the design complexity. However, with ever faster transistors the time-domain accuracy is strongly enhanced, which may open the opportunity to novel analog circuit design in the time domain.

In recent years, several publications [1-4] have demonstrated that the ring VCO (voltage-controlled oscillator)-based time-domain delta-sigma ADC has many promising advantages compared with the conventional voltage-based ones, such as an order of magnitude reduction in chip area, a high DC gain and a reduced design complexity by replacing many circuit blocks such as the integrators, DAC, quantizer... [5] by only a ring VCO and some standard digital blocks [1]. Besides these advantages, there are also inevitable drawbacks. The primary one is the severe nonlinearity of the K_{vco} (the voltage

to frequency conversion coefficient of the VCO), which limits the linearity of the published designs to mostly between 30-50dB [1][3][4]. As results it can not be used in many applications without special treatment such as digital calibration. Another consideration is that the VCO frequency is very sensitive to the ambient environment, such as the temperature or the power supply. To guarantee the chip performance, calibration needs to be performed frequently. Therefore a calibration-less or an intrinsically linear VCO-based ADC is in demand. Besides that, only 1st-order quantization noise shaping has been demonstrated in the published converters without the help of feedback loop or integrators, which brings back all the difficulties of the conventional delta-sigma modulators design.

This paper introduces the model and design considerations of the two innovations to use VCOs in a time-domain delta-sigma ADC, which are the guaranteed linearity without digital calibration and the 2nd-order quantization noise shaping without feedback loop and integrators.

The paper is organized as follows. The new architecture is presented in section II. The full operation principle is presented in section III A, and section III B and C will discuss the modeling and design considerations for each sub-block. The circuit implementation will be covered in section IV. Section V presents the measurement results and finally some conclusions are given in section VI.

II. THE LINEAR DOUBLE-VCO ARCHITECTURE

The proposed linearity solution is depicted in Fig. 1. The signal flow in both the time domain and the frequency domain is shown. We can observe that instead of driving the VCO by a commonly used continuous analog voltage or current signal, which has to suffer from the severe nonlinearity of K_{vco} , the VCO is now driven by a time-domain PWM (pulse width modulation) signal which has only two operating states: 'high level' or 'low level', therefore only two points from the K_{vco} nonlinear transfer curve will be used. As shown in the lower part of Fig. 1, the corresponding VCO oscillation frequency entering the integrator contains only two speeds (high and low), which is intrinsically linear. Therefore the nonlinearity of K_{vco} will be completely kicked out of the signal path and of the output spectrum. The motioned continuous analog signal to time-domain PWM signal conversion will be achieved on chip by a high-performance asynchronous delta-sigma modulator (ADSM) [6-8].

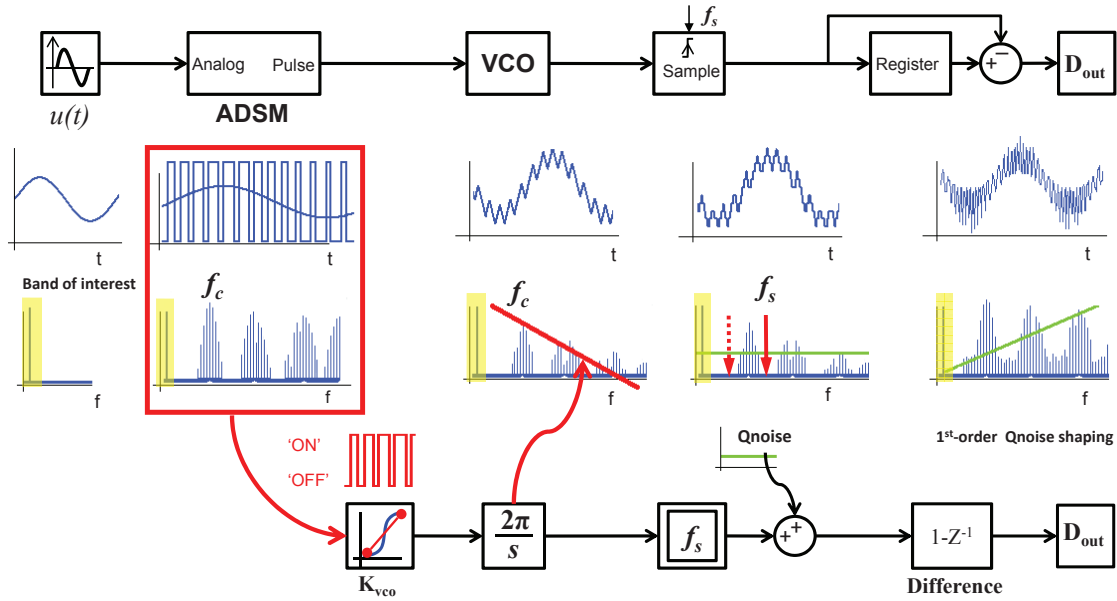


Figure 1. The schematic and the signal flow with the proposed method to linearize K_{vco} .

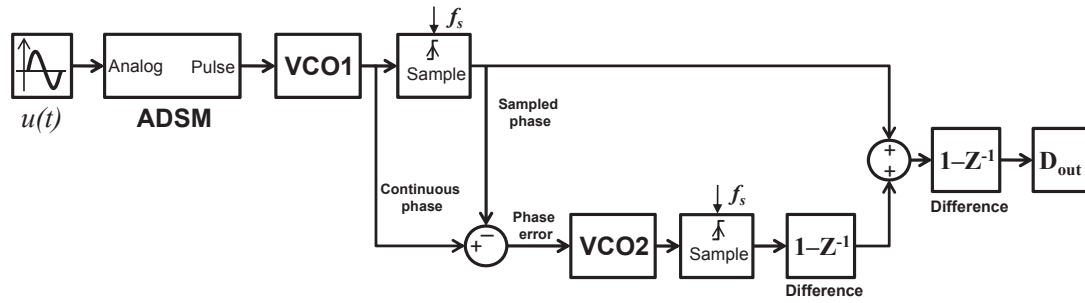


Figure 2. The block diagram of the ADC architecture.

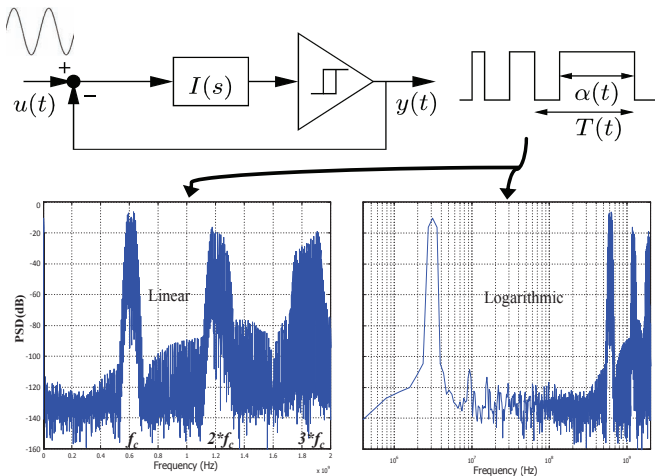


Figure 3. The 1st-order ADSM and its output spectrum (both on linear and logarithmic scale).

The other novelty of this paper is the 2nd-order noise shaping. The overall architecture is shown in Fig. 2, after the

quantization error is calculated by a subtract block, a second VCO (VCO2) is used to process it and add it back to the output of the first VCO (VCO1) in the digital domain, therefore achieving the 2nd-order quantization noise shaping similar to the conventional MASH converters. This is why we call it a double-VCO-based architecture.

III. SYSTEM-LEVEL DESIGN

A. Full system

As shown in Fig. 2, the full system block diagram of the proposed architecture consists of the ADSM, VCO1, VCO2 and some standard digital blocks. The ADSM is as described in [7], converting the amplitude of the input signal into self-oscillating PWM waveforms. When the input amplitude is zero, it oscillates at the self-oscillation frequency f_c , which is determined by the loop coefficient and will be discussed in detail later. Fig. 3 shows a first-order ADSM and a typical output waveform spectrum with a large OCR (over cycling ratio: the ratio between f_c and the input signal bandwidth) and a small M (modulation depth: the ratio between the input signal amplitude and the reference value of the feedback path). The x-axis is linear in the lower left plot and logarithmic in the lower

right plot of Fig. 3. As seen on the left, the ADSM output spectrum contains some sidebands around the multiples of the average oscillation frequency [9]. On the right plot we can see that the baseband information is preserved.

VCO1 is connected after the ADSM. First, it converts the two levels of the PWM pulse to two oscillation frequencies (f_{high} and f_{low}) according to K_{vco} . It will be mentioned later, the maximum achievable signal to noise ratio (SNR) is determined by the minimum delay of a single VCO delay stage, not the actual VCO oscillating frequency. But the value of the higher oscillation frequency f_{high} will influence the selection of the following blocks. If f_{high} is larger than the sampling frequency $f_s/2$, it means that some of the VCO delay stages will alter more than once within a sampling period. This requires a multi-bit counter [1] to successfully sense the phase output. The higher the VCO frequency, the deeper the counter. In contrast, if f_{high} is smaller than $f_s/2$, none of the VCO delay stages will change more than once. This implies that a single-bit counter or a register can be sufficient to sense the output. To simplify the design, we will choose a proper number of delay stages to ensure that f_{high} is always smaller than $f_s/2$.

As we can see from Fig.1, the output phase of the VCO1 is sampled at the sampling frequency f_s which is different from f_c . Ideally, the sampling frequency is located slightly before or after f_c where high-frequency spurs do not exist and the widest clean-frequency bands are available. After the sampling occurs, the clean bands and its multiples are folded back and added to the baseband. Therefore theoretically the baseband spectrum should not be influenced by those high-frequency spurs since they should be clean. But in practice, according to the spectrum analysis of the ADSM output [9], the widths of the clean bands gradually shrink when approaching the higher frequencies; a few high-frequency components will be folded back and potentially affect the baseband as in-band noise. Fortunately, their magnitudes also become smaller at higher frequency. In addition, similar to conventional delta-sigma modulators; the signal transfer function of the VCO-based ADC behaves as a low-pass filter with a corner frequency of f_s/π [8]. Therefore those high-frequency components will be attenuated by 20dB/dec before sampling, alleviating their influences. In the proposed 2nd-order topology, a second-order low-pass filter with 40dB/dec attenuation will further alleviate such impact. As an example, the signal to noise ratio simulation of a fixed sampling frequency f_s (640MHz) and modulation depth M (0.4, 0.45) as a function of the self-oscillation frequency f_c is plotted in Fig.4. When f_c approaches f_s , it means the corresponding bands which are folded back to baseband is not clean, some high-frequency spurs will show there, thus a significant SNR drop is noticed. In contrast, when f_c is far from f_s , there will be no spur folded into the baseband, thus only the shaped quantization noise will be there. As we can see from Fig. 4, the green part is quite flat; the system-level simulation shows that the SNR is relatively constant across the clean band of the ADSM output. Therefore the performance of the ADC is insensitive to the absolute value of f_c . Only the relative position between f_c and f_s is important. Furthermore this property offers some flexibility and margin for the ADSM design.

To achieve the 2nd-order noise shaping, a similar structure like the conventional MASH delta-sigma modulator is

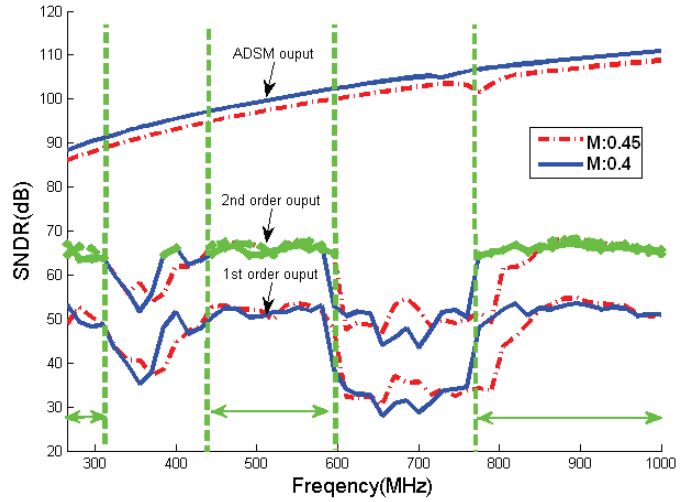


Figure 4. SNDR as a function of f_c when f_s (640MHz) and M (0.4&0.45) are fixed

proposed: the phase quantization error is derived by subtracting the sampled phase from the continuous one, as depicted in Fig. 2. After two times differentiation, only the quantization noise of the second VCO appears in the final output, therefore enabling the 2nd-order noise shaping of the VCO-based time-domain ADC. The other merit of this MASH topology is that the open loop leads to absolute stability; therefore the integrator coefficient can be designed very large compared to the conventional feedback modulators.

B. ADSM

As shown in the upper part of Fig. 3, the ADSM is a closed-loop system that consists of an integrator $I(s)$, a hysteresis comparator and a feedback path which is formed by a single-bit DAC. It converts the amplitude information of the analog input signal $u(t)$ to a time-domain PWM signal without information loss. The pulse width $\alpha(t)$ and the actual oscillation frequency $f(t)$ are analyzed in [8] as:

$$\frac{\alpha(t)}{T(t)} = \frac{1+u(t)}{2} \quad \text{and} \quad \frac{f(t)}{f_c} = 1-u^2(t) \quad (1)$$

$$\text{with} \quad |u(t)| < 1, \quad f(t) = \frac{1}{T(t)}$$

In the first-order ADSM the self-oscillation frequency f_c is determined as follows:

$$f_c = \frac{\pi}{2h} f_{unity} \quad (2)$$

where h represents the hysteresis value of the comparator and f_{unity} is the integrator unity gain frequency. As depicted in (2), if the self-oscillation frequency f_c is fixed regard to the sampling frequency, then a design tradeoff can be made between the integrator f_{unity} and the comparator hysteresis. Since most of the power is consumed by the analog integrator, a smaller f_{unity} will lead to a power-optimized design, although some difficulties transfer to design the hysteresis comparator.

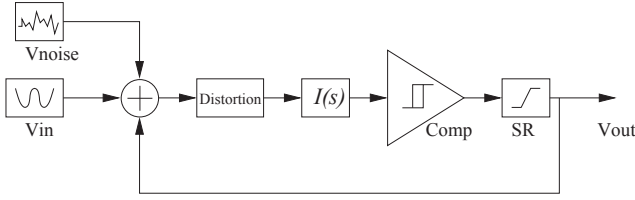


Figure 5. Simulink model of the ADSM with nonidealities.

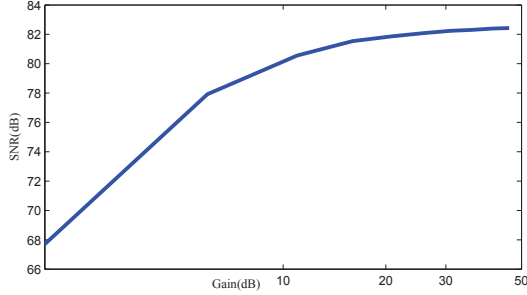


Figure 6. ADSM SNR as a function of the integrator opamp gain.

There is no sampling in this type of modulator; therefore the output PWM signal is free of quantization noise. Theoretically, this ADSM output signal also contains some in-band harmonic distortion spurs, as has been analyzed in [6][8]. The worst-case third-harmonic distortion coefficient, which is when the third harmonic distortion spurs are located at the signal bandwidth, can be estimated by:

$$\Delta_3 = \frac{\pi^2}{216} \frac{M^2}{(1-M^2/2)^2} \frac{1}{OCR^2} \quad (3)$$

According to the ADC's system requirements, such as SFDR, the required value of modulation depth (M) and OCR can be determined. As shown in Fig. 3, once a relatively small M and large OCR are chosen, the harmonic distortion spurs are insignificant and will be eventually below the noise floor. As shown in Fig 4, the simulated SNR is improving with increasing f_c and worsening with increasing value of M.

Although the harmonic distortion is important and needs to be carefully considered, more importantly in this design is the value of M which strongly affects the width of the clean bands (1). As seen from Fig 4, when M is increased from 0.4 to 0.45, the available clean bands (green) shrink about 40MHz. Therefore, we have to limit M in our design in order to have enough frequency margins to guarantee a clean band. Similarly, from (3) (1) a larger OCR not only offers a better theoretical distortion performance, it also provides wider clean bands for the same M. Therefore the OCR should be designed as large as possible for given power consumption and technology constrains. In our design f_c is chosen to be 560MHz, hence the OCR equals 28 for a 20MHz input bandwidth. As shown in Fig. 4, this results in about 150 MHz clean bands with the targeted specifications.

Fig. 5 shows the ADSM Matlab-Simulink model with non-idealities such as integrator opamp finite gain/GBW, nonlinearities and comparator slew rate (SR). The system-level

simulations show that more than 80dB SNDR is achieved with the first-order ADSM. The corresponding requirement on non-idealities can be obtained by simulations. An example of the SNR versus opamp gain simulation is shown in Fig 6. We can see that once the integrator opamp gain is above 30dB the influence on the performance can be negligible.

C. VCOs

The conventional VCO-based time-domain ADC and its corresponding 1st-order noise shaping have been analyzed in detail in [4]. The theoretical signal to quantization noise ratio can be expressed as:

$$SNR \approx 6.02 \log_2 \left(\frac{f_{tune} N}{f_s} \right) + 30 \log(OSR) - 3.41 \quad (4)$$

where f_{tune} is the tuning range of the VCO that equals the input dynamic range times the K_{vco} . N is the number of VCO output phases. When we consider the two-states driving scheme resulting from the preceding ADSM, the $f_{tune} N$ factor in (4) simply becomes either the maximum or the minimum speed of a single VCO delay stage. The SNR can thus be approximated as:

$$SNR \approx 6.02 \log_2 \left(\frac{f_{diff}}{f_s} \right) + 30 \log(OSR) - 3.41 \quad (5)$$

where f_{diff} is the difference between the maximum and minimum speed of a single VCO delay stage. When the minimum speed is much smaller than the maximum one, f_{diff} can be approximated by the maximum speed of the VCO delay stage. OSR is the oversampling ratio, which equals to f_s over two times the input bandwidth. As we can see, f_s appears in both parts of equation (5): the first part corresponds to the counting performance (how many different phase steps can be detected within one clock period); the second part is the conventional 1st-order noise shaping. As a conclusion, for a given technology and input bandwidth, doubling f_s will only add 3dB to the SNR instead of 9dB for a conventional 1st-order noise shaping. But each time the transistor speed doubles, 6dB will be added to the SNR, showing that the VCO-based ADC benefits more from the technology scaling.

Instead of using only one VCO and be restrict to 1st-order noise shaping, the second VCO (VCO2) is proposed to deal with the quantization error of VCO1, similar to the MASH topology. Unfortunately, the phase quantization error of VCO1 is a continuous signal. Therefore the VCO2 has to operate in continuous mode and the K_{vco2} nonlinearity is unavoidable. Fortunately, this nonlinearity at the final ADC output will be 1st-order shaped already by VCO1. Therefore, the linearity requirement for VCO2 is reduced. The system-level simulation shows that with a 7-bit linearity for VCO2, the overall linearity of the ADC can be more than 12-bit without digital calibration. A second remark is that if VCO2 is used, the first VCO must avoid the state 'OFF' for the lowest frequency: when VCO1 would be fully stopped, the equivalent input quantization error becomes a DC value (a fixed sampled phase minus an unchanged continuous phase); when passed through VCO2, the integration effect will show a large low-frequency variation, destroying the 2nd-order noise shaping. Therefore the lower frequency of VCO1 must be chosen at a low idle value instead of zero.

In conventional delta-sigma modulators, the clock-jitter-induced noise in the feedback path is directly added to the input signal; hence it is not possible to separate them afterwards. The proposed topology is an open-loop topology without feedback path. Thus the clock-jitter-induced sampling error will not be added to the input signal. Furthermore such error will be considered as part of its quantization noise and will be processed by VCO2, therefore making it theoretically possible to cancel it later in the digital part.

As has been analyzed in [4][5], the phase noise of both VCOs are processed in the same way as its quantization noise, which is 1st-order shaped. Hence the phase noise in the VCOs can be modeled as an extra thermal noise source at the input. The exact specifications are determined while taking into account the available noise budget. In our design, the phase noise specifications of VCO1 and VCO2 are -110dBc/Hz at 1MHz offset from its f_{high} and -100dBc/Hz at 1MHz offset from its free running frequency.

Fig. 7 shows the Simulink simulated SNR of the first-order VCO-based (left) and the second-order VCO-based (right) ADC. For the targeted 20MHz input bandwidth, a 640MHz sampling frequency and 560MHz self oscillation frequency as chosen. Both the first- and second-order noise shaping are clearly observed. The signal to noise ratio of 53.3dB and 70dB is obtained in the first- and the second-order case respectively.

IV. CIRCUIT IMPLEMENTATION

A. ADSM

As shown in Fig. 8, the first-order ADSM uses an active-RC integrator for good linearity. From the system-level simulation, the gain and GBW requirements for the amplifier are determined. As has been shown in Fig. 6, 30dB DC gain results in less than 1 dB loss of SNR. Since no sampling occurs in this stage, the amplifier GBW is not related to the sampling frequency and can be designed independently, other than a multiple of f_s in a conventional modulator, in this design the amplifier GBW is designed to equal f_c , which is in reality small then f_s . The extra loop delay introduced by finite GBW can be compensated by reducing the comparator hysteresis value. Such a hysteresis comparator is designed similar to the one described in [7].

B. VCOs

As shown in Fig. 9, VCO1 is designed with 31 delay cells. The ‘ON’ frequency of VCO1 is designed to be slightly below

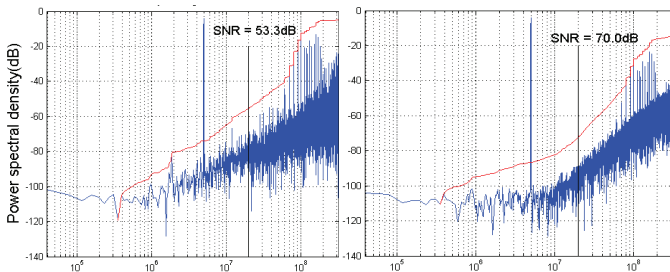


Figure 7. System-level simulation of 20MHz input bandwidth, $f_s=640\text{MHz}$ and $f_c=560\text{MHz}$.

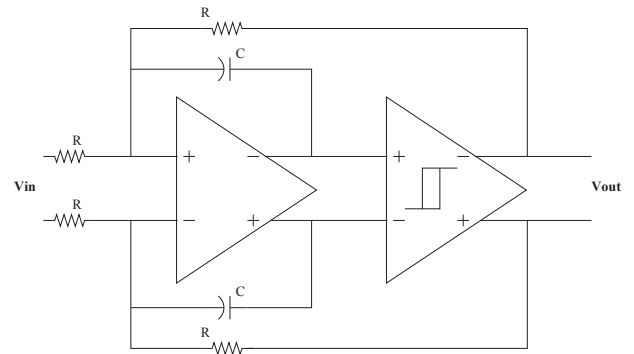


Figure 8. ADSM schematic with active-RC integrator.

$f_s/2$ to avoid phase overflow and to avoid a multi-bit counter as mentioned in III.A. The delay cell is designed similarly to a single-ended inverter with both PMOS and NMOS current-starving switches. Two small bypass transistors connected to bias voltage Vb1 and Vb2 are placed in parallel with those switches; therefore a small amount of current constantly drives the delay stage and avoids VCO1’s full stop during the ‘OFF’ state.

VCO2 is designed in a similar way but with continuous input. It comprises of 31 delay cells. Again the simple inverter-based delay cell is adopted. Since its phase noise specification is more relaxed compared with VCO1, smaller-sized transistors are used.

C. Phase error detector

The phase error is detected by a mathematical subtraction operation between the continuous phase and the sampled phase of VCO1. Such a detector is implemented by digital XOR gates. Each gate is responsible for one phase output node. Once a phase error is detected on that node, a corresponding control signal is generated to drive a unit cell of a 5-bit current-steering DAC. The output of this DAC, which is an analog signal, then drives VCO2.

V. MEASUREMENT RESULTS

A prototype converter has been fabricated in standard 1P9M 90nm CMOS technology. Fig. 10 shows the die photograph. The core size is 0.026mm^2 including both the ADSM and the VCOs.

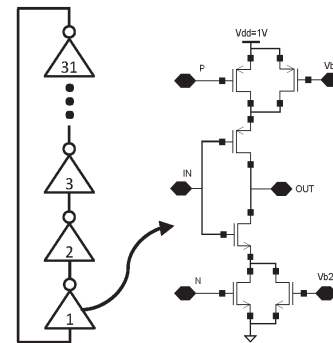


Figure 9. The VCO1 schematic and its delay cell.

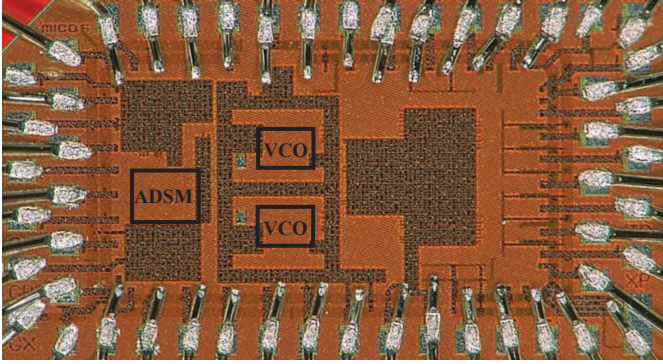


Figure 10. The die photograph of the VCO-based ADC

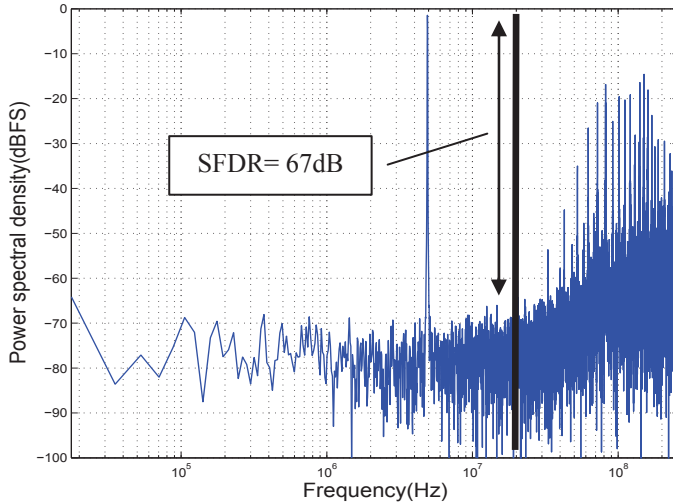


Figure 11. Measured power spectral density of the ADC after VCO1.

For the ADSM, 67.3dB SNDR is measured for 20MHz bandwidth, which means that the signal entering the VCO is qualified. The power consumption is 6.3mW for both the ADSM and VCO1. Fig. 11 shows the first part of the ADC (ADSM + VCO1) measured power spectral density for an input test tone at 4.3MHz. The peak SFDR, DR, SNR and SNDR are 67dB, 53dB, 46.2dB and 46dB respectively. The detailed performance of the ADSM and the ADC is listed in table I. This work demonstrates the good SFDR, linearity and DR of this ADC without any calibration.

Unfortunately, due to some layout error, causing poor isolation between digital circuits and the sensitive analog part, the interference of the switching noise worsens the noise floor; further noise shaping by the second VCO could be observed but did not reduce the total in-band noise. Therefore, the further improvement of the SNR could not be measured.

VI. CONCLUSION

This paper has presented a novel ADC architecture using two VCOs to achieve a time-domain ADC. The VCO is driven by a high-performance ADSM which converts the continuous analog input amplitude to a self-oscillating PWM pulse. Only two points on the K_{vco} nonlinear transfer curve are selected, hence the linearity is guaranteed. Furthermore 2nd-order noise shaping is obtained with a MASH 1-1 topology. The measured SFDR is 67dB without calibration for a 20MHz bandwidth in a 90nm CMOS technology. This work has demonstrated that the VCO-based time-domain ADC has a strong potential with scaled technologies and that it is able to overcome its drawbacks such as VCO nonlinearity or low-order noise shaping by adopting novel circuit techniques.

TABLE I. PERFORMANCE SUMMARY

Technology		90nm CMOS	
Supply voltage		1V	
Calibration		NO	
Bandwidth		20MHz	
ADSM		ADC (ADSM + VCO1)	
f_c	560 MHz	f_s	640 MHz
M	0.5	SFDR	67 dB
SFDR	74 dB	DR	53 dB
SNR	68.4 dB	SNR	46.2 dB
SNDR	67.3 dB	SNDR	46 dB
Power	3.1mW	Power	6.3mW
Active area	0.01 mm ²	Active area	0.026 mm ²

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