A Symbolic Technique for Automated Characterization of the Uniqueness and Similarity of Analog Circuit Design Features

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Abstract—This paper presents a technique for automated generation of hierarchical classification schemes to express the main similarities and differences between analog circuits. The produced classification schemes offer insight about the uniqueness and importance of specific design features in setting various performance attributes as well as the limiting factors of designs. Hence, the classification schemes serve as a systematic way of relating one circuit design to alternatives. The automatically produced classification schemes for a set of OpAmps are discussed.

I. INTRODUCTION

Circuit macromodels are very important in expressing the main characteristics of an analog circuit, e.g., the mathematical dependency of the voltages and currents of circuit nodes on the design variables, e.g., transistor dimensions [1], [2], and the expression of performance attributes as functions of the circuit design variables [3], [4]. The first type of macromodels are usually called structural models and the latter type are called box models. Circuit macromodels are mainly utilized for fast performance evaluation, automated generation of symbolic equations for circuit design and synthesis, and gaining insight into circuit operation. Existing macromodeling methods can successfully address a variety of performance attributes, including small-signal AC performance [1], [3], weakly nonlinear distortion analysis [5], [6], and large-signal analysis [4].

A very interesting extension of the existing macromodeling techniques is to generate descriptions that not only characterize a circuit in isolation but systematically relate it to a group of circuits with similar functionality. Highlighting the common and unique design features of different circuits, e.g., the similar and distinct symbolic terms of their pole and zero expressions helps in understanding the performance advantages and limitations of a circuit compared to other circuits, the performance impact of circuit nodes and their structural connections to other nodes, the conditions under which alternative circuits exhibit similar performance, and the design aspects that boost or limit the performance of a circuit as compared to alternatives. To the best of our knowledge, automated generation of analog circuit classification schemes has not been studied before. This problem is difficult because selecting the best design features to distinguish among circuits is an NP-complete problem.

This paper presents a symbolic technique for automated generation of hierarchical classification schemes to express the main similarities and differences between structurally different analog circuits with similar functionality. The produced schemes offer insight through symbolic expressions that characterize the similar and dissimilar features. The method includes three main steps: (i) producing the possible sets of classification criteria, (ii) analyzing the criteria sets with respect to their potential of finding the main similar and dissimilar features, and (iii) building the hierarchical classification scheme such that the main criteria are expressed first in the scheme. The separation score for classification is based on entropy [7] and we give experimental results for a collection of OpAmp circuits.

II. PROBLEM DESCRIPTION

Given a set of circuits, $C_1$, $C_2$, ..., $C_n$, the goal is to build a symbolic description (model) that expresses the main similarities and differences with respect to how the structural (topological) features of the circuit designs influence performance. A good classification scheme should easily distinguish the circuits, e.g., there should be a minimum number of criteria that separates any circuit from the other circuits in the set with respect to the considered attributes.

Figure 1 illustrates the theoretical formulation of the problem. Three circuits $C_i$ are shown in the figure. Each circuit is described by the set of its nodes $V_i$. This captures the circuit structure, which is important to understand how similarities and differences correlate to the structural elements of the circuits. Nodes are connected through functions $F_{k,p}$ to describe the coupling between nodes. The nature of the functions $F$ depends on the performance attributes used for classifications. For AC performance, functions $F$ are continuous functions in the $s$-domain. For example, Figure 3 shows the node structure of three current mirrors. Functions $F$, describing the...
AC coupling between nodes, correspond to the arc labels in the figure.

Producing a classification scheme for the set of circuits $C_i$ should (i) identify the nature of criteria used in finding similarities and differences between the circuits and (ii) find the topological features that realize the similarities and differences. There are always more criteria sets possible to classify circuits. For example in Figure 1(a), the characteristics of the nodes $V_{1,i}$, $V_{2,j}$ and $V_{3,j}$ along curve $D_1$ could be used for distinguishing the circuits. Alternatively, nodes $V_{1,i}$, $V_{2,j}$ and $V_{3,j}$ along curve $D_2$ could be used for classification. The two curves generate different classification schemes.

Each possible criteria set (corresponding to a curve $D_k$) defines the space for classification. For example, Figure 1(b) shows the classification scheme using the features of the nodes along curve $D_1$. Node $V_{1,i}$ of circuit $C_1$ and node $V_{2,j}$ are clustered together as they share similar features, and node $V_{3,j}$ forms a different cluster as its features are different. The node features used in this classification scheme are defined by set $SF_1$ which relates to performance $P_1$. For example, for $AC$ domain, the shared node features in set $SF$ could represent the common symbolic expressions of the poles of the two nodes, and performance $P_1$ defines the position of the common pole on the magnitude and phase response of the circuit. At the second level, the remaining nodes $V_{2,i}$ and $V_{3,i}$ are placed in separate categories according to the node features $SF_2$. Figure 1(c) illustrates a different scheme in which the nodes are classified according to the criteria induced by the nodes along curve $D_2$. Sets $SF_i$ describe the classification criteria and the nodes (on the curve) corresponding to a given $SF$ which defines the related topological features.

The design features present in a set $SF_k$ are defined based on the impact of the nodes. The impact of a node includes the coupling to all other nodes in the circuits, e.g., all functions $F$ through which the node is connected to the rest of the circuit. For example, the impact of node $V_{1,i}$ of circuit $C_1$ in Figure 1(a) is characterized by functions $F_{1,3}$, the coupling to node $V_{out}$, and functions $F_{1,1}$ and $F_{1,2}$, the coupling to node $V_{in}$.

The quality of a classification scheme depends on the relevance of the distinguishing criteria, including their impact on performance, and insight on circuit design, e.g., uniqueness of a criterion in controlling a certain performance attribute and brevity of the related expression [7]. Good distinguishing criteria have short mathematical expressions and are unique and important with respect to setting performance attributes.

### III. AUTOMATED GENERATION OF CLASSIFICATION SCHEMES

Figure 2 illustrates the proposed algorithm to automatically construct circuit classification schemes. The first step produces the set of classification curves $D_i$ which define implicitly the alternative criteria (circuit node features) that can be used for describing the similarities and differences between the circuit nodes. Then, the curves are ordered to reflect any ordering specific to the circuit. For example, design features describing the signal flow between the circuit nodes must be ordered to reflect the flow: curve $D_i$ is before curve $D_j$, if all the nodes of $D_i$ have outward edges to the nodes of curve $D_j$. The curve with the highest cost is selected to produce the next level of the classification scheme (steps (6)-(8)). Each entry of the new level represents clusters of similar nodes. The procedure continues with generating the next classification level based on the remaining curves $D_i$. Well matched nodes are on top of the hierarchy and unmatched (separating) nodes at the bottom.

The remaining of this section illustrates the proposed algorithm’s steps for generating the classification scheme for frequency domain performance. The discussion refers to a set of five 2-stage operational amplifiers (OpAmp) circuits using different current mirror loads [8]. Circuit $C_1$ uses a simple current mirror (SCM), circuit $C_2$ a Wilson current mirror (WCM), circuit $C_3$ an Improved Wilson current mirror (IWCM), circuit $C_4$ a cascode current mirror (CCM), and circuit $C_5$ a wide swing cascode current mirror (WSCCM).

First, the algorithm constructs the specific circuit model used for classification. For $AC$-domain classification, a structural model, called Uncoupled Building-Block Behavioral model (UBBB), is produced for every circuit using the method described in [1]. The macromodels are directed signal-flow graphs, with nodes corresponding to every node in the circuit, and arcs capturing the signal coupling between nodes, also including poles. The initial coupled macromodel describes every circuit node $n_x$ as:

$$V_x = \frac{R_x}{1 + sR_x C_x} \times \sum_j (sC_{mj} \pm G_{mj})V_j$$
$R_x$ and $C_x$ form the node’s pole, and $sC_{mj} + G_{mj}$ represents VCCSs from the macromodel of block $n_x$.

Next, the nodal cross-correlations in the coupled circuit model are eliminated. The decoupling sequence is determined by using the signal path tracing algorithm [2], and then the feedback dependencies between internal nodes are replaced by equivalent input dependencies.

Figure 3 presents the resulting UBBB models for SCM, WCM, and IWCM current mirror circuits. Each model indicates the circuit nodes, the poles at the circuit nodes, and the coupling arcs between the nodes labeled by their symbolic expressions. For example, $Pole_1$ for the SCM circuit is expressed as:

$$gmd_4 + gmd_3 + gmg_3$$

The second step of the classification scheme generation method identifies the possible classification curves $D_i$ by finding the circuit nodes that offer similar behavior. Each matched group includes nodes from different circuits (two nodes of the same circuit cannot be in the same group), such that groups of maximum size are produced. Finding groups of maximum size is necessary because this step attempts to identify the maximum amount of similarities (matching) between the nodes of the circuit set. The actual matching procedure uses an optimization method based on Simulated Annealing that minimizes the following cost function:

$$COST_{matching} = \alpha \times N + \beta \times TotalError$$

$\alpha$ and $\beta$ are weights associated with the two terms. $N$ represents the total number of matched groups. The total error term is the cumulative error over the entire set of groups. For a specific group, the error shows the differences in the symbolic expressions of the matched circuit nodes, considering both the node’s pole and the arcs coupling to the other nodes.

The matching procedure generates groups (clusters) of matched nodes from different circuits. For the set of five OpAmps, the result of the matching procedure includes 17 groups, all having a zero matching error (Figure 4).

The third step of the algorithm uses the signal path tracing algorithm [2] and the macromodel decoupling sequence [1] to further cluster the 17 groups into the level sets from Figure 4. The node ordering fixed by the signal path tracing algorithm decides the sequencing of the these clusters.

The resulting classification scheme is a hierarchical graph. The upper levels of the scheme refer to criteria that produce the best matching of the circuits, so that the more dominant similarities are on top and differences are at the bottom in the hierarchy.

Entropy is used to describe similarities and differences between circuits and is inspired by classification procedures in data mining [7]. We define the cluster’s information content:

$$Info(C_k) = - \sum_{i=1}^{N} p_i \log N p_i$$

$N$ is the total number of circuits with nodes in cluster $C_k$ and $p_i$ is the probability that a circuit from cluster $C_k$ is associated with a set of similar nodes. For each set $G_j$ of similar nodes in cluster $C_k$, the probability is expressed as: $|G_j|/|C_k|$. This measure gives information about the distribution of nodes within the cluster’s sets of similar nodes as well as the distribution of sets within the cluster: it equals zero when all circuits in the cluster form a single set of similar nodes, and is maximum when each circuit forms its own set within the cluster (or zero matching). If two clusters have equal cost, the order is decided based on the number of sets of similar nodes contained in each cluster.

The UBBB macromodel descriptions used for classification offer insight into the operation of the circuits [1]. As a result, the produced classification scheme from Figure 4 can also be correlated with the frequency domain performance of the circuits. Figure 5 illustrates specific AC performance for the considered OpAmps, and highlights aspects that were inferred from the hierarchy in Figure 4. For example, for circuits $C_3$ and $C_4$, the same DC gain is fixed by the common resistive component of the poles of all circuit nodes (the poles of groups $G_7, G_{10}$ and $G_6, G_9$ are equivalent). In contrast, circuit
The capacitive component of the node’s pole of circuit differs by the symbolic expressions for their poles and zeros. This results in a similar slope of the phase plot as indicated located at the same points on the frequency axis for all circuits. Output nodes introduce non-dominant poles and zeros that are the differential pair bias, current mirror output, and amplifier circuit’s gain. Similarly, the difference in gain between therefore does not benefit from their influence on increasing mirror nodes: circuit the different features of the sets of the intermediate current circuit’s components, and the amplifier’s gain. Similarly, the difference in gain between the symbolic expressions related to DC gain, poles and zeros, and phase margin. The design variables (e.g., , , , etc.) that appear in the distinguishing symbolic expressions are an indication of the available flexibility in setting the positions of poles and zeros, deciding pole-zero separation and stability margin, and attempting pole-zero cancellation. The described methods can be further extended through improved circuit models to capture other performance attributes, such as linearity and noise aspects that are currently not considered from the UBBB models [1].

The AC transfer function’s phase plot in Figure 5 indicates that circuits , , and share the first pole fixed by the common symbolic expressions of groups and . Analyzing the symbolic expressions of the edges from groups and together with the equivalent groups indicates the zero distribution at the intermediate current mirror nodes between circuits , , and . Since the poles at these nodes are not matched , the differences in the phase plots of these circuits can be located in the Hz to Hz range. The common characteristics of the differential pair bias, current mirror output, and amplifier output nodes introduce non-dominant poles and zeros that are located at the same points on the frequency axis for all circuits. This results in a similar slope of the phase plot as indicated by groups , , and .

The hierarchy also helps in getting insight on an OpAmp’s flexibility in setting its pole and zero positions and their degree of separation as compared to other OpAmps. This can be important for compensation and obtaining a required phase margin. For example, considering the CM input cluster’s level of the hierarchy in Figure 4, circuits (or ) and differ by the symbolic expressions for their poles and zeros. The capacitive component of the node’s pole of circuit is defined by two additional device parameters, namely two variables. This suggests that circuit offers more flexibility than circuit (or ) in controlling the node’s pole position. The increased number of variables in the pole’s expression can offer more possibilities for setting the pole’s position, even though this position may be closer to the origin than for circuit (or ). Similarly, for the first intermediate current mirror node level, circuits and are distinguished by the associated outgoing edge. The added dependence on a variable for circuit potentially allows better control of the related zero position than for circuit , including for pole-zero cancellation.

IV. CONCLUSION

This paper presents a symbolic technique for automated generation of hierarchical classification schemes to indicate the main similarities and differences between structurally-different analog circuits. The method includes three main steps, producing the possible sets of classification criteria, analyzing the criteria sets with respect to their capability of distinguishing the circuit features, and building the hierarchical classification scheme to highlight the main classification criteria. The produced classification schemes offer insight, through symbolic expressions, about the similar and dissimilar circuit features, including the common and distinct symbolic sub-expressions related to DC gain, poles and zeros, and phase margin.

ACKNOWLEDGMENT

This work was supported by the major collaborative research National Science Foundation CreativeIT grant no. IIS 0856038.

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