Obstacle-Aware Multiple-Source Rectilinear Steiner Tree with Electromigration and IR-Drop Avoidance

Jin-Tai Yan  
Department of Computer Science and Information Engineering, Chung-Hua University, Hsinchu, Taiwan, R.O.C

Zhi-Wei Chen  
College of Engineering, Chung-Hua University, Hsinchu, Taiwan, R.O.C

Abstract—Based on the width determination of any current-driven connection for electromigration and IR-drop avoidance, an area-driven multiple-source routing tree can be firstly constructed to minimize the total wiring area with satisfying the current flow in Kirchhoff’s current laws and the electromigration and IR-drop constraints. Furthermore, some Steiner points can be assigned onto feasible locations to reduce the total wiring area under the electromigration and IR-drop constraints. Finally, an obstacle-aware multiple-source rectilinear Steiner tree can be constructed by assigning the obstacle-aware minimum-length physical paths for all the connections. Compared with Lienig’s multiple-source Steiner tree[7], the experimental results show that our proposed approach without any IR-drop constraint can reduce 10.5% of the total wiring area. Under 10%Vdd and 5%Vdd IR-drop constraints, the experimental results show that our proposed approach can satisfy 100% electromigration and IR-drop constraints and reduce 7.5% and 4.9% of the original total wiring area on the average for tested examples, respectively.

I. INTRODUCTION

In general, electronic interconnections in modern integrated circuits have an intended MTTF (mean time to failure) of at least 10 years. The failure of a single interconnection caused by electromigration can result in the failure of the entire circuit. At the end of the 1960s, the physicist J. R. Black developed an empirical model to estimate the MTTF of any interconnection and to take the electromigration factor into consideration[1] as follows:

\[ \text{MTTF} = \frac{A}{J} \exp\left(\frac{E_a}{kT}\right), \]

where \( A \) is a material constant based on the cross-sectional area of the interconnection, \( J \) is the current density, \( E_a \) is the activation energy, \( k \) is the Boltzmann constant, \( T \) is the temperature and \( n \) a scaling factor.

The MTTF mainly depends on temperature and current density due to electromigration. Unlike digital circuits, analog circuits must handle a multitude of different current levels, including extremely large currents in some applications. Hence, the interconnection must be designed with the current that will be imposed on it in mind. Interconnect with an insufficient width may be subject to electromigration and eventually might cause the failure of the circuit at any time during its lifetime [1-3]. For analog signal wires, the DC currents where the metal is subject to an electron wind from a constant direction are considered. Because the ongoing reduction of circuit feature sizes has aggravated the electromigration problem, it becomes crucial to address the problems of current densities and electromigration during the routing of the interconnections for analog circuits.

In this paper, based on the width determination of any current-driven connection for electromigration and IR-drop avoidance, an area-driven multiple-source routing tree can be firstly constructed to minimize the total wiring area with satisfying the current flow in Kirchhoff’s current laws and the electromigration and IR-drop constraints. Furthermore, some Steiner points can be assigned onto feasible locations to reduce the total wiring area under the electromigration and IR-drop constraints. Finally, an obstacle-aware multiple-source rectilinear Steiner tree can be constructed by assigning the obstacle-aware minimum-length physical paths for all the connections.

II. PRELIMINARIES AND PROBLEM FORMULATION

In current-driven analog circuits, the determination of the realistic current value of each terminal in a signal net is important. Most approaches[4-8] use the equivalent current value to model the current value of any terminal in a signal net.
By simulating a circuit netlist, a set of the current values is manually attached to the terminals in the schematic netlist. Furthermore, each terminal is labeled with its equivalent root mean square (RMS) current value derived from the set of the simulated values at the terminal.

A. Width Determination for Electromigration and IR-Drop Avoidance

Given a connection, \( T_i \rightarrow T_j \), between two terminals, \( T_i \) and \( T_j \), based on the maximum tolerant current density, \( J_{\text{max}}(T_{\text{ref}}) \), in a given temperature, \( T_{\text{ref}} \), the maximum current value, \( I_{\text{max}} \), and the minimum process width, \( w_{\text{min}} \), the minimum width, \( w'_{ij} \), of the given connection, \( T_i \rightarrow T_j \), can be obtained to satisfy the electromigration constraint on the connection, \( T_i \rightarrow T_j \), as

\[
     w'_{ij} = \text{Max} \left\{ \frac{I_{ij,s}}{dJ_{\text{max}}(T_{\text{ref}})/dJ_{\text{peak}}}, w_{\text{min}} \right\}
\]

where \( I_{ij,s} \) is the current value on the connection, \( T_i \rightarrow T_j \), \( s \) is the safety factor, \( d \) is the thickness of the routing layer and \( J_{\text{peak}} \) is the layer-dependent peak current density. If the phenomenon of the peak current density is ignored, it is clear that \( w'_{ij} \) is equal to \( w_{\text{min}} \) if \( I_{ij,s} \leq \frac{w_{\text{max}} \cdot d \cdot J_{\text{max}}}{s} \) and \( w'_{ij} \) is equal to \( \frac{I_{ij,s}}{dJ_{\text{max}}(T_{\text{ref}})/dJ_{\text{peak}}} \) if \( I_{ij,s} > \frac{w_{\text{max}} \cdot d \cdot J_{\text{max}}}{s} \). On the other hand, the IR-drop, \( V_i - V_j \), between the voltages, \( V_i \) and \( V_j \), on the connection, \( T_i \rightarrow T_j \), must be constrained as IR-drop constraint to maintain the propagation quality of a signal net. It is assumed that \( V_{\text{max}} \) is the maximum tolerant IR-drop voltage of the connection, \( T_i \rightarrow T_j \). If the wiring resistance of the connection, \( T_i \rightarrow T_j \), is considered to satisfy IR-drop constraint, the minimum width, \( w'_{ij} \), of the connection, \( T_i \rightarrow T_j \), with the current value, \( I_{ij,s} \), and the connection length, \( L_{ij} \), can be obtained as

\[
     w'_{ij} = \frac{I_{ij,s}}{r_{\text{w}}}
\]

where \( r_{\text{w}} \) is the wiring resistance per unit square.

In order to simultaneously maintain the electromigration and IR-drop constraints on the connection, \( T_i \rightarrow T_j \), the width, \( w'_{ij} \), of the connection, \( T_i \rightarrow T_j \), can be determined as \( \text{Max} \{ w'_{ij}, w'_{ij} \} \). It is clear that \( w'_{ij} \) is equal to \( w'_{ij} \) if \( L_{ij,s} \leq \frac{w_{\text{max}} \cdot d \cdot J_{\text{max}}}{s} \) and \( w_{ij} \) is equal to \( \frac{I_{ij,s}}{V_{\text{w}}/s} \) if \( L_{ij,s} > \frac{w_{\text{max}} \cdot d \cdot J_{\text{max}}}{s} \). Based on the width determination for electromigration constraint, the width, \( w_{ij} \), for electromigration and IR-drop constraints can be determined and divided into four different conditions as follows:

\[
     w_{ij} = \begin{cases} 
     w_{\text{min}}, & \text{if } L_{ij} \leq \frac{w_{\text{max}} \cdot d \cdot J_{\text{max}}}{s} \text{ and } L_{ij} \leq \frac{w_{\text{max}} \cdot d \cdot J_{\text{max}}}{s} \\
     \frac{I_{ij,s}}{V_{\text{w}}/s}, & \text{if } L_{ij} \leq \frac{w_{\text{max}} \cdot d \cdot J_{\text{max}}}{s} \text{ and } L_{ij} > \frac{w_{\text{max}} \cdot d \cdot J_{\text{max}}}{s} \\
     \frac{I_{ij,s}}{dJ_{\text{max}}(T_{\text{ref}})/dJ_{\text{peak}}}, & \text{if } L_{ij} > \frac{w_{\text{max}} \cdot d \cdot J_{\text{max}}}{s} \text{ and } L_{ij} < \frac{w_{\text{max}} \cdot d \cdot J_{\text{max}}}{s} \\
     \frac{I_{ij,s}}{dJ_{\text{max}}(T_{\text{ref}})/dJ_{\text{peak}}}, & \text{if } L_{ij} > \frac{w_{\text{max}} \cdot d \cdot J_{\text{max}}}{s} \text{ and } L_{ij} > \frac{w_{\text{max}} \cdot d \cdot J_{\text{max}}}{s} 
     \end{cases}
\]

According to the electromigration-constrained current, \( \frac{w_{\text{min}} \cdot d \cdot J_{\text{max}}}{s} \), and IR-drop-constrained length, \( \frac{V_{\text{w}}}{I_{ij,s}} \), of the connection, \( T_i \rightarrow T_j \), the 2D distribution of the determined width of the connection, \( T_i \rightarrow T_j \), can be illustrated in Fig. 1.

B. Problem Formulation

Given a set of \( n \) terminals, \( \{T_1, T_2, \ldots, T_n\} \) including \( m \) current sources which is indicated by the negative RMS current values and \( (n-m) \) current sinks which is indicated by the positive RMS current values in a signal net, a set of \( r \) rectangular obstacles, \( \{O_1, O_2, \ldots, O_r\} \), the maximum current density, \( J_{\text{max}} \), the maximum IR-drop voltage, \( V_{\text{w}} \), and the minimum wire width, \( w_{\text{min}} \), based on the width determination of any current-driven connection for electromigration and IR-drop avoidance, the problem is to construct an obstacle-aware multiple-source rectilinear Steiner tree to minimize the total wiring area of the signal net with satisfying the current flow under Kirchoff’s current laws and the electromigration and IR-drop constraints. Given a set of \( 7 \) terminals, \( \{T_1, T_2, T_3, T_4, T_5, T_6, T_7\} \) including 3 current sources, \( T_1, T_2, \) and \( T_3 \), and 4 current sinks, \( T_4, T_5, T_6, \) and \( T_7 \), with a set of their equivalent RMS current values, \( \{-7, +8, +4, -3, -9, +2, +5\} \), in a signal net, and a set of 3 rectangular obstacles, \( \{O_1, O_2, O_3\} \) with the dimensions, 4x3, 3x3 and 3x2, in the locations, \( (2, 8), (6, 2), \) and \( (11, 8) \) as illustrated in Fig. 2(a). Based on the determined width for electromigration and IR-drop avoidance, an obstacle-aware multiple-source rectilinear Steiner tree is constructed to minimize the total wiring area with satisfying the current flow in Kirchoff’s current laws and the electromigration and IR-drop constraints as illustrated in Fig. 2(b) if it is assumed that the determined width for electromigration and IR-drop avoidance is obtained as

\[
     w_{ij} = \begin{cases} 
     0.2, & \text{if } L_{ij} \leq 2 \text{ and } L_{ij} \leq 20 \\
     0.1, & \text{if } L_{ij} \leq 2 \text{ and } L_{ij} > 20 \\
     0, & \text{if } L_{ij} > 2 \text{ and } L_{ij} \leq 10 \\
     0.1, & \text{if } L_{ij} > 2 \text{ and } L_{ij} > 10 
     \end{cases}
\]
III. OBSTACLE-WARE MULTIPLE-SOURCE STEINER TREE WITH ELECTROMIGRATION AND IR-DROP AVOIDANCE

For a multiple-source signal in analog circuits, it becomes more important to consider the effect of the electromigration and IR-drop in the construction of a rectilinear Steiner tree. Based on the width determination for electromigration and IR-drop avoidance, an efficient approach is proposed to minimize the total wiring area in the multiple-source rectilinear Steiner tree and the proposed approach is divided into three phases: Area-driven multiple-source routing tree with electromigration and IR-drop avoidance, Area-driven Steiner-point assignment under electromigration and IR-drop constraints and Obstacle-aware physical path assignment.

A. Area-Driven Multiple-Source Routing Tree with Electromigration and IR-Drop Avoidance

Given a set of $n$ terminals, $\{T_1, T_2, ..., T_n\}$, including $m$ current sources which is indicated by the negative RMS current values and $(n-m)$ current sinks which is indicated by the positive RMS current values in a signal net and a set of $r$ rectangular obstacles, $\{O_1, O_2, ..., O_r\}$, a routing tree must be constructed by building a set of two-endpoint connections, $T_i \rightarrow T_j$, from any current source, $T_i$, to any current sink, $T_j$, to satisfy the current requirement of all the current sinks in a signal net. Clearly, there are $(n-m)$ possible connections from any current source to all the current sinks and there are $m$ possible connections from all the current sources to any current sink. For any possible connection, $T_i \rightarrow T_j$, the maximum available current value, $I_{ij}$, can be obtained as Min($[I_i, I_j]$) according to the providing current on $T_i$ and the required current on $T_j$. To avoid the given obstacles in a routing plane, the obstacle-aware minimum distance, $L_{ij}$, of the connection, $T_i \rightarrow T_j$, can be obtained by computing the length of the obstacle-aware shortest path between the terminals, $T_i$ and $T_j$. Furthermore, the assigned width, $w_{ij}$, of the connection, $T_i \rightarrow T_j$, can be obtained according to the maximum available current value, $I_{ij}$, and the obstacle-aware minimum distance, $L_{ij}$, of the connection, $T_i \rightarrow T_j$, for electromigration and IR-drop constraints.

Based on the obstacle-aware minimum distances and the assigned widths of all the $m(n-m)$ possible connections, an area-driven multiple-source routing tree with electromigration and IR-drop avoidance can be constructed to minimize the total wiring area by using an iterative selection approach[8] with the assignment of minimum-length zero-current connections. Refer to the routing specification including a set of 4 source terminals and 3 sink terminals, $\{T_1, T_2, T_3, T_4, T_5, T_6\}$, and a set of 3 obstacles, $\{O_1, O_2, O_3\}$, in Fig. 2(a), the weight value, $(L_{ij}, w_{ij})$, and the routing-area penalty, $p_{ij}$, of any possible connection, $T_i \rightarrow T_j$, can be obtained in the iterative selection approach[8] and assigned on the connection, $T_i \rightarrow T_j$. After completing the selection process for all the 12 possible connections, an area-driven multiple-source routing tree with electromigration and IR-drop avoidance can be obtained and illustrated in Fig. 3. In the area-driven multiple-source routing tree, the pairs, $(L_{ij}, w_{ij})$, of the obstacle-aware minimum distance, $L_{ij}$, and the assigned width, $w_{ij}$, and the distributed current, $I_{ij}$, of 6 selected connections are assigned and the final total wiring area is obtained as 15.0. 

Fig. 2 Obstacle-aware multiple-source rectilinear Steiner tree with electromigration and IR-drop avoidance

Fig. 3 Area-driven multiple-source routing tree with electromigration and IR-drop avoidance
According to the attached current value and the 
\( V_i - V_j \), Manhattan wirelength of the given connection. Furthermore, a
given connection with the assigned P-oriented(C-oriented or V-oriented) width, the connection can be defined as a P-oriented(C-oriented or V-oriented) connection.

Based on the classification of three kinds of connections, P-V or C-V merging process can be obtained as

\[
\begin{align*}
T_i \rightarrow T_k, & \quad \text{in P-P, P-C or C-C merging process can be obtained as} \\
\text{if } (I_{i,j} + I_{j,k}) \leq \frac{w_{\text{wire}} \cdot d_{\text{max}}}{s}, \\
\text{if } (I_{i,j} + I_{j,k}) > \frac{w_{\text{wire}} \cdot d_{\text{max}}}{s}.
\end{align*}
\]

Furthermore, it is assumed that the connection, \( T_i \rightarrow T_k \), in P-V or C-V merging process is a V-oriented connection and the voltage, \( V_s \), of the Steiner point, S, can be obtained as

\[
V_s = V_j + I_{i,j} \left( \frac{L_{i,j} - L_{s,j}}{r_L} \right) w_j.
\]

In V-V merging process, it is clear that the voltage of the terminals, \( T_j \) and \( T_k \), in two V-oriented connections, \( T_j \rightarrow T_j \) and \( T_i \rightarrow T_k \), is \( (V_j, V_{\text{IR}}^{\max}) \). To minimize the total wiring area, \( L_{i,j}w_{ij} + (L_{i,j} - L_{s,j})w_{ij} + (L_{i,j} - L_{s,j})w_{ij} \), of the three connection, \( T_i \rightarrow T_j \), \( T_j \rightarrow T_k \) and \( T_i \rightarrow T_k \), under the IR-drop constraint, the optimal voltage, \( V_s \), of the Steiner point, S, can be obtained as

\[
V_s = V_j - \sqrt{\frac{I_{i,j} + I_{j,k}}{I_{i,j} + I_{j,k}} + \frac{I_{i,j} - I_{j,k}}{I_{i,j} + I_{j,k}}} y_{\text{max}}.
\]

Based on the optimal voltage, \( V_s \), of the Steiner point, S, the final widths, \( w_{i,j} \) and \( w_{k,j} \), of the three connections, \( T_i \rightarrow T_j \), \( T_j \rightarrow T_k \) and \( T_i \rightarrow T_k \), in V-V merging process can be obtained as

\[
\begin{align*}
w_{i,j} = \frac{L_{i,j}w_{ij}}{V_j - V_i + \frac{I_{i,j} + I_{j,k}}{I_{i,j} + I_{j,k}} + \frac{I_{i,j} - I_{j,k}}{I_{i,j} + I_{j,k}}} y_{\text{max}}, \\
w_{k,j} = \frac{L_{i,j}w_{ij}}{V_j - V_i + \frac{I_{i,j} + I_{j,k}}{I_{i,j} + I_{j,k}} + \frac{I_{i,j} - I_{j,k}}{I_{i,j} + I_{j,k}}} y_{\text{max}}.
\end{align*}
\]
For the merging process of two adjacent connections, \( T_j \rightarrow T_k \) and \( T_j \rightarrow T_l \), the widths of three merged connections in six different merging processes are also obtained according to the similar discussion under electromigration and IR-drop constraints. Based on the determined widths of three resultant connections in the Y-type structure after completing any merging process, the wasted wiring area under the electromigration and IR-drop constraint. In order to reduce the total wiring area, the P-oriented connections can be firstly considered to be merged with their adjacent P-oriented or C-oriented connections. If any P-P or P-C merging process reduces the wasted wiring area, the feasible Steiner points will be assigned in the construction of an area-driven multiple-source Steiner tree. As no P-P or P-C merging process reduces the wasted wiring area, the C-oriented connections can be further considered to be merged with their adjacent C-oriented or V-oriented connections. If any C-V, C-V or V-V merging process reduces the total wiring area, the feasible Steiner points will be further assigned in the construction of an area-driven multiple-source Steiner tree. As no C-V, C-V or V-V merging process reduces the wasted wiring area, the C-oriented connections can be further considered to be merged with their adjacent C-oriented connections. Generally speaking, any C-C merging process cannot reduce the total wiring area under the electromigration and IR-drop constraint. However, any C-C merging process cannot reduce the total wirelength. If any C-C merging process does not increase the total wirelength, the \( \Lambda \)-type structure of two connections, \( T_j \rightarrow T_k \) and \( T_j \rightarrow T_l \), can be transformed into the Y-type structure of three connections, \( T_j \rightarrow T_{Sj} \), \( T_j \rightarrow T_{Sj} \), \( T_j \rightarrow T_{Sj} \), by introducing a Steiner tree, \( S_j \). After completing three merging processes, the total wiring area of the final area-driven Steiner tree in Fig. 5 is obtained as 14.3.

![Fig. 5 Steiner-point assignment under electromigration and IR-drop constraint](image_url)

**C. Obstacle-aware Physical Path Assignment**

After completing area-driven Steiner-point assignment, a final area-driven multiple-source Steiner tree is constructed by introducing some Steiner points into the initial routing tree. In general, all the connections are independent in a multiple-source Steiner tree. Based on the determined widths of all the connections and the given obstacles in a routing plane, the empty space among obstacles can be partitioned into some rectangular space regions and the physical paths of all the connections in the Steiner tree can be routed one by one by finding the shortest paths among space regions and assigning some I-type, L-type or Z-type routing patterns onto space regions. Furthermore, the widths of all the connections can be assigned onto the corresponding physical paths in obstacle-aware physical path assignment and an obstacle-aware multiple-source rectilinear Steiner tree can be obtained. Refer to the determined widths of all the connections in the Steiner tree in Fig. 5, an obstacle-aware multiple-source rectilinear Steiner tree can be obtained to minimize the total wiring area as illustrated in Fig. 6. As a result, the total wirelength in the final rectilinear Steiner tree is 33, the number of routed vias is 7 in two-layer routing model and the number of used Steiner points is 3.

**IV. EXPERIMENTAL RESULTS**

For the construction of an obstacle-aware multiple-source rectilinear Steiner tree, Lienig’s Steiner-tree-based approach[7] and our proposed approach have been implemented using standard C++ language and run on a Pentium IV 2.8GHz machine with 2GB memory. The set of useful parameters in
the with determination for electromigration and IR-drop avoidance is based on 0.18μm technology in the SIA’s 97 roadmap and listed in Table I.

![Fig. 6 Physical path assignment for the construction of an obstacle-aware multiple-source rectilinear Steiner tree](image)

<table>
<thead>
<tr>
<th>Terminals</th>
<th>Wiring resistance per unit square</th>
<th>Power voltage</th>
<th>Maximum tolerant current density</th>
<th>Thickness on the routing layer</th>
<th>Safety factor</th>
<th>Minimum process wiring width</th>
</tr>
</thead>
<tbody>
<tr>
<td>c06</td>
<td>0.0688(Ω/μm²)</td>
<td>1.8(V)</td>
<td>8.2E05(A/cm²)</td>
<td>0.55(μm)</td>
<td>1.1</td>
<td>0.22(μm)</td>
</tr>
<tr>
<td>c05</td>
<td>0.0583(Ω/μm²)</td>
<td>1.21(μm)</td>
<td>6.4E05(A/cm²)</td>
<td>0.55(μm)</td>
<td>1.1</td>
<td>0.22(μm)</td>
</tr>
<tr>
<td>c04</td>
<td>0.0583(Ω/μm²)</td>
<td>1.21(μm)</td>
<td>6.4E05(A/cm²)</td>
<td>0.55(μm)</td>
<td>1.1</td>
<td>0.22(μm)</td>
</tr>
<tr>
<td>c03</td>
<td>0.0583(Ω/μm²)</td>
<td>1.21(μm)</td>
<td>6.4E05(A/cm²)</td>
<td>0.55(μm)</td>
<td>1.1</td>
<td>0.22(μm)</td>
</tr>
<tr>
<td>c02</td>
<td>0.0500(Ω/μm²)</td>
<td>1.15(μm)</td>
<td>4.8E05(A/cm²)</td>
<td>0.55(μm)</td>
<td>1.1</td>
<td>0.22(μm)</td>
</tr>
<tr>
<td>c01</td>
<td>0.0500(Ω/μm²)</td>
<td>1.15(μm)</td>
<td>4.8E05(A/cm²)</td>
<td>0.55(μm)</td>
<td>1.1</td>
<td>0.22(μm)</td>
</tr>
</tbody>
</table>

If the IR-drop constraint of any connection is set as $V_{IR} = p \cdot V_{dd}/100$, for the given power voltage, $V_{dd}$, the determined width, $w_{a}$, for electromigration and IR-drop avoidance can be obtained as:

$$w_{a} = \begin{cases} 0.22 & \text{if } I_{i,j} \leq 0.902 \text{ and } L_{i,j} \leq 58.234 \text{μm} \\ \frac{I_{i,j} L_{i,j}}{264.7 \text{μm}^2} & \text{if } I_{i,j} \leq 0.902 \text{ and } L_{i,j} > 58.234 \text{μm} \\ \frac{I_{i,j} L_{i,j}}{41.1 \text{μm}^2} & \text{if } I_{i,j} > 0.902 \text{ and } L_{i,j} \leq 64.562 \text{μm} \\ \frac{I_{i,j} L_{i,j}}{264.7 \text{μm}^2} & \text{if } I_{i,j} > 0.902 \text{ and } L_{i,j} > 64.562 \text{μm} \end{cases}$$

In the following experiment, six tested signal nets, c01, c02, c03, c04, c05 and c06, are randomly generated in a road map and listed in Table I.

![Fig. 6 Physical path assignment for the construction of an obstacle-aware multiple-source rectilinear Steiner tree](image)

**Table I Parameters on 0.18μm Technology in SIA’s 97**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$r_{b}$</td>
<td>Wiring resistance per unit square</td>
<td>0.0688(Ω/μm²)</td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>Power voltage</td>
<td>1.8(V)</td>
</tr>
<tr>
<td>$J_{max}$</td>
<td>Maximum tolerant current density</td>
<td>8.2E05(A/cm²)</td>
</tr>
<tr>
<td>$d$</td>
<td>Thickness on the routing layer</td>
<td>0.55(μm)</td>
</tr>
<tr>
<td>$s$</td>
<td>Safety factor</td>
<td>1.1</td>
</tr>
<tr>
<td>$w_{min}$</td>
<td>Minimum process wiring width</td>
<td>0.22(μm)</td>
</tr>
</tbody>
</table>

**Table II Experimental Results for Obstacle-Aware Rectilinear Steiner Tree with Electromigration and IR-Drop Avoidance**

<table>
<thead>
<tr>
<th>Nets</th>
<th>Terminals</th>
<th>Obstacles</th>
<th>Lienig’s Rectilinear Steiner Tree?</th>
<th>Our Proposed Steiner Tree</th>
</tr>
</thead>
<tbody>
<tr>
<td>#Sinks</td>
<td>#Sources</td>
<td>(No IR-drop constraint)</td>
<td>(5% $V_{dd}$) IR-drop constraint</td>
<td>(10% $V_{dd}$) IR-drop constraint</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total Wiring Acreas(μm²)</td>
<td>%Satisfied sinks for p=5</td>
<td>Total Wiring Acreas(μm²)</td>
</tr>
<tr>
<td>c01</td>
<td>5</td>
<td>6</td>
<td>324.27(100%)</td>
<td>46.67%</td>
</tr>
<tr>
<td>c02</td>
<td>10</td>
<td>8</td>
<td>385.61(100%)</td>
<td>66.78%</td>
</tr>
<tr>
<td>c03</td>
<td>15</td>
<td>7</td>
<td>412.39(100%)</td>
<td>68.75%</td>
</tr>
<tr>
<td>c04</td>
<td>20</td>
<td>11</td>
<td>528.67(100%)</td>
<td>87.72%</td>
</tr>
<tr>
<td>c05</td>
<td>25</td>
<td>13</td>
<td>598.92(100%)</td>
<td>86.08%</td>
</tr>
<tr>
<td>c06</td>
<td>30</td>
<td>17</td>
<td>644.37(100%)</td>
<td>97.69%</td>
</tr>
</tbody>
</table>

**Total** | 2932.48(100%) | 417.97% | 4638.52% | 4.29 | 2644.32(90.3%) | 4.29 | 2712.81(92.5%) | 4.57 | 5487(90.3%) | 4.57 | 5487(90.3%) | 4.57 |

**V. CONCLUSIONS**

Based on the width determination of any current-driven connection for electromigration and IR-drop avoidance and a set of given obstacles in a routing plane, an obstacle-aware multiple-source rectilinear Steiner tree with electromigration and IR-drop avoidance can be constructed to minimize the total wiring area.

**REFERENCES**