Abstract—This paper demonstrates a deterministic, variability-aware reliability modeling and simulation method. The purpose of the method is to efficiently simulate failure-time dispersion in circuits subjected to die-level stress effects. A Design of Experiments (DoE) with a quasi-linear complexity is used to build a Response Surface Model (RSM) of the time-dependent circuit behavior. This reduces simulation time, when compared to random-sampling techniques, and guarantees good coverage of the circuit factor space. The DoE consists of a linear screening design, to filter out important circuit factors, followed by a resolution 5 fractional factorial regression design to model the circuit behavior. The method is validated over a broad range of both analog and digital circuits and compared to traditional random-sampling reliability simulation techniques. It is shown to outperform existing simulators with a simulation speed improvement of up to several orders of magnitude. Also, it is proven to have a good simulation accuracy, with an average model error varying from 1.5 to 5% over all test circuits.

I. INTRODUCTION

Scaling towards smaller transistor sizes in order to achieve smaller, faster, lower power and less expensive chips, creates evermore design problems. Die level reliability issues (e.g., Negative Bias Temperature Instability (NBTI) and Hot Carrier degradation (HC)) and increasing process variability are at the forefront of problems to be dealt with in modern and future CMOS technologies [1]. The effect of transistor ageing (i.e., NBTI and HC) on circuit behavior, especially when combined with process variability, is very complicated and not always well understood. The lack of adequate knowledge about circuit ageing can cause unreliable products or unnecessary design margins.

Existing solutions (e.g., post-production accelerated stress testing) become too expensive due to an increasing demand for very low failure rates augmented with evermore reliability and variability problems. A designer needs a statistical circuit analysis tool that includes circuit ageing. Such a tool must be fast (i.e., no more than a few hours of simulation time, even for large circuits) but must also have a good simulation accuracy. Moreover, a designer must be able to extract information (i.e., weak-spot detection) to improve his design or to implement countermeasures (i.e., circuit tuning). In literature, most reliability simulation methods have been developed a few years ago and are therefore intended for CMOS technologies where variability was not yet an issue [2], [3]. To make a reliable design in a sub 90nm technology, however, this is no longer satisfactory. Bestory et al. [4] did include the effect of variability, using a Monte-Carlo (MC) simulation wrapped around a nominal reliability simulator based on high-level behavioral transistor models. This approach is fast, but it lacks accuracy, especially for analog circuits where the effects of time-varying stress voltages are important. In previous work [5], the authors presented a more accurate reliability simulator able to cope with time-varying stress. In this work, the authors also used a MC-approach in order to include variability effects. But, although an MC-based reliability simulation is accurate, it also has a large number of disadvantages: i) It is very cpu intensive. ii) There are no weak-spot detection capabilities. And iii) the simulation has to be rerun every time new or extra process data is included.

In this paper, a reliability modeling and simulation method to tackle the before-mentioned problems is presented:
1) The method is systematic and applicable to analog, digital and mixed-signal circuits.
2) A set of experimental designs ensures the generation of valid, defensible and accurate engineering conclusions.
3) A screening design identifies circuit weak spots and reduces circuit simulation time guaranteeing a quasi-linear complexity.
4) A regression design enables the generation of a circuit Response Surface Model (RSM) of the circuit behavior as a function of time.

The method, presented in this work, is built around a nominal reliability simulator, the authors presented earlier [5]. A brief review of this work is given in section II. The variability-aware simulation framework is introduced in section III. Section IV presents experimental simulation results and compares the results with random-sampling based techniques. Finally conclusions are drawn in section V.

II. NOMINAL RELIABILITY SIMULATION

The core of a reliability simulator is a method to calculate the ageing of a circuit with fixed design parameters (i.e., without process variability). Following subsections give a brief overview of both the simulation method and the degradation models used in this work and described in more detail in work presented elsewhere [5], [6].

A. Simulation Methodology

Most degradation effects have an exponential dependence on the transistor gate voltage. Therefore, time-varying stress voltages have to be included when calculating circuit degradation. To obtain accurate information about the time-varying stress

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at every circuit node, a transient simulation is required. Extrapolation of transistor degradation ensures a fast simulation result over very long circuit life-times. In Fig. 1 a schematic representation of the nominal simulation method is depicted. The input to the simulator is a fresh (i.e. unstressed) netlist. In a first step, a transient simulation over one period of the input signal is performed. Then, the waveform on every node of every transistor is extracted and passed on to the transistor degradation model. Next, the degradation of every transistor is calculated and extracted over a longer time scale. And finally, a degraded version of the netlist is generated [6]. This algorithm has a linear complexity $O(n)$ with respect to the number of transistors in the circuit.

B. Transistor Degradation Modeling

In this work, both HC degradation and NBTI are taken into account, since these effects are considered to be two of the most important phenomena in modern and future nanometer CMOS designs [1]. Both phenomena affect different transistor model parameters, e.g. threshold voltage $V_{TH}$. The time-dependent behavior of these parameters can, for HC as well as for NBTI, be described as a power-law function of time [7]:

$$V_{TH} = V_{TH0} + At^n$$

$$A = f(V_{DS}, V_{GS}, V_{TH0}, T, W, L, \ldots)$$

where $V_{TH0}$ is the initial threshold voltage (for an unstressed device) and $n$ is a time-related parameter (about 0.5 for HC and 0.18 for NBTI). $A$ is a function of design parameters (e.g. $L, W$), environmental parameters (e.g. temperature $T$) and process-related parameters (e.g. $V_{TH0}, t_{ox}$). A general degradation model, including the effect of time-varying stress and valid for both NTBI and HC, can be deduced from [7]:

$$V_{TH}(t) = \left[V'_{TH} \frac{1}{1/n} + \left(C_{exp} \left(\frac{\beta V_{GS}}{\alpha}\right)^{1/n} (t - t')\right)^n\right]$$

where $V'_{TH}$ represents the degradation present at time $t'$, $\alpha$ is a process-dependent parameter, to be determined through measurements, $\beta$ is a parameter to include the effect of time-varying stress signals, with a DC value equal to $V_{GS}$. $C$ is a parameter that is a function of other transistor parameters (e.g. $V_{DS}, T, L, \ldots$) and is different for each degradation phenomenon.

III. VARIABILITY-AWARE RELIABILITY SIMULATION

A. Simulation Methodology

Existing random-sampling techniques (e.g. Monte-Carlo) are accurate, but very cpu intensive, since they often tend to sample designs with a high probability of occurrence. It therefore takes a long time to identify designs at the edge of the design space (i.e. designs that typically create yield problems). An RSM of the circuit behavior, on the other hand, can be evaluated very fast and thus allows quick yield calculation. To build a sufficiently accurate circuit model, a design of experiments (DoE) can be used. These well-known information gathering techniques [8] allow to extract a maximum of information, with a minimum of experiments (or simulations). Unfortunately, the time to build an RSM grows exponentially with the number of transistors in a circuit. For example, to model a linear system with $n$ factors (i.e. inputs), including possible interactions between different factors, a design with a $O(2^n)$ complexity is needed [8]. In order to reduce circuit model build time, the number of factors to build the RSM must thus be limited. However, for a designer, it is very hard to distinguish important design factors from less important ones, since the relationship between circuit design factors and circuit ageing can be very complex and is circuit and application dependent.

In this work, first relevant circuit factors are filtered out, using a simple screening design and then a more complex regression design is used to build an RSM of the circuit. Finally, this RSM can be evaluated to calculate the circuit yield. Fig. 2 shows a schematic representation of the new simulation method. The simulator input is a circuit SPICE-netlist and
a corresponding testbench (see Fig. 2). The simulator itself consists of three main parts:

1) In a first step (Circuit Factor Extraction on Fig. 2), a circuit factor list, with values for all circuit design, environmental and input parameters, is extracted from the input netlist. The combination of both the circuit factor list and a process parameter file define the circuit factor space (see Fig. 3, top left).

2) The nominal reliability simulator (NRS), presented in section II, is used to evaluate the time-dependent behavior (measured via circuit performance parameters) of a single sample in the circuit factor space. Evaluation of all samples will create a corresponding performance space (see Fig. 3, top right). In this work, the NRS is applied on samples defined by a screening and a regression design, which allows to analyze the circuit factor space with a limited number of simulations.

3) The results of the analysis in the second step are used to create an RSM to quantify the link between the circuit parameter space and the performance space. Adding specification limits to the circuit (i.e. minimum and maximum values for performance parameters) will allow to calculate the time-dependent production yield $Y$ can be calculated (bottom).

**B. Circuit Factors**

Every circuit is considered as a black box (see Fig. 4) with a number of inputs and the circuit yield as an output.

where $f_{\text{mean}}$ represents the mean value for every factor (specified in the input circuit netlist), $f_{in}$ is a vector with normalised variations for every factor and $A_{\text{var}}$ is a diagonal denormalisation matrix (defined in the process parameter file, also see Fig. 2). Vector $f_{in} = [f_1, \ldots, f_n]^T$, with $n$ the number of factors, can be changed to walk over the circuit factor space. The output of the system is the production yield of the circuit.

**C. Experimental Design: Screening and Regression**

To analyze and to model the circuit, a screening design, a linear and a non-linear regression experimental design are used (see Algorithm 1). This combination of experimental designs results in a simulator with a quasi-linear complexity $O(n + n^2/100)$, with $n$ the number of circuit factors, and is therefore very cpu efficient. Each experimental design $D$ consists of a set of different input factor vectors $f_{in}$:

$$D = [f_{in,1}; \ldots; f_{in,q}]$$

with $q$ the number of experiments in the design. The different experimental designs, used in this work, will now be explained in more detail.

**Algorithm 1 Experimental Design Analysis**

1: **Inputs:** $f_{in} = [f_1, \ldots, f_n]$  
2: **Outputs:** $f_{in}^*, D_R \in \mathbb{R}^{m \times k}$, $P_R \in \mathbb{R}^{m \times p}$  
3: **SCREENING Analysis:**  
4: Set up $D_S \in \mathbb{N}^{(2n+1)\times n}$ {see Table I}  
5: $P_S \in \mathbb{R}^{2n+1} = \text{NRS}(D_S)$  
6: $k = 0$  
7: for $i = 1$ to $n$ do  
8: Eliminate factors using $P_S$ and Eq. 7 and 8:  
9: if $|a_i + \sum_{j \neq i} a_{ij}| > 0$, with $i \neq j$ then  
10: $f_i \in f_{in}^*$  
11: $k++$  
12: end if  
13: end for  
14: **REGRESSION Analysis:**  
15: Set up $D_R[0:q-1,:] \in \mathbb{R}^{q \times k}$ {see Eq. 9 and Table II}  
16: Set up $D_R[q:m,:] = D_{CC} \in \mathbb{R}^{(2k+1)\times k}$ {see Table III}  
17: $P_R \in \mathbb{R}^{m} = \text{NRS}(D_R)$

In the first step, a 2-level systematic fractional replicate screening analysis [9], with a $O(2n + 2)$ complexity, is used.
to screen out the factors with the largest impact on the circuit output $P$. This results in a factor set $f_{in}$, a subset of the original input factor set $f_{in}$. The screening design $D_S$ and the corresponding output vector $P_S$ are listed in Table I. Vector $P_S = [P_S,1, \ldots, P_S,2n+2]$ is obtained by applying the Nominal Reliability Simulator (indicated as NRS in Algorithm 1) on the input circuit netlist. For every simulation a different input factor combination, defined by $D_S$, is used.

$P_S = [P_S,1, \ldots, P_S,2n+2]$ is used to find a suitable R5 FF design for every circuit. Sanchez [10] presented a method, using a Hadamard-ordered matrix to generate the Walsh functions. This matrix $H_v$, with dimensions $2^n \times 2^n = N \times N$ can be generated using:

$$H_0 = (1) \quad \text{and} \quad H_{v+1} = \begin{pmatrix} H_v \\ H_v \end{pmatrix} = \begin{pmatrix} H_v & -H_v \\ H_v & H_v \end{pmatrix}$$

The columns $i_0, \ldots, i_{N-1}$ of $H_v$ define the Walsh functions with corresponding Walsh indices $0 \ldots N-1$ and all elements take values $+1$ or $-1$. A R5 FF design for $k$ factors, coincides with a subset of the $N$ Walsh functions. The elements of each function in this subset each represent one factor in the design. The Walsh indices can be found through an algorithm that is described in [10]. Table II lists the Walsh indices for R5 FF designs up to 11 factors. For example, for a circuit with 4 factors, the columns with indices $\{1, 2, 4, 8, 15\}$ of a $H_4$ Hadamard matrix represent a R5 FF design. In Algorithm 1, $q$ indicates the number of experiments for the R5 FF design, which can only be used to estimate the linear effect of all relevant factors in the circuit. To also capture non-linear effects, the design is augmented with a central composite design and a center design, which requires $2k + 1$ extra simulations. The setup of these experiments and the corresponding outputs are listed in Table III. To perform the entire regression analysis $m = q + 2k + 1$ experiments are needed (also see Algorithm 1).
TABLE III
CENTER AND CENTRAL COMPOSITE DESIGN SETUP

<table>
<thead>
<tr>
<th>INPUT</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$D_{CC} \in \mathbb{R}^{(2k+1) \times k} = [f'<em>{m,1}, \ldots, f'</em>{m,2k+1}]$</td>
<td>$P_{CC} \in \mathbb{R}^{2k+1}$</td>
</tr>
<tr>
<td>$D_{CC}[0:] = [0, \ldots, 0]$</td>
<td>$P_{CC}[0]$</td>
</tr>
<tr>
<td>$D_{CC}[1:k] = \begin{bmatrix} \sqrt{k} &amp; 0 &amp; \cdots &amp; 0 \ 0 &amp; \sqrt{k} &amp; \cdots &amp; 0 \ \vdots &amp; \vdots &amp; \ddots &amp; \vdots \ 0 &amp; 0 &amp; \cdots &amp; \sqrt{k} \end{bmatrix}$</td>
<td>$P_{CC}[1 : k]$</td>
</tr>
<tr>
<td>$D_{CC}[k + 1 : 2k + 1] = \begin{bmatrix} -\sqrt{k} &amp; 0 &amp; \cdots &amp; 0 \ 0 &amp; -\sqrt{k} &amp; \cdots &amp; 0 \ \vdots &amp; \vdots &amp; \ddots &amp; \vdots \ 0 &amp; 0 &amp; \cdots &amp; -\sqrt{k} \end{bmatrix}$</td>
<td>$P_{CC}[k + 1 : 2k + 1]$</td>
</tr>
</tbody>
</table>

D. Response Surface Modeling

The output of the regression analysis (see section III-C) is a set of reliability simulation results $P_R$, which are used to create a circuit model $\phi$:

$$P = \phi(x)$$

where $x \in$ circuit factor space and $P \in$ circuit performance space (see Fig. 3). For this work, a radial basis function was used which offers, according to [11], a good global fit in space (see Fig. 3). For this work, a radial basis function was used which offers, according to [11], a good global fit in space (see Fig. 3).

$$\phi(x) = \sum_{i=1}^{m} \beta_i \| x - f_i \|$$

where $\| \|$ represents the $l_2$ norm, $f_i$ is the $k$-dimensional input vector for the $i$th regression simulation with $k$ the number of circuit factors included in the model, $m$ is the number of regression simulations and $P_R$ is the simulation output vector (see section III-C) and the $\beta_i$’s are the constants to be estimated:

$$\beta = A^{-1}P_R, \quad A = [a_{ij}]$$

$$a_{ij} = \left( \sum_{r=1}^{k} (f_{i,r} - f_{j,r})^2 \right)^{1/2}, \quad 1 \leq i, j \leq m$$

$$f_i = [f_{i,1}, \ldots, f_{i,k}], \quad P_R = [P_1, \ldots, P_m]$$

The behavior of the circuit, as a function of $f_{m}'$ varies over time. The nominal reliability simulation produces values for the circuit behavior at different time-points, which are converted into an RSM of the circuit at every time-point. An interpolation between these different models gives an approximation of the behavior of the circuit at a given time-point and for a given set of input factors.

Fig. 5. Simulator flow for a one-stage amplifier.

Fig. 6. Simulation result for two versions of the one-stage amplifier over a lifetime of 4 months.

IV. EXPERIMENTAL RESULTS

The following experiments were conducted, the results of which will be described in the succeeding sections:

- Simulation of a one-stage amplifier: a simple example allows to demonstrate the simulator and to also illustrate how to use circuit weak-spot detection to create a more reliable circuit.
- Validation of the simulator: five analog and digital circuits were simulated using this work and compared to traditional random-sampling simulation techniques.

The circuits under study are designed in a 90nm CMOS technology. The experiments were executed on a dual-quad core 2.8GHz Intel Xeon processor with 8GB of RAM.

A. Reliability simulation of a one-stage amplifier

A one-stage resistive amplifier (depicted in Fig. 5 on the right) was used as a simple circuit to demonstrate the simulator. Two performance parameters were monitored: the AC output voltage $V_{out}$ and the DC output voltage $V_{OUT}$. The circuit was simulated over a lifetime of 4 months in which the circuit degrades due to hot carrier effects. Fig. 5 gives a schematic representation of the simulation flow and the corresponding outputs. Screening indicated that i) factor $L$ (the transistor length) has the largest impact on the circuit reliability and ii) increasing this factor improves the circuit reliability. Therefore, a second amplifier was designed and simulated for which both the width and the length of the transistor were doubled. This is expected to improve...
circuit reliability, while circuit performance remains the same. Note that this improvement in reliability, due to an increased transistor length, cannot be quantified, since the RBF-model is based on process variations over a small range, rather than design variations (e.g. 2xL) over a large range. The RBF-models were evaluated for both circuits, in 50 points randomly distributed over the circuit factor space and at time t=0 and time t=4 months. The results are shown in Fig. 6. Due to circuit ageing, both circuit performance parameters change over time. However, the improved circuit degrades much less compared to the original circuit and is therefore much more reliable.

B. Validation of speed and accuracy

To validate the accuracy and speed-up of this work, five commonly used circuits were simulated. The resulting RBF-model for each circuit was compared to the simulation result of a traditional random-sampling simulation with a uniform distribution of the input factors (see Table IV). Every circuit was simulated over a life-time of 4 months. Since the RBF, to model the circuit behavior, is a type of neutral network, the set of training vectors (i.e results of the regression analysis) was used to train the model, while a set test vectors is needed to test the model accuracy. The test data consists of 500 samples, randomly distributed over the circuit factor space. For every sample s, the model error over the circuit life-time was calculated:

$$ \varepsilon_s[\%] = \frac{100}{N} \sum_{i=1}^{N} \frac{|S_i - M_i|}{|S_i|} \quad (13) $$

where N represents the number of time-points (i.e. 50) and S_i and M_i the simulation and model result at the ith time-point respectively. Fig. 7 depicts the distribution of the model error for every circuit under test. The largest average error between a circuit model and the simulations is 5%, while the simulation speed-up is at least three orders in magnitude. To further reduce the model error, extra simulations can be performed, though, this would dramatically increase simulation time, which is not always wanted. The simulator speed-up is defined as the ratio of the time to simulate one sample with the nominal reliability simulator to the time to evaluate the same sample with the RBF-model, both at a life-time of 4 months.

V. CONCLUSIONS

This paper presents a novel deterministic modeling and simulation method to calculate circuit ageing, including time-varying stress and process variability. An RSM model of the circuit behavior is build, based on the result of an experimental designs. To speed up the analysis, a regression design is combined with a screening analysis. When compared to a traditional random-sampling based reliability simulation, up to three orders reduction in simulation time is achieved. Both the simulation and modeling part of the method was demonstrated and validated using five commonly used analog and digital circuits.

ACKNOWLEDGMENT

The first author of this work is funded by FWO-Vlaanderen. The work is also supported in part by EUFP7 and IWT SBO.

REFERENCES


<table>
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<th>Design [Spec]</th>
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<th>Average Accuracy</th>
<th>Speed-up @ 4 months</th>
<th>Model Build Time</th>
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<tr>
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