Enhanced Design of Filterless Class-D Audio Amplifier

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Abstract

In this work, we propose an enhanced design method for filterless class-D audio amplifier based on multilevel architecture. The multilevel technique consists of a multilevel converter and a time division adder followed by modulator. In this method, the modulated signal is arranged into several time divisions and then be integrated into a binary numeric. After that, the binary numeric is encoded to be a set of parallel control signal for multilevel converter. The multilevel converter will deliver multilevel signal to loudspeaker instead of conventional two-level signals. Consequently, improve the total-harmonic-distortion (THD) and signal-noise-ratio (SNR) significantly without sacrificing power efficiency. Moreover, we can apply the proposed method to many class-D amplifier designs simply insert a time division adder behind modulator and replace output stage with multilevel converter.

1. Introduction

In the past few years, along with advance in consuming electronics, audio power amplifiers have applied to many multi-media applications. Especially for portable and low power devices, the system volume and power efficiency are the major concern [1]. The conventional class-A amplifier has high fidelity, but its power efficiency is poor due to large static current. The class-B or class-AB amplifiers are compromise on audio quality and power consumption. However, the system volume still too large due to required heat sink. Therefore, the class-D amplifier is widely used in portable device because of it has very high power efficiency, simple heat sink, and can meet industrial standard of Hi-Fi [2-5].

Through modulation process, Class-D amplifier converts audio signal to two-level signal stream and control the on/off status of power transistors to deliver current. The class-D amplifier therefore achieve very high power efficiency since the power transistors are operated in linear and cut-off region and the power loss occurs only at the moment that power transistor changes its status [6]. Moreover, with fixed power delivery, the class-D amplifier requires smaller power transistors and heat sink so that significantly reduces the system volume [7-8]. The major inferiority of class-D amplifier is the need of LC filter used to remove the high order harmonic and recover audio signal [11]. The inductances of filter increase the production cost as well as required PCB space. Especially for portable applications, the LC filter is probably expensive than ICs [12-13]. For this reason, developing a filterless design approach is valuable and directly reducing the cost [9-10].

Recent years, multilevel pulse width modulation (PWM) converter is widely used in the area of motor control, power system control and so on. The multilevel converter combines several voltage levels and outputs signals as stairway so that improves total harmonic distortion [14-18]. The multilevel PWM converter presents significant advantages over two-level PWM converter. It requires lower power in high frequency band and has higher resolution in comparison with two-level converter using the same switching frequency [19]. In addition, the instantaneous variation of output voltage is small and achieves lower electromagnetic interference (EMI) purpose [20]. The common implement architectures of multilevel converter are diode-clamped converter, flying capacitor converter and cascade full-bridge converter [18]. For diode-clamped converter, the circuit is complicated due to the required diode is proportional to the number of voltage levels. For flying capacitor converter, we need to balance the voltage of capacitor loop that increase the complexity of controlling circuit. The most used architecture is cascade full-bridge converter with floating DC voltage source. However, implement full-bridge converter by integrating discrete elements on PCB is easy but not for VLSI chips. Because the substrate of chip is biased to the most positive or negative voltage, the

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conventional cascade full-bridge converters cannot produce expected voltage levels. Therefore, we present a dual H-bridge multilevel converter in this work. The proposed multilevel converter provides thirteen voltage levels by using only nine transistors and the controlling circuit is quite simple.

Another important issue of implement multilevel converter is the modification of modulation process. There are two categories of modified modulation strategy, which are carrier-based PWM and space vector PWM [21-22]. The carrier-based PWM modulates audio signal simultaneously by several carriers with different amplitude and phase. The space vector PWM is suitable for those applications on digital control system, but the number of multilevel is quite limited that no more than five levels [21]. Nevertheless, implement the carrier-based PWM on chip raise too much design effort due to the required carriers with different amplitude and phase. In order to overcome the difficulties of implement multilevel PWM on chip, we propose an innovative multilevel PWM in this paper. The new approach converts two-level PWM signal to multilevel signal directly by a proposed time division adder and it can increase the number of levels flexibly.

The remainder of this paper is organized as follows. Section 2 introduces the basic structure of open loop class-D amplifier. Section 3 describes the proposed enhanced design of filterless class-D amplifier in detail and presents mathematical explanation to demonstrate its theory. Then, the proposed dual H-bridges multilevel converter is described in section 4. Section 5 and section 6 will show experiment results of a practical design and conclusion.

2. Basic structure of class-D amplifier

The basic open loop class-D amplifier consists of modulation circuit, power transistors, and low-pass filter as shown in Fig. 1. The audio signal is modulated to two-level signal by PWM or sigma-delta-modulation (SDM) and indeed, the amplitude of original audio signal is represented as pulse width. After that, the modulated two-level signal controls the power transistors to deliver current to low-pass filter and speaker.

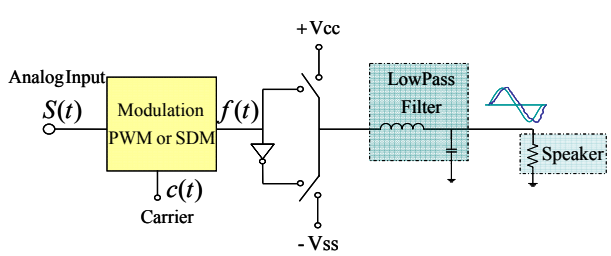


Fig. 1. Open loop class-D amplifier

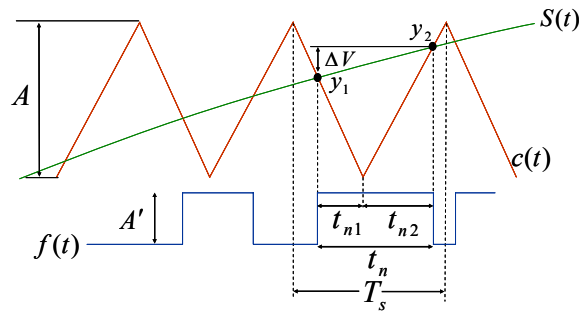


Fig. 2. Relationship of signals in Fig. 1

The relationship of input signal $S(t)$, PWM carrier $c(t)$ and modulated signal $f(t)$ in Fig. 1 is shown in Fig. 2. Because the frequency of carrier is usually much higher than input signal, the relationship between two sample points is treated to be linear. We accordingly represent the position of two sample points as:

$$y_1 = \frac{A \cdot t_{n1}}{0.5T_s} \quad \text{and} \quad y_2 = \frac{A \cdot t_{n2}}{0.5T_s}$$

, where A is amplitude of carrier, T_s is period of carrier and $t_{n1} + t_{n2} = t_n$ which is pulse width of modulated signal. We can furthermore describe the magnitude of input signal in a sample period through its average value expressed as:

$$y_{ave} = \frac{y_1 + y_2}{2} = \frac{1}{2}\frac{A \cdot (t_{n1} + t_{n2})}{0.5T_s}$$
$$= A \cdot \frac{t_n}{T_s} = A \cdot D \text{ .....(1)}$$

, where D is called duty ratio in general. That is, the duty ratio of modulated signal represents the magnitude of input signal.

In order to enhance the performance of circuit, second order low-pass filter with feedback structure is usually adopted to reduce distortion. In addition, using SDM will result in better performance because it has higher sample rate than PWM and with noise shaping mechanism. However, for portable application, using SDM or second order low-pass filter with feedback structure will increase both power consumption and system volume. For this reason, we develop an enhanced design method for class-D amplifier without increasing sampling rate of system and using extra filter.

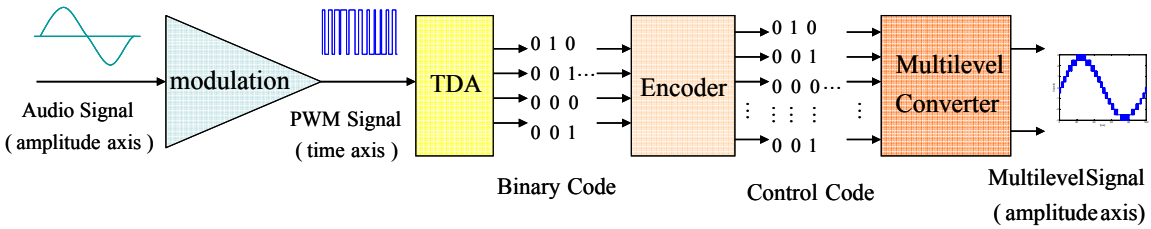


Fig. 3. Input/Output relationship of multilevel class-D amplifier

3. Enhanced design of class-D amplifier

As mentioned above, using multilevel architecture for class-D amplifier not only enhances performance but also reduces cost. In this section, we will present a novel multilevel architecture as shown in Fig. 3. The audio input signal is modulated to two-level signals by PWM which is the same as conventional method. Then, a time division adder (TDA) is inserted for transforming the pulse width of two-level signal into binary numeric. After that, the binary numeric is encoded to be a set of parallel control signal and drive multilevel converter to deliver multilevel signal. Because the voltage scale between each voltage level is smaller, the proposed method enhances the signal resolution as well as reduces EMI and THD.

The one of important components in our method is TDA as shown in Fig. 4.

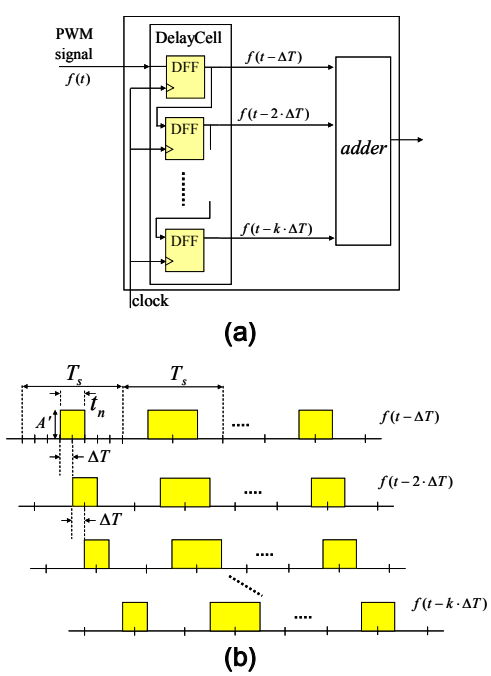


Fig. 4. (a) Functional blocks of TDA

(b) Timing diagram of TDA

The TDA consists of an adder and delay cell, which is a series of D flip-flop. Each flip-flop provides a propagation delay ΔT. The modulated signal $f(t)$ with period T_s, amplitude A', and pulse width t_n is fed into delay cell. Consequently, the modulated signal is propagated to be $f(t-k\cdot\Delta T)$. If the number of flip-flop is M and with propagation delay $\Delta T=\frac{T_s}{M}$, then the delayed modulated signal will be $f(t-k\cdot\frac{T_s}{M})$. That is, the time slot of one period T_s can be divided into M time slots and the modulated signal is arranged in each time slot. After that, the adder integrates the value of signal in each time slot and results in a summation:

$$m(t)=\sum_{k=1}^{M} f(t-k\cdot\frac{T_s}{M})$$

Because the value of $m(t)$ varies with delayed modulated signal immediately, we have to describe this value by a macro point of view if we want to observe its trend. An intuitive expression is taking average value within one period as:

$$\begin{aligned} m(t)_{ave} &= \frac{1}{T_s}\int_0^{T_s} m(t)dt \\ &= \frac{1}{T_s}\int_0^{T_s}\sum_{k=1}^{M} f(t-k\cdot\frac{T_s}{M})dt \\ &= \frac{1}{T_s}\sum_{k=1}^{M}\int_0^{T_s} f(t-k\cdot\frac{T_s}{M})dt \\ &= \frac{1}{T_s}\sum_{k=1}^{M}\int_0^{t_n} A'dt \\ &= \frac{1}{T_s}\sum_{k=1}^{M} A't_n \\ &= A'M\frac{t_n}{T_s} = A'MD \quad \ldots\ldots..(2) \end{aligned}$$

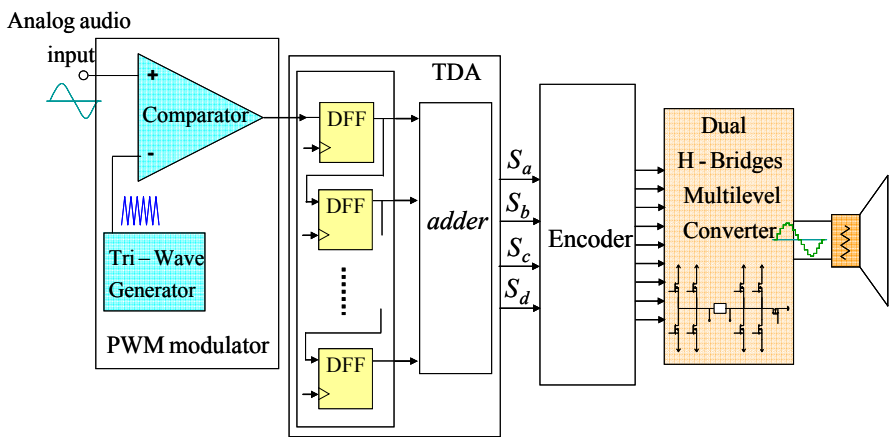


Fig. 5. Enhanced design for open loop filterless class-D audio amplifier with PWM

According to Eq. (1) and Eq. (2), the average value of TDA output is proportional to duty ratio of modulated signal and it can represents magnitude of input audio signal linearly. In other words, the TDA is a multilevel signal generator and expresses multilevel signal by all digital binary codes.

Based on the presented TDA, we apply it to a simple open loop filterless class-D audio amplifier with PWM as shown in Fig. 5. The hardware architecture of this class-D amplifier is compact and only consists of open loop PWM modulator, TDA, encoder and multilevel converter. Except triangular wave generator, comparator and power transistors, we can implement most of components by digital circuits. The input audio signal is modulated by PWM and be transformed into multilevel signal that expressed by binary codes. After that, the encoder encodes these binary codes to parallel signal for controlling multilevel converter. Without extra filter, multilevel converter can output smoother signal to speaker. That is, SNR increased and THD reduced. In addition, the EMI will be reduced significantly because the proposed method does not use higher sample rate in modulation and the instantaneous voltage variation of output signal is lesser.

4. Dual H-bridge multilevel converter

As we knew, the cascaded full-bridge multilevel converter [20] is difficult to implement on chip. Therefore, we attempt to develop a feasible architecture to be implemented on chip easily. The proposed dual H-bridge multilevel converter is shown in Fig. 6. From TDA output S_a to S_d, the encoder transforms binary codes into parallel control signals S_1 to S_9. With four power supply voltages $\pm V_1$ and $\pm V_2$, the proposed multilevel converter requires nine power transistors to acquire thirteen levels multilevel signal. Furthermore, this is a flexible architecture since it can provides five, nine or thirteen levels according to choice of power supply voltage. For the conditions, $V_2 = V_1$ and $V_2 = 2V_1$, there are five and nine levels respectively. For $V_2 = 1.5V_1$ or $V_2 = 3V_1$, thirteen levels are produced. The relationships between TDA output signal, control signal and output voltage of multilevel converter are listed detailed in Table 1 and the functions of required encoder also can be derived as:

$$S_1 = S_a \cdot S_b + S_b \cdot S_c + S_a \cdot S_d$$
$$S_2 = \overline{S}_a \cdot \overline{S}_b \cdot \overline{S}_c \cdot \overline{S}_d + \overline{S}_a \cdot \overline{S}_b \cdot S_c \cdot S_d$$
$$S_3 = S_b \cdot \overline{S}_c \cdot S_d + S_a \cdot \overline{S}_b \cdot \overline{S}_d$$
$$S_4 = \overline{S}_a \cdot S_b \cdot \overline{S}_c \cdot \overline{S}_d + \overline{S}_a \cdot \overline{S}_b \cdot \overline{S}_c \cdot S_d + \overline{S}_a \cdot \overline{S}_b \cdot S_c \cdot \overline{S}_d$$
$$S_5 = \overline{S}_a \cdot \overline{S}_b \cdot S_c \cdot \overline{S}_d + S_b \cdot S_c \cdot S_d$$
$$S_6 = S_a \cdot S_c$$
$$S_7 = \overline{S}_a \cdot \overline{S}_b \cdot \overline{S}_c + S_b \cdot \overline{S}_c \cdot S_d + S_b \cdot S_c \cdot \overline{S}_d$$
$$S_8 = S_a \cdot S_b$$
$$S_9 = \overline{S}_a \cdot S_b \cdot \overline{S}_c \cdot \overline{S}_d + \overline{S}_a \cdot \overline{S}_b \cdot S_c \cdot S_d + S_a \cdot \overline{S}_b \cdot \overline{S}_c$$

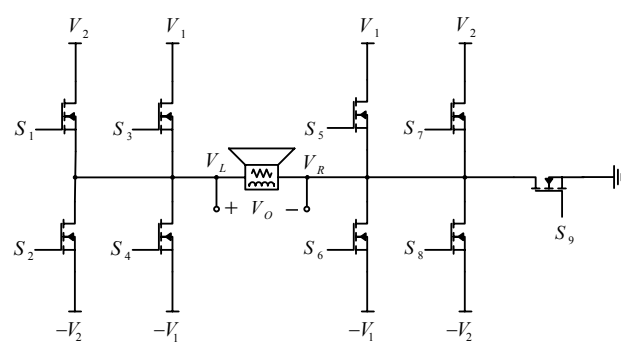


Fig. 6. Dual H-bridge multilevel converter

Table 1. Relationship of TDA output and multilevel converter Input/Output

TDA output signal	S_a	1	1	1	1	1	0	0	0	0	0	0	0	0
	S_b	1	0	0	0	0	1	1	1	1	0	0	0	0
	S_c	0	1	1	0	0	1	1	0	0	1	1	0	0
	S_d	0	1	0	1	0	1	0	1	0	1	0	1	0
Control Signal of Multilevel Converter	S_1	1	1	0	1	0	1	1	0	0	0	0	0	0
	S_2	0	0	0	0	0	0	0	0	0	1	0	0	1
	S_3	0	0	1	0	1	0	0	1	0	0	0	0	0
	S_4	0	0	0	0	0	0	0	0	1	0	1	1	0
	S_5	0	0	0	0	0	1	0	0	0	0	1	0	0
	S_6	0	1	1	0	0	0	0	0	0	0	0	0	0
	S_7	0	0	0	0	0	0	1	1	0	0	0	1	1
	S_8	1	0	0	0	0	0	0	0	0	0	0	0	0
	S_9	0	0	0	1	1	0	0	0	1	1	0	0	0
Output V_o (V) with $V_{1=1V}$, $V_{2=1.5V}$		3	2.5	2	1.5	1	0.5	0	-0.5	-1	-1.5	-2	-2.5	-3

5. Experiment result

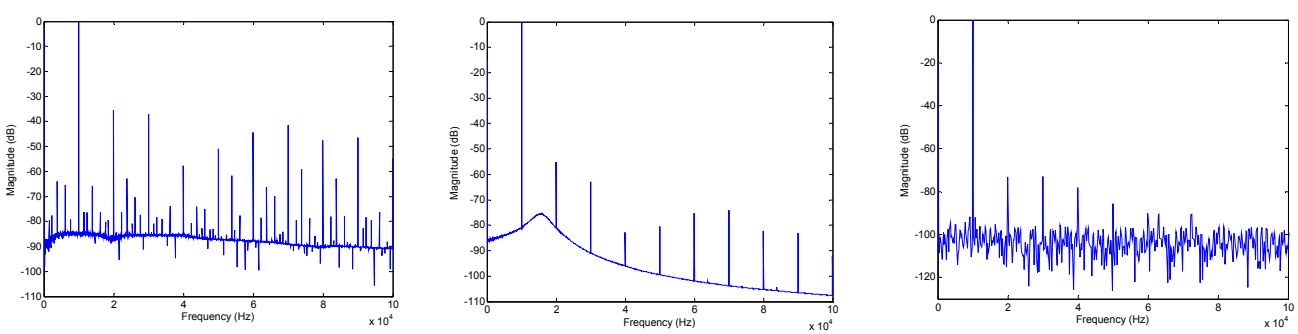
In this section, to demonstrate the performance, we used TSMC CMOS 0.35μ process to implement three different structures of class-D amplifier and compared with each other. Firstly, we designed two conventional open loop class-D amplifiers using PWM and its structure is shown in Fig. 1. One of these class-D amplifiers is filterless since it uses the impedance of speaker which the resistance $R = 8\Omega$ and inductance $L = 33\mu H$. Another class-D amplifier uses an extra filter to remove distortion and noise. Then, we based on conventional class-D amplifier; the proposed method was applied to show the enhancement of the performance.

Table 2 shows the comparison of performance with 10kHz sinusoidal input signal and 200kHz carrier of PWM. The THD of conventional open loop filterless class-D amplifiers is 1.68%. It seems disappointed because only impedance of speaker is used for filtering. The noise interference is therefore large and its SNR is barely 55dB as shown in Fig. 7(a). The THD and SNR of open loop class-D amplifier with extra filter are 0.176% and 58dB respectively. The THD certainly reduced since the second and third order harmonic distortion decayed as shown in Fig. 7(b).

Based on open loop filterless class-D amplifier, we applied the proposed enhanced design by using TDA and dual H-bridge multilevel converter as shown in Fig. 5. All of circuits had been implemented on chip except power transistors that because available chip area is restrictive. The photograph of chip is shown in Fig. 8 and power transistors were implemented on a PCB with its output signal is shown in Fig. 9. Without extra filter, the THD is reduced to 0.022% and SNR is increased to 85dB as shown in Fig. 7(c). According to comparison with filterless open loop class-D amplifier in Table 1, the proposed enhanced design significantly reduces THD and increased SNR that almost 76 and 30 times respectively. Even compared to that of using filter, the proposed method has 8 times THD improvement yet. Moreover, the power consumption and power efficiency do not be sacrificed since the degeneration of them is under control.

Table 2. Comparison of performance

	THD (%)	SNR (dB)	Power	Efficiency (%)
Proposed	0.022	85	220mW	80
Open loop without filter	1.68	55	190mW	82
Open loop with filter	0.176	58	190mW	82



(a) (b) (c)

Fig. 7. Spectrum of (a) open loop class-D amp. without filter (b) with filter (c) proposed method

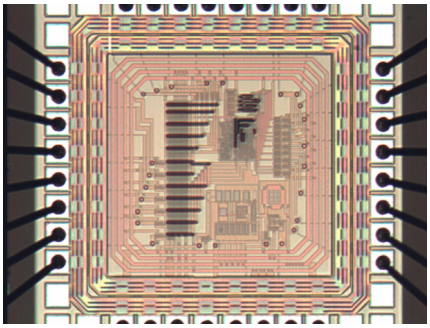


Fig. 8. Photograph of chip

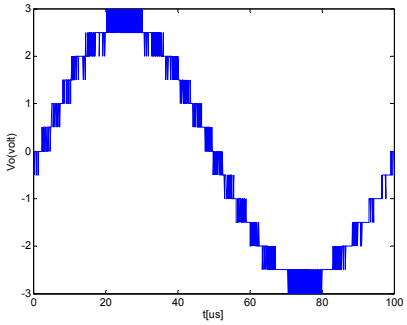


Fig. 9. Output of proposed class-D amplifier

6. Conclusion

In this paper, we have proposed an enhanced design of filterless class-D amplifier. The method is based on proposed TDA and dual H-bridge multilevel converter. To demonstrate the practicability, we applied this method to a simple open loop class-D amplifier and show very good result. The THD and SNR are significantly improved without sacrificing power consumption and efficiency. Moreover, the EMI is also reduced due to less voltage variation in transient state. Another merit of the method is that it can be applied to many design of class-D amplifier by inserting TDA and replacing multilevel converter. The proposed method not only enhances performance but also can be implemented on chip easily.

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