A Design Methodology for Fully Reconfigurable Delta-Sigma Data Converters

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***Abstract*- This paper presents a design methodology for fully reconfigurable low-voltage Delta-Sigma converters as for instance used in next-generation wireless applications. The design methodology first finds the power-optimized noise transfer functions for the different standards at system level and then translates them into optimal granularities of programmability and circuit parameters such as resistance and capacitance values for the integrators. Reconfiguration is done in the passive component arrays, modulator orders, number of quantizer bits and transconductance for optimal power consumption. This gives the design the best trade-off between power and performance for every configuration mode.**

1. Introduction

Driven by the explosive demand for wireless and portable applications, the next generation of wireless systems (4G radios) is required to seamlessly integrate the existing and future wireless technologies on a single handset, with fast speed and more functions. The flexibility becomes the key issue in 4G telecom systems. Additionally, even within one mode, these transceivers should adapt to the environment (presence of received blockers or not, status of battery power levels, etc.) to minimize power consumption and optimize performance according to the needs of the customer and the desired Quality of Service [1]. As one of the key blocks in the receivers, the AD converter should be fully reconfigurable for the different modes in 4G radios. This requires that the converter switch its resolution and bandwidth depending on the communication mode, but it can also relax its specifications with fine granularity within a given mode to save power.

Among the different types of data converters, ΔΣ modulators (DSMs) are normally favored in multi-mode designs due to their robustness to circuit errors and the inherent trade-off between speed and accuracy. Existing design techniques are mainly focused on single-mode topologies, while systematic multi-mode design methodologies have only been reported recently. The design methodology in [2] only tackles the topology reconfiguration without considering the component reconfiguration (e.g., integrators). In [3], a top-down synthesis process is proposed for multi-mode discrete-time expandable cascade DSMs. However, the power consumption is not involved in the high-level synthesise, and optimizations are carried out separately for each mode without taking into account possible parasitics caused by the reconfigurability circuitry. Our work presents a design methodology for continuous-time DSMs with full reconfigurability to adapt to different modes at both topology and building block level. As the power consumption and reconfigurability parasitics are fully taken into account at an early stage, power-optimized solutions are guaranteed.

This paper is organized as follows. Section 2 briefly gives the modulator architecture and discusses the reconfiguration. In section 3, power-optimal noise-transfer functions (NTFs) are generated for different modes by optimizing the phase-margin and then the noise transfer functions are translated into reconfigurable circuit parameters such as resistor and capacitor values. The determination of the control bits for reconfigurability is also given. Section 4 presents the simulations results. Finally, section 5 concludes this paper.

2. Reconfigurable Modulator architecture

The 4G telecom systems cover a wide range of different standards ranging from the most widely used GSM, UMTS and DVB to the newest wireless network standard (WLAN 802.11n) and Worldwide Interoperability for Microwave Access (WiMAX). In order to meet all the specifications of these standards, a flexible AD converter should adapt its signal bandwidth from a few hundred kHz up to 40MHz, while the dynamic range (DR) performance also needs to be scaled from 85dB to 55dB for different standards [4]. Note that ever when different modulation methods are used, the dynamic range requirements are different. Thus, the AD converter should be able to scale its performance in one mode when different modulation approaches are available.

3 Design methodology for reconfigurable DSMs

The design complexity of the reconfigurable circuits increases dramatically as much programmability is introduced for various kinds of specifications. With power consumption, noise and parasitic issues taken into account, the determination of the integrator coefficients, circuit parameters (resistance and capacitance value, etc) and granularities of the programmability is not trivial. In this section, a design methodology is proposed to generate the circuit parameters and determine the reconfiguration granularity. The flow of this

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design methodology as shown in Fig. 1 is comprised of 4 steps, which are now explained in details.

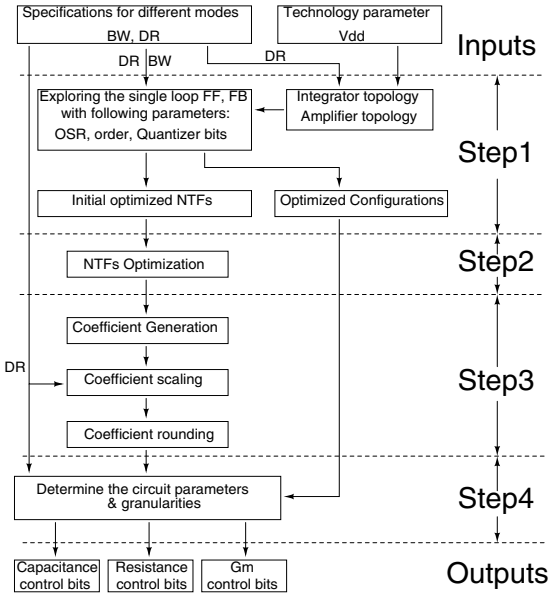


Fig. 1 Flow of the design methodology

3.1 Step1: Design-Space exploration

As shown in Fig.1, the inputs of the design methodology are the specifications of different modes and technology parameters such as supply voltage. As an example, the specifications used are the major 4G standards [4], and the targeting supply voltage is 1V, making it easy to adapt to the newest technology. With these parameters, the target of this step is to find out the power-optimal architecture at system level to guarantee optimal power consumption for every configuration mode, and the corresponding initial optimal NTFs, which will be further processed in the next step.

It is commonly known that the performance of a DSM can be determined by system parameters such as oversampling ratios (OSR), modulator orders and number of quantizer bits. And different combinations of these parameters can be used to achieve the same signal-to-noise ratio (SNR). However, the power efficiencies for the various design combinations in the design space are different. In this step, all the design combinations for each mode, which will be implemented in the reconfigurable DSM, are explored for single-loop DSMs. This is done by first find out an initial NTF for each design combination. As a rule of thumb, the infinity norm $\|H\|_\infty$ of the NTF is traditionally chosen to be 1.5 to guarantee a stable modulator. When multi-bit is used, $\|H\|_\infty$ can be increased to improve the SNR. However, this can't be pushed too far as the input range starts to decrease. For thermal noise dominant low-voltage application, extra power is needed to maintain the same DR. Thus, the optimal $\|H\|_\infty$ should be chosen to minimize the quantization noise, while maximize the input range. As an example, Fig. 2 shows the SNR performance of a third-order modulator with a 2-bit quantizer (OSR=128). The optimal $\|H\|_\infty$ is around 2 here since the SQNR increases very slowly when $\|H\|_\infty$ is larger than 2. Further increase of the $\|H\|_\infty$ leads to rapid decrease of the signal power, which in turn increases the power consumption budget used to reduce the thermal noise for the same DR. The optimal $\|H\|_\infty$ for the other design combinations can be chosen in the same manner and are shown in Table I. Once the $\|H\|_\infty$ is fixed, the corresponding NTFs with optimized zero positions for different specifications can be generated by using *synthesizeNTF* function in [5] with proper OSRs (Enough margin should be taken into account when choosing the OSR.).

The integrator and amplifier topologies are also chosen in this step based on the input specifications and the supply voltage. As only a limited supply voltage is available, 2-stage Miller OTA is used to maximize the output signal swing. To meet all the DR requirements for different standards, an R-C integrator is chosen for its superior linearity. Then, based on the initial NTFs and the circuit topologies, the power estimation method in [4] can be used to estimate the power consumption, both for feedforward (FF) and feedback (FB) topologies with different design combinations. Thermal noise, slew rate requirements, circuit stability, parasitic capacitances including the reconfigurability parasitics have been taken into account in the power estimation process.

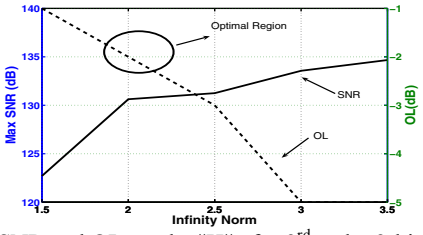
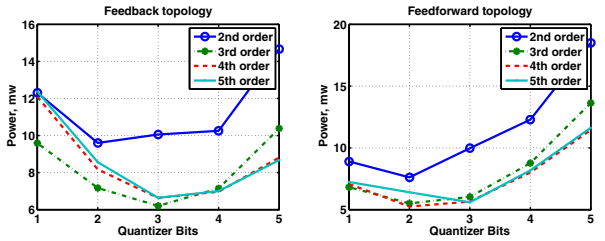


Fig. 2 SNR and OL vs. the $\|H\|_\infty$ for 3rd-order 2-bit DSM

Table I: Optimal $\|H\|_\infty$ of the NTF for DSM from 2nd to 5th order with number of quantizer bits from 1 to 5

	1 bit	2 bits	3 bits	4 bits	5 bits
Order 2	2	2.5	3	3.5	3.5
Order 3	1.5	2	3	3.5	4
Order 4	1.5	2	2.5	3.5	4
Order 5	1.5	2	2.5	4	5

The power-estimation results show that high-order DSMs with 2-3 bit quantizer are more power-efficient for WLAN mode, while DSMs with lower order modulator show better power-efficiency in GSM mode due to the increased overloading level compared to the high-order ones [4]. Between the two single-loop topologies, FF topology shows higher power efficiency and linearity due to the reduced signal swings. The power-estimation results for WLAN mode are shown in Fig. 3 as an example. All these results lead to the reconfigurable architecture shown in Fig. 4. It is a single-loop 4th order FF modulator with local-feedback path to form two resonators. These two resonators help to further suppress the quantization noise around the signal bandwidth. A variable delay caused by the quantizer is solved by introducing an explicit delay between the 2 DACs and the quantizer. This also relaxes the speed requirement of the quantizer. The fixed delay introduced in the feedback path is then compensated by the internal loop formed by DAC2.



WLAN mode BW=20MHz DR=55dB

Fig. 3: Power estimation results for WLAN mode

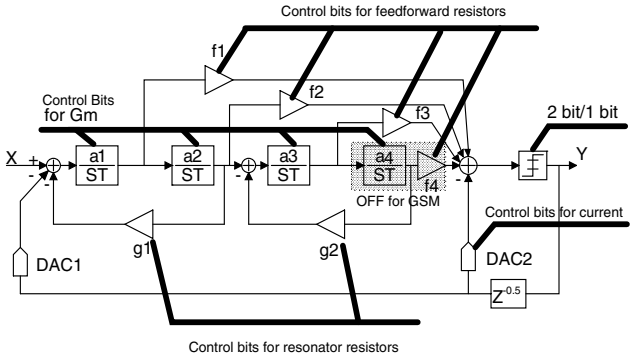


Fig. 4: Architecture of the reconfigurable DSM

In WLAN, DVB-H and UMTS mode, all four integrators in the loop filter are turned on and 2-bits quantizer is used for optimal power consumption. For the standards with lower bandwidth, the modulator allows to progressively switch off the last one or two integrators. In GSM mode, the first 3 integrators are turned on while the last stage is powered off. Single-bit quantizer is used in GSM mode for high linearity requirement. Two resonators are used in the WLAN mode to improve the SNR due to the low OSR. In UMTS and DVB-H mode, the local feedback coefficients become much smaller due to the increased OSR, which means big resistors have to be used in the local feedback path when R-C integrators are used. To avoid extremely large resistor, only the resonator with larger resonator frequency is used while still providing enough noise suppression. For the same reason, no resonators are used in GSM mode. In summary, the optimal configurations for 4 major standards are listed in Table II. The optimal $\|H\|_\infty$ for each configuration can be found from Table I and are also included in Table II.

Table II: Configurations for different modes

Standard	BW(MHz)	Configuration	OSR	$\|H\|_\infty$
WLAN	20	4th order, 2bit	16	2
DVB-H	3.8	4th order, 2bit	24	2
UMTS	2	4th order, 2bit	32	2
GSM	0.2	3rd order, 1bit	128	1.5

3.2 Step2: NTFs optimization

The second step of the design methodology which is very important for power optimization is to determine at system level the final NTFs, which maximize the stability, for different modes. With the optimal $\|H\|_\infty$ and OSR values summarized in Table II, the NTFs for different modes can be generated by using *synthesizeNTF* function in [5]. This function guarantees a maximally flat response outside the signal bandwidth while the stability is not optimized. For a fully reconfigurable design, large number of passive components and switches contribute a lot of parasitics, which will increase the power consumption compared to single-mode design and cause stability problem. To optimize the stability while lower down the power consumption, a stability optimization process is used here and described in the following steps. First, the initial NTFs for different modes are generated by *synthesizeNTF* using the parameters in Table II as a reference. Then, the target NTF (4th order is used here as an example) can be represented in the form of zeros and poles as follows

$$NTF = k\frac{(Z-z_{11})(Z-z_{12})(Z-z_{21})(Z-z_{22})}{(Z-p_{11})(Z-p_{12})(Z-p_{21})(Z-p_{22})} \quad (1)$$

where k is a constant. For a physically realizable system, there are two pairs of complex-conjugate zeros. The optimal value of the zeros and k value can be taken from the initial NTFs calculated in the first step. The two pairs of complex-conjugate poles can be written as

$$\begin{cases} p_{11} = r_1(\cos\theta_1 + i\sin\theta_1) \\ p_{12} = r_1(\cos\theta_1 - i\sin\theta_1) \end{cases} \begin{cases} p_{21} = r_2(\cos\theta_2 + i\sin\theta_2) \\ p_{22} = r_2(\cos\theta_2 - i\sin\theta_2) \end{cases} \quad (2)$$

From the above NTF, the loop filter transfer function can be derived and is given by [7]:

$$H_{loop} = \frac{1}{NTF} - 1 \quad (3)$$

By optimizing the phase margin of this loop-filter function, the stability can be maximized as will be explained further. To maintain the same SNR performance, the in-band noise gain should be no larger than the original one. Thus a constraint should be added during the optimization process.

$$rmsGain(NTF_{target}) \le rmsGain(NTF_{reference}) \quad (4)$$

where *rmsGain* represents the in-band root-mean-square noise gain. Mathematical calculation of the optimal phase-margin of the loop-filter is difficult, so numeric optimization by scanning r_1, r_2, θ_1 and θ_2 value is used here to find out the optimal positions of the poles. The maximum value of r_1, r_2 is set to 0.9 here to keep all the poles inside the unit circle. Fig.4 shows the positions of the poles of the NTF for WLAN mode before and after the phase-margin optimization. As shown in Fig. 5, both θ_1 and θ_2 become smaller. The radius of one pole is increased while the other one is reduced, as they were split apart.

After the optimization process, the out-band response is no longer maximally flat, and $\|H\|_\infty$ becomes larger than the original one. However, as the in-band noise doesn't change, the OL stays the same while stability becomes better. The response of the loop-filter around the unity-gain frequency is mainly determined by the first-order path. In the fully forward topology as shown in Fig. 4, the feedforward path is composed by the first integrator and the adder, which means extremely fast amplifiers are needed for both the first integrator and the adder, leading to large power consumption. By optimizing the phase margin of the loop filter, the speed requirement of these two blocks is greatly relaxed and their power consumption can

be lowered. Compared to the optimal parameters in [7] which are used to maximize the performance, the strategy used here focuses on robustness and power minimization while guaranteeing minimum performance levels, considering the increased parasitic effect for reconfigurable circuits.

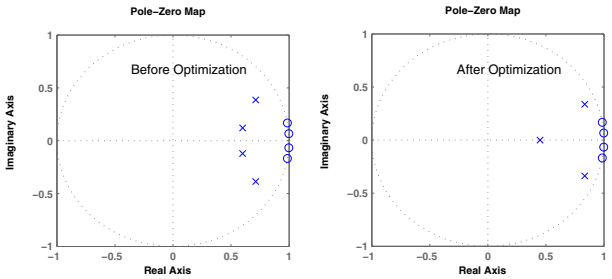


Fig. 5: Pole-zero map of the NTF before and after optimization

3.3 Step3: Coefficients Determination

In this step, the coefficient of the internal loop is first calculated. As mentioned in step 1, a common method used to tackle the quantizer delay while using the non-return-to-zero (NRZ) DAC pulse is to introduce a full clock delay in the feedback path to absorb the varying quantizer delay. In order not to influence the original impulse response of the loop filter, an internal feedback branch is introduced around the quantizer. Instead of a full period, a half clock period is used here as the explicit delay in the feedback path to further reduce the power consumption of the first integrator due to the relaxed speed requirement [6], while still providing enough time for the output of the quantizer to settle to the final value. When a multi-bit quantizer is used, the dynamic element matching (DEM) can be done before the quantizer without introducing any additional delay. The coefficient of the internal loop can be calculated by using the method in [6], and then the discrete-time function can be converted to the continuous-time domain using the impulse-invariant transformation [8]. Then, the coefficients of the integrators can be computed by comparing the general parametric equation of the system in Fig. 4, with the system loop functions which are calculated during the second step. Since there are 10 variables and 6 equations in the forth-order modulator, some initial values should be assigned to part of them. Here, all the scaling coefficients a_1 to a_4 of the integrators as shown in Fig.4 are set to be one initially. In reality, the output swings of the integrators are limited by supply voltage and linearity requirement. The scaling method in [9] is used to make the scaling for different modes. After scaling, the scaled coefficients for different modes are normally quite different from each other due to the different specifications and difference between NTFs. This would make the design of the reconfigurable array and layout difficult. To ease the design, the coefficients are rounded here to maximize the coefficient sharing between different modes. As the same number of integrators and quantizer bits are used in WLAN, DVB-H, and UMTS modes, these three modes can be grouped together. Minimum coefficient among the three modes is chosen for each integrator to meet different requirements. In a certain mode, as the non-idealities of the other stages are already shaped by the first integrator, more freedom is allowed to choose the coefficient. Therefore, the coefficient of the first integrator is used as a reference, and the other coefficients are rounded as

$$a_i = 2^n a_1 \tag{5}$$

where n is an integrator number which can be either positive or negative. The final coefficients for the integrators after scaling and rounding are shown in Table III.

Table III Integrator coefficients after scaling and rounding

Standards	a_1	a_2	a_3	a_4
WLAN	0.4	0.4	0.4	0.1
DVB-H	0.4	0.4	0.4	0.1
UMTS	0.4	0.4	0.4	0.1
GSM	0.4	0.4	0.1	N/A

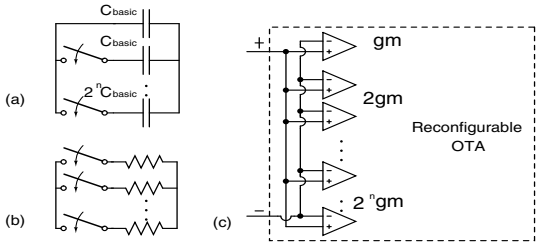


Fig. 6: (a) capacitor array (b) resistor array (c) OTA array

3.4 Step4: Calculation of the circuit parameters

As mentioned previously, the reconfiguration at architecture level is done by changing the order of noise shaping, number of resonators and quantizer bits. At the circuit level, the tuning of the integrator coefficients is realized by reconfiguring the passive elements such as capacitor and resistor arrays. To adapt to the various signal bandwidth and DR requirement, the transconductance of the OTA should also be scalable for optimal power consumption. By tuning the biasing current, the GWB can be scaled for different modes. However, this method decreases the speed and only a limited tuning range is available. To allow fully digital control, the concept of Switchable Op-Amp (SOA) [10] can be used to implement the OTAs in the integrator. Each SOA can be powered on or off by switching the voltage at the gate of all the transistors in the OTA simultaneously. By connecting the SOAs in a binary scaled array as shown in Fig. 6, a fully reconfigurable OTA is obtained. The basic unit SOA can be used for all the integrator stages and the adder in front of the quantizer. As a basic robust unit is used, the design complexity is reduced and fully digital control is available.

The forth step is to determine the circuit parameters such as the resistor and capacitor values for the modulators and granularities of the reconfiguration array. The starting point of this step is to determine the value of the input resistor in front of the first integrator. For linearity reason, no switches are used in front of the first integrator. Thus, a fixed resistor should be used for all the modes. In the thermal-noise dominated low-voltage design, the input resistor is given by [4]

$$R_{\text{int1}} \approx \frac{3}{16} \frac{(OL \cdot V_{ref})^2 V_{gst,DAC}}{kT \cdot DR \cdot BW \left(3V_{gst,DAC} + 4V_{ref}\right)} \tag{6}$$

where $V_{gst,DAC}$ is the overdrive voltage of the current transistor of the DAC; V_{ref} , which is the product of feedback current and R_{int1}, is the equivalent feedback reference voltage; To minimize the power consumption, $V_{gst,DAC}$ and V_{ref} are maximized for a certain supply voltage. Thus, $V_{gst,DAC}$ and V_{ref} are normally kept the same between different modes. In this case, the input resistor is determined by the mode with the largest $DR{\cdot}BW$ value. From Table II, GSM mode determines the R_{int1} here. To cover a wide range of sampling frequencies, a large capacitor array is needed for the first integrator. Two considerations should be kept in mind when designing the capacitor array. First, the capacitor array should not only be reconfigured to different modes but also can be finely tunable to overcome the process variations of the passive components. Second, the switches in the capacitor are normally connected to the virtue ground nodes for linearity reason and the output nodes of the OTA are directly connected to the bottom plate of the capacitor array. Therefore, it is important to minimize the total capacitance of capacitors in the array to reduce the parasitic capacitance and save area. The integration capacitance for a certain mode for the first integrator is determined by:

$$C_{\text{int}1} = \frac{1}{2 \cdot a_1 \cdot OSR \cdot BW \cdot R_{\text{int}1}} \tag{7}$$

Thus, the maximum capacitance value is determined by the GSM mode. When taken into account coefficients spreading, the maximum capacitance value is given by:

$$\frac{1}{a_{1,GSM} \cdot F_{S,GSM} \cdot R_{\text{int}1}}(1+\delta) \le C_{\max} \tag{8}$$

with $a_{1,GSM}$ the coefficient of the first integrator in GSM mode, $F_{S,GSM}$ the sampling frequency in GSM mode, δ the max amount of the coefficient spreading. The smallest nominal integration capacitor is determined by the WLAN mode. To cover the coefficient spreading, the basic capacitor unit value is given by:

$$C_{basic} = \frac{1}{2^{Num\_WLAN}}\left(\frac{1}{1-\delta} - \frac{1}{1+\delta}\right) \cdot C_{\text{int}1,WLAN} \tag{9}$$

where Num_WLAN is the tuning step in WLAN mode for coefficient spreading; $C_{\text{int}1,WLAN}$ is the nominal integration capacitor value for WLAN mode. Special care should be taken in choosing the C_{basic} which should not be too small to be influenced by the parasitic capacitances. Thus, tuning accuracy is lower bounded by the C_{basic} value, which is a fundamental limitation of the reconfigurable design. When a binary scaled capacitor array is used, the number of control bits needed to cover the whole range from WLAN to GSM can be calculated from (8) and (9) as follows:

$$N_{cap1} = \left\lceil \log_2\left(2^{Num\_WLAN} \cdot \frac{a_{1\_WLAN} \cdot F_{S,WLAN} \cdot (1+\delta)(1-\delta^2)}{2 \cdot a_{1\_GSM} \cdot F_{S,GSM} \cdot \delta}\right) \right\rceil \tag{10}$$

where [..] is the ceiling function.

Compared to the first one, the non-idealities of the other integrators such as thermal noise and non-linearity are suppressed by the gain of the first integrator. Thus, the input resistor can be scaled up without influence the input-referred noise level. For the fixed coefficient, the corresponding integration capacitor value can be scaled down to reduce the parasitics, area and power consumption. In order not to degrade the total performance, the scaling factor should be smaller than the gain of the first integrator.

$$f_{scale} \le \left(\frac{a_1 Fs}{2\pi \cdot BW}\right)^2 = \left(\frac{a_1 \cdot OSR}{\pi}\right)^2 \tag{11}$$

Thus, the minimum nominal capacitor value for the second integrator is given by:

$$C_{\text{int}2} \ge \frac{\pi^2}{(a_1 \cdot OSR)^2} \cdot \frac{1}{R_{\text{int}1} \cdot a_2 \cdot F_S} \tag{12}$$

As discussed previously, the C_{basic} should be large enough to overcome the parasitic influence. Therefore, C_{int2} is also limited by:

$$C_{int\,2} \ge C_{basic} \cdot 2^{Num\_min} \cdot \left(\frac{2\delta}{1-\delta^2}\right) \tag{13}$$

where Num_min is the minimum tuning step to guarantee a reasonable accuracy. Based on the chosen value of the C_{basic} here for the reconfigurable design, (13) determines the lower limitation of the C_{int2}. For better matching and easier reconfiguration, it is better to make the input-resistor array binary scaled. Thus, the available sampling frequency is also binary scaled. As the crude tuning is done by resistor arrays, the space between two available sampling frequencies can be covered by the capacitor arrays. This can be done by making the maximum capacitor twice the value as (13). In this way, the reconfigurable DSM is able to adapt to all the sampling frequencies ranging from WLAN mode to GSM mode with minor tuning steps. Thus, the number of control bits needed for the capacitor array of the second integrator can be calculated as follows:

$$N_{cap2} = \left\lceil Num\_min + 1 + log_2\left(\frac{1-\delta^2}{2\delta}\right) \right\rceil \tag{14}$$

(13) and (14) can also be used to determine the capacitor arrays for the last two stages. The corresponding resistor value can be derived from Table II and Table III, once the nominal capacitor values are fixed.

Besides the passive component array, the reconfigurable OTA arrays which are made up by SOAs are used here for flexible power configuration. For the high speed requirement, the OTA for the first integrator in the WLAN mode needs the largest transconductance to guarantee enough open loop GBW and phase margin. The equivalent transconductance is given by:

$$Gm_{\text{int}1,WLAN} = c \cdot F_{S,WLAN}(C_{\text{int}1,WLAN} + C_{load1}) \tag{15}$$

where c is a constant to maintain enough GBW for loop stability [11], C_{load1} is the load capacitance of the first integrator. The minimum transconductance is needed for the second to third stage in the GSM mode. The corresponding transconductance can be determined by:

$$Gm_{int\,2,GSM} = \frac{Gm_{int1,GSM}}{f_{scale}} = Gm_{int1,GSM} \frac{C_{basic} \cdot 2^{Num\_min} \cdot \frac{1-\delta^2}{2\delta}}{\frac{1}{a_{1,GSM} \cdot F_{S,GSM} \cdot R_{int1}}} \tag{16}$$

Unlike the coefficients, the transconductance values don't have to be very accurate. So $Gm_{int2,GSM}$ can be used as the basic unit for all the integrators. Thus, by using (7), (15) and

(16), the number of control bits needed for the reconfigurable OTA of the first integrator is given as follows:

$$N_{ctr} = \left\lfloor log_2 \left(\frac{\frac{2\delta}{(1-\delta^2)F_{S,GSM}} \left(\frac{1}{a_{1,WLAN} R_{int1}} + C_{load1} F_{S,WLAN} \right)}{2^{Num\_min} (1 + a_{1,GSM} R_{int1} C_{load1} F_{S,GSM}) C_{basic}} \right) \right\rfloor \quad (17)$$

The control bits for the other OTAs can be determined in the same manner as described above.

4. Results and discussions

The above 4-step design methodology is implemented in a MATLAB program. Given a certain technology, the inputs of the program are the specifications and configurations for different modes, while the outputs are the circuit parameters and program granularities for the capacitor, resistor and OTA arrays. Based on these results, the number of OTA units used for different configurations are summarized in Table IV. To evaluate the effectiveness of the design methodology, an accurate macro model was built for the basic unit SOA based on standard 90nm CMOS technology. Non-idealities such as parasitic capacitance, loop delay, and limited slew rate are also modeled. Then, long-time simulations using ELDO are used to simulate the macro-model of the reconfigurable DSM. The performances of the DSM for each configuration are shown in Table V. The simulated spectra are shown in Fig. 7. Hann window is used for the FFT to minimize the noise leakage. The number of samples is chosen as 4096 samples for enough accuracy. The input frequencies for corresponding modes are shown in the plots. For better comparison, both the initial NTFs (synthesized by [5]) and optimized NTFs are used to implement the DSM, and the estimated power consumptions based on the simulation results are also listed. From Table V, the average power saving by using the optimized NTFs is up to 30%. As the modulator is able to adapt to all the sampling frequencies between the WLAN mode and GSM mode, it is also able to adapt to other modes such as Bluetooth (BT) and the modes of WiMAX with requirements in between these two extremes. Although this design methodology is now only able to synthesize a power-optimized reconfigurable single-loop DSM, it is easily extendible to include the cascaded topologies in the design space exploration without changing the basic steps of the methodology, leading to a more general result.

5. Conclusions

A design methodology for power-optimal design of digitally controllable, fully reconfigurable continuous-time DSM has been presented. Given the specifications for different modes, this design methodology determines the optimal circuit parameters and the granularity of component programmability while leveraging power consumption, parasitics and reconfigurability. The synthesized modulator is able to adapt its architecture- and circuit-level specifications for various modes at optimal power performance.

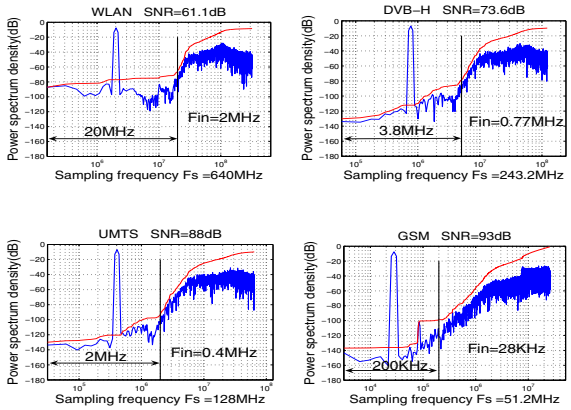


Fig. 7: Simulated spectra for WLAN, DVB-H, UMTS and GSM

Table IV: Number of unit SOAs used for different configurations

Standards	integrator1 (5 bit)	integrator2 (4 bit)	integrator3 (4 bit)	integrator4 (4 bit)	adder (5bit)
WLAN	24 unit	8 unit	8 unit	8 unit	24 unit
DVB-H	12 unit	4 unit	4 unit	4 unit	8 unit
UMTS	8 unit	2 unit	2 unit	2 unit	6 unit
GSM	8 unit	1 unit	1 unit	N/A	3 unit

Table V: Simulated SNRs and power consumption

Modes	Configuration	BW (MHz)	OSR	SNR (dB)	Power(mw)		
					Optimized NTF	Initial NTF	Saved Power
WLAN	4thorder 2 bit	20	16	60.2	9	13.8	34%
DVB-H	4thorder 2 bit	3.8	24	69.6	4.2	6	36%
UMTS	4thorder 2 bit	2	32	80	3.2	4.3	26%
GSM	3thorder 1 bit	0.2	128	88.5	1.8	2.3	24%

References

[1] L. Guojun, "Quality of service management in distributed multimedia systems", IEEE International Conference on Systems, Man, and Cybernetics, 1996.,Vo. 2, Issue, pp:1321 - 1326. Oct 1996

[2] W. Yin, D. Alex, "Systematic methodology for designing reconfigurable ΔΣ modulator topologies for multimode communication systems." IEEE Transactions Computer Aided Design, vol. 26, 480-496, 2007.

[3] R. Lopez, A. Morgado, et al "Systematic top-down design methodology of reconfigurable ΣΔ modulators for multi-standard transceivers" Springer Analog Integrated Circuits and Signal Processing, Nov. 2008

[4] K. Yi, J. Craninckx, Gielen G. "A Design Approach for Power-Optimized Fully Reconfigurable ΣΔ A/D converter for 4G Radios", IEEE *Trans. Circuit Syst. II,* vol.55, pp.229-233, Mar. 2008.

[5] R. Schreier "The Delta-Sigma Toolbox Version 7.1" , http://mathworks.com/matlabcentral/fileexchange

[6] K, Yi, R. Soheil, C, Jan. V. Guy, and G. Gielen "A systematic design methodology for power-optimal design of high-order multi-bit continuous-time Delta-Sigma modulators" Springer Analog Integrated Circuits and Signal Processing, Jan. 2008

[7] M. Augusto, P. Vincenzo, and S. Michile "Optimal Parameters for ΣΔ modulator Topologies", IEEE *Trans. Circuit Syst. II,* vol.45, pp.1232-1241, Sep. 1998

[8] J. A. Cherry, W. M. Snelgrove, *Continuous-Time Delta-Sigma Modulator for High-Speed A/D Conversion,* Kluwer Academic Pubishers, 2000

[9] S. Paton, et al. "Optimization algorithm for linearity enhancement in the design of continuous-time ΔΣ modulators." Proceedings of SPIE, VLSI Circuits and Systems II, Vol. 5873, pp. 93-99. 2004

[10] V. Giannini, J. Craninckx, et al., "Fully reconfigurable Active-Gm-RC biquadratic cells for Software Defined Radio applications," *Proc. ISCAS,* pp. 1047-1050, May, 2006.

[11] M. Ortmanns, F. Gerfers, and Y. Manoli, "Compensation of Finite Gain-Bandwidth induced Errors in Continuous-Time Sigma-Delta Modulators," IEEE *TCAS II,* vol.51, pp.1088-1100, June 2004.