Improving Compressed Test Pattern Generation for Multiple Scan Chain Failure Diagnosis

Xun Tang¹, Ruifeng Guo², Wu-Tung Cheng², Sudhakar M. Reddy¹

¹Department of Electrical and Computer Engineering, University of Iowa, Iowa City, IA 52242, USA {xutang, reddy}@engineering.uiowa.edu

²Mentor Graphics Corporation, 8005 S.W. Boeckman Rd., Wilsonville, OR 97070, USA {ruifeng_guo, wu-tung_cheng}@mentor.com

Abstract

To reduce test data volumes, encoded tests and compacted test responses are widely used in industry. Use of test response compaction negatively impacts fault diagnosis since the errors in responses due to defects which are captured in scan cells are not directly observed. We propose a simple and effective way to enhance the diagnostic resolution achievable by production tests with minimal increase in pattern counts. In this work we present experimental results for the case of multiple scan chain faults to demonstrate the effectiveness of the proposed method.

1. Introduction

Cost of test of manufactured VLSI circuits using scan based structural tests is determined by test application time and tester memory costs. Several methods to reduce these costs have been recently developed and are used in industry [Lee 99], [Ham 00], [Raj 04], [Bar 01], [Who 03]. All these methods divide the scan cells in to large number of scan chains and use compressed tests which are decompressed using on-chip decompression logic. This allows use of a small number of tester channels to load tests. Test response data is also compacted typically by a linear circuit and observed through a small number of tester channels. Compacted test responses negatively impact fault diagnosis due to reduced observability. Earlier methods to improve fault diagnosis for circuits using test response compaction include the use of bypass of compaction circuits, use of additional tests beyond production tests used to only detect defects [Kun 94], [Li 05], [Guo 07]. Bypassing compaction requires additional on-chip circuits and increased test data volume. Using additional tests to improve diagnosis can be done in two ways. One is to augment production tests. However since this approach increases test application time it is typically not used. The other approach is to use production tests first to detect defects and then use additional tests for diagnosis purpose. Additional tests may be based on diagnosis using the production tests [Guo 07]. However this method may require mounting the failing chips on the testers a second time. Use of additional tests to improve diagnostic resolution may not be applicable in volume diagnosis used for yield learning and yield ramp up [Chu 08]. Yield learning for VLSI circuits designed at current and future technology nodes of 45 nm and below will require diagnosis of tens to hundreds of thousands of failing chips [Sha 08]. The ideal solution for improved diagnosis is to improve the diagnosis achieved by production tests without increasing pattern counts by much. In this work we provide a simple method to achieve this goal.

The rest of this paper is organized as follows. Section 2 introduces background. Section 3 explains the proposed method. Section 4 gives experimental results on several industrial designs and Section 5 concludes this paper.

2. Preliminaries

In this section we review test response compactors and discuss the problem considered in this work.

2.1 Test response compactors

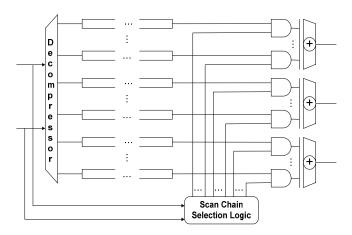


Figure 1: A space compactor with 3 output channels

Typically test responses are compacted either using multiple input signature registers (MISRs) [Elg 97] or trees of Exclusive ORs (XORs) called space compactors [Sal 83]. If MISRs are used then one has to prevent unknown values entering the compactor. Using XOR trees permits unknown values in test responses entering the compactors. In this work we consider circuits using space compactors. Figure 1 shows a typical space compactor which compacts several scan chains into 3 output channels.

The test response data in scan chains go through the XOR trees and are scanned out using the output channels. For space compactors, unknown values are permitted to enter the compactor. However, an unknown value corrupts all the test response data in the same scan cycle of the scan chains connected to the same output channel, thus masking the faults which are propagated to these scan cells. In order to maximize the detection ability of a test pattern and minimize the effect of unknown values, scan chain selection logic is usually utilized. Scan chain selection logic includes a mask register and a decoder as shown in Figure 2 for one output channel. The mask bits, determined separately for each pattern, are delivered through the test inputs to the mask register and the decoder is usually a linear logic circuit to decode the mask bits into masking signals. The masking signals drive inputs to AND gates. Usually the number of mask bits of a mask register is smaller than the number of masking signals. To reduce test data volume, mask bits are determined for each test pattern and the decoded masking signal for each scan chain doesn't change during scan unload. As shown in Figure 2, all the scan cells on chain1 is observed through XOR tree and all the scan cells on the other chains are masked since the scan chain selection logic sets all except the input to the first AND gate to 0.

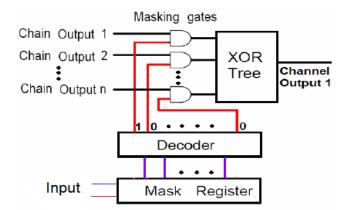


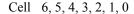
Figure 2: Scan chain selection logic

2.2 Problem formulation

When space compactors are used, internal scan chains are not observed directly at the output channel. The reduced observability of internal scan chains and the interaction between them can adversely impact scan-based diagnosis.

Scan chain failures are the cause for substantial proportion of failing chips. As 30%-50% of logic gates of a typical chip impact the operation of scan chains, it is very likely that scan chain operations will be impacted by random and/or systematic defects. Meanwhile failures on multiple scan chains are observed much more frequently than they were before. [Bas 08] reported that 32% of 529 units with scan chain failures contained multiple chain failures. Note that with the space compactor, the number of scan chains is much larger than that of traditional scan designs, thus the probability to have multiple scan chain failures is even higher in a modern scan compression designs than traditional scan designs. Multiple scan chain failures can be caused by either independent defects that land on different scan chains or by defects on a global signal driving multiple scan chains. For example, delay fault in a buffer in a clock tree can cause hold-time violations on multiple chains. Diagnosis of multiple chain failures with space compactors are challenging when multiple scan chains of the same output channel fail.

Figure 3 shows an example of how a space compactor can mess up the failures at an output channel when more than one scan chain among those observed through the output channel are faulty.



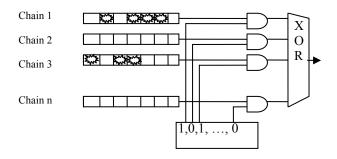


Figure 3: Illustrating multiple chain failures

From Figure 3, it can be seen that in the failing chain "chain1" there are 4 failing bits at scan cell 1, 2, 3 and scan cell 5. In the failing chain "chain3" there is 3 failing bit at scan cell 3, 4, 6. The masking signals from the chain selection logic are shown in the figure. Failing chain "chain1" and failing chain "chain3" are both observed through the space compactor with single output. So after the space compactor due to compaction there are 5 failing bits at scan cell 1, 2, 4, 5 and scan cell 6. For diagnosis purposes, given the 5 failing bits, it becomes difficult for the diagnosis tool to know which scan chain is causing which failing bit. If two failing chains have failing bits at the same scan shift cycle, the two failing bits cancel each other, which also makes the chain diagnosis difficult. As shown in Figure 3, failing bits at scan cell 3 of "chain1" and scan cell 3 of "chain3" cancel each other. In the example illustrated in Figure 3 if "chain3" is masked then the failures at the output will be caused only by the errors captured in "chain1" and

this aids diagnosis. This example also illustrates the key idea behind the simple strategy we are proposing to improve diagnosis by production patterns. The idea is to mask or not observe at least one selected scan chain among those that are driving a single output of the compactor. However, in order to keep the pattern counts close to those normally obtained, we do this only when all the scan chains are selected for observation by the normal test generation flow. Thus we attempt to minimally disturb the normal test generation flow. Details of this procedure are given in the next section.

In a regular production test pattern set, in the chain-test step, flush tests are applied and they include the tests which only observe one chain in each output channel at one time. Thus, which chains are faulty can be readily identified [Hua 05]. However, identifying which scan cells are faulty on faulty chains is very challenging. For regular production test patterns the scan chain selection logic observes all scan chains when no unknown value is in the scan cells in order to maximize the detection ability and minimize the pattern count. As discussed above, diagnosis of failing scan cells is made difficult when more than one chain observed through a single compactor output are faulty. In [Guo 07], a diagnostic pattern set was proposed for diagnosing failing scan cells in designs with space compactors. These additional patterns are generated based on the results of diagnosis using production patterns that detected the failing chip. Since the approach requires testing the failing chips a second time, it may be too expensive, if not impossible, to use in some test flows. The optimal solution and our goal in this work is to improve the diagnostic resolution achievable by production tests without increasing pattern counts or requiring additional test time.

3. A method to improve diagnostic resolution of production tests

We first give definitions of some terms used in this paper. These terms define the nature of tests with respect to how the responses to them are observed through the output channels of a space compactor. **Non-masking pattern** denotes the patterns whose responses in all scan chains are observed through compactor outputs. **Partial-masking pattern** denotes the patterns whose responses in more than one chain are observed and the rest of the chains are masked by the chain selection logic. **1-hot pattern** denotes the patterns whose response in only one scan chain in each output channel is observed and all the other chains are masked.

3.1 Normal test generation flow

In Figure 4, a normal scan chain selection algorithm for a test pattern is shown. After a test pattern is generated, the procedure enters the chain selection flow.

First the pattern is fault simulated to determine fault propagation sites and unknown value locations in the scan chains. Based on the results of fault simulation, masking signals are assigned to one scan chain at a time and the masking signals are encoded together with the test or in additional bits scanned in after the test. Mask assignments and encoding is repeated until the encoding capability is reached. The number of mask bits of a mask register is less than the number of masking signals. So encoding capability is reached when all the mask bits of the mask register are determined, at which time the remaining masking signals are determined by the mask bits.

Detection of undetected faults is the priority for the normal chain selection procedure. For this reason, for most test patterns the scan chain selection logic selects all chains for observation when X (unknown values) ratio is not high. However these patterns may not provide efficient information for diagnosis purpose.

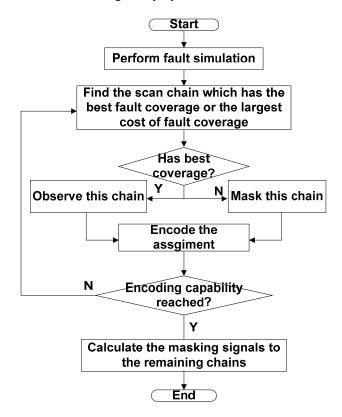


Figure 4: Normal chain selection procedure

3.2 Proposed chain selection procedure

In order to improve the diagnostic resolution by production patterns with minimal pattern count increase, we propose a new chain selection procedure in the test generation flow. While the normal chain selection procedure only considers detection ability of each pattern and observes all scan chains when there is no unknown values in scan chains that affect fault coverage, the proposed chain selection procedure considers the diagnosability of each pattern and masks a small number of chains without much loss of detection ability of a test pattern. This difference is the basic idea for an effective and simple method to increase the diagnosis capability of production patterns.

The proposed scan chain selection procedure is shown in Figure 5. It is explained below.

After a test pattern is generated, first the normal chain selection flow is performed. At the exit of the normal flow, only if all the scan chains are observed, the proposed flow is entered.

If the proposed scan chain selection flow is entered, first the mask bit encoding is rolled back. In order to keep the detection ability of the pattern, we start assigning the masking signals as in the normal flow until 5% of all the scan chains are assigned masking signals. The 5% threshold can be changed. However our experiments suggest that in general this threshold is good for most circuits.

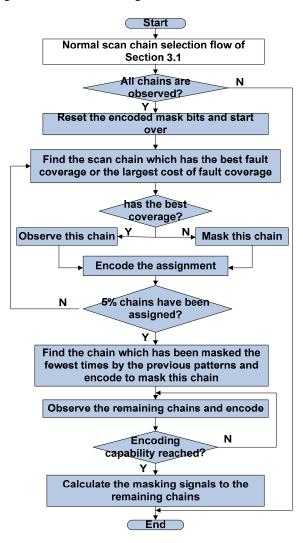


Figure 5: The proposed chain selection procedure

Next, we go through all the scan chains which have not been assigned masking signals and find the chain which has been masked the fewest times by the previous test patterns and we mask this chain. Then we set the mask bits to observe the remaining chains until the encoding capability is reached. Thus we attempt to mask a single chain that has been masked least number of times in earlier generated patterns. It is possible that the encoded mask may mask additional chains or observe other chains but at least one scan chain is masked by this procedure.

In the last step based on the determined mask bits, the masking signals of all the scan chains are set by the decoder in the scan selection logic and the scan chain selection flow is complete for this test pattern.

In the proposed procedure, in order to preserve the fault coverage, for each scan pattern, several chains which provide the best fault coverage gains are observed as in the normal flow. The rest of the scan chains are set to be masked or observed based on the improvement of diagnosis capability for multiple chain failures. The diagnosis capability of multiple chain failures are measured by the frequency of a scan chain being masked/observed. The most frequently observed scan chains are given higher priority to be masked while the least frequently observed scan chains are given higher priority to be observed. By balancing the masking and observation of the scan chains, we improve the probability that some failing scan chains are observed while other chains are masked for some scan patterns. The proposed chain selection algorithm masks a small portion of the scan chains even when there are no X (unknown) states or limited X states for the generated test pattern. So there are more partial masking patterns and fewer non-masking patterns in the generated production test pattern set. This enhances the diagnosis capability of the production test pattern set by improving the possibility of differentiating multiple faulty chains.

The diagnosis results on several industrial designs in the next section show the effectiveness of the proposed technique.

4. Experimental results

We modified an existing commercial ATPG tool that accommodates test response compactors to derive production tests using the proposed strategy. We injected different types of defects in multiple scan chains. Diagnosis based on response to the production tests was done using a commercial fault diagnosis tool.

Experimental results are given for four industrial designs. All the designs used space compactors shown in Figure 1. Different types of single faults are injected at random scan cells locations into 2 or 3 scan chains connected through a space compactor to the same output channel. As we indicated earlier the faulty chains are identified by production tests during the chain-test phase using 1-hot patterns. Thus, the objective of diagnosis is to determine the faulty scan cells in the defective scan chains.

In addition to the proposed method, we also implemented a random method for comparison. The two methods differ in only one step. In the proposed method as shown in Figure 5, in one step we go through all the scan chains which have not been assigned masking signals and find the chain which has been masked the fewest times by the previous test patterns and we mask this chain. In the random method, in this step we randomly select a chain from those which have not been assigned masking signals and mask this chain. The statistics of the four designs are shown in Table 1 together with the pattern counts of the normal production tests and the production tests generated using random method and using the proposed method. The pattern count increase from the normal production tests to the tests generated using the proposed method is shown in the last row of Table 1.

	Design	Design	Design	Design
	1	2	3	4
# of chains	401	160	400	160
# output channels	8	4	8	2
# of gates	320K	496K	1.1M	1.4M
X ratio*	0.003%	0.04%	0.004%	0.98%
# of normal patterns	4755	2065	5561	2847
# of rand. patterns*	4761	2081	5639	2875
# of proposed patterns	4757	2070	5611	2866
Pattern count increase*	0.04%	0.24%	0.90%	0.67%
1 77 1 1 0	** 1 *		•	11

Table 1: The statistics and pattern counts of 4 designs

* X ratio: the ratio of X bits in test responses in scan cells * # of rand. patterns: the number of the test patterns generated using the random method From Table 1, we can see that the pattern count increase varies from 0.04% to 0.90%, the maximum of which is less than 1%. The fault coverage for all the designs are the same using either the normal production tests or the proposed test patterns. Also we can see that the numbers of patterns generated using random method are larger than the numbers of patterns generated using proposed method for all the four designs.

In Table 2, the diagnosis results for injected stuck-at faults in 2 scan chains are given. In Table 3, the diagnosis results for injected stuck-at faults in 3 scan chains are given. In Table 4, the diagnosis results for injected timing faults in 2 scan chains are given. The timing faults for each design have the same number of slow-to-rise, slow-to-fall, fast-to-fall, fast-to-fall, fast-to-rise and hold-time faults.

If the number of suspect scan cells reported by the diagnosis tool for a failing chain is no more than 5 and the defective scan cell is in the reported suspect scan cells, we consider that this chain is diagnosed. Otherwise, we consider that it is not diagnosed successfully.

Table 2: Experimental results for stuck-at faults on 2 faulty chains
--

Design	Design 1 (64 cases)			Design 2 (40 cases)			Design 3 (40 cases)			Design 4 (40 cases)		
	Nor.	Rand	Prop.									
Result						-			_			
2 chains	4	33	45	26	35	38	0	21	22	23	26	31
1 chain	21	29	17	12	4	2	7	16	16	15	13	9
0 chain	39	2	2	2	1	0	33	3	2	2	1	0
Ave. Res.	17%	57%	68%	72%	78%	82%	16%	49%	50%	61%	65%	69%

Table 3: Experimental results for stuck-at faults on 3 faulty chains

Design	Design 1 (24 cases)			Design 2 (20 cases)			Design 3 (24 cases)			Design 4 (20 cases)		
Result	Nor.	Rand	Prop.									
3 chains	0	9	11	6	12	17	0	5	9	9	10	13
2 chain	1	7	10	4	5	2	2	12	7	6	8	7
1 chain	8	6	3	6	3	1	3	5	6	2	1	0
0 chain	15	2	0	4	0	0	19	2	2	3	1	0
Ave. Res.	10%	47%	56%	47%	69%	84%	10%	40%	51%	53%	58%	64%

Table 4: Experimental	results for	timing f	aults on 2	faulty chains
···· · · · · · · · · · · · · · · · · ·				

Design	Design 1 (40 cases)			Design 2 (40 cases)			Design 3 (40 cases)			Design 4 (30 cases)		
Result	Nor.	Rand	Prop.									
2 chains	2	24	32	19	27	31	6	21	27	24	27	28
1 chain	13	9	3	11	8	5	4	18	12	0	2	1
0 chain	25	7	5	10	5	4	30	1	1	6	1	1
Ave. Res.	18%	69%	80%	53%	73%	81%	15%	57%	70%	75%	88%	90%

In each table, we list the number of scan chains that are successfully diagnosed by the normal test patterns, by the test patterns that are generated using the random method, and by the test patterns that are generated using the proposed scan chain masking selection technique. The rows with "N chains" where N is 0, 1, 2, or 3, show the number of scan chains that are successfully diagnosed by the commercial diagnosis tool used.

As can be seen from Tables 2-4, the proposed method is very effective in improving the diagnostic resolution. For example from Table 2, for design 1 with two faulty chains, using normal scan chain selection flow for only 4 out of 64 cases can we have no more than 5 suspect scan cells identified in both the failing chains. However, using the tests by the proposed method in 45 out of 64 cases the number of suspect scan cells is within 5 for both the failing chains. This higher success rate is achieved at the cost of only 0.04% increase in pattern count.

Meanwhile, we can see that the proposed method is more effective in improving the diagnostic resolution than the random method. For example from Table 3, for design 3 with three faulty chains, using the random method for only 5 out of 24 cases can we have no more than 5 suspect scan cells identified in all the three failing chains. However, using the tests by the proposed method in 9 out of 24 cases the number of suspect scan cells is within 5 for all the three failing chains.

We also calculated the average diagnostic resolution for each design. The average diagnostic resolution is calculated as follows: The diagnostic resolution of a failing chain is the reciprocal of the number of the suspect scan cells for this chain. For example, if the diagnosis result gives 4 suspect scan cells for a chain including the defective scan cell, then the diagnostic resolution is 25%. The average resolution, given in the last row of Tables 2-4, is the average over all the injected faults. From Table 2 we note that the average resolution for Design 1 is also improved from 17% to 68%. Similar improvements in average resolution can be observed for the cases of stuck-at faults in 3 scan chains and for timing faults given in Tables 3 and 4, respectively. As can be seen, for all the cases from Table 2 to Table 4, the random method improves diagnostic resolution but not as much as the proposed method has improved.

The proposed method can be readily adapted to any space compactor designs using any test flow. With minimal increase in test pattern counts and without fault coverage degradation diagnostic resolution can be improved effectively. Thus we can potentially avoid using additional diagnostic test patterns for some diagnosis of multiple scan chain failures.

5. Conclusions

In this paper, we investigated the diagnosis capability of production test patterns of designs with space compactors to compact test response data. We proposed a simple and effective method to improve the diagnostic resolution of multiple chain failures with minimal increase in pattern counts. This method can be easily adopted into any test flow environment as it does not require any changes to test flows.

References

[Sal 83] K. K. Saluja and M. Kiupovsky, "Testing computer hardware through data compression in space and time," Proc. ITC, pp. 83-88, 1983.

[Kun 94] S.Kundu, "Diagnosis Scan Chain Faults", IEEE Trans. On VLSI System, Vol. 2, No. 4, 1994, pp.512-516.

[Elg 97] F. Elguibaly and M. W. El-Kharashi, "Multiple-Input Signature Registers: An Improved Design", Communications, Computers and Signal Processing 1997, Vol. 2, pp 519-522.

[Lee 99] K.-J. Lee, J.-J. Chen, and C.-H. Huang. "Broadcasting Test Patterns to Multiple Circuits", IEEE Trans. on CAD, 18(12):1793-1802, Dec. 1999.

[Ham 00] I. Hamzaoglu and J. H. Patel, "Reducing test application time for full scan embedded cores", VTS 2000, pages 369–375.

[Bar 01] C. Bar, V. Brunkhorst, F. Distler, O. Farnsworth, B. Keller and B. Koenemann, "OPMISR: The Foundation for Compressed ATPG Vectors", ITC 2001, paper 27.4.

[Who 03] P. Wohl, L. Huisman, "Analysis and Design of Optimal Combinational Compactors", VTS 2003, pp 101-106.

[Raj 04] J. Rajski, J. Tyszer, M. Kassab and N. Mukherjee, "Embedded Deterministic Test", IEEE trans. on CAD, VOL. 23, NO. 5, May 2004, pp 776-792.

[Hua 05] Y. Huang, W.-T. Cheng, J. Rajski, "Compressed Pattern Diagnosis For Scan Chain Failures", ITC 2005, paper 30.3.

[Li 05] J. C.-M. Li, "Diagnosis of Multiple Hold-time and Setup-time Faults in Scan Chains", IEEE Trans. on Computers, Vol. 54, No. 11, 2005, pp. 1467-1472.

[Raj 06] J. Rajski, J. Tyszer, G. Mrugalski, W.-T. Cheng, N. Mukherijee, M. Kassab, "X-Press Compactor for 1000X Reduction of Test Data", ITC 2006, paper 18.1.

[Guo 07] R. Guo, Y. Huang, W.-T. Cheng, "A Complete Test Set to Diagnose Scan Chain Failures", ITC 2007, paper 7.2.

[Bas 08] N. Basturkmen, R. Guo and S. Venkataraman, "Diagnosis of Multiple Scan Chain Failures", Proc. ETS 2008.

[Sha 08] M. Sharma, B. Benware, L. Ling, D. Abercrombie, L. Lee, M. Keim, H. Tang, W.-T. Cheng, T.-P. Tai, Y.-J. Chang, R. Lin and A. Man, "Identifying Physical Root Causes for Yield Excursions from Test Fail Data", Proc. ETS 2008.

[Chu 08] W.-S. Chuang, W.-C. Liu and J. C-M. Li, "Diagnosis of Multiple Scan Chain Timing Faults", IEEE trans. on CAD of Integrated Circuits and Systems, Vol. 27, No. 6, June 2008, pp1104-1116.