A MEMS Reconfigurable Quad-Band Class-E Power Amplifier for GSM Standard

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***Abstract*—In this paper we present a reconfigurable Class-E Power Amplifier (PA) whose operation frequency covers all uplink bands of GSM standard. We describe the circuit design strategy to reconfigure PA operation frequency maximizing the efficiency. Two dies, manufactured using CMOS and MEMS technologies, are assembled through bondwires in a SiP fashion. Prototypes deliver $20dBm$ output power with 38% and 26% drain efficiencies at lower and upper bands, respectively. MEMS technological issues degrading performance are also discussed.**

I. Introduction

Mobile phone transceivers work on different frequency bands to comply with telecommunication standards. The GSM protocol employs four uplink bands, demanding Power Amplifier (PA) solutions that have to deal with a wide frequency range. Designing PAs with bandwidth exceeding $100MHz$ is not an issue [1]–[3]. Commercial solutions for GSM employ usually two PAs, whose operation frequencies are centered at $\approx 900MHz$ and $\approx 1800MHz$ to allow signal amplification at lower or upper bands, respectively [2]. Unfortunately, this solution requires to duplicate the circuitry, even though just one PA is operating at a time. For this reason, a reconfigurable PA covering both lower and upper bands is strongly desirable to reduce chip area.

In this scenario, we propose in this work a reconfigurable mid-power Class-E PA operating at $\approx 900MHz$ and $\approx 1800MHz$, realized assembling two chips manufactured using $0.35\mu m$ CMOS and Micro Electro Mechanical Systems (MEMS) technologies, respectively. The CMOS chip realizes the active part of the circuit, whereas MEMS switches and passives realize the reconfigurable PA output network working at lower and upper bands.

The adoption of a Class-E topology mitigates the circuit sensitivity against components variation. Indeed, in spite of very high performance, MEMS technology for RF applications still needs to reach a completely controlled process leading to a very small component variability [4]. Nevertheless, switches able to deal with RF signals [5] and compact models suitable for circuit simulations [6] are available, allowing RF designers to develop MEMS based solutions. The paper is organized as follows. Section II describes theoretical aspects and circuit design of a reconfigurable Class-E PA. In Section III we present and discuss experimental results. Conclusions follow.

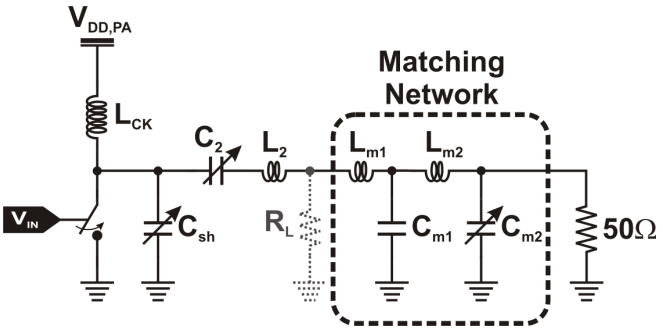

Fig. 1. Schematic of a reconfigurable Class-E PA. The Matching Network down transforms the 50Ω antenna to R_L optimum load.

II. Reconfigurable Class-E Power Amplifier Design

Class-E power amplifiers, invented by Sokal in 1975 [7], are switched amplifiers whose components, shown in fig. 1, are sized according to simple design equations [8].

$$R_L = \frac{\alpha V_{DD}^2}{P_{out}} \;\; ; \;\; C_{sh} = \frac{\beta}{\omega_0 R_L}$$
$$C_2 = \frac{\gamma}{\omega_0 R_L} \;\; ; \;\; L_2 = \frac{Q_{out} R_L}{\omega_0} \qquad (1)$$

α, β, γ are parameters that depend on the output network quality factor Q_{out}; P_{out} is the output power with ideal 100% efficiency; V_{DD} is the voltage supply; ω_0 is the frequency; R_L is the load resistance.

For a maximum output power $\approx 21dBm$ at both lower and upper bands, assuming a real $\approx 40\%$ efficiency and a $Q_{out} = 2.5$, and considering a maximum $V_{DD} = 3V$ for reliability constraints [9], leads to $R_L = 12\Omega$.

The matching network required to down-transform the 50Ω antenna resistance at both lower and upper bands is completely realized by an external MEMS based network. It is comprised of two LC ladder which down transforms the antenna resistance at $\approx 900MHz$ and $\approx 1800MHz$ using a minimum

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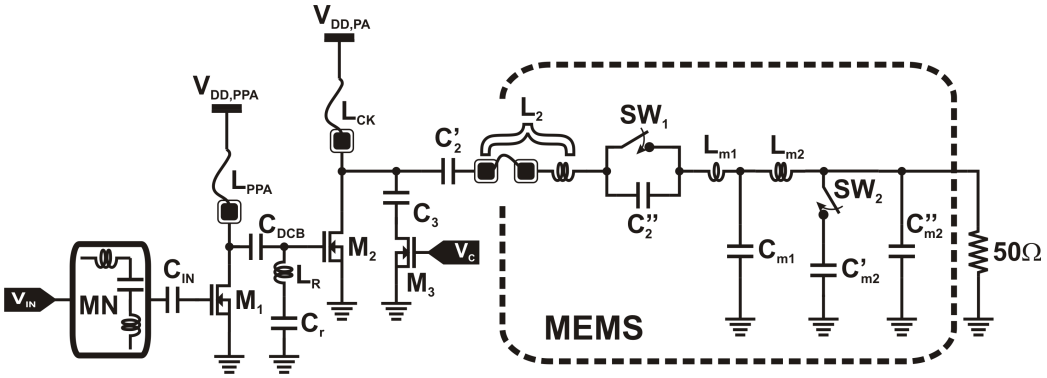


Fig. 2. Schematic of the proposed reconfigurable Class-E PA. The MEMS based matching network implements the LC series filter and the matching network, comprised of two LC sections. The input matching network MN is realized using external components.

number of reconfigurable components, namely C_2 and C_{m2}. In order to reduce power losses we avoid to switch inductors.

To make the Class-E PA working efficiently at both operating frequencies, output network components (C_{sh}, C_2 and L_2) have to be reconfigured according to (1). Since switch losses are one of the most significant power loss contributions, we reduced the number of switches used to modify component values, keeping L_2 constant regardless operation frequency. Therefore, the output network quality factor doubles at $1800MHz$ according to (1), increasing slightly P_{out} because of the α dependence on Q_{out}. Selecting a low Q_{out} is beneficial to reduce output network power losses [1], hence we choose $Q_{out} = 2.5$ at $900MHz$, giving $C_{sh,L} = 3.2pF$ and $C_{2,L} = 14.9pF$, whereas $C_{sh,H} = 1.6pF$ and $C_{2,H} = 2pF$ at $1800MHz$.

The circuit schematic of the reconfigurable power amplifier including the external MEMS network is shown in fig. 2. It is comprised of two stages. A common source topology has been chosen for the final power stage. To avoid gate oxide breakdown, we used MOSFETs with high breakdown voltage ($7.5V$) and limited the supply voltage of the PA driving stage to $V_{DD,PPA} = 1.25V$, thus keeping maximum oxide stress below DC breakdown limits $V_{dg,MAX} < 7V$ [9].

The reconfigurable shunt capacitor is realized using M_3 to switch C_3 to ground and employing M_2 ($C_{dd,M2}$) and M_3 ($C_{dd,M3}$) drain parasitic capacitances. At lower and higher bands M_3 is switched ON and OFF, implementing the capacitance at $\approx 900MHz$ ($C_{sh,L}$) and $\approx 1800MHz$ ($C_{sh,H}$), respectively.

$$\begin{cases} C_{sh,L} = C_{dd,M2} + C_3 \\ C_{sh,H} = C_{dd,M2} + \dfrac{C_{dd,M3}\, C_3}{C_{dd,M3} + C_3} \end{cases} \tag{2}$$

Assuming $C_3 = k \cdot C_{dd,M3}$ and forcing $C_{sh,L} = 2 \cdot C_{sh,H}$ allows deriving MOSFET parasitic capacitances and C_3 as a function of k after some mathematical manipulations.

$$\begin{cases} C_{dd,M2} = \dfrac{k-1}{2k} C_{sh,L} \\ C_{dd,M3} = \dfrac{k+1}{2\,k^2} C_{sh,L} \\ C_3 = \dfrac{k+1}{2\,k} C_{sh,L} \end{cases} \tag{3}$$

$k > 1$ should be selected to maximize the efficiency. MOSFET power loss ($P_{L,MOS}$) depends inversely on transistor width (W), hence a large W is desirable to minimize on-state resistance [1]. However this increases the drain capacitance, which results to be proportional to $1/P_{L,MOS}$. Thus, minimizing MOSFET power losses requires to increase both $C_{dd,M2}$ and $C_{dd,M3}$, but this cannot be done acting on k, as their dependence on k is opposite. The optimum $k = 3.56$ is found from $C_{dd,M2} = 2 \cdot C_{dd,M3}$, which corresponds to equalize the power loss due to M_2 to the half of the M_3 one. We considered only the half of the power loss due to M_3 because this transistor is ON only at lower frequency band, i.e. the half of time assuming to operate the same time at $900MHz$ and $1800MHz$. Substituting $k = 3.56$ into (3) allows calculating the optimum M_2 ($W = 6000\mu m$) and M_3 ($W = 4500\mu m$) widths and $C_3 = 9.5pF$. The finite RF Choke inductor $L_{CK} = 2.1nH$ is realized by a bondwire inductor.

To drive efficiently M_2 gate, we used a double resonant matching network synthesizing a high impedance at both frequency bands. This network is comprised of the bondwire inductor $L_{PPA} = 1.8nH$, the planar inductor $L_R = 3.1nH$, $C_r = 4.2pF$ and the M_2 gate-source capacitance.

The MEMS network realizing the series $L_2 - C_2$ filter and the matching network is shown in fig. 2. L_2, realized by the series of a bondwire and a planar inductor, is kept constant over both frequency bands. C_2 is reconfigured by an ohmic series switch SW_1 shorting C_2''. Thus, $C_{2,H}$ is realized as the series between C_2' and C_2'' while $C_{2,L}$ is implemented only by C_2'.

The matching network is comprised of two cascaded LC sections designed to down transform the antenna impedance to 12Ω at both frequency bands. At $900MHz$ the ohmic shunt MEMS switch SW_2 is actuated, and $C_{m2} = C'_{m2} + C''_{m2}$.

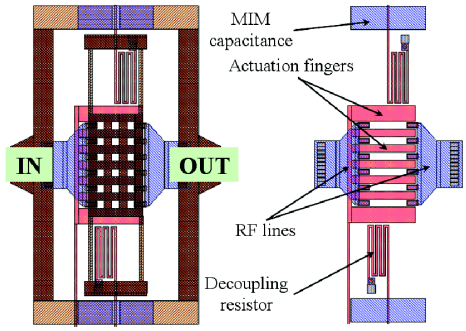


Fig. 3. Close-up of the MEMS ohmic series switch needed to reconfigure C_2. The left figure shows the layout of the entire switch while the right one reports only the bias and RF lines scheme. In particular, the non-connected input/output RF lines are visible.

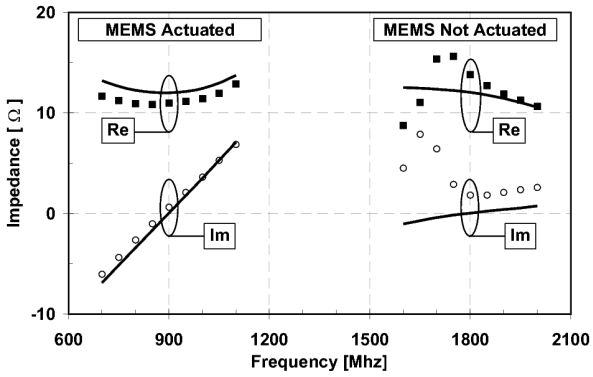


Fig. 5. Simulated (solid lines) vs. measured (symbols) input impedance of the MEMS matching network at both lower and upper frequency bands.

The close up of the switch SW_1 used to reconfigure C_2 is depicted in fig. 3. It is an ohmic series switch [10] that can be modelled as the parallel of the two MIM capacitors when the plate is not actuated. On the contrary, when the bridge is actuated, the two capacitors are shorted by the ohmic contact between the suspended membrane and the input/output RF lines. The right plot in fig. 3 shows the scheme of bias and RF lines, with the gold metalization hidden. This allows getting a clear view of the actuation fingers to bias the suspended plate and the RF lines, realized on two different conductive layers.

On the other hand, SW_2 is an ohmic shunt switch, whose behavior is opposite to the SW_1 one. SW_2 is open when the plate is not actuated and shorted when the plate reaches the pull in. L_{m1} and L_{m2} are 3/4-a-circle gold inductors.

III. Measurements Results

The photomicrograph of the prototype of the PA circuit we realized is shown in fig. 4. Two dies manufactured in CMOS and MEMS technologies have been glued on top of a DC biasing board on FR4 substrate. These dies have been connected through bondwires in a System in a Package (SiP) fashion (fig. 4). The chip realized using AMS $0.35\mu m$ technology implements the active part of the PA circuit. The MEMS network implementing series filter and matching network has been manufactured using fully compatible surface micromachining process available at the Bruno Kessler Foundation (FBK, Trento, Italy) [11]. The network is configured for

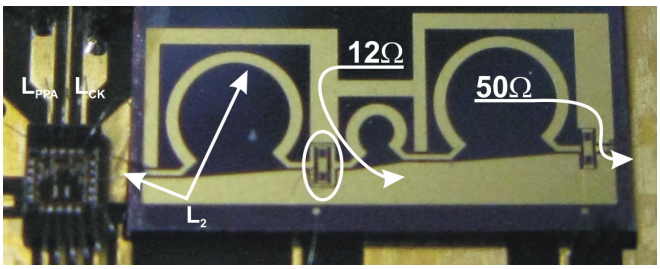


Fig. 4. Photograph of the PA prototype realized connecting through bondwires CMOS and MEMS dies implementing the active part of the circuit and the output network, respectively.

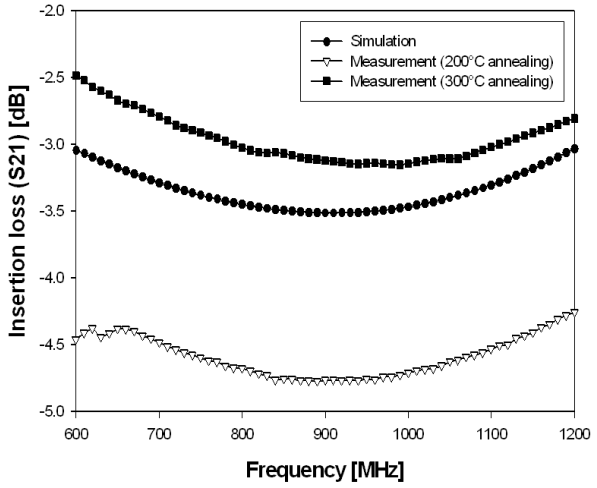
GSG (Ground Signal Ground) probing, enabling also the characterization of the network alone. Grounding is provided by means of 10 bondwires while two dedicated ground bonding are used to connect the MEMS output network to ground.

The CMOS die area is $1.44mm^2$ including pads while the MEMS network area occupation is $29.88mm^2$.

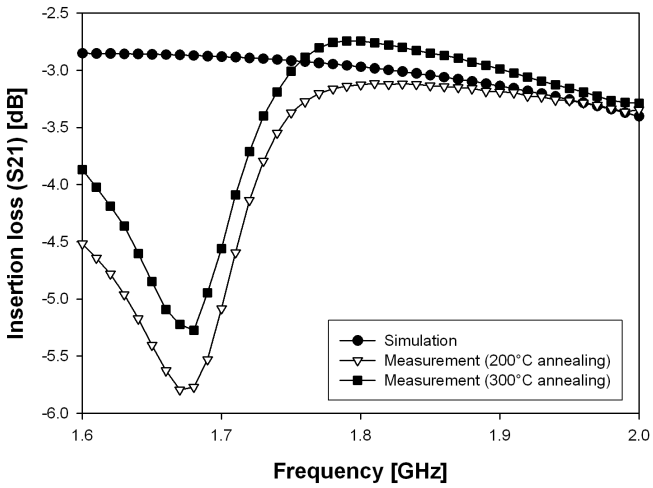
Samples of MEMS matching network alone (not shown here for brevity) were available for characterization. They have been measured through a VNA and GSG probes. Fig. 5 shows real and imaginary parts of MEMS matching network impedances at $900MHz$ (switch SW_2 actuated) and $1.8GHz$ (SW_2 not actuated), respectively. It can be seen that impedance synthesized by the MEMS network is not equal to the 12Ω target value at both frequencies. Interestingly, discrepancies between simulations (solid lines) and measurements (symbols) are wider at $1.8GHz$.

This difference is due to a not perfect vias opening through the oxide connecting the buried multi-metal layer to the above electrodeposited gold layer (see fig. 3). This technology issue introduces a large series parasitic capacitance that influences the RF behavior of the network at low frequency, and additional losses on the whole frequency span. Such losses have been reduced by increasing the annealing temperature during vias processing from the standard 200°C to 300°C. Unfortunately, we had the chance to introduce this process change too late, and therefore we used standard process to manufacture PA MEMS output network. Nevertheless, S parameters measured on the standalone MEMS networks processed with both 200°C and 300°C annealing are available, and measured insertion losses are compared to circuit simulations at both $900MHz$ and $1800MHz$ in figures 6(a) and 6(b), respectively.

A significant improvement is achieved at $900MHz$: measured insertion losses are $-4.76dB$ (200°C annealing) and $-3.12dB$ (300°C annealing), while simulations provide $-3.51dB$, see fig. 6(a). As shown in Fig. 6(b), at $1.8GHz$ the simulated insertion loss is $-2.97dB$ while the measured values are $-3.13dB$ (200°C annealing) and $-2.74dB$ (300°C annealing). Table I reports the real and imaginary part of the input impedance of the MEMS network extracted from Smith



(a) Low Frequency Band - $900MHz$



(b) High Frequency Band - $1800MHz$

Fig. 6. Simulated vs. measured insertion loss at both operating bands. Measurements are referred to two MEMS network samples processed with 200°C and 300°C annealing steps.

Chart plots referred to the return loss (not shown here). Interestingly at $900MHz$ the improved (300°C) annealing treatment makes the real part of the input impedance close to the targeted 12Ω. Unfortunately, at $1.8GHz$ the higher temperature annealing leads only to a reduction of the imaginary part of the input impedance, whereas the real part remains around 14Ω. This could be due to distributed parasitic effects along the MEMS network (more significant as the frequency raises), requiring 3D EM simulations to be properly taken into account when synthesizing the targeted input impedance value. In conclusion, the high temperature annealing step reduced the MEMS network insertion loss and improved the impedance matching particularly at $900MHz$, allowing improving the hybrid power amplifier performances when assembled with the CMOS PA core.

The complete PA has been measured using microprobes to connect input and output GSG pads. Control signals needed to reconfigure the PA operation frequency are provided by external biasing. To make the PA working at lower frequencies, $V_C = 3V$ (see fig. 2) is provided while MEMS switches are actuated supplying $30V$ DC biasing. The input matching network MN is realized with external components.

Fig. 7 shows the output power and the drain efficiency of the PA prototype measured at $900MHz$ and $1.8GHz$.

TABLE I
REAL AND IMAGINARY PART OF THE MEMS NETWORK INPUT IMPEDANCE. SIMULATED AND MEASURED VALUES ARE REPORTED.

	$900MHz$		$1.8GHz$	
	$\Re[\Omega]$	$\Im[\Omega]$	$\Re[\Omega]$	$\Im[\Omega]$
Simulation	11.994	0.036	12.023	0.018
Measured (200°C annealing)	9.759	1.207	14.164	2.981
Measured (300°C annealing)	12.661	1.709	14.612	0.127

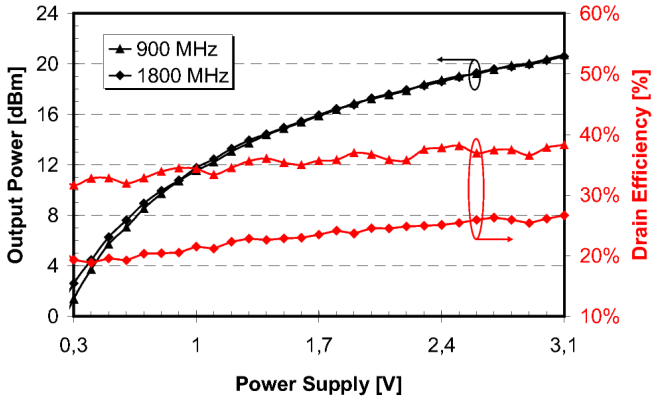
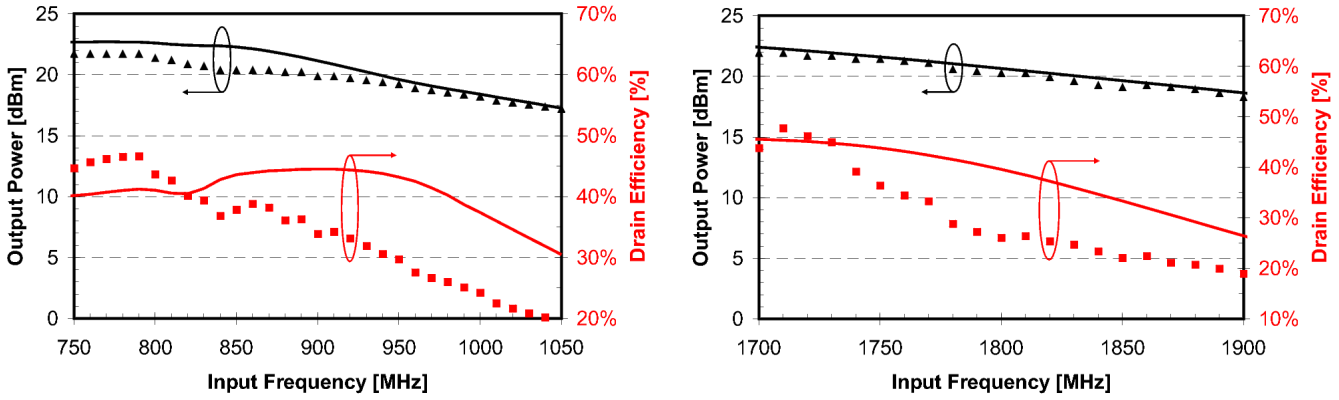


Fig. 7. Output power and drain efficiency measured at 900MHz and 1.8GHz.

With maximum $V_{DD,PA} = 3V$ supply, the PA delivers $20dBm$ with 38% and 26% drain efficiencies at $900MHz$ and $1.8GHz$, respectively. The efficiency is significantly lower than that obtained from post-layout simulations (44% and 40% at $900MHz$ and $1800MHz$, respectively).

The difference, as previously discussed, is mainly caused by the non ideal behaviour of the MEMS matching network (even though enhanced in subsequent technology runs) that forces the power amplifier to operate with a mistuned output network, degrading circuit performance, as shown in fig. 8.

In addition, the unavoidable uncertainty on L_{PPA} and L_{ck} bondwire inductances worsens further PA performance, explaining the difference between forecasted and measured results. This shown in fig. 8, which shows output power and drain efficiency measured and simulated over both frequency bands. Circuit simulations (solid lines) are performed considering the measured MEMS network impedance, shown in fig. 5, and with nominal bondwire inductors. Despite these technological issues partially related to the non perfect MEMS



(a) Low Frequency Band

(b) High Frequency Band

Fig. 8. Output power (triangles) and drain efficiency (squares) measured at both lower and upper frequency bands. Solid lines depict circuit simulations performed with post-layout data obtained from MEMS measurements.

process control, the low output network quality factor we selected reduces circuit sensitivity against component variations, allowing the PA delivering more than $18dBm$ over both lower and upper bands.

IV. Conclusion

In this paper we presented a reconfigurable Class-E power amplifier working over all up-link bands of GSM standard. A reconfigurable solution is desiderable to amplify signals on both lower and upper GSM bands as it allows avoiding to duplicate the PA circuitry. It is worth stressing that employing more than one power amplifier requires to deal with PA coexistence issues, that cannot be solved inexpensively adopting both on-chip and off-chip solutions. In fact, the off-chip solution increases the amount of components and the PCB complexity. On the other hand, the fully integrated solution usually requires to duplicate not only the active devices but also the matching networks needed to match the 50Ω antenna impedance. This increases the chip area, which is mainly required by passives. In addition, the fully integrated solution requires to cancel any interference between the two PAs, which is today a challenging unsolved task. All these issues are intrinsically solved by a reconfigurable solution as the one proposed here. Prototypes realized assembling in a SiP fashion two dies manufactured using CMOS and MEMS technologies deliver $20dBm$ with 38% and 26% drain efficiencies at both $900MHz$ and $1800MHz$, respectively. PA performance are negatively affected by technological issues (switch losses and parasitics) due to the still not perfect MEMS manufacturing process control. Nevertheless, we believe that MEMS technology can play a key role in future RF applications, provided that the technology is improved.

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