Joint Logic Restructuring and Pin Reordering against NBTI-Induced Performance Degradation*

Kai-Chiang Wu and Diana Marculescu
Department of Electrical and Computer Engineering
Carnegie Mellon University
{kaichiaw, dianam}@ece.cmu.edu

Abstract

Negative Bias Temperature Instability (NBTI), a PMOS aging phenomenon causing significant loss on circuit performance and lifetime, has become a critical challenge for temporal reliability concerns in nanoscale designs. Aggressive technology scaling trends, such as thinner gate oxide without proportional downscaling of supply voltage, necessitate a design optimization flow considering NBTI effects at the early stages. In this paper, we present a novel framework using joint logic restructuring and pin reordering to mitigate NBTI-induced performance degradation. Based on detecting functional symmetries and transistor stacking effects, the proposed methodology involves only wire perturbation and introduces no gate area overhead at all. Experimental results reveal that, by using this approach, on average ***56%*** *of performance loss due to NBTI can be recovered. Moreover, our methodology reduces the number of critical transistors remaining under severe NBTI and thus, transistor resizing can be applied to further mitigate NBTI effects with low area overhead.*

1. Introduction

Circuit reliability, usually measured by *failure-in-time* (FIT), has become a critical challenge for achieving robustness in nanoscale designs. The 2007 International Technology Roadmap for Semiconductor (ITRS) [1] projects that the long-term reliability of sub-100nm integrated circuits is in the order of 50-2000 FITs (failures in a billion hours). Soft errors, process variations, and *negative bias temperature instability* (NBTI) are currently some of the main factors in reliability degradation. With the continuous scaling of transistor dimensions, NBTI effects, which cause significant loss on circuit performance and lifetime, are becoming increasingly dominant for temporal reliability concerns. Therefore, the need of an optimization flow considering NBTI effects in early design stages emerges.

NBTI [2] is a PMOS aging phenomenon that occurs when PMOS transistors are stressed under **N**egative **B**ias ($V_{gs} = -V_{dd}$) at elevated **T**emperature. The NBTI-induced PMOS aging refers to the generation of interface traps along the silicon-oxide (Si-SiO_2) interface due to the dissociation of *Si-H* bonds. These traps incur an increase in the magnitude of PMOS threshold voltage ($|V_{th}|$, as much as 50mV over 10 years [3]), and in turn slow down the rising propagation of logic gates. If the performance degradation continues and finally exceeds a tolerable limit, the circuit lifetime will also be influenced since the timing specification is no longer met. In contrast, the aging mechanism can be recovered partially by annealing generated interface traps when the stress condition is relaxed ($V_{gs} = 0$).

At traditional technology nodes, the NBTI problem is not so severe because the electric field across gate oxide is small. However, as technology scaling proceeds aggressively, *e.g.*, thinner gate oxide without proportional downscaling of supply voltage and higher operating temperature due to higher power density, the dissociation of *Si-H* bonds is accelerated and thus, the rate of NBTI-induced performance degradation is getting faster. Experiments on PMOS aging [4] indicate that NBTI effects grow exponentially with thinner gate oxide and higher operating temperature. If the thickness of gate oxide shrinks down to 4nm, the circuit lifetime will be dominated by NBTI [5].

In addition to the oxide thickness and operating temperature, NBTI-induced performance degradation highly depends on the amount of time during which a PMOS transistor is stressed. In [6][7][8], the increase in threshold voltage has been demonstrated to be a logarithmic function of the corresponding stress time. A PMOS under DC stress (*i.e.*, duty cycle = 1) suffers from static NBTI and ages very rapidly. Under a real AC stress condition (*i.e.*, duty cycle < 1), the NBTI impact is periodical and can be recovered, which results in a lower extent of degradation. The stress time of a PMOS under AC stress is associated with its stress probability; that is, the probability that V_{gs} is equal to $-V_{dd}$. For a **NAND** gate with parallel pull-up PMOS transistors, the stress probability of any PMOS is just the probability of its input signal being logic "0"; for a **NOR** gate with series pull-up PMOS transistors, the stress probability of a PMOS is the product of signal probabilities of its input and input(s) to its upper PMOS transistor(s). This parameter, based on the circuit topology and input vectors, is distributed non-uniformly from transistor to transistor. The non-uniformity may lead to 3-5X difference in the analysis of NBTI [8].

In this paper, we manipulate *stress probabilities* by employing *logic restructuring* and *pin reordering* such that NBTI effects on those gates (transistors) along timing-critical paths can be reduced. Based on detecting functional symmetries and transistor stacking effects, our proposed methodology involves only wire perturbation and introduces no gate area overhead. Hence, this methodology is widely applicable to logic synthesis and post-layout optimization. Subsequent to logic restructuring and pin reordering, transistor resizing can also be utilized for additive improvement in NBTI-induced performance degradation, with less design penalties than stand-alone NBTI-aware resizing.

* This research was supported in part by NSF Grant No. CNS-07020653.

978-3-9810801-5-5/DATE09 © 2009 EDAA

The rest of this paper is organized as follows: Section 2 gives an overview of related work and outlines the contribution of our paper. In Section 3, we illustrate two key observations which motivate our proposed approaches. In Section 4, the overall NBTI-aware methodology is presented. Section 5 reports the experimental results for a set of standard benchmarks. Finally, we conclude our work in Section 6.

2. Related Work and Paper Contribution

2.1. Previous Work on NBTI-aware Optimization

The optimization of NBTI-induced performance degradation can be formulated as a timing-constrained area minimization problem with consideration of NBTI effects. Existing NBTI-aware techniques basically follow this formulation. The author of [9] proposes a gate sizing algorithm based on Lagrangian relaxation (LR). The LR-based algorithm determines the optimal values of gate sizes, which are assumed to be continuous, by solving a non-linear area minimization problem. An average of 8.7% area penalty is required to ensure reliable operation for 10 years. Other methods related to gate sizing can be found in [10][11]. A novel technology mapper considering signal probabilities for NBTI is developed in [12]. This technique first characterizes each gate in a given standard cell library in terms of its NBTI impact, as a function of its input signal probabilities. Then, the technology mapper takes signal probabilities as inputs when searching for the best matching in the library. About 10% area recovery and 12% power saving are accomplished, compared to the most pessimistic case where static NBTI is applied on all PMOS transistors in the design.

Instead of reducing NBTI effects during active mode as described above, an idea of NBTI-aware optimization during standby mode is presented in [13]. Input vectors for minimum standby-mode leakage are selected to mitigate PMOS aging. Furthermore, for gates that are deep in a large circuit and cannot be well controlled by primary input vectors, another technique also in [13] internally assigns logic "1" to those gates if they are on the critical paths. The logic "1" relaxes the stress condition and can thus relieve the NBTI impact.

2.2. Paper Contribution

We propose an optimization framework using joint *logic restructuring* and *pin reordering* against NBTI-induced performance degradation. Pin reordering is used to change the order of input signals belonging to a **single** gate, while logic restructuring is used to exchange two wires feeding **different** gates. The two wires to be exchanged must be functionally symmetric to keep the circuit behavior unaltered. Our NBTI-aware methodology, which iteratively performs logic restructuring and pin reordering, has several advantages over other existing techniques:

- First, the proposed logic restructuring and pin reordering approaches involve only wire reconnection without touching gates or transistors. In addition, the average switching activity, an important factor of power dissipation, will be theoretically decreased during the process of wire reconnection for NBTI. As a result, changes in silicon area and power dissipation of circuits are never adverse.
- Second, after iterative logic restructuring and pin reordering, we can utilize the method in [14] to identify critical gates under NBTI in which PMOS transistors are resized. The PMOS resizing technique acts as an optional post-processing procedure and targets only critical transistors still under severe NBTI. The area overhead incurred by transistor resizing at this stage is very low since there are fewer target transistors to be resized after logic restructuring and pin reordering.
- Third, the proposed methodology relies on a NBTI modeling and analysis framework developed in [8][14][15]. The framework provides a mathematical model, taking into account both aging and recovery mechanisms, for predicting the long-term PMOS degradation due to NBTI. Hence, the performance (timing) estimation in our methodology is more accurate and efficient than that in existing techniques which ignore the recovery mechanism or employ expensive cycle-by-cycle (short-term) simulations. The error of the long-term prediction versus the short-term simulation is within 5%.

3. Key Observations and Motivations

Before illustrating the key observations on NBTI effects, we briefly introduce the NBTI modeling and analysis framework [8][14][15] used in our paper. This framework enables us to analyze the long-term behavior of NBTI-induced PMOS degradation. First, the degradation of threshold voltage at a given time t can be predicted as:

$$\Delta V_{th} = \left(\frac{\sqrt{K_v^2 \cdot T_{clk} \cdot \alpha}}{1 - \beta_t^{1/2n}} \right)^{2n} \quad \textbf{(1)}$$

where K_v is a function of temperature, electrical field, and carrier concentration, α is the stress probability, n is the time exponential constant which is 0.16 for the used technology, and

$$\beta_t = 1 - \frac{2\xi_1 \cdot t_e + \sqrt{\xi_2 \cdot C \cdot T_{clk} \cdot (1-\alpha)}}{2t_{ox} + \sqrt{C \cdot t}}$$

The detailed explanation of each parameter can be found in [15]. Next, the authors of [14] simplify this prediction model to be:

$$\Delta V_{th} = b \cdot \alpha^n \cdot t^n = b \cdot (\alpha \cdot t)^n \quad \textbf{(2)}$$

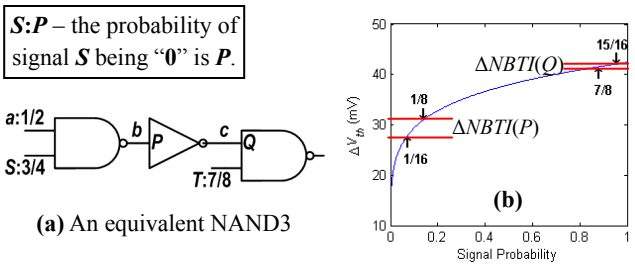
where $b = 3.9 \times 10^{-3}$ V·s$^{-1/6}$.

Finally, the rising propagation delay of a gate through the degraded PMOS can be derived as a first-order approximation:

$$\tau_p' = \tau_p + a \cdot (\alpha \cdot t)^n \quad \textbf{(3)}$$

where ι_p is the intrinsic delay of the gate without NBTI degradation and a is a constant.

In the remaining of this paper, we will apply Equation (3) to calculate the delay of each gate under NBTI, and further estimate the performance of a circuit. The coefficient a in Equation (3) for each gate type and each input pin is extracted by fitting SPICE simulation results in 70nm PTM technology. The simplified long-term model successfully predicts the PMOS degradation with negligible error. For more details about this mathematical NBTI model, please refer to [8][14][15].



(a) An equivalent NAND3

Figure 1. NBTI effect vs. signal probability

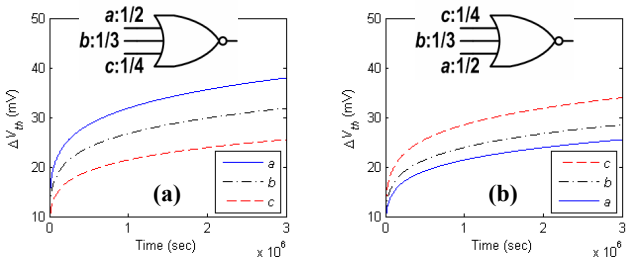


Figure 2. NBTI effect vs. transistor stacking

3.1. NBTI Effect vs. Signal Probability (SP)

Figure 1 shows the NBTI effect versus the probability of an input signal to a PMOS transistor over 3×10^6 seconds. The circuit in Figure 1(a) is simply equivalent to a 3-input NAND gate. Signals *S* and *T* are both inputs to this NAND3 and can be swapped with each other while maintaining the NAND3 functionality. Throughout this paper, ***S*:*P*** denotes the fact that probability of signal ***S*** being logic "**0**" is ***P***. The signal probability of being "**0**", denoted by *SP*, is defined such that *SP*(***S***) = ***P***.

If we swap signals *S* and *T* in Figure 1(a), *SP*(*b*) decreases from 1/8 to 1/16 while *SP*(*c*) increases from 7/8 to 15/16. As shown in Figure 1(b), the NBTI effect increases very rapidly when *SP* is close to 0 and tends to saturate when *SP* approaches 1. Therefore, it is beneficial to make the probability of a signal (*e.g.*, signal *b* in Figure 1(a)) which is small **even smaller**, by exchanging a signal (*e.g.*, signal *S*) whose probability is large with another signal (*e.g.*, signal *T*) whose probability is **even larger**, assuming that *S* and *T* are functionally exchangeable. In this case, the NBTI effect on pin *Q* is worsened only marginally (*i.e.*, $\Delta NBTI(Q)$), but we can obtain a significant reduction in the NBTI effect on pin *P* (*i.e.*, $\Delta NBTI(P)$); namely, $\Delta NBTI(P)$ is significantly larger than $\Delta NBTI(Q)$.

This observation is the major motivation for our logic restructuring approach proposed later in Section 4.1.

3.2. NBTI Effect vs. Transistor Stacking

In the pull-up network of a NOR gate where PMOS transistors are connected in series, the NBTI effect of a PMOS transistor closer to the output signal is smaller than that of a PMOS transistor closer to the power supply (V_{dd}), due to the stacking effect. Therefore, it is beneficial to connect an input signal whose probability is small to a pin (PMOS) closer to V_{dd} for protecting the PMOS transistors below it. Figure 2 shows the NBTI effect versus operation time with two opposite pin orders in a 3-input NOR gate. As it can be seen, the overall degradation is slower if the input signal with the smallest probability is assigned to the highest pin (*i.e.*, the PMOS closest to V_{dd}). Nevertheless, the arrival time of the signal with a small probability may be large. In this case, connecting such a signal to a higher pin will increase the arrival time of the output signal, even though the NBTI effects of PMOS transistors below are effectively mitigated. In order to obtain the input ordering for the smallest NBTI-induced performance degradation, not only signal probabilities but also arrival times of input signals should be considered.

This observation is the major motivation for our logic restructuring and pin reordering approaches proposed later in Section 4.1 and Section 4.2.

4. Proposed Methodology

In this section, we present the overall methodology for mitigation of NBTI-induced performance degradation. The objective of our methodology is to minimize the circuit delay under NBTI over 10 years while incurring as little area overhead as possible. The main procedure iteratively performs *logic restructuring* and *pin reordering*, with minimum area penalty, until no further improvement can be made. These two approaches are synergistic and can provide potential benefits to each other. *Transistor resizing* is an optional post-processing procedure for additional NBTI reduction, with low area overhead.

4.1. Logic Restructuring

The logic restructuring approach is based on *functional symmetries*. Functional symmetries (FSs) provide substantial benefits for various synthesis and verification applications [16][17][18]. Generally, FSs are classified into two categories: non-equivalence symmetry (NES) and equivalence symmetry (ES), as defined in the sequel.

Two variables *x* and *y* in a Boolean function $F(\ldots, x, \ldots, y, \ldots)$ are *non-equivalence symmetric* (NES) if and only if:

$$F(\ldots,x,\ldots,y,\ldots) = F(\ldots,y,\ldots,x,\ldots) \Rightarrow F_{\bar{x}y} = F_{x\bar{y}}$$

Two variables *x* and *y* in a Boolean function $F(\ldots, x, \ldots, y, \ldots)$ are *equivalence symmetric* (ES) if and only if:

$$F(\ldots,x,\ldots,y,\ldots) = F(\ldots,\bar{y},\ldots,\bar{x},\ldots) \Rightarrow F_{xy} = F_{\bar{x}\bar{y}}$$

Two variables *x* and *y* in a Boolean function $F(\ldots, x, \ldots, y, \ldots)$ are *functionally symmetric* if they are either NES or ES.

We use the concept of *generalized implication supergates* (GISGs) to identify functional symmetries in a given circuit. A generalized implication supergate (GISG) [17] is a group of connected gates that is logically equivalent to a big AND/OR gate with a large number of inputs. For simplicity, we will use only *supergate* (SG) to refer to a generalized implication supergate in the rest of this paper. In practice, maximal supergates, which include maximal numbers of gates and cannot expand anymore, are extracted for symmetry identification. To extract all maximal supergates from a gate-level netlist, we first assign non-controlling values to all primary output gates and treat them as SG roots. For each gate in a reverse topological order (from primary outputs to primary inputs), backward implication is applied to determine the values of all input gates until no more implication can be made or the current gate is not fanout-free. Gates at which backward implication stops are treated as new SG roots. We then assign non-controlling values to those new SG

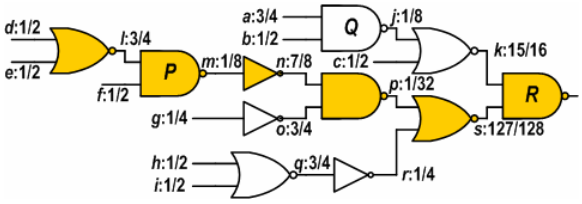


Figure 3. A supergate and its most critical path segment (MCPS)

roots and apply backward implication recursively. The whole process terminates while all primary inputs are reached. Figure 3 shows a supergate with 9 inputs and 11 gates. This 9-input supergate behaves as a 9-input big NAND gate with some inputs inverted.

Functional symmetries can be easily identified after all maximal supergates are extracted. Two wires S (to gate P) and T (to gate Q) are symmetric if (*i*) P and Q belong to the same supergate rooted at gate R, and (*ii*) S (T) is **not** on the path from Q (P) to R. More specifically, S and T are non-equivalence symmetric if P and Q are assigned the same value; otherwise, S and T are equivalence symmetric. To swap two wires (S and T) that are equivalence symmetric without changing the circuit behavior, two inverters fed by S and T are required. For example in Figure 3, two wires f (to gate P) and a (to gate Q) are non-equivalence symmetric because P and Q are both assigned "0" while being extracted.

The time and space complexities of the supergate extraction algorithm are both linear in the gate count. We can extract maximal supergates for efficient symmetry identification. However, not all functional symmetries are effective against NBTI-induced performance degradation. Subsequently, we develop a NBTI-aware optimization flow, guided by the first key observation (Section 3.1), to identify pairs of symmetric wires which have significant impact on NBTI.

Given a network in gate-level netlist, the probability of each signal being "0" is calculated by using logic simulation. We then do a static timing analysis under NBTI over 10 years where degraded propagation delays are predicted by Equation (3).

Definition 1 (***NBTI-critical path***)**:** After the timing analysis under NBTI, a path is called a *NBTI-critical path* if and only if its delay is larger than the delay of the longest path **without** consideration of NBTI effects.

Definition 2 (***NBTI-critical node***)**:** After the timing analysis under NBTI, a node is called a *NBTI-critical node* if and only if it is on a NBTI-critical path.

Theorem: A non-NBTI-critical node will not degrade the circuit performance even if the node itself is degraded by NBTI.

Proof: Let D be the delay of the longest path in a circuit **without** consideration of NBTI effects. According to Definitions 1 and 2, a non-NBTI-critical node lies on a path whose delay under NBTI is smaller than or equal to D. In other words, even if this node is degraded by NBTI, all paths passing through it still have delays smaller than or equal to D, and thus will not dominate the circuit performance. **Q.E.D.**

For each extracted supergate rooted at gate R, we check whether gate R is a NBTI-critical node or not. Only those supergates whose roots are NBTI-critical nodes need to be

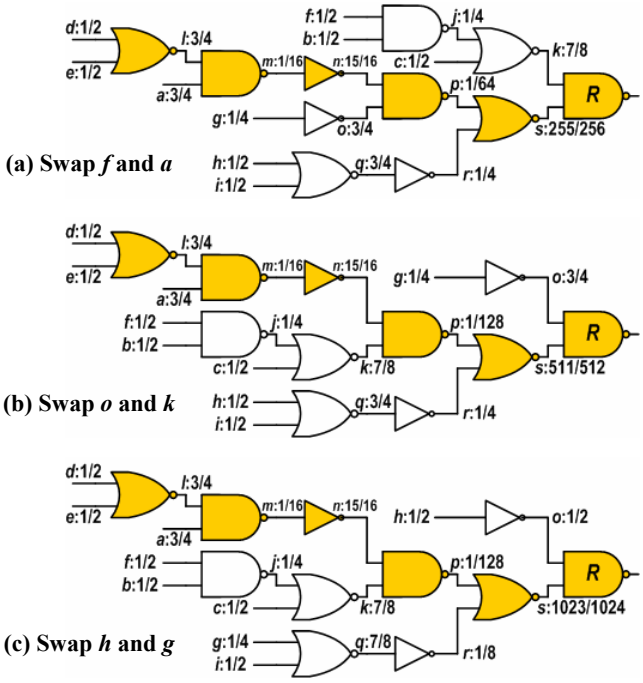


Figure 4. An example of logic restructuring

considered for logic restructuring; other supergates, whose roots are not NBTI-critical nodes, will not degrade the circuit performance and can be discarded. Deciding whether a node is NBTI-critical is trivial as long as its slack time is stored during static timing analysis.

Definition 3 (***NBTI-critical supergate***)**:** A maximal supergate is called a *NBTI-critical supergate* if and only if it is rooted at a NBTI-critical node

Up to this point, we have a list of NBTI-critical supergates. The signal probability and timing information including arrival, required, and slack times of each gate/wire inside can be retrieved. For each NBTI-critical supergate, we backwards trace the *most critical path segment* (MCPS) from its root according to slack times. Rather than the longest **local** path in the supergate, the MCPS is the intersection of the supergate and the longest **global** path passing through its root. Slack times are used to trace the MCPS in constant time.

Definition 4 (***NBTI-aware swappee***)**:** Given a NBTI-critical supergate G, a wire S (to gate P, belonging to G) is a *NBTI-aware swappee* if (*i*) S is a side input to the MCPS of G, **or** (*ii*) P is in the fanin cone of a side input to the MCPS of G.

Definition 5 (***NBTI-aware swapper***)**:** Given a NBTI-critical supergate G and a NBTI-aware swappee S, a wire T (to gate Q, belonging to G) is a *NBTI-aware swapper* if (*i*) S and T are functionally symmetric, (*ii*) the swap of S and T may not cause any timing violation, **and** (*iii*) the swap of S and T is beneficial in terms of NBTI effects as discussed in Section 3.

We process the MCPS downstream to locate NBTI-aware swappees. For each NBTI-aware swappee, a depth-first search is performed to find the best NBTI-aware swapper in the current NBTI-critical supergate. The best swapper here is the wire that,

once swapped, has the highest impact on NBTI. For the purpose of minimum area overhead, we skip the ES case, in which two extra inverters are required for swapping. Finally, the identified swappee and swapper are swapped to obtain an improvement in NBTI-induced performance degradation. Every time a swap is done, we update the affected arrival times and signal probabilities incrementally, also in constant time.

Consider the supergate in Figure 3 where the highlighted region is the MCPS. The first NBTI-aware swappee is wire *f* and its best NBTI-aware swapper is wire *a*. The swap of these two wires (see Figure 4(a)) makes *SP*(*m*) and *SP*(*p*) become smaller, which is beneficial for NBTI mitigation, as illustrated in Section 3. Moreover, *SP*(*m*) and *SP*(*p*) can become even smaller by swapping wires *o* and *k* (see Figure 4(b)).

NBTI-aware swappees and swappers identified with respect to the original MCPS may lead to a local optimum. In order to jump out of the local optimum and explore more solution space for our NBTI-aware logic restructuring approach, we redistribute paths in a supergate based on functional symmetries, too. The path redistribution cannot destroy the circuit timing. For example in Figure 3, we may exchange wire *m* with wire *h* to generate a new MCPS, which in effect allows for more possibilities to get a better solution.

4.2. Pin Reordering

The pin reordering approach is motivated by the second key observation (Section 3.2) on the NBTI effect versus transistor stacking. This observation indicates that, due to the transistor stacking effect, the farther from the power supply a PMOS in a transistor stack is, the less NBTI impact this PMOS suffers. For the smallest overall degradation, it is reasonable to assign inputs to the series PMOS transistors of a NOR gate in increasing order of signal probabilities, from top to bottom. However, our concern is the resulting circuit "timing" itself instead of the timing "degradation." To minimize the circuit delay under NBTI, not only signal probabilities but also arrival times of input signals should be considered for pin reordering. In our proposed framework, the NBTI-aware pin reordering approach is basically an exhaustive search for the best input ordering. For each gate in a topological order, we enumerate all possible permutations of its input signals and find out the one resulting in the smallest arrival time of its output signal, with NBTI effects taken into account. This strategy is absolutely tractable because every gate type in our cell library has up to four input pins.

Note that pin reordering is always synergistic with logic restructuring. Pin reordering changes the input order of a gate and thereby, may also change the most critical path segment (MCPS) used for NBTI-aware swappee/swapper identification in logic restructuring. On the other hand, logic restructuring exchanges wires between gates so that it may bring about a better solution when doing pin reordering. For example, the next NBTI-aware swappee-swapper pair in Figure 4(b) is wire *h* and wire *g*. By swapping these two wires (see Figure 4(c)), *SP*(*r*) decreases from 1/4 to 1/8, which is beneficial for the subsequent pin reordering procedure since a signal with smaller *SP* can better protect the PMOS (connected to wire *p*) on the MCPS. The synergistic influences indeed help reduce circuit delay under NBTI. This is the main reason why logic restructuring and pin reordering working together can succeed in combating NBTI-induced performance degradation.

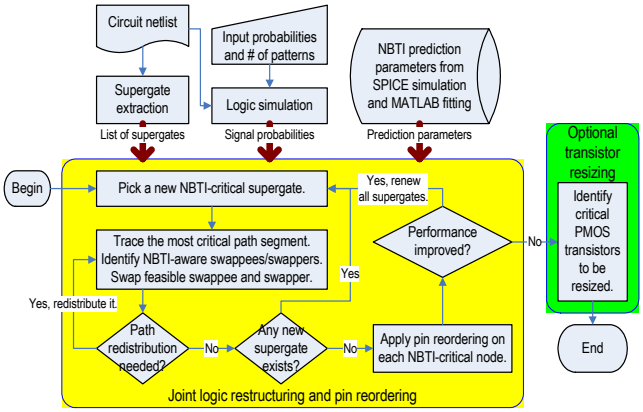


Figure 5. The overall algorithm

The proposed methodology bounds the scope where switching activities are affected and localizes the impact on power consumption. This can be intuitively explained by the fact that: (*i*) the signal probability of the root *R* is constant, and (*ii*) all gates in the supergate except the root are fanout-free. Furthermore, consider a simple analysis that the switching activity of a signal is computed as $2 \times SP \times (1\text{-}SP)$ where *SP* is the signal probability. As shown from Figure 4(a) to Figure 4(c), our methodology tries to push *SP*'s towards 0 or 1. The switching activity and thus the power consumption can even be reduced.

Our overall NBTI-aware optimization flow, which includes joint logic restructuring and pin reordering, and optional transistor resizing, is given in Figure 5.

5. Experimental Results

We have implemented the proposed framework for NBTI-induced performance degradation and conducted experiments on a subset of benchmarks from ISCAS and MCNC suites. The technology used is 70nm, Predictive Technology Model (PTM). The supply voltage is 1.2V and the operating temperature is assumed to be 300K. The standard cell library consists of inverter, NAND and NOR gates with 2 to 4 inputs. Our framework aims at enhancing circuit temporal reliability under 10-year NBTI, with no design penalty. For each benchmark, logic simulation with 10,000 random patterns, assuming that the probabilities of all primary inputs are 0.5, is applied to calculate the probability of each signal. In the case of real applications with various workloads, we can apply different sets of input probabilities and use average signal probabilities instead. Given signal probability α of the input to a PMOS, the 10-year threshold degradation of the PMOS can be predicted by Equation (2). For each gate type and input pin (PMOS), SPICE simulations with its nominal and degraded threshold voltages are performed for a discrete set of signal probabilities from 0 to 1. We fit these SPICE results to obtain coefficient *a*'s for Equation (3). Therefore, the gate delay and circuit timing under NBTI can be estimated.

Table 1 reports the experimental results of our NBTI-aware methodology. All baseline circuits, listed in column one, are optimized and mapped in terms of delay, and their nominal delays (without consideration of NBTI effects) are shown in column two.

Table 1. Recovery of NBTI-induced performance degradation

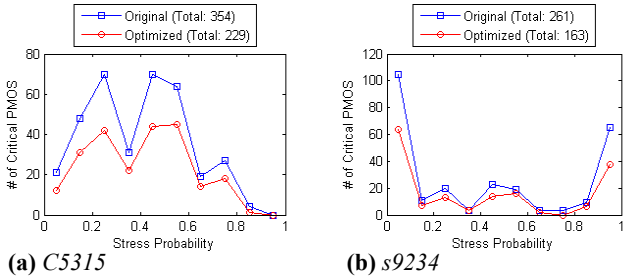
Circuit	Nominal	NBTI	%	PR	%	LR+PR	%
alu2	1128	1237	9.66%	1212	7.45%	1171	3.81%
alu4	1430	1560	9.09%	1511	5.66%	1488	4.06%
des	895	978	9.27%	956	6.82%	937	4.69%
C1355	935	1021	9.20%	991	5.99%	985	5.35%
C1908	1469	1621	10.35%	1561	6.26%	1547	5.31%
C2670	1239	1343	8.39%	1291	4.20%	1259	1.61%
C3540	1850	2020	9.19%	1987	7.41%	1923	3.95%
C5315	1373	1497	9.03%	1443	5.10%	1424	3.71%
C7552	1582	1725	9.04%	1697	7.27%	1667	5.37%
s641	904	980	8.41%	952	5.31%	919	1.66%
s713	906	991	9.38%	956	5.52%	933	2.98%
s832	583	626	7.38%	618	6.00%	609	4.46%
s1196	780	843	8.08%	825	5.77%	817	4.74%
s1238	846	931	10.05%	893	5.56%	889	5.08%
s9234	1134	1240	9.35%	1205	6.26%	1176	3.70%
	(ns)	(ns)	**9.10%**	(ns)	**6.04%**	(ns)	**4.03%**
			1.00		**0.66**		**0.44**

Columns three and four show the circuit delays under NBTI and percentages of degradation compared to the nominal cases. Columns five and six demonstrate the improved delays and corresponding percentages when only pin reordering is used, while columns seven and eight demonstrate those when logic restructuring and pin reordering are applied jointly. For example, the nominal delay of circuit *alu2* is 1,128ns and the delay considering NBTI effects is 1,237ns, which means 9.66% performance degradation. The pin reordering approach can reduce the circuit delay to 1,212ns (7.45% degradation). If we apply joint logic restructuring and pin reordering, the circuit delay becomes 1,171ns and the performance degradation is recovered to 3.81%. On average across all listed benchmarks, **56%** of NBTI-induced performance degradation can be recovered by our methodology.

Figure 6 shows the number of critical transistors versus stress probability for a combinational circuit *C5315* and a sequential circuit *s9234*. Each point in the plot denotes the number of critical PMOS transistors (*y*-axis) whose stress probabilities are in the interval (*x*-axis) with step of 0.1. As it can been seen, the number of critical PMOS transistors in the optimized circuit is significantly reduced, by an average of **36%**. If one considers utilizing transistor resizing for further NBTI mitigation, the required area overhead will be much smaller than that incurred by applying the resizing technique alone.

6. Conclusion

In this paper, we present a NBTI mitigation framework using joint logic restructuring and pin reordering. Two principal observations motivating the proposed methodology are introduced. The logic restructuring approach relies on detecting functional symmetries which can mitigate NBTI-induced performance degradation; the pin reordering approach depends on finding the best input ordering so that critical PMOS transistors can be protected due to stacking effects. Experiments reveal that our framework successfully recovers benchmark circuits from performance degradation with minimum cost. In addition, the recovered circuits have fewer critical transistors, leading to low overhead for post-processing transistor resizing.



(a) *C5315* **(b)** *s9234*

Figure 6. Number of PMOS transistors vs. stress probability

References

[1] International Technology Roadmap for Semiconductor, 2007.

[2] D. K. Schroder and J. A. Babcock, "Negative Bias Temperature Instability: Road to Cross in Deep Submicron Silicon Semiconductor manufacturing," *Journal of Applied Physics*, Vol. 94, No. 1, Jul. 2003.

[3] J. H. Stathis and S. Zafar, "The Negative Bias Temperature Instability in MOS Devices: A Review," *Microelectronics Reliability*, Vol. 46, No. 2-4, Feb.-Apr. 2006.

[4] S. Chakravarthi *et al.*, "A Comprehensive Framework for Predictive Modeling of Negative Bias Temperature Instability," *Proc. of Int'l Reliability Physics Symp.* (IRPS), pp. 273-282, Apr. 2004.

[5] N. Kimizuka *et al.*, "The Impact of Bias Temperature Instability for Direct-tunneling Ultra-thin Gate Oxide on MOSFET Scaling," *Proc. of Symp. on VLSI Technology*, pp. 73-74, Jun. 1999.

[6] V. Reddy *et al.*, "Impact of Negative Bias Temperature Instability on Product Parametric Drift," *Proc. of Int'l Test Conf.* (ITC), pp. 148-155, Oct. 2004.

[7] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "An Analytical Model for Negative Bias Temperature Instability," *Proc. of Int'l Conf. on Computer-Aided Design* (ICCAD), pp. 493-496, Nov. 2006.

[8] W. Wang *et al.*, "The Impact of NBTI on the Performance of Combinational and Sequential Circuits," *Proc. of Design Automation Conf.* (DAC), pp. 364-369, Jun. 2007.

[9] B. C. Paul *et al.*, "Temporal Performance Degradation under NBTI: Estimation and Design for Improved Reliability of Nanoscale Circuits," *Proc. of Design, Automation, and Test in Europe* (DATE), pp. 780-785, Mar. 2006.

[10] R. Vattikonda, W. Wang, and Y. Cao, "Modeling and Minimization of PMOS Nanomater Design," *Proc. of Design Automation Conf.* (DAC), pp. 1047-1052, Jul. 2006.

[11] X. Yang and K. Saluja, "Combating NBTI Degradation via Gate Sizing," *Proc. of Int'l Symp. on Quality Electronic Design* (ISQED), pp. 47-52, Mar. 2007.

[12] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "NBTI-Aware Synthesis of Digital Circuits," *Proc. of Design Automation Conf.* (DAC), pp. 370-375, Jun. 2007.

[13] Y. Wang *et al.*, "Temperature-Aware NBTI Modeling and the Impact of Input Vector Control on Performance Degradation," *Proc. of Design, Automation, and Test in Europe* (DATE), pp. 546-551, Apr. 2007.

[14] W. Wang *et al.*, "An Efficient Method to Identify Critical Gates under Circuit Aging," *Proc. of Int'l Conf. on Computer-Aided Design* (ICCAD), pp. 735-740, Nov. 2007.

[15] S. Bhardwaj, "Predictive Modeling of the NBTI Effect for Reliable Design," *Proc. of Custom Integrated Circuits Conference* (CICC), pp. 189-192, Sep. 2006.

[16] K.-H. Chang, I. L. Markov, and V. Bertacco, "Post-Placement Rewiring and Rebuffering by Exhaustive Search for Functional Symmetries," *Proc. of Int'l Conf. on Computer-Aided Design* (ICCAD), pp. 56-63, Nov. 2005.

[17] C.-W. Chang *et al.*, "Fast Post-Placement Rewiring Using Easily Detectable Functional Symmetries," *Proc. of Design Automation Conf.* (DAC), pp. 286-289, Jun. 2000.

[18] C.-W. Chang *et al.*, "Fast Post-Placement Optimization Using Functional Symmetries," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 23, No. 1, Jan. 2004.