2026 Design, Automation & Test in Europe Conference (DATE)

April 20 – April 22, 2026 **Verona, Italy**



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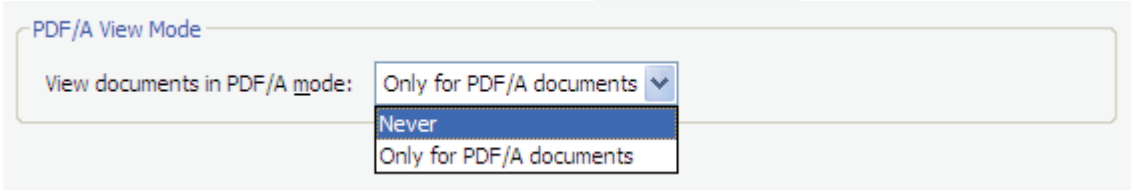

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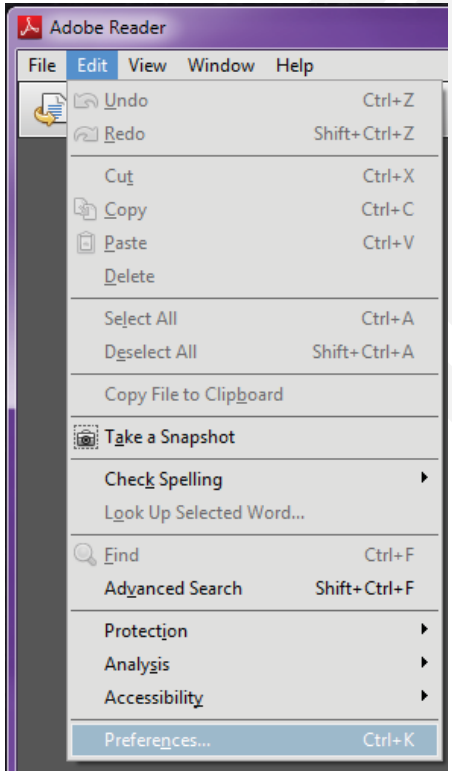

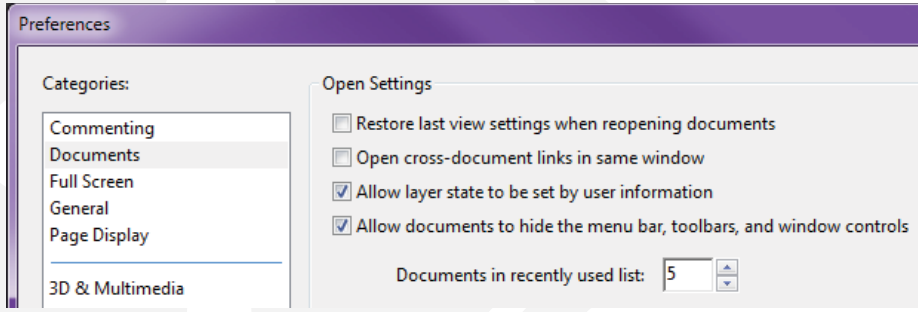

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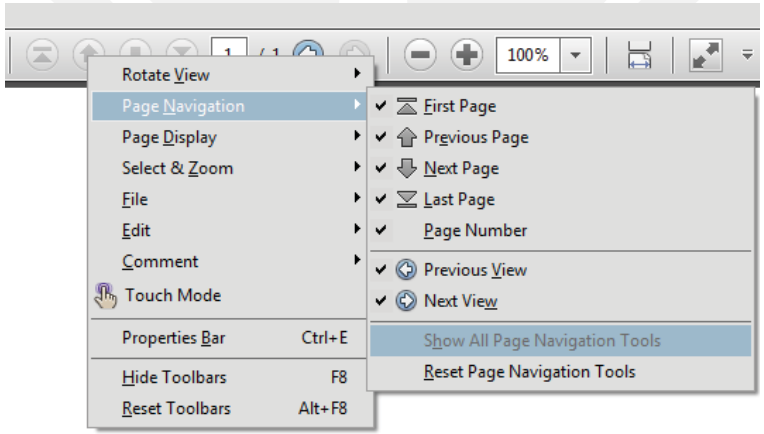

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Welcome

Welcome to the **2026 Design, Automation & Test in Europe Conference (DATE)** on USB. This eGuide is designed so that you may locate papers by session or author, as well as with full text search.

Papers originated as electronic fi les and were converted to Adobe Acrobat PDF fi le format for cross-platform access. Even though the viewing quality on your monitor may vary, all papers print clearly.

Be sure to read the “Getting Started” section for useful recommendations on how to use this electronic guide.

Thank you and enjoy!

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DATE 2026 Foreword

Dear Colleague,

We proudly present the Programme of the Design, Automation, and Test in Europe conference, DATE 2026. From the 20th to 22nd of April 2026, the community meets at the Palazzo della Gran Guardia, Verona, Italy for Europe's largest design automation conference to discuss innovative ideas on all aspects of electronic design, automation and test – from system-level hardware and software implementation, to integrated circuit design and new electronics devices and systems. We warmly welcome you to this event!

DATE 2026 is structured as an intensive three-day event focused on in-person interactions, further strengthening the already close-knit community of hardware and electronic systems designers. The majority of regular research papers will be presented in technical sessions featuring short pitch presentations supported by live poster interactions. Additional full-length presentation videos will be available before, during, and after the conference. This presentation format ensures that attendees can spend their time meeting, discussing, and exchanging ideas with colleagues—the very essence of what conferences are meant to be.

Technical Research Programme

The main conference programme over the three days of the conference includes **41 Interactive Technical Research Sessions and 4 Sessions dedicated to the presentation of Best Research Paper Award candidates.** All sessions are organized in parallel tracks aligned with the four areas of DATE, specifically:

D – Design Methods & Tools,

A – Application Design,

T – Test and Dependability, and

E – Embedded Systems Design.

This year, we experienced a moderate increase in paper submissions, with 8% additional valid submissions



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compared to DATE 2025. Out of a total of 1,642 abstract submissions, 1,310 full complete manuscripts were received, checked for compliance to submission policies, and sent to the Technical Programme Committee for review. All these manuscripts underwent a rigorous review procedure with the support and contributions by the 604 members of the Technical Programme Committee, who carried out 4,940 reviews, with the vast majority of the submissions receiving four reviews. As a result of this process, 321 papers (24.5%) were finally selected for regular presentation, with 78 additional submissions invited for presentation as extended abstracts. We would like to sincerely thank all the members of the Technical Programme Committee for their efforts on this demanding and timely task!

Most importantly, our thanks also go to all the research paper authors and presenters whose contributions constitute the very foundation of DATE. Collectively, the authors of the submitted research manuscripts have affiliations spanning all main world regions: ~24% are from Europe-Middle East-Africa, ~19% are from the Americas, and ~57% are from Asia and Oceania. Submissions were authored by 2,973 individuals, with affiliations located in 36 different countries – a distribution that clearly demonstrates DATE's international profile, global reach and impact.

Monday Keynotes

After the Opening Ceremony on Monday, a plenary keynote lecture will be offered by Luc Van den hove, Chair of the Board of Directors of imec, on "It's Time to Futureproof our Prosperity by Superfueling Innovation, Enabling Next-Gen AI". The presentation will be followed by a second plenary keynote lecture by Bettina Heim, Nvidia, on "Ultra-Low Latency Real-Time Processing for Quantum Computing". Later in the day, a third keynote sponsored by IEEE CEDA, will be delivered immediately after the conference lunch by Zhiru Zhang of Cornell University, on "Unifying Accelerator Design and Programming for Evolvable Computing." A "Later… with the keynote speakers" session in the early afternoon hour will welcome all conference participants to engage in a deeper discussion and exchanges with all three keynote speakers.

Focus Sessions

The DATE 2026 programme includes several **Focus Sessions on Hot Topics**, that are relevant for



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timely introduction and discussion with the DATE community. The 2026 Focus Sessions are:

- PANEL - European Startups on Quantum - Is the Breakthrough Near?
- Architecting Intelligence: Next-Gen Acceleration for Generative AI
- Challenges and Perspectives in Advanced Packaging: Design, Reliability, and Security of 3D and Chiplet-Based Systems
- PANEL - Chiplets: How Far From Making Promise a Reality?
- Beyond Conventional Hardware Security: Next-Generation Design and Security Evaluation for Hardware Architectures
- PANEL - Who is Best suited To Do Verification?
- From Concept to Silicon: End-to-End Agentic AI for Smarter Chip Design
- MLIR, QIR, and Other Intermediate Representations: Towards Production-Ready Compilation for Quantum Computing
- Autonomous Systems Dependability in the Era of AI: Design Challenges in Security, Reliability and Certification
- Crypto-agility in the Age of Quantum Computers

The programme also includes **Executive Sessions** that bring industry perspective to the DATE audience; **Late Breaking Results** sessions covering novel research approaches and breakthrough results on a variety of DATE subdomains. There will also be dedicated sessions with presentations covering results and lessons learned from **Multi-Partner Projects** spanning the full range of DATE topics.

Special Days

Two Special Days, embedded in the conference programme, will focus on areas that are the forefront of the discussions within the system design community: the 2026 special day topics are **Embracing AI in Education and Research,** and **Open-Source Design Ecosystem**. Each of the Special Days includes a full programme throughout the day and comprising a lunchtime keynote, technical presentations and panels.

The Special Day on **Embracing AI in Education and Research** seeks to bring together educators and researchers, from academia and industry, to share ideas and best practices on how the community should evolve the way it educates and carries out research in the AI era. The Special Day programme will be



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offered on Tuesday, with an invited session featuring a series of insightful talks about “Generative AI in Practice: Tools, Workflows, Education, and Research”. The lunch time keynote will be offered by Rolf Drechsler from the University of Bremen, “On My Perfect Life: A Tenured Position While AI Does the Job”. The Special Day will conclude with a panel on “Educating Tomorrow’s EDA Engineers in the Generative AI Era.”

The Special Day on **Open-Source Design Ecosystem** will discuss the most recent advances in the open design of circuits and systems, including recent initiatives and ongoing projects that support the ecosystem’s educational and training resources. The goal is to engage more designers and developers in this space and foster discussions that identify mid- to long-term priorities to bridge the gap between open-source solutions and their commercial counterparts.

The Special Day programme will be featured on Wednesday with one session spanning presentations on the topic of “Open-Source Hardware Landscape”, followed by a panel about “Empowering Education through Open-Source Hardware.” Closing the Special Day programming will be a lunch time keynote by Luca Benini, from ETHZ and the Università di Bologna, on “Democratizing Silicon: The Rise of Open-Source EDA and Europe’s Strategic Roadmap.”

Young People Programme

The Young People Programme (YPP), an initiative targeting doctoral students with the goal of supporting and promoting their career development, will take place on Monday. The programme kicks off on Monday morning with the **University Fair** and the **Student Teams Fair**. The University Fair is a platform for disseminating mature academic research activities, particularly demonstrations and prototypes that are ready for transfer to other units in academia or industry. The Student Teams Fair is an opportunity for selected university student teams involved in international competitions to present their success stories and challenges, and to receive support from companies and DATE attendees. In the afternoon, these junior researchers will have the opportunity to attend the **YPP Career Fair** and **Career Panel** - where participating companies, universities, and research centres outline open positions within their teams and share their work culture. Then, an informal networking event encourages meetings between attendees and recruiters to exchange business cards and curriculum vitae. The **PhD Forum** will close the first day of the conference, and will showcase the work of 41 senior students who have completed, or are about to complete, their PhD thesis.



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Workshops

Over the course of the conference, **five half-day Workshops** cover several pressing topics from areas such as:

- Reactive CPS (ReCPS): Workshop on Reactive Cyber-Physical Systems: Design, Simulation, and Coordination
- Rapid Design Space Explorations of Novel Hardware Solutions: from Atoms to Applications
- Workshop on Nano Security: From Nano-Electronics to Secure Systems
- Reconciling Implementation Performance and Confidence in Machine Learning
- EMEC: Energy and Material Efficiency in the Cloud-Edge Continuum

Technical Tutorials

The rich DATE 2026 programme will also include **five Embedded Tutorials** offered by leading experts in their respective fields. The topics span:

- Introduction to Post Quantum Cryptography for Embedded and IoT Systems
- Quantum Circuit Compilation and Optimisation
- Thermally Robust Photonic AI Chips: From Diamond and Graphene Integration to System-level Optimisation
- Open-Source Hardware Design: From High-Level Code to Silicon with Bambu and SODA
- 3DIC Advanced Packaging, Test & SLM

Finally, the technical programme includes two opportunities to unwind and reconnect with colleagues: the **Welcome Reception** on Monday evening and the traditional **DATE Party** on Tuesday evening. Both events are unique networking opportunities for the community to meet, discuss and exchange.

For further information, please visit: www.date-conference.com

Overall, this year's programme provides a broad, deep and exciting coverage of all the topics our community stands for. We sincerely thank everyone who participated in its organisation and execution, including the Technical Programme Committee and the DATE Executive Committee. And, of course, we wish you an exciting and memorable experience at DATE 2026 in Verona, Italy!



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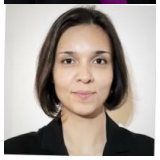

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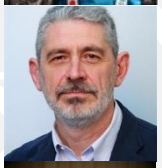

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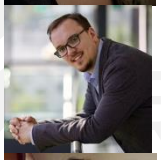

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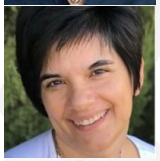

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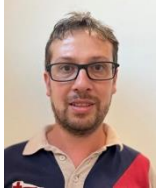

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DT4 Design and Test for Analog and Mixed-Signal Circuits and Systems, and MEMS
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D9 Low-power, Energy-efficient and Thermal-aware Design
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Co-Chair: Grace Li Zhang, TU Darmstadt, DE

D10 Approximate Computing
Chair: Jie Han, University of Alberta, CA
Co-Chair: Alexandra Kourfali, EuroHPC Joint Undertaking, LU

D11 Reconfigurable Systems
Chair: Dionisios Pnevmatikatos, National Technical University of Athens & ICCS, GR
Co-Chair: Stefania Perri, University of Calabria - DIMEG, IT

D12 Logical Analysis and Design
Chair: Elena Dubrova, Royal Institute of Technology - KTH, SE
Co-Chair: Jie-Hong Roland Jiang, National Taiwan University, TW

D13 Physical Analysis and Design
Chair: Matthias Fuegger, CNRS & LMF, ENS Paris-Saclay, FR
Co-Chair: Patrick Groeneveld, DAC, US

D14 Emerging Design Technologies for Future Computing
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Co-Chair: Sonal Shreya, Aarhus University, DK

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Co-Chair: Carmen G. Almudever, Technical University of Valencia, ES

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Co-Chair: Maxime Pelcat, IETR-INSA, FR

A2 Smart Society and Digital Wellness

Chair: Tiziana Margaria, University of Limerick and Lero, IE
Co-Chair: Florenc Demrozi, Department of Electrical Engineering and Computer Science, University of Stavanger, NO

A3 Secure Systems, Circuits, and Architectures

Chair: Mirjana Stojilovic, EPFL, CH
Co-Chair: Cedric Marchand, Ecole centrale Lyon, FR

A4 Autonomous Systems and Smart Industry

Chair: Antonio Miele, Politecnico di Milano, IT
Co-Chair: Heba Khdr, Karlsruhe Institute of Technology (KIT), DE

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Chair: Guillermo Botella, Complutense University of Madrid, ES
Co-Chair: Yuanqing Cheng, Beihang University, CN

A6 Applications of Artificial Intelligence

Chair: Qing Wang, Delft University of Technology, NL
Co-Chair: Stefanos Laskaridis, Amazon Science, GB

T1 Modeling and Mitigation of Defects, Faults, Variability, and Reliability

Chair: Arnaud Virazel, LIRMM, FR
Co-Chair: Cristina Meinhardt, UFSC, BR

T2 Test Generation, Test Architectures, Design for Test, and Diagnosis

Chair: Sybille Hellebrand, Paderborn University, DE
Co-Chair: Jerzy Tyszer, Poznan University of Technology, PL

T3 Dependability and System-Level Test

Chair: Stefano Di Carlo, Politecnico di Torino, IT
Co-Chair: Giulio Gambardella, Synopsys, IE

DT4 Design and Test for Analog and Mixed-Signal Circuits and Systems, and MEMS

Chair: Ricardo Martins, Instituto de Telecomunicações / Instituto Superior Técnico – Universidade de Lisboa, PT
Co-Chair: Salvador Mir, CNRS/Univ. Grenoble Alpes/TIMA, FR

DT5 Design and Test of Hardware Security Primitives

Chair: Michael Hutter, UniBw M & PQShield, DE
Co-Chair: Fatemeh Ganji, Worcester Polytechnic Institute, US

DT6 Design and Test of Secure Systems

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Co-Chair: Tobias Schneider, NXP Semiconductors, AT

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Chair: Michele Lora, University of Verona, IT
Co-Chair: Sara Royuela, Barcelona Supercomputing Center, ES

E2 Real-time, dependable and privacy-enhanced systems

Chair: Mohammad Ashjaei, Mälardalen University, SE
Co-Chair: Federico Reghenzani, Politecnico di Milano, IT

E3 Machine Learning Solutions for Embedded and Cyber-Physical Systems

Chair: Francesco Conti, University of Bologna, IT
Co-Chair: Irem Boybat, IBM Research Europe - Zurich, CH

E4 Design Methodologies for Machine Learning Architectures

Chair: Marian Verhelst, KU Leuven, BE
Co-Chair: Hadjer Benmeziane, IBM Research, CH

E5 Design, Specification, Modeling and Verification for Embedded and Cyber-Physical Systems

Chair: Chung-Wei Lin, National Taiwan University, TW
Co-chair: Gianluca Palermo, Politecnico di Milano, IT

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Yao Chen, National University of Singapore, SG
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Lorenzo Ferretti, Micron Technology, US
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Christian Pilato, Politecnico di Milano, IT
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D2 System Simulation and Validation

Chair: Prabhat Mishra, University of Florida, US
Co-Chair: Samuele Germiniani, University of Guglielmo Marconi, IT

Ansuman Banerjee, Indian Statistical Institute, IN
Kanad Basu, RPI, US
Supratik Chakraborty, IIT Bombay, IN
Mingsong Chen, East China Normal University, CN
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D3 Formal Methods and Verification

Chair: Stefano Quer, Politecnico di Torino, IT
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Chair: Massimo Poncino, Politecnico di Torino, IT
Co-Chair: Grace Li Zhang, TU Darmstadt, DE

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Tohru Ishihara, Nagoya University, JP
Iris Hui-Ru Jiang, National Taiwan University, TW
Trevor Yap, Nanyang Technological University, SG

D7 Network-on-Chip and On-Chip Communication

Chair: Amlan Ganguly, Rochester Institute of Technology, US
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Maurizio Palesi, University of Catania, IT
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D8 Architectural and Microarchitectural Design

Chair: Diana Goehringer, TU Dresden, DE
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Chair: Jie Han, University of Alberta, CA
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Zdenek Vasicek, Brno University of Technology, CZ
Lan Wei, University of Waterloo, CA
Tingting Zhang, McGill University, CA

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Chair: Dionisios Pnevmatikatos, National Technical University of Athens & ICCS, GR
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Ilias Giechaskiel, Independent Researcher, GB
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Lilia Zaourar, CEA LIST, FR
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Grigorios Chrysos, Technical University of Crete, GR
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Davide Conficconi, Politecnico di Milano, IT
Georgi Gaydadjiev, Delft University of Technology, NL
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Dimitris Theodoropoulos, Institute of Communication and Computer Systems, GR
Pedro Trancoso, Chalmers University of Technology, SE
Sotirios Xydis, National Technical University of Athens, GR

D13 Physical Analysis and Design

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Milos Krstic, IHP, DE
Yi-Chen Lu, Nvidia, US
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Chair: Elena Dubrova, Royal Institute of Technology - KTH, SE
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D14 Emerging Design Technologies for Future Computing

Chair: Michael Niemier, University of Notre Dame, US
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Zhiang Wang, Fudan University, CN
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Chia-Lin Yang, National Taiwan University, TW
Wenjian Yu, Tsinghua University, CN

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Siyuan Niu, University of Central Florida, US
Joschka Roffe, University of Edinburgh, GB
Yunong Shi, AWS Quantum Technologies, US
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Laura Harms, Kiel University, DE
Alexandros Kouris, Samsung AI and Imperial College London, GB
Christos Kyrkou, KIOS CoE, University of Cyprus, CY
Rui Li, Samsung AI Center Cambridge, GB
Xiaoli Liu, University of Helsinki, FI
Giulio Masinelli, CSEM, CH
Ioannis Papaefstathiou, Aristotle University of Thessaloniki, GR
Yeonhong Park, Seoul National University, KR
Veljko Pejovic, University of Ljubljana, SI
Tommaso Polonelli, ETH Zürich, CH
Zhiqiang Que, University of Bristol, GB
Valentin Radu, University of Sheffield, GB
Olga Saukh, Graz University of Technology, AT
Giuseppe Tagliavini, University of Bologna, IT
Mahdi Taheri, BTU Cottbus, DE
Stylianos Venieris, Samsung AI, GB
Erwei Wang, AMD, US
Alberto Marchisio, New York University Abu Dhabi (NYUAD), AE
Shinobu Miwa, The University of Electro-Communications, JP
M. Hassan Najafi, Case Western Reserve University, US
Ratko Pilipović, University of Ljubljana, Faculty of Computer and Information Science, SI
Carmen Ruiz, IM2NP, FR
Tathagata Srimani, Carnegie Mellon University, US
Himanshu Thapliyal, Southern Methodist University (SMU), US
Daniel Tille, Siemens EDA, DE
Ying Wang, State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences, CN
Shigeru Yamashita, Ritsumeikan University, JP

T1 Modelling and Mitigation of Defects, Faults, Variability, and Reliability

Chair: Arnaud Virazel, LIRMM, FR
Co-Chair: Cristina Meinhardt, UFSC, BR

Jaume Abella, Barcelona Supercomputing Center (BSC-CNS), ES
Mohammad Hasan Ahmadilivani, Tallinn University of Tehnology, EE
Hussam Amrouch, Technical University of Munich (TUM), DE
Davide Appello, Technoprobe, IT
Daniel Arumi, UPC, ES
Sarah Azimi, Politecnico di Torino, IT
Riccardo Cantoro, Politecnico di Torino, IT
Eric Faehn, STMicroelectronics, FR
Rene Krenz-Baath, TH-Wildau, DE
Angeliki Kritikakou, Univ Rennes, Inria, CNRS, IRISA, FR
Bram Kruseman, NXP Semiconductors, NL
Huawei Li, Institute of Computing Technology, Chinese Academy of Sciences, CN
Lirida Naviner, Télécom Paris, FR



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Lei Xun, Imperial College London, GB
Hanting Ye, Duke University, US
Kasim Sinan Yildirim, University of Trento, IT
Ran Zhu, Delft University of Technology, NL

T2 Test Generation, Test Architectures, Design for Test, and Diagnosis

Chair: Sybille Hellebrand, Paderborn University, DE
Co-Chair: Jerzy Tyszer, Poznan University of Technology, PL

Stephan Eggersgluess, Siemens EDA, DE
Stefan Holst, Kyushu Institute of Technology, JP
Yu Huang, HiSilicon, US
Maksim Jenihhin, Tallinn University of Technology, EE
Maria K. Michael, Electrical and Computer Engineering & KIOS Center of Excellence, University of Cyprus, CY
Chrysovalantis Kavousianos, Department of Computer Science and Engineering, University of Ioannina, GR
Grzegorz Mrugalski, Siemens EDA, PL
Frank Poehl, FP Consulting, DE
Annachiara Ruospo, Politecnico di Torino, IT
Melanie Schillinsky, NXP Germany GmbH, DE

DT4 Design and Test for Analog and Mixed-Signal Circuits and Systems, and MEMS

Chair: Ricardo Martins, Instituto de Telecomunicações / Instituto Superior Técnico – Universidade de Lisboa, PT
Co-Chair: Salvador Mir, CNRS/Univ. Grenoble Alpes/TIMA, FR

Revna Acar Vural, Yildiz Technical University, TR
Engin Afacan, Gebze Technical University, TR
Tiago Balen, UFRGS, BR
Manuel Barragan, TIMA Laboratory, FR
Hung-Ming Chen, Institute of Electronics, National Yang Ming Chiao Tung University, TW
William Eisenstadt, University of Florida, US
Renato Feitoza, PROPHESEE, FR
Jaan Raik, Tallinn University of Technology, EE
Christian Sauer, Synopsys, DE
Hank Walker, Texas A&M University, US

T3 Dependability and System-Level Test

Chair: Stefano Di Carlo, Politecnico di Torino, IT
Co-Chair: Giulio Gambardella, Synopsys, IE

Cristiana Bolchini, Politecnico di Milano, IT
Ramon Canal, Universitat Politècnica de Catalunya, ES
Harish Dixit, Meta Platforms Inc., US
Bo Fang, University of Texas at Arlington, US
Fernando Fernandes dos Santos, INRIA, FR
Yanjing Li, Northeastern University, US
George Papadimitriou, University of Patras, GR
Filippo Persia, Marvell, IT
Marcello Traiola, Inria / IRISA, FR

DT5 Design and Test of Hardware Security Primitives

Chair: Michael Hutter, UniBw M & PQShield, DE
Co-Chair: Fatemeh Ganji, Worcester Polytechnic Institute, US

Aydin Aysu, North Carolina State University, US
Scott Best, Rambus, Inc., US
Lukasz Chmielewski, Masaryk University (Brno, Czechia), CZ
Milos Drutarovsky, Technical University of Kosice, SK
Wieland Fischer, Infineon Technologies, DE
Sylvain Guilley, Secure-IC, FR
Xiaolu Hou, Nanyang Technological University, SG
Tuba Kiyan, Technische Universität Berlin, DE
Sandhya Koteshwara, IBM Research, US
Paolo Maistri, TIMA Laboratory, FR
Debdeep Mukhopadhyay, Department of Computer Science and Engineering, Indian Institute of Technology Kharagpur, IN
Michael Pehl, Technical University of Munich, DE



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Piero Malcovati, University of Pavia, IT
Po-Cheng Pan, Synopsys Inc., TW
Fabio Passos, University of Lisbon and INESC-ID, PT
Rosa Rodríguez-Montañés, UPC, ES
Armin Tajalli, University of Utah, US
Yasuhiro Takashima, University of Kitakyushu, JP
Jose Tejada, Analog Devices Inc, ES
Ender Yilmaz, Rambus, US

DT6 Design and Test of Secure Systems

Chair: Elif Bilge Kavun, Barkhausen Institut & TU Dresden, DE
Co-Chair: Tobias Schneider, NXP Semiconductors, AT

Tolga Arul, University of Passau, DE
Josep Balasch, Rambus, NL
Davide Bellizia, Telsy, IT
Ileana Buhan, Radboud University, NL
Anupam Chattopadhyay, Nanyang Technological University, SG
Ricardo Chaves, INESC-ID, IST, Universidade de Lisboa, PT
Giorgio Di Natale, TIMA - CNRS, FR
Nisha Jacob Kabakci, Fraunhofer AISEC, DE
ayesha khalid, Queen's University Belfast, GB
Johann Knechtel, New York University Abu Dhabi, AE
Georg Land, Intel Labs, US
Itamar Levi, Faculty of Engineering, Bar-Ilan University, IL
Soundes Marzougui, Deutsches Elektronen-Synchrotron (DESY), DE
Ahmet Can Mert, Belfort Labs, AT
Svetla Petkova-Nikova, KU Leuven, BE
Kazuo Sakiyama, The University of Electro-Communications, JP
Sujoy Sinha Roy, TU Graz, AT
Marc Stottinger, Hochschule RheinMain, DE
Rei Ueno, Kyoto University, JP
Trevor Yap, Nanyang Technological University, SG

E1 Embedded Software Architecture, Compilers and Tool Chains

Chair: Michele Lora, University of Verona, IT
Co-Chair: Sara Royuela, Barcelona Supercomputing Center, ES

João Bispo, Faculty of Engineering (FEUP), University of Porto, PT
Timothy Bourke, Inria / ENS, FR
Jeronimo Castrillon, TU Dresden, DE
Hsiang-Yun Cheng, Academia Sinica, TW
Nicola Dall'Ora, Guglielmo Marconi University, IT
Raul de la Cruz, Collins Aerospace, IE
Giorgio Delzanno, University of Genoa, IT
August Ernstsson, Linköping University, SE
Frank Hannig, Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), DE
Leonidas Kosmidis, Barcelona Supercomputing Center (BSC) and Universitat PolitÃ¨cnica de Catalunya (UPC), ES
Bangtian Liu, AMD, CA
Rakesh Nattoji Rajaram, Meta Platforms Inc., US
Alan Oliveira de Sá, LASIGE, Faculty of Sciences of the University of Lisbon, PT
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Rodolfo Pellizzoni, University of Waterloo, CA
Shubham Rai, Robert Bosch Research GmbH, DE
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Dolly Sapra, University Van Amsterdam, NL
Martin Schoeberl, Technical University of Denmark, DK



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Junko Takahashi, NTT Social Informatics Laboratories, JP

E2 Real-time, Dependable and Privacy-Enhanced Systems

Chair: Mohammad Ashjaei, Mälardalen University, SE
Co-Chair: Federico Reghenzani, Politecnico di Milano, IT

Yasmina ABDEDDAIM, Univ Gustave Eiffel, CNRS, LIGM, FR
Jatin Arora, VORTEX CoLab and CISTER Research Centre, PT
Emmanuel Grolleau, LIAS, ISAE-ENSMA, Universite de Poitiers, FR
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Lisa Maile, Eindhoven University of Technology (TU/e), NL
Patrick Meumeu Yomsi, CISTER Research Centre, ISEP, Polytechnic Institute of Porto, PT
Behnaz Ranjbar, Ruhr University Bochum, DE
Luca Santinelli, BMW, DE
Jean-Luc Scharbarg, Université de Toulouse - IRIT/ENSEEIHT/INPT, FR
Yue Tang, Northeastern University, CN
Peter Ulbrich, Technische Universität Dortmund, DE
An Zou, Shanghai Jiao Tong University, CN
Alexander Zuepke, Technical University of Munich, DE

E4 Design Methodologies for Machine Learning Architectures

Chair: Marian Verhelst, KU Leuven, BE
Co-Chair: Hadjer Benmeziane, IBM Research, CH

Marjan Sirjani, Mälardalen University, SE
Yi Wang, Shenzhen University, CN

E3 Machine Learning Solutions for Embedded and Cyber-Physical Systems

Chair: Francesco Conti, University of Bologna, IT
Co-Chair: Irem Boybat, IBM Research Europe - Zurich, CH

Amir Aminifar, Lund University, SE
Mladen Berekovic, Universität zu Lübeck, DE
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Alessandro Cilardo, University of Naples Federico II, IT
Lev Denisov, Politecnico di Milano, IT
Chao Fang, KU Leuven, BE
Angelo Garofalo, University of Bologna, ETH Zurich, IT
Maryam Hemmati, University of Auckland, NZ
Shashikant Ilager, University of Amsterdam, NL
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Gokul Krishnan, Apple, US
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Pietro Mercati, Intel, US
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Ozcan Ozturk, Sabanci University, TR
Flavio Ponzina, San Diego State University, US
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Mohammad Sadrosadati, ETH Zurich, CH
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Lirong Zheng, Fudan University, CN

E5 Design, Specification, Modelling and Verification for Embedded and Cyber-Physical Systems



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Arnab Raha, Intel Corporation, US
Arijit Raychowdhury, Georgia Institute of Technology, US
Gopalakrishnan Srinivasan, IIT Madras, IN
Fan Zhang, Google, US

Chair: Chung-Wei Lin, National Taiwan University, TW
Co-Chair: Gianluca Palermo, Politecnico di Milano, IT

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Christian Haubelt, University of Rostock, DE
Chadlia Jerad, University of Manouba, TN
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Hokeun Kim, Arizona State University, US
Frederic Mallet, Universite Cote d'Azur, FR
Vittoriano Muttillo, University of Teramo, IT
Georgios L. Stavrinides, KIOS Research and Innovation Center of Excellence, University of Cyprus, CY

Late Breaking Results (LBR)

Chair: Annachiara Ruospo, Politecnico di Torino, IT

Domenico Balsamo, Newcastle University, UK
Elif Bilge Kavun, Barkhausen Institut & TU Dresden, DE
Piedad Brox Jiménez, CSIC, ES
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Deborah Volpe, Istituto Nazionale Geofisica e Vulcanologia, IT
Qing Wang, Delft University of Technology, NL



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DATE 2026 Best Paper Awards

The **DATE 2026** best papers are:

D Track

To be announced

A Track

To be announced

T (&DT) Track

To be announced

E Track

To be announced



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Best Paper Award Nominations

3D Integration of Hybrid IGZO/Si and IGZO eDRAMs for High-Density/High-Performance On-Chip Memory

Munhyeon Kim[1], Sukhyun Choi[2], Yulhwa Kim[3] and Jae-Joon Kim[2]
[1]Seoul National University of Science and Technology, KR; [2]Seoul National University, KR; [3]Sungkyunkwan University, KR

An Operator-Circuit Co-design Digital SOT-MRAM Computing-in-Memory Accelerator with Double Bit Density and Full-Utilized Bandwidth/Throughput

Tianshuo Bai[1], Jingcheng Gu[1], Lehao Tan[1], Wente Yi[1], Haolin Ge[2], Han Zhang[1], Zhenyu Xue[1], He Zhang[1], Na Lei[1] and Biao Pan[3]
[1]Beihang University, CN; [2]Beijing University of Aeronautics and Astronautics, CN; [3]Beihang Unversity, CN

FSDB: A Folded-Store Dynamic-Broaden Hybrid Compute-in-ROM/SRAM Architecture for Deploying Large-Scale DNNs On-Chip

Tianyi Yu, Teng Yi, Huazhong Yang and Xueqing Li, Tsinghua University, CN

SCALER: A Stream-Aware Accelerator with Hierarchical Memory for Sparse LU Factorization on HBM FPGAs

Xin Xu[1], Zhiying Zhu[1], Zishu Li[2], Dan Niu[3], Cheng Zhuo[1] and Zhou Jin[1]
[1]Zhejiang University, CN; [2]Nankai University, CN; [3]Southeast University, CN

Torrent: A Distributed DMA for Efficient and Flexible Point-to-Multipoint Data Movement

Yunhao Deng[1], Fanchen Kong[2], Xiaoling Yi[2], Ryan Antonio[3] and Marian Verhelst[2]
[1]MICAS - KU Leuven, BE; [2]KU Leuven, BE; [3]MICAS KU Leuven, BE

KirbyMM: Outer-Product Based Matrix Multiplication on ARMv9 Processor

Lanshu Huang, Han Huang, Zhiguang Chen and Yutong Lu, Sun Yat-sen University, CN

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SecIC3: Customizing IC3 for Hardware Security Verification

Qinhan Tan, Akash Gaonkar, Yu-Wei Fan, Aarti Gupta and Sharad Malik, Princeton University, US

INSPIRE: In-Sensor Compressed Weight Retrieval for Enhancing ViT Efficiency at Edge

Sabbir Ahmed[1], Deniz Najafi[2], Mohaiminul Al Nahian[1], Navid Khoshavi[3], Abdullah Al Arafat[4], Mamshad Nayeem Rizve[5], Mahdi Nikdast[6], Adnan Siraj Rakin[7] and Shaahin Angizi[2]
[1]Binghamton University (SUNY), US; [2]New Jersey Institute of Technology, US; [3]AMD, US; [4]Florida International University, US; [5]Adobe, US; [6]Colorado State University, US; [7]Binghamton University, US

LoRA-Edge: Tensor-Train–Assisted LoRA for Practical CNN Fine-Tuning on Edge Devices

Hyunseok Kwak[1], Kyeongwon Lee[1], Jae-Jin Lee[2] and Woojoo Lee[1]
[1]Chung-Ang University, KR; [2]ETRI, KR

Lithography Hotspot Detection for Complex Non-Manhattan Layouts via Graph Neural Network

Bohao Li[1], Ranran Liu[1], Yumeng Liu[1], Cong Jiang[2], Kang Liu[2], Bei Yu[3], Kun Ren[1], Qi Sun[1] and Cheng Zhuo[1]
[1]Zhejiang University, CN; [2]Huazhong University of Science and Technology, CN; [3]The Chinese University of Hong Kong, HK

RIFT: A Scalable Methodology for LLM Accelerator Fault Assessment using Reinforcement Learning

Khurram Khalil, Muhammad Mahad Khaliq and Khaza Anuarul Hoque, University of Missouri, US

Smart-PCLib: A LLM-based Multi-Agent Framework for Automated PCB Component Library Generation

Zhaohai Di[1], Jindong Tu[1], Zhiyuan HE[2], Yuan Pu[2], Jiawei Liu[3], Chong Tong[1], Tsung-Yi Ho[2], Bei Yu[2] and Tinghuan Chen[1]
[1]The Chinese University of Hong Kong, Shenzhen, CN; [2]The Chinese University of Hong Kong, HK; [3]Beijing University of Posts and Telecommunications, CN

DATE 2026 Special Day Embracing AI in Education and Research

Tuesday, 21 April 2026

Modern AI solutions are quickly evolving, each day improving their ability to tackle growing levels of complexity. However, the ability to extract common meta-principles from experiences across multiple real-life domains remains a unique skill that humanity holds. Meta-principles, in turn, enable the ability to synthesize completely new ideas, and to reason about complex and abstract problems by decomposing them into smaller and simpler challenges - small and simple enough to be tackled by an AI engine. Thus, the AI revolution is enabling a new framework for human activities, where the human can focus on the creative and innovative aspects and the decomposition structure of their creative ideas, and AI engines can tackle the simpler tasks.
In this context, the innovation and opportunities brought forth by AI present an opportunity to change and improve how research and education are carried out in academic settings (and beyond) as informed by the widespread availability of AI-powered systems. To this end, the special day seeks to bring together educators and researchers, from academia and industry, to share ideas and best practices on how the community should evolve the way it educates and carries out research in the AI era, what are the most critical skills that a computer scientist and engineer should develop to succeed in the industry, and what new opportunities AI unlocks in the education and research domains.

Time: 8:30 – 10:00 CET

SD01 Generative AI in Practice: Tools, Workflows, Education, and Research

Session chair: Natesan Venkateswaran, IBM
Organisers: Marcello Traiola, Inria, FR; Cristiana Bolchini, Politecnico di Milano, IT

SD01.1 A Design Blueprint for Scalable Multi-Agent Architectures in Complex EDA Workflows

Valerio Tenace[1] and Pierre-Emmanuel Gaillardon[2]
[1]PrimisAI, US; [2]University of Utah, US

Abstract: Electronic Design Automation (EDA) workflows involve complex, tightly coupled tools and artifacts that require high reliability and traceability. Recent advances in Large Language Models (LLMs) have opened new avenues for AI-driven automation through Multi-Agent Systems (MASs), which can decompose complex tasks into manageable subtasks. However, deploying MASs in EDA remains challenging due to weak coordination, unstructured communication, and limited reproducibility. In this paper, we propose a design blueprint for scalable, LLM-based, MASs tailored to EDA workflows, emphasizing hierarchical orchestration, explicit task interfaces, tool-grounded execution, structured communication, modular memory management, and observability with recovery paths. We also introduce Nexus, an open-source Software Development

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Kit (SDK) that implements these principles, thus enabling low-code workflow specification and robust agent interactions. We validate our approach on open-source benchmarks, achieving 100% functional accuracy on RTL generation (VerilogEval-Human), up to 98.78% functional pass rate on HumanEval, and timing closure with 26.64% average LUT reduction and almost 30% lower total power on VTR designs.

SD01.2 GUIDE: GenAI Units In Digital Design Education

Weihua Xiao[1], Jason Blocklove[2], Matthew DeLorenzo[3], Johann Knechtel[4], Ozgur Sinanoglu[4], Kanad Basu[5], Jeyavijayan Rajendran[6], Siddharth Garg[1] and Ramesh Karri[1]
[1]New York University, US; [2]New York University, N/; [3]Texas A&M University, N/; [4]New York University Abu Dhabi, AE; [5]RPI, US; [6]Texas A&M University, US

Abstract: GenAI Units In Digital Design Education (GUIDE) is an open courseware repository with runnable Google Colab labs and other materials. We describe the repository's architecture and educational approach based on standardized teaching units comprising slides, short videos, runnable labs, and related papers, together with recommended metadata and student deliverables. This organization enables consistency for both the students' learning experience and the reuse and grading by instructors. We demonstrate GUIDE in practice with three representative units: VeriThoughts for reasoning and formal-verification-backed RTL generation, enhanced LLM-aided testbench generation, and LLMPirate for IP Piracy. We also provide details for three example course instances (GUIDE4ChipDesign, Build your ASIC, and GUIDE4HardwareSecurity) that assemble GUIDE units into full semester offerings, learning outcomes, and capstone projects, all based on proven materials. For example, the GUIDE4HardwareSecurity course includes a project on LLM-aided hardware Trojan insertion that has been successfully deployed in the classroom and with CSAW, a worldwide competition for teaching cybersecurity awareness. The GUIDE repository is open for contributions and available at: https://github.com/FCHXWH823/LLM4ChipDesign.

SD01.3 AI for Research: Practical Approaches, Real Benefits, and Hidden Risks

Todd Austin, University of Michigan, US

Abstract: AI has become one of the most valuable "power tools" in my research workflow. In this talk, I'll share the techniques I have developed over the last two years to use AI for generating ideas, designing experiments, reading papers, and writing and presenting research. I'll also share some of the potential risks of using AI for research and the guardrails I have put in place to mitigate those risks. Please join the session and share what has (and hasn't) worked in your own research.

Time: 13:15 – 14:00 CET

LK02 Special Day Lunchtime Keynote – On my perfect life: a tenured position while AI does the job

Rolf Drechsler, University of Bremen, DE

Moderator: Aida Todri-Sanial (TU Eindhoven)

Abstract: Artificial Intelligence is reshaping how we explore, create, and teach. Tasks once considered inherently human are now increasingly delegated to systems that appear to reason, learn, and even invent. This development challenges long-standing notions of expertise, authorship, and the role of human judgment in science and education. Through this development, AI already influences how research is conducted, published, and taught - often with remarkable

efficiency, yet also with opaque mechanisms and uncertain reliability. The enthusiasm surrounding these tools must be balanced by a critical assessment of their capabilities and limitations. What AI systems produce can be impressive, but their results often lack genuine understanding or intent. The central question is how to preserve creativity, responsibility, and depth of insight in a world where machines can assist with almost everything - except understanding what they do.

Time: 14:00 – 15:30 CET

SD02 Engineering the Future: Educating Tomorrow's EDA Engineers in the Generative AI Era (Panel)

Session chair: Marcello Traiola, Inria, FR
Session co-chair: Cristiana Bolchini, Politecnico di Milano, IT
Organisers: Marcello Traiola, Inria, FR, Cristiana Bolchini, Politecnico di Milano, IT
Panellists: *Francesco Bruschi[1], Maksim Jenihhin[2], Gunar Schiner[3], Natesan Venkateswaran[4] and Marina Zapater[5]*
[1]Politecnico di Milano, IT; [2]Tallinn University of Technology, EE; [3]Northeastern University, US; [4]IBM, US; [5]University of Applied Sciences Western Switzerland (HES-SO), CH

DATE 2026 Special Day Open Source Design Ecosystem

Wednesday, 22 April 2026

The open-source design ecosystem has been growing steadily over the past several years. The maturity of open-design processes relies on a decentralised model that simplifies and enables the integration of new design facilities, including open-source Electronic Design Automation (EDA) tools, methodologies, and Process Design Kits (PDKs).

Existing open-source toolchains support complete circuit designs targeting several mature nodes suitable for a wide variety of application domains. However, to unlock the use of open workflows based on advanced design flows and cutting-edge design nodes, a joint effort by the entire community is needed.

This special day will discuss the most recent advances in the open design of circuits and systems, including recent initiatives and ongoing projects that support the ecosystem's educational and training resources. The goal is to engage more designers and developers in this space and foster discussions that identify mid- to long-term priorities to bridge the gap between open-source solutions and their commercial counterparts.

The Special Day opens with a session with three technical contributions (30 minutes each including Q&As), totalling 90 minutes, focusing on different aspects of open-source hardware ecosystem including design flow, fabrication and industrial perspective. It continues with a panel (90 minutes) to discuss the role of open-source hardware in microelectronics education, including the presentation of successful case studies and new teaching methodologies. The panellists will also highlight open challenges in open-source for education. Finally, we close with a Special Day Luchtime Keynote to present open-source EDA and Europe's strategic roadmap (45 minutes including Q&As).

Time: 8:30 – 10:00 CET

SD03 Open-Source Hardware Landscape

Session chair: Piedad Dr. Brox, Instituto de Microelectrónica de Sevilla (CSIC/US), ES
Session co-chair: Milos Dr. Krstic, IHP – Leibniz Institute for High Performance Microelectronics, DE

SD03.1 Open Silicon Fabrication – Made In Europe

Gerhard Kahmen, Leibniz-Institut für innovative Mikroelektronik, DE

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Abstract: Open source hardware development has gained worldwide momentum in the last years. Significant investments and effort in the open source CAD-ecosystem and the development of the support services, such as Tiny Tapeout, gave a significant momentum to education, research, and the development community.
One of the important pillars of the open source hardware development are corresponding ASIC manufacturing capabilities. There are only few foundries worldwide, supporting open source ASIC manufacturing. In this talk the activities of IHP – Leibniz Institute for High Performance Microelectronics, which is a key research institute in Europe with focus on silicon based high frequency microelectronics and systems, will be elaborated. Already for several years IHP is very active in the domain of open source hardware, and providing the corresponding fabrication services and implementation support, including open-PDK, for its 130 nm SiGe BiCMOS process, with cutting edge HBT bipolar transistors. In this presentation, we will introduce the overview of the established open fabrication ecosystem and provide the outlook of the future developments and possibilities.

SD03.2 From Schematic to Silicon: Mixed Signal IC Design in Open Source Flows

Harald Pretl, Johannes Kepler University Linz, AT

Abstract: Open source electronic design automation (EDA) has advanced rapidly in the last few years. Spurred by the availability of open source process design kits (PDKs) from SkyWater, GlobalFoundries, and IHP, interest in using free and open tools for chip design has surged. Initiatives such as TinyTapeout, the IEEE Chipathon, and Code a Chip have broadened access, but robust end to end flows— especially for analog and mixed signal design— are not yet complete. In this talk, we present recent analog and mixed signal case studies that combine open source EDA tools with open PDKs, and we assess where the ecosystem stands today. We highlight what works, where current flows fall short, and we identify key gaps and concrete opportunities for further development.

SD03.3 Bringing Software Design Thinking to Chip Design

Tomi Rantakari, ChipFlow, UK

Abstract: The semiconductor industry is changing fast, but access to custom silicon is still limited to a handful of major players. In this keynote, Tomi Rantakari, CEO of ChipFlow, explores how applying software design thinking can open up chip design to a much broader audience. He discusses the growing role of open-source EDA tools, the hybrid business models needed to make them sustainable, and Europe's opportunity to lead in enabling SMEs. His message: custom chips are no longer the preserve of tech giants like Apple or Tesla—they're becoming accessible to innovators everywhere.

Time: 11:00 – 12:30 CET

SD04 Empowering Education through Open-Source Hardware (Panel)

Organizer: *Norbert Wehn/Lukas Krupp (RPTU Kaiserslautern-Landau, Chipdesign Germany)*
Panellists: *Luca Benini[1], Luca Carloni[2], Oscar Gustafsson[3], Patrick Haspel[4], Gerhard Kahmen[5], Matthew Venn[6] and Norbert Wehn[7]*
[1]ETH Zurich, CH | Università di Bologna, IT; [2]Columbia University, US; [3]Linköping University, SE; [4]Synopsys, DE; [5]Leibniz-Institut für innovative Mikroelektronik, DE; [6]TinyTapeout, ES; [7]University of Kaiserslautern-Landau, DE

The democratization of chip design is a key enabler for innovation and technological sovereignty. Easy access to chip design ecosystems – comprising Process Design Kits (PDKs), reusable IP blocks, and Electronic Design Automation (EDA) flows – are key to transforming how pupils, students and their educators engage with microelectronics. Such infrastructures enable hands-on chip design experiences across the entire design stack, from system, RTL to GDSII. In this panel, the participants will demonstrate how open-source and proprietary technologies can complement each other in microelectronics education at all levels —from school outreach to university curricula and advanced research training. They will present successful case studies of integrating open-source hardware into school, academic courses and training programs to inspire new teaching methodologies and joint initiatives for inclusive chip design education. Finally, they will discuss how open-source and proprietary technologies complement each other in education – (when to use what and how).

Time: 13:15 – 14:00 CET

LK03 Special Day Lunchtime Keynote – Democratizing Silicon: The Rise of Open-Source EDA and Europe's Strategic Roadmap

Luca Benini, ETHZ, CH / Università di Bologna, IT

Abstract: In recent years, the paradigm of open source has moved beyond software to transform the landscape of semiconductor design. Open-source Electronic Design Automation (EDA) tools offer a transformative path toward lowering barriers to entry, ensuring technological sovereignty, and accelerating engineering productivity. This talk provides a comprehensive overview of the current state of the open-source hardware ecosystem and its future potential. We will take a deep dive into Europe's strategic investments in these frameworks and explore how fostering a robust open-source toolchain is the essential catalyst for the next generation of open-source chips.



DATE 2026 Focus Sessions

Date: Monday, 20 April 2026
Time: 11:00 - 12:30 CET

FS01 Focus Session: European Startups on Quantum – Is the Breakthrough Near? (Panel)

Session chair: Anton Klotz, Fraunhofer, DE
Session co-chair: Andrea Kells, Arm, UK
Panellists: *Cyril Condemine[1], Felix Rautschke[2], Ulrich Meier[3], Brendan Barry[4] and Robert Wille[5]*
[1]Quobly, FR, US; [2]Alice & Bob, FR; [3]IQM, DE; [4]Equal1, IE; [5] TU Munich, DE

After decades of academic research on quantum computing and the latest Nobel prize for physics for the research on Josephson junction, quantum computing has transitioned into an emerging commercial frontier. While industry giants such as Google, IBM, Intel, and Microsoft dominate the field, several European start-ups are advancing their own hardware and software solutions. The European Commission's funding programmes, coupled with a growing talent pipeline, create a unique opportunity for a sustainable quantum ecosystem in Europe. The panel participants are founders or high-level representatives of European quantum companies. The aim of the panel is to present these companies to the DATE audience, highlight technological profiles and capabilities and their expectations how they want to compete with big companies. What is the realistic current status of quantum computing and what is the vision, how quantum computing will look like in the near future and it will fulfil its expectations, these questions will be addressed by the panel participants. The audience will be invited to participate in the discussion, if quantum computing will have a prosperous future or will become a technological dead end.

Date: Monday, 20 April 2026
Time: 16:30 - 18:00 CET

FS02 Focus Session: Architecting Intelligence: Next-Gen Acceleration for Generative AI (Hot-Topic)

Session chair: Akash Kumar, Ruhr University Bochum, DE
Session co-chair: Behnaz Ranjbar, Ruhr University Bochum, DE
Organisers: Sudeep Pasricha, Colorado State University, US, Partha Pratim Pande, Washington State University, US

FS02.1 Hardware/Software Co-Design to Accelerate Generative AI Workloads on Heterogeneous Architectures

Pratyush Dhingra, Vibhanshu Sharma, Janardhan Doppa and Partha Pande, Washington State University, US
Abstract: Effective acceleration of Generative AI workloads is constrained by the heterogeneous computational and memory characteristics. Large Language Models (LLMs), for example, are composed of diverse kernels, ranging from memory bound attention mechanisms to compute intensive feed forward networks. Such variability

leads to poor resource utilization and renders homogeneous architectures inefficient. This paper addresses this challenge using two synergistic innovations. First, we present the design of a three-dimensional (3D) manycore architecture enabled by heterogeneous integration to address these bottlenecks. Specifically, the architecture leverages emerging non-volatile memory alongside CMOS-based computing cores to create an optimized kernel-to-compute mapping. Second, a hardware and software co-design framework is developed to enable fine-tuning of unimodal and multimodal LLMs. The co-design ensures thermally robust inference when leveraging emerging non-volatile memories within the heterogeneous architecture. Experimental results on multiple LLMs demonstrate the efficacy of the 3D heterogeneous architecture and the co-design framework.

FS02.2 Accelerating Diffusion Models for Generative AI Applications with Silicon Photonics

Tharini Suresh, Salma Afifi and Sudeep Pasricha, Colorado State University, US

Abstract: Diffusion models have revolutionized generative AI, with their inherent capacity to generate highly realistic state-of-the-art synthetic data. However, these models employ an iterative denoising process over computationally intensive layers such as UNets and attention mechanisms. This results in high inference energy on conventional electronic platforms, and thus, there is an emerging need to accelerate these models in a sustainable manner. To address this challenge, we present a novel silicon photonics-based accelerator for diffusion models. Experimental evaluations demonstrate that our photonic accelerator achieves at least 3x better energy efficiency and 5.5x throughput improvement compared to state-of-the-art diffusion model accelerators.

FS02.3 Hardware and Software Techniques for Accelerating Multimodal Foundation Models

Muhammad Shafique[1], Abdul Basit[1], Muhammad Abdullah Hanif[1], Alberto Marchisio[1], Rachmad Vidya Wicaksana Putra[1] and Minghao Shao[2]
[1]New York University Abu Dhabi, AE; [2]Graduate Research Assistant, AE

Abstract: This work presents a multi-layered methodology for efficiently accelerating multimodal foundation models (MFMs). It combines hardware and software co-design of transformer blocks with an optimization pipeline that reduces computational and memory requirements. During model development, it employs performance enhancements through fine-tuning for domain-specific adaptation. Our methodology further incorporates hardware and software techniques for optimizing MFMs. Specifically, it employs MFM compression using hierarchy-aware mixed-precision quantization and structural pruning for transformer blocks and MLP channels. It also optimizes operations through speculative decoding, model cascading that routes queries through a small- to-large cascade and uses lightweight self-tests to determine when to escalate to larger models, as well as co-optimization of sequence length, visual resolution & stride, and graph-level operator fusion. To efficiently execute the model, the processing dataflow is optimized based on the underlying hardware architecture together with memory-efficient attention to meet on-chip bandwidth and latency budgets. To support this, a specialized hardware accelerator for the transformer workloads is employed, which can be developed through expert design or an LLM-aided design approach. We demonstrate the effectiveness of the proposed methodology on medical-MFMs and on code generation tasks, and conclude with extensions toward energy-efficient spiking-MFMs.

Date: Tuesday, 21 April 2026
Time: 08:30 - 10:00 CET

FS03 Focus Session: Challenges and Perspectives in Advanced Packaging: Design, Reliability, and Security of 3D and Chiplet-Based Systems (Hot-Topic)

Session chair: Hussam Hussam Amrouch, TU Munich, DE
Organisers: Dragomir Dragomir Milojevic, Université libre de Bruxelles and IMEC, BE

AI workloads are driving exceptional demand for performance and energy efficiency, forcing semiconductor innovation to advance along two major directions simultaneously. On the device roadmap, the transition from FinFETs to gate- all-around nanosheet FETs and, subsequently, monolithic 3D Complementary FETs (CFETs) is enabling scaling toward the 2nm era and beyond while targeting aggressive logic density. In parallel, advanced packaging, spanning 2.5D integration on silicon interposers, true 3D stacking, and hybrid 5.5D assemblies, is becoming essential to deliver ultra-high bandwidth, low-energy die-to-die connectivity required by rapidly growing AI model sizes and the resulting memory-wall bottlenecks. This focus session discusses the opportunities and challenges of this co-evolution, with emphasis on system-technology co-optimization and the inevitable need for multiphysics analysis across electrical, thermal, mechanical, and reliability domains. We highlight how reliability and security concerns are increasingly shaping architectural and packaging choices, and we discuss the role of deep learning as a practical enabler for faster simulation and design-space exploration under rising complexity.

FS03.1 AI-Driven Reliability Estimation from Beyond-3nm Transistors to Chiplet-Based Architectures

Hussam Amrouch, TU Munich, DE

Abstract: The relentless demand for higher performance in artificial intelligence (AI) systems is pushing current semiconductor technologies and scaling strategies to their limits. Advanced packaging has emerged as a promising path forward, enabling multiple dies to be interconnected in 2.5D or 3D configurations. Such heterogeneous integration opens new opportunities for optimizing performance, cost, and energy efficiency. However, it also introduces critical reliability challenges. The confined geometries of advanced packaging architectures exacerbate thermal issues, leading to elevated temperatures that accelerate device aging and degradation mechanisms. In this talk, we will demonstrate how neural networks can be leveraged to accelerate reliability analysis across multiple abstraction levels—from transistors to full systems—in the era of advanced packaging. We will first present techniques for accurate thermal analysis of chiplet-based architectures using multi-physics simulations, and show how deep neural networks (DNNs) can dramatically accelerate this process to enable fast yet accurate design exploration. We will then discuss how machine learning can be employed to predict and accelerate aging analysis, starting from individual transistor degradation up to complex circuit blocks and processor-level reliability estimation. The talk will highlight recent advances in technology nodes, focusing particularly on 3 nm nanosheet transistors and the next generation of beyond-2 nm devices, including the upcoming complementary FETs (CFETs) technology.

FS03.2 System Technology Co-Optimization in 5.5D

Dragomir Milojevic, IMEC, BE

Abstract: Advanced packaging enables implementation of 5.5D-ICs, where both lateral and vertical Die-to-Die connectivity are combined to link a flexible number of dies within a single IC package. These dies may originate from different CMOS process technologies. While migrating existing system architectures onto such technology platforms can bring advantages—and is already practiced in industry—the full potential of 5.5D integration emerges only with a system-level architectural redesign. This design philosophy, known as System Technology Co-Optimization (STCO), enables exploration of design points that would be impractical or unattainable in conventional 2D-ICs due to power, performance, or area limitations. In this talk, we will highlight the advantages of adopting STCO in hardware accelerator design and present a quantitative analysis of trade-offs at both the application (workload) level and the physical design level.

FS03.3 Security and Trust in 3D and Chiplet-Based Designs

Giorgio Di Natale, TIMA Laboratory, FR

Abstract: As 3D integration and chiplet-based design become increasingly adopted in high-performance and heterogeneous systems, security and trust issues are emerging as critical challenges. While Known Good Dies (KGDs) are assumed to be functionally verified before integration, practical deployment often requires additional post-distribution steps such as tuning, programming of secure elements, and final testing after stacking. These operations cannot rely on traditional debug and test infrastructures without introducing significant security risks, including potential exposure of IP and secret data. Moreover, the reduced physical accessibility and multi-vendor nature of chiplet-based assemblies increase the difficulty of detecting threats such as hardware Trojans and tampering during integration. This talk will explore these challenges, analyze current limitations in secure test architectures, and outline emerging perspectives and research directions to enhance trust, protect assets, and support secure in-field test and runtime monitoring in 3D-integrated systems.

FS03.4 Advances in Multiphysics Simulation for Multi-Die Systems

Jerome Toublanc, ANSYS, FR

Abstract: As electronic systems advance toward 3D integration, stacked dies, heterogeneous chiplet architectures, and advanced packaging, the coupled electrical, thermal, and mechanical interactions become increasingly complex. Traditional design and verification flows, based on simplified or isolated physics models, are no longer sufficient to confirm performance accurately, especially as reduced physical accessibility in 3D ICs limits direct testing and measurement. This talk will present advances in multiphysics simulation methodologies that capture electrical, thermal, mechanical, and electromagnetic effects across design implementation phases, from pre-layout to SignOff. Emphasis will be placed on AI-assisted strategies, co-simulation frameworks for predictive behavior analysis, and uncertainty quantification. Multiphysics simulation is essential not only for integrity and reliability, but also for hardware security. These innovations enable more accurate, scalable, and predictive design environments, supporting the robust optimization of next-generation 3D and chiplet-based systems.

Date: Tuesday, 21 April 2026
Time: 11:00 - 12:30 CET

FS04 Focus Session: Chiplets – How Far from Making Promise a Reality? (Panel)

Session chair: Andrea Kells, Arm, UK
Session co-chair: Anton Klotz, Fraunhofer EMFT, DE
Panellists: *Dominic Brown[1], Vincent Casillas[2] and Bart, Placklé[3]*
[1]ARM, US; [2]SiPearl, FR; [3]IMEC, BE

The future of chiplets is defined by modularity, scalability, and accelerated innovation in silicon design. As compute demands grow more specialized, the adoption of chiplets will make it possible to combine best-in-class components—each optimized for a specific function—into flexible, high-performance systems. This approach has the potential to reduce development time and cost while enabling greater customization across a wide range of markets. With growing ecosystem support and standardization, chiplets are paving the way for a more agile and collaborative era of semiconductor innovation. However, multiple challenges remain in making an open chiplet marketplace a reality, including interface standardization, simulation, security, and thermal and packaging considerations. This focus session will bring together organisations and companies working at different levels in the chiplet supply chain, to discuss how they are tackling some of these challenges, both individually and collaboratively, and what all of this means for the DATE community.

Date: Tuesday, 21 April 2026
Time: 14:00 - 15:30 CET

FS05 Focus Session: Beyond Conventional Hardware Security: Next-Generation Design and Security Evaluation for Hardware Architectures (Hot-Topic)

Session chair: Stjepan Picek, University of Zagreb & Radboud University, NL
Session co-chair: Nele Mentens, Leiden University and KU Leuven, BE
Organisers: Stjepan Picek, University of Zagreb & Radboud University, NL

Modern computing systems depend on the trustworthiness of their underlying hardware, particularly the increasingly complex System-on-Chip (SoC) and CPU architectures that power devices across cloud, edge, and IoT environments. The attack surface has expanded dramatically as these architectures integrate heterogeneous components into single, compact dies, including processors, accelerators, and third-party IPs. In recent years, academia and industry have reported numerous security-critical vulnerabilities in commercial SoCs and CPUs, underscoring the urgent need for scalable, automated techniques to detect hardware-level flaws before fabrication. Unlike software vulnerabilities, hardware flaws are immutable once silicon is produced, making pre-silicon security validation technically essential and economically critical. At the same time, the exponential rise of Artificial Intelligence (AI) has revolutionized computing, driving an unprecedented demand for specialized hardware such as GPUs and NPUs. These accelerators now form the backbone of AI infrastructure used by governments, enterprises, and research institutions worldwide. Ensuring the security and integrity of these AI hardware platforms is crucial, as their compromise could undermine model reliability, data confidentiality, and national-scale AI systems. The hardware foundations of AI must therefore be secure, verifiable, and trustworthy to maintain the current pace of innovation. Interestingly, this technological convergence also gives rise to a

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new paradigm, AI for hardware security. Researchers have recently begun applying AI-driven methodologies to enhance security validation, automate design-space exploration, and detect vulnerabilities more efficiently. Leveraging learning-based models, adaptive search strategies, and generative techniques, AI is now reshaping how hardware security analysis is performed. However, these same advancements also introduce novel risks, such as adversarial manipulation of AI-guided verification tools or unintended bias in automated test generation. This focus session will present diverse perspectives from academia and industry on advanced hardware security analysis techniques, the potential and challenges of using AI to advance hardware security evaluation, and emerging risks and mitigation strategies that accompany this evolution. Motivated by long-term community efforts such as the HackTheSilicon hardware security competitions, which, since 2018, have engaged in discovering vulnerabilities in realistic SoCs, this session emphasizes how hands-on insights and open evaluation frameworks are shaping the next generation of secure hardware design. Together, these experiences highlight the growing need for intelligence-driven, scalable, and proactive security validation frameworks to protect the hardware that creates modern computing and AI ecosystems. This Focus Session brings together leading experts from academia and industry to explore emerging methodologies, case studies, and research challenges in next-generation hardware security validation, focusing on: 1. Emerging vulnerabilities and security validation challenges in SoCs, CPUs, and AI accelerators. 2. Hybrid hardware verification techniques like formal-fuzzing and AI-guided validation techniques integrate symbolic reasoning with adaptive automation. 3. AI-assisted hardware security techniques include learning-based fuzzing, predictive bug detection, and automated verification. 4. Risks introduced by AI in hardware security workflows and potential countermeasures for safe adoption. 5. Collaborative directions toward integrating security validation into standard hardware design and verification pipelines. Through these discussions, the session will deliver a holistic industry and academia view of advanced hardware security verification methods, how AI depends on and enables hardware security, and offer a roadmap for developing trustworthy systems.

FS05.1 Emerging Threats in SoCs, CPUs, and AI Accelerators

Rosario Cammarota, Intel Labs, US

Abstract: Modern SoCs, CPUs, and AI accelerators are increasingly complex, integrating heterogeneous components that expand the attack surface. This presentation will highlight recent security-critical vulnerabilities, illustrate real-world examples, and discuss the emerging threat landscape. Attendees will gain insights into the types of attacks targeting both conventional and AI-specialized hardware, as well as the challenges in detecting and mitigating these threats.

FS05.2 Advanced Hybrid Hardware Fuzzing

Chen Chen[1], Stephen Muttathil[1], Mohamadreza Rostami[2], Nikhilesh Singh[2], Lichao Wu[3], Ahmad-Reza Sadeghi[2] and Jeyavijayan Rajendran[1]
[1]Texas A&M University, US; [2]TU Darmstadt, DE; [3]University of Bristol, GB

Abstract: While hardware fuzzing has proven effective in uncovering vulnerabilities, certain design spaces that require specific conditions remain challenging to explore due to its inherently random nature. This session will first present an example of a hard-to-reach design space in CPUs. It will then demonstrate how the conditions of this design space can be translated into inputs for formal verification tools. Finally, a quantitative analysis will be provided, highlighting the potential of using formal methods as a catalyst to generate targeted inputs for more efficient and comprehensive hardware fuzzing.

FS05.3 What the Fuzz! Pushing Beyond Randomness in Hardware Security with Generative AI

Nikhilesh Singh[1], Mohamadreza Rostami[1], Lichao Wu[2], Chen Chen[3], Stephen Muttathil[3], Jeyavijayan Rajendran[3] and Ahmad-Reza Sadeghi[1]
[1]TU Darmstadt, DE; [2]University of Bristol, GB; [3]Texas A&M University, US

Abstract: This session will explore advanced hardware fuzzing frameworks, including coverage-guided, AI-assisted, and hybrid approaches. The presenter, co-founder of HackTheSilicon, will provide real-world insights on the future of hardware verification techniques, demonstrating how these methods systematically uncover vulnerabilities in complex hardware designs and enhance security validation.

FS05.4 Exploring Semantic Leakage in Edge FPGA Implementations of Neural Networks

Zhuoran Liu[1], Konstantina Miteloudi[2], Durba Chatterjee[1] and Lejla Batina[3]
[1]Radboud University, NL; [2]Radboud University, N/; [3]Radboud University Nijmegen, NL

Abstract: This session will examine the risks introduced by AI in hardware security workflows, including potential pitfalls in AI-assisted verification and fuzzing. The speaker will also discuss countermeasures for safe adoption and explore collaborative directions to integrate security validation into standard hardware design and verification pipelines, highlighting practical strategies for building trustworthy and resilient hardware systems.

Date: Tuesday, 21 April 2026
Time: 16:30 - 18:00 CET

FS06 Focus Session: Who is Best Suited to do Verification? (Panel)

Session chair: Wolfgang Kunz, RPTU Kaiserslautern-Landay, DE
Session co-chair: Keerthikumara Devarajegowda, Siemens EDA, DE
Organiser: Wolfgang Ecker, Infineon Technologies, DE
Panellists: *Subhasish Mitra[1], Luca Benini[2] and Wolfgang Ecker[3]*
[1]Stanford University, US; [2]ETH Zurich, CH | Università di Bologna, IT; [3]Infineon Technologies, DE

Despite many improvements and a continuously increasing number of engineers verifying and validating designs, the number of re-spins required for a working chip is continuously increasing, so Harry D. Foster – _Chief Scientist Verification at Siemens EDA – _*in the 2024 Wilson Research Group IC/ASIC func-tional verification trend report*. This session approaches the long-lasting topic of the verification gap by discussing if the right people with the right skills are responsible for verification: Verification Engineers, Design Engineers, or Concept Engineers. We discuss how roles, skills and responsibilities may be distributed among these groups with the goal to make verification more efficient, with a higher quality and less costly.

Date: Wednesday, 22 April 2026
Time: 08:00 - 10:30 CET



FS07 Focus Session: From Concept to Silicon – End-to-End Agentic AI for Smarter Chip Design (Hot-Topic)

Session chair: Rolf Drechsler, University of Bremen, DE
Session co-chair: Francesco Regazzoni, ALaRI, CH
Organisers: Annachiara Ruospo, Politecnico di Torino, IT

From Concept to Silicon: End-to-End Agentic AI for Smarter Chip Design presents a unified and forward-looking vision of how artificial intelligence is transforming electronic design automation (EDA) across every stage of the chip design lifecycle. While most current efforts focus on applying large language models (LLMs) to specific tasks such as code generation or tool assistance, this session emphasizes a truly end-to-end perspective that integrates agentic and generative AI across high-level synthesis (HLS), physical design, testing, and security verification. The session brings together leading experts from academia and industry to demonstrate how multi-agent frameworks and reasoning-driven intelligence can achieve autonomous, adaptive, and continuously improving design flows. Topics include scalable datasets and benchmarks for LLMs in high-level synthesis, agentic automation for PPA-aware synthesis and constraint-driven test generation, generative AI for physical implementation, and adaptive AI frameworks for system-on-chip security verification. The talks converge on a cohesive vision for intelligent design systems capable of understanding intent, optimizing performance, and ensuring trustworthiness throughout the full EDA stack, marking the transition from isolated automation to true design autonomy.

FS07.1 Stepping Stones towards Domain Acceleration using AI-Driven High-Level Synthesis Design

Stefan Abi-Karam[1], Miaoyan Zhou[2] and Cong "Callie" Hao[1]
[1]Georgia Tech, US; [2]Georgia Tech, N/

Abstract: Field-programmable gate arrays (FPGAs) combined with high-level synthesis (HLS) enable domain-specific accelerators from high-level algorithmic descriptions, but HLS has not yet democratized hardware design in practice. High-performance HLS design for accelerators still requires expert knowledge in HLS optimization, design space exploration (DSE), performance analysis, and toolflows with limited debuggability and analysis even for expert human designers. To reduce this expertise burden, the community has explored ML-guided DSE, quality-of-results (QoR) proxy models, and LLMs for HLS code generation, editing, and optimization. However, progress remains constrained by scarce, accessible, high-quality HLS datasets and the difficulty of building diverse design collections. Many existing benchmarks sample design variations from a small pool of kernels rather than expanding the base pool of diverse designs. At the same time, most LLM hardware-design benchmarking emphasizes HDLs (e.g., Verilog), leaving comprehensive benchmarking infrastructure for HLS tasks comparatively limited. Furthermore, LLM-driven agents have shown strong automation and performance for software development tasks while agentic HLS design workflows still commonly lack robust interfaces to HLS tools, structured access to HLS reports, and feedback loops spanning HLS and downstream implementation. To address these gaps, we present progress toward end-to-end rapid design of domain-specific accelerators using AI-driven approaches for HLS by targeting three problems: (1) HLS design datasets, (2) LLM benchmarking for HLS design, and (3) end-to-end agentic HLS design. For HLS design datasets, we present HLSFactory, an end-to-end framework for building diverse HLS datasets that

expands individual HLS designs into diverse, cross-vendor design spaces, runs HLS/FPGA toolflows at scale, and aggregates standardized outputs into packaged datasets for benchmarking and ML, deep learning, and LLM research. HLSFactory is API-driven and extensible, enabling users to contribute designs or results and plug in custom toolflows at any stage. For LLM benchmarking, we present HLS-Eval, a benchmark and evaluation framework for LLM-driven HLS design that targets HLS code generation from natural language and HLS-specific optimization edits to existing code. It includes an "LLM-ready" benchmark for zero-shot evaluation, primarily drawing designs from HLSFactory for benchmarking. Finally, we also present our ongoing effort toward an end-to-end agentic HLS design workflow that unifies accelerator design stages in a multi-agent framework, with integrated HLS design tools from our prior works including LightningSim (fast cycle-accurate simulation), FIFO-Advisor (automated HLS FIFO sizing), AutoDSE/OptDSL/HLSFactory (structured DSE for HLS), deep-learning proxy models (QoR prediction), and libvhls (programmatic HLS tool interaction and hierarchical report analysis). Through this effort, we also plan to extend HLS-Eval to enable large-scale, parallel evaluations on realistic open-source HLS accelerators from academic projects, collecting agentic metrics on correctness, performance, agent runtime, and compute cost.

FS07.2 Do Agentic LLMs Change the Paradigm of Hardware Test Generation?

Farshad Firouzi[1], Pragya Sharma[2], Agastya Seth[2], Peter Domanski[2], Bahar Farahani[3], Sanmitra Banerjee[4], Jonti Talukdar[4] and Krishnendu Chakrabarty[2]
[1]ASU, US; [2]ASU, N/; [3]Cyberspace Research Institute, Shahid Beheshti University, N/; [4]NVIDIA Corp., N/

Abstract: Technology scaling and increasing System-on-Chip (SoC) complexity exacerbate reliability challenges arising from both structural defects and runtime-dependent failures, including Silent Data Corruptions (SDCs) that evade traditional error detection mechanisms. Structural testing remains essential for detecting modeled faults such as stuck-at faults; however, it is inherently limited in capturing failures that arise under dynamic operating conditions. In contrast, functional testing can expose workload-dependent failures, albeit at the cost of high testing overhead and largely unguided workload generation. This paper presents an agentic testing framework that integrates Large Language Models (LLMs) with Reinforcement Learning (RL) and Tree-structured Parzen Estimators (TPE) to guide functional workload generation and Automatic Test Pattern Generation (ATPG) settings under user-defined constraints. The proposed approach leverages feedback-driven optimization to steer test generation toward failure-prone behaviors while reducing reliance on manual expertise. Experimental evaluation on a RISC-V processor core demonstrates that the method outperforms manually generated workloads for functional testing, while experiments on six benchmark circuits show test quality comparable to expert-generated ATPG scripts for structural testing, with improved efficiency and scalability.

FS07.3 Large Language Models in Physical Design: From Data Generation to Intelligent Agents

Bing-Yue Wu[1], Atmadip Dey[2], Austin Rovinski[3] and Vidya A. Chhabria[1]
[1]Arizona State University, US; [2]Arizona State University, N/; [3]New York University, US

Abstract: Physical design remains one of the most complex stages of chip implementation, requiring deep expertise in electronic design automation (EDA) tools, workflows, and design knowledge. While open-source

EDA tools have improved accessibility and reproducibility, the effective use of physical design flows still requires significant manual effort and domain expertise. In parallel, large language models (LLMs) have rapidly evolved from data-driven language models to assistants and tool-interacting agents capable of reasoning, code generation, and closed-loop execution. This paper presents a perspective on the evolution of LLM usage in physical design, tracing a progression from early data-driven question answering and script generation to tool-aware assistants and closed-loop agentic workflows for physical design tasks. This paper highlights this evolution using representative open-source efforts and case studies. Further, we outline emerging research directions in which agentic LLMs move toward optimization and algorithm discovery, including the automation of tasks such as engineering change orders (ECOs) and the exploration of algorithm discovery within physical design tools. The work also highlights opportunities and challenges of LLM-driven design automation.

FS07.4 VERICHAT: An Agentic Conversational AI Assistant for Hardware Security Verification

Farimah Farahmandi, University of Florida, US

Abstract: Hardware security verification is a multi-stage process in which engineers must navigate complex design analyses, threat considerations, and verification strategies. They often need security-focused guidance, yet current verification environments provide little structured support for such assistance. Although conversational AI could offer such on-demand assistance, directly using general-purpose chatbots like ChatGPT or Gemini is risky due to their tendency to hallucinate and their reliance on static, outdated knowledge. We present VeriChat, a domain-specialized conversational assistant designed to support, rather than replace, existing verification workflows by providing context-aware security guidance. VeriChat employs a retrieval-augmented, multi- agent workflow in which three specialized agents collaboratively minimize hallucinations while improving the transparency and reliability of the response. Evaluated using a comprehensive methodology, VeriChat achieves a Faithfulness score of 87.73%, significantly outperforming the leading proprietary models.

Date: Wednesday, 22 April 2026
Time: 11:00 - 12:30 CET

FS08 Focus Session: MLIR, QIR, and Other Intermediate Representations –Towards Production-Ready Compilation for Quantum Computing (Hot-Topic)

Session chair: Robert Wille, TU Munich, DE
Session co-chair: Shigeru Yamashita, Ritsumeikan University, JP
Organisers: Robert Wille, TU Munich, DE, Shigeru Yamashita, Ritsumeikan University, JP

Quantum computing is transitioning from academic research into an emerging industry, with increasing demand for robust and scalable software and compiler infrastructures. Over the past decade, many compilers and frameworks for quantum programming have been created—mostly in academic contexts and in big parts developed by the design automation community. While valuable for prototyping, these fragmented, stand-alone tools lack the interoperability,

consistent abstractions, and mature workflows required for industry adoption. Additionally, they often have a hard time to scale to large qubit numbers required for relevant real-world applications.

FS08.1 Quantum Application Development Using CUDA-Q

Bettina Heim, NVIDIA Corp., CH

Abstract: Impactful quantum applications are hybrid in nature, meaning they take advantage of both classical and quantum resources for computing. While the integration of quantum processors (QPUs) into HPC systems gives rise to unique opportunities for accelerating subroutines that would be prohibitive to execute on classical processors, it also poses unique challenges for coordination between different processors. Integration efforts today are still in their infancy, and further research is needed to ex-plore how to build and leverage heterogeneous quantum-classical systems to their fullest extent. As QPUs continue to grow in size and capabilities, it is important to co-develop the classical hardware and software needed for the efficient compilation and execution of hybrid applications. In this context, intermediate representations such as QIR (Quantum Intermediate Representation) and MLIR (Multi-Level Intermediate Representation) play a crucial role in enabling flexible, scalable compilation flows and facilitating interoperability across diverse hardware and software platforms. CUDA-Q is an open-source platform for quantum computing that offers a unified programming model designed for CPUs, GPUs, and QPUs to work together effectively in a high-performance system. In this talk, I will introduce the CUDA-Q toolchain and how to take advantage of GPUs for accelerating the development and execution of quantum applications today, highlighting the integration of QIR/MLIR in the compilation process. I will discuss current integration strategies before outlining some of the necessary steps to allow for more tightly coupled interactions between classical and quantum resources in future large-scale systems.

FS08.2 How Do We Make LLVM Quantum? Bringing Industry-Scale Compilation Through LLVM And MLIR

Josh Izaac, Xanadu, CA

Abstract: Up until recently, most quantum programming frameworks have been written in Python, and serialize solely the quantum part of the workflow to simplistic string-based representations that are sent to cloud-connected quantum hardware (while the classical part executes locally!). But this ignores the history of classical programming infrastructure, and the fact that no algorithm is purely quantum — there is bound to be expensive and interwoven classical processing, and we need to take this into account. In this talk, I'll chat about how we are approaching this at Xanadu with PennyLane and Catalyst, a framework for quantum just-in-time compilation (QJIT). Using QJIT, full quantum-classical pro-grams written in Python are automatically captured and compiled using standard compiler technolo-gies such as MLIR and LLVM — which can lead to not only performance improvements, but increasing-ly new opportunities to interface with quantum computers. I'll also provide an overview of how we are building this compilation infrastructure to support both high-level algorithms and applications, and low-level execution on the next-generation of quantum photonic hardware — as well as the fu-ture challenges and obstacles we face and need to overcome. Overcoming these challenges and build-ing out this infrastructure will require collaboration between many disciplines, from quantum physi-cists and compiler developers to application developers and system engineers.

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FS08.3 HUGR: A Structured IR for Scalable Quantum-Classical Programs

Agustín Borgna, Quantinuum, GB

Abstract: We present HUGR, a production ready structured IR for quantum–classical programs. HUGR is designed with expressivity, extensibility, and machine-friendliness in mind, allowing it to capture capabilities of next-generation quantum computing devices with dynamic runtimes, enable program analysis and optimization beyond the traditional flat circuit picture, and ensure correctness via its linear type system. In this talk we discuss how a quantum-first IR approach compares with MLIR/QIR, how quantum-classical hybrid systems change the balance between compilation trade-offs, and how our stack integrates with the existing LLVM compiler ecosystem.

FS08.4 QIR-Based Software Stack for Trapped-Ion Quantum Computing

Daniel Borcherding, QUDORA, DE

Abstract: QUDORA Technologies is building trapped-ion quantum computers with a QCCD architecture and its unique Near Field Quantum Control (NFQC) technology, enabling high-fidelity operations. Our software stack spans from job preparation to execution, with the aim of minimizing ion movement, reducing noise impacts, and enabling low-latency hybrid quantum– classical computation. Through the QUDORA Cloud, users can already access our emulator, which incorporates a detailed noise model and is tightly integrated into the entire software stack. This provides researchers with a unique opportunity to explore hybrid quantum–classical algorithms in a realistic environment, accelerating the development of applications that benefit from the connectivity, coherence time, and scalability of our trapped-ion platform. This talk presents an overview of QUDORA's latest developments and the role of our QIR-based software stack in enabling them.

FS08.5 THE MQT Compiler Collection: A Blueprint for a Future-Proof Quantum-Classical Compilation Framework

Lukas Burgholzer, Daniel Haag, Yannick Stade, Damian Rovara, Patrick Hopf and Robert Wille, TU Munich, DE

Date: Wednesday, 22 April 2026
Time: 14:00 - 15:30 CET

FS09 Focus Session: Autonomous Systems Dependability in the era of AI: Design Challenges in Security, Reliability and Certification (Hot-Topic)

Session chair: Jeronimo Castrillon, TU Dresden, DE
Session co-chair: Behnaz Ranjbar, Ruhr University Bochum, DE
Organisers: Akash Kumar, Ruhr University Bochum, DE; Behnaz Ranjbar, Ruhr University Bochum, DE

The design of embedded safety-critical systems such as those used in next-generation automotive and autonomous platforms, is increasingly challenged by escalating system complexity, hardware–software heterogeneity, and the integration of intelligent, data-driven components. Ensuring dependability in such systems requires a holistic approach that spans multiple abstraction layers and encompasses both design-time and run-time assurance. Traditional methods for

reliability, safety, and security management often fall short in addressing the dynamic and uncertain behaviors introduced by Artificial Intelligence (AI) and Machine Learning (ML) components, especially under stringent real-time, power, and safety constraints. While AI and ML offer powerful predictive, adaptive, and self-optimizing capabilities that can enhance system dependability, their inherent non-determinism, data-dependence, and lack of formal guarantees introduce new challenges for verification, validation, and certification. This session will explore emerging methodologies, architectures, and frameworks for designing dependable autonomous and embedded systems in the era of AI. It will highlight advances in reliability modeling, secure system design, and certification approaches that account for imperfect, learning-enabled components, aiming to bridge the gap between AI innovation and certifiable system-level dependability.

FS09.1 ML for Cross-Layer Reliability in Autonomous Safety-Critical Systems

Behnaz Ranjbar and Akash Kumar, Ruhr University Bochum, DE

Abstract: The increasing complexity and autonomy of embedded safety-critical systems, such as autonomous vehicles, demand advanced methods to ensure system reliability under uncertain operating conditions. In modern automotive applications, in addition to increasing the complexity of the application, the technology scaling in embedded platforms has dramatically exacerbated the rate of manufacturing defects and physical fault rates. Increased unreliability has led to the increasingly complex problem of ensuring the reliable execution of applications on increasingly unreliable hardware. Since failure in such safety-critical systems may cause catastrophic consequences, improving reliability under all circumstances of stress and environmental changes plays a vital role in these systems. To design a reliable system, fault mitigation and reliability methods need to be applied in multiple system abstraction layers, like hardware, application, and system software. Cross-layer solutions are applied to provide application-specific and low-cost fault-tolerance by distributing the fault mitigation activity across the layers. The system should adapt to the operating environment during run-time to optimize other metrics. ML techniques are suitable for adaptive run-time operation, including fault prediction, detection, and tolerance. However, employing ML may introduce new challenges in ensuring requirements and trustworthiness. The talk first underscores that ensuring reliability in autonomous embedded systems requires addressing faults across all stack levels. Such cross-layer analysis is critical in domains like autonomous vehicles, where faults can propagate through hardware and software layers and selective protection mechanisms must be applied to maintain safety. Then, this talk highlights the potential of ML to achieve cross-layer reliability assurance in future safety-critical autonomous architectures, as well as its upcoming challenges.

FS09.2 Cross-Layer Security for Safety-Critical Automotive Systems

Kirankumar Raveendiran and Sudeep Pasricha, Colorado State University, US

Abstract: Modern automotive systems are rapidly evolving into complex cyber-physical ecosystems, integrating advanced computation, communication, and control across multiple layers—from hardware to software to network interfaces. As vehicles become increasingly autonomous and connected, ensuring robust security across these layers is paramount, especially for safety-critical functions where failures can have catastrophic consequences. This talk presents a cross-layer security framework tailored for automotive cyber-physical systems (CPS). The unique threat landscape of automotive CPS will be discussed, highlighting vulnerabilities at the hardware, firmware, operating system, and communication layers. Promising approaches will be discussed that integrate lightweight cryptographic primitives, attestation protocols, and real-time anomaly detection within vehicle networks and multimodal perception pipelines and using machine-learning. We will describe how cross-

layer coordination can significantly enhance resilience against both remote and physical attacks. The trade-offs between security, performance, and energy efficiency will also be discussed. Lastly, insights into future research directions, including adaptive security policies and integration with emerging standards for automotive cybersecurity will be presented.

FS09.3 Designing Safe Autonomous Systems with Imperfect ML Components

Samarjit Chakraborty, UNC Chapel Hill, US

Abstract: Modern autonomous systems now routinely use machine learning (ML) components. To ensure safety and reliability, the goal has been to use increasingly sophisticated ML algorithms to improve inference accuracy and new neural network verification techniques to ensure reliability and certification. However, it is proving to be nearly impossible to guarantee perfect inference accuracy and consequently ensuring dependability in autonomous systems with ML components is turning out to be one of the biggest design and verification challenges. In this talk we will pivot from the conventional aim of trying to design perfect ML inference engines and will instead characterize their imperfection as a first class citizen in the design process. Towards this, we will focus on system-level safety--instead of the safety or inference accuracy of ML components in isolation--and derive bounds on the allowed imperfectness of ML inferences. Second, we will use this characterization to ensure that controllers in autonomous systems can work with inaccurate ML inferences to ensure the satisfaction of the desired system-level safety specifications. We will illustrate this approach using multiple case studies to show how it can not only ensure certifiable safety, but also lead to much more cost-effective designs compared to what is possible today.

FS09.4 Challenges and Regulations in Reliable and Secure AI Sensing Systems

Cecilia Carbonelli, Infineon Technologies, DE

Abstract: Our contribution presents a practical and actionable roadmap for building trustworthy, user centric AI at the edge for safety and mission critical sensing applications. The approach centers on compliance, transparency, and reliability, combining lightweight uncertainty quantification, interpretable rule extraction across sensor pipelines, and calibration strategies that link performance, explainability, and user experience. Illustrative examples include environmental sensing and radar applications on resource constrained devices. We will show how adopting Trustworthy AI engineering best practices not only aligns with evolving governance (such as the EU AI Act) but delivers strategic benefits, accelerating innovation, unlocking new business opportunities, and strengthening market differentiation. As requirements and standards remain in flux, it is important to foster AI literacy and build awareness and competencies across organizations to shape the future of responsible AI and sensing. This is highly relevant for automotive applications, where edge AI powers ADAS and in cabin sensing under stringent functional safety and cybersecurity expectations, making uncertainty aware, interpretable, and well calibrated sensor pipelines essential for safety cases, homologation, and long-term reliability in harsh operating conditions.

Date: Wednesday, 22 April 2026
Time: 16:30 - 18:00 CET

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FS10 Focus Session: Crypto-agility in the Age of Quantum Computers (Hot-Topic)

Session chair: Mike Hutter, University of the Bundeswehr Munich, DE and PQShield, UK
Session co-chair: Paolo Palmieri, University College Cork, IE
Organisers: Francesco Regazzoni, University of Amsterdam, NL and Università della Svizzera italiana, CH; Elif Bilge Kavu, Barkhausen Institut and TU Dresden, DE

As NIST recently defined, "Cryptographic (crypto) agility refers to the capabilities needed to replace and adapt cryptographic algorithms in protocols, applications, software, hardware, and infrastructures without interrupting the flow of a running system in order to achieve resiliency"". Crypto-agility is a fundamental extra functional requirement for cryptographic systems, since they are exposed to state-of-the-art attacks, but also, possibly, to attacks that will materialize in the future. This last aspect is extremely relevant when the computation environment is rapidly changing, for instance because of novel attacks and threat coming up (such as the one caused by quantum computational power). This is exactly the case of devices and applications that use asymmetric cryptography, that will be outdated by the deployment of scalable quantum computers. This special session addresses the topic of crypto-agility focusing on the design, integration, and deployment of quantum resistant primitives, presenting tools to rapidly design efficient hardware primitives resistant against quantum computational power, and discussing design methodologies and interfaces to integrate these primitives with the rest of the system, maintaining agility while not affecting the performance. The topic is timely and of interest to the attendees of DATE. On the one hand, a variety of cryptosystems are demanded to be deployed in an environment that requires agility. On the other hand, it is crucial to exploit tools to efficiently design these cryptosystems and to interface them with the rest of the system. It is thus of crucial importance that designers of future systems are aware of all the facets of crypto-agility, and that they have full knowledge of specific architectures and designs that help to provide such extra functional requirements.

FS10.1 LLM4PQC – Accurate and Efficient Synthesis of PQC Cores by Feedback-Driven LLMS

Buddhi Perera[1], Zeng Wang[1], Weihua Xiao[2], Mohammed Nabeel[3], Ozgur Sinanoglu[4], Johann Knechtel[4] and Ramesh Karri[2]
[1]New York University, N/; [2]New York University, US; [3]New York University, AE; [4]New York University Abu Dhabi, AE

Abstract: The design of post-quantum cryptography (PQC) hardware is a complex and hierarchical process with many chal- lenges. A primary bottleneck is the conversion of PQC reference codes from C to high-level synthesis (HLS) specifications, which re- quires extensive manual refactoring [1]–[3]. Another bottleneck is the scalability of synthesis for complex PQC primitives, including number theoretic transform (NTT) accelerators and wide memory interfaces. While large language models (LLMs) have shown remarkable results for coding in general-purpose languages like Python, coding for hardware design is more challenging; feedback- driven and agentic integration are key principles of successful state-of-the-art approaches. Here, we propose LLM4PQC, an LLM-based framework that refactors high-level PQC specifica- tions and reference C codes into HLS-ready and synthesizable C code. Our framework generates and verifies the resulting RTL code. For correctness, we leverage a hierarchy of checks, covering fast C compilation and simulation as well as RTL simulation. Case studies on NIST PQC reference designs demonstrate a reduction in manual effort and accelerated design-space

exploration compared to traditional flows. Overall, LLM4PQC provides a powerful and efficient pathway for synthesizing complex hardware accelerators.

FS10.2 AI-Driven Generation of Efficient Post-Quantum Hash and Hardware Primitives

Ethan Cornett[1], Rahul Magesh[1], Sharath Pendyala[2], Abdelrahman Elwan[3], Giuseppe Manzoni[4], Elif Bilge Kavun[5] and Aydin Aysu[1]
[1]North Carolina State University, US; [2]NC State University, US; [3]Barkhausen Institut, TU Dresden, DE; [4]Barkhausen Institut gGmbH, DE; [5]Barkhausen Institut & TU Dresden, DE

Abstract: As quantum computing threatens the foundations of today's public-key cryptography, the hardware design community faces an urgent need for crypto-agility, the rapid and reliable deployment of new PQC primitives across diverse platforms. Building on our prior exploration of AI-assisted optimal hardware generation for the "bottleneck" units of PQC algorithms (such as sampler), this work broadens the scope to encompass the automated design of PQC-relevant hash functions (e.g., SHA-3, SHAKE, and SPHINCS+ components) and their integration into agile hardware frameworks. We investigate the use of LLMs as autonomous hardware co-designers, capable of generating, refining, and validating synthesizable C/HLS and RTL code for cryptographic accelerators under strict area-delay and security constraints. Our design flow enables on-demand regeneration and adaptation of cryptographic modules as algorithmic standards evolve, which is an essential capability for future crypto-agile embedded systems. Through extensive benchmarking across model families (i.e., GPT-4, Claude, Gemini, Grok) and hardware targets (ASIC, FPGA), we quantify LLM-generated implementations in terms of performance, resource utilization, and correctness against NIST PQC portfolio and previous candidates. We further discuss key challenges in AI-driven hardware co-design, ranging from prompt stability and verification scalability to algorithmic bias, and outline a road map for achieving trustworthy, quantum-resilient crypto-agile systems.

FS10.3 Design of Efficient Interfaces for Crypto-Agility

Francesco Regazzoni, University of Amsterdam and Università della Svizzera Italiana, CH

Abstract: Crypto-agility is a fundamental feature that security architectures and algorithms have to provide. It is crucial to ensure security, allowing algorithms to be updated thus withstand attacks not known at the deployment, and it is crucial for sustainability, extending the lifetime of devices. One of the key problems for providing crypto-agility is to design efficient interfaces that allow designers to integrate agile architectures with the rest of the system without affecting the performance. In fact, often, the interfaces are optimized on parameters such as key length, that are not to be fixed in agile architectures. This talk presents the efficient design of interfaces that, on the one hand, support changing parameters, on the other, ensure high performance and limited energy consumption.



DATE 2026 PhD Forum

Date: Monday, 20 April 2026
Time: 18:30 - 20:00 CET

The PhD Forum is a poster session hosted by EDAA, ACM SIGDA, and IEEE CEDA for PhD students who have completed their Ph.D. thesis within the last 12 months or are close to completing their thesis work. It represents an excellent opportunity for them to get feedback on their research and for the industry to get a glance at the state-of-the-art in system design and design automation.

Admitted Presentations

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Ardhendu Sarkar; Institute of Engineering & Management, Saltlake, IN

DESIGN OF ENERGY-EFFICIENT, HIGH-THROUGHPUT RECONFIGURABLE SYSTEMS THROUGH CROSS-LAYER APPROXIMATION AND IN-NETWORK COMPUTING
Zahra Ebrahimi[1] and Akash Kumar[2]; [1]Technische Universität Dresden, DE; [2]Ruhr University Bochum, DE

EFFICIENT COMPILATION FOR COARSE-GRAINED RECONFIGURABLE ARRAYS
Cristian Tirelli and Laura Pozzi; USI Lugano, CH

A STUDY OF PERFORMANCE OPTIMIZATION TECHNIQUES OF DIGITAL INTEGRATED CIRCUIT TEST GENERATION SYSTEM
Zhiteng Chao; University of Chinese Academy of Sciences, CN

TOWARDS PERFORMANCE-DRIVEN ANALOG LAYOUT DESIGN
Peng Xu and Bei Yu; The Chinese University of Hong Kong, HK

FROM THEORY TO SILICON: MAPPING NESTED LOOPS TO TIGHTLY COUPLED PROCESSOR ARRAYS (TCPAS)
Dominik Walter and Jürgen Teich; Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), DE

TOWARDS ULTRA-RELIABLE AUTOMOTIVE SYSTEMS-ON-CHIP
Giusy Iaria and Paolo Bernardi; Politecnico di Torino, IT

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Suraj Mandal and Debapriya Basu Roy; Indian Institute of Technology Kanpur, IN

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Tobias Hahn and Jürgen Teich; Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), DE

METHODS FOR ANALOG LAYOUT DESIGN AUTOMATION
Sungyu Jeong; Pohang University of Science and Technology (POSTECH), KR

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Alessandro Verosimile and Marco D. Santambrogio; Politecnico di Milano, IT

AI-DRIVEN TOPOLOGY SYNTHESIS AND SYSTEM-LEVEL OPTIMIZATION OF ANALOG/MIXED-SIGNAL CIRCUITS
Jiaqi Wang and Georges Gielen; KU Leuven, BE

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Dylan Leothaud; Univ Rennes, IRISA, FR

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Junjiao Sun; Centro de Electrónica Industrial, Universidad Politécnica de Madrid, ES

CO-DESIGN OF LIGHTWEIGHT INTRUSION DETECTION SYSTEMS FOR IOT DEVICES
Qingyu Zeng[1] and Yuko Hara[2]; [1]Institute of Science Tokyo, JP; [2]CNRS, FR

TOWARDS AUTONOMOUS ANALOG IC DESIGN: SAMPLE-EFFICIENT, PVT-ROBUST, AND EXPLAINABLE SIZING VIA AGENTIC AI
Mohsen Ahmadzadeh and Georges Gielen; KU Leuven, BE

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Jiacong Sun; KU Leuven, BE

A BATTERY-LESS ENERGY HARVESTING FRONT-END FOR POWERING MULTIPLE IOT NODES
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Minghao Shao; Independent Researcher, CN

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Chandranshu Gupta and Gaurav Varshney; Indian Institute of Technology Jammu, IN

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Vittorio Turco, Matteo Sonza Reorda and Annachiara Ruospo; Politecnico di Torino, IT

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Grafika Jati, Martin Molan, Francesco Barchi and Andrea Acquaviva; University of Bologna, IT

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DATE 2026 Keynotes

Opening Keynotes

Date: Monday, 20 April 2026
Time: 09:00 - 09:45 CET

Opening Keynote 1: It's Time to Futureproof our Prosperity by Superfueling Innovation, Enabling Next-Gen AI

Luc Van den hove, imec, Belgium

Abstract: The AI field is evolving at an incredibly fast pace, with major models and updates being released almost every month. As these models evolve beyond Large Language Models towards next-gen AI with advanced reasoning capabilities, compute systems struggle to handle the heterogeneous workloads in a performant and sustainable way. However, developing new, AI-optimised compute architectures and the enabling semiconductor technologies takes much more time than writing algorithms. To prevent bottlenecks slowing down AI-based advancements, we must reinvent compute architectures and semiconductor technology platforms.

The presentation will shed light on the need for flexible, versatile compute architectures implemented in flexible, versatile technology platforms while addressing the increasing challenges of density, power and memory. To speed up both advanced semiconductor technology R&D and full stack innovation for future AI applications, imec is expanding its pilot line infrastructure under the EU Chips Act. Next to new infrastructure, imec aims to boost innovation through intensified collaborations with complementary knowledge partners and through further internationalisation, attracting global talent and building strong, local ecosystems for diverse application domains, like health and automotive.

Transformative innovations for humankind hinge on the innovation pace of the semiconductor industry. It's time to supercharge our innovation engine, it's time to futureproof our prosperity.

Date: Monday, 20 April 2026
Time: 09:45 - 10:30 CET

Opening Keynote 2: Ultra-Low Latency Real-Time Processing for Quantum Computing

Bettina Heim, Nvidia, Switzerland

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Abstract: Quantum computing is one of the most promising technologies of our era. The fundamentally different nature of quantum processors (QPUs) requires a highly interdisciplinary effort to tackle challenges across the entire system to effectively leverage quantum resources. To realise the commercial potential of quantum acceleration, significant HPC resources are required to accelerate workloads necessary to the operation of a QPU. These workloads involve tasks related to quantum error correction, system calibration, and optimal control, and hence require an ultra-low latency exchange between the quantum system controllers (QSCs) and traditional processors such as GPUs.

Introducing a tight coupling between HPC and QPU environment presents a number of challenges that have become a focus within the quantum-HPC community.

Most QSCs are implemented using FPGAs or RFSoC devices, which run a firmware-defined pulse processor unit (PPU). Connecting the QSC via PCIe card can enable direct communication but poses scaling challenges. A potentially preferable alternative that offers better options for distribution is the use of a network interface card (NIC) for connection via Ethernet or InfiniBand.

In this talk I will discuss NVIDIA's effort to facilitate the development of advanced QPUs using real-time processing on GPUs using the NVQLink architecture. NVQLink leverages the RDMA over Converged Ethernet (RoCE) protocol to bypass traditional network stacks and CPU involvement, enabling sub-microsecond data transfer. This is essential to achieve real-time quantum error correction, where latency tolerances are of the order of tens of microseconds for some QPU architectures. While most existing solutions are limited to using FPGA for real-time processing, the availability of real-time compute on GPUs greatly facilitates the use of machine learning and AI for automation and accuracy improvements. First realisations of NVQLink systems thus enable a big step forward towards achieving fault tolerant quantum computing at scale by enabling data-driven research and co-develop of hardware and software solutions to achieve the necessary throughput and latency for commercial applications.

Lunchtime Keynotes

Date: Monday, 20 April 2026
Time: 13:15 - 14:00 CET

IEEE CEDA Distinguished Lecturer Lunchtime Keynote: Unifying Accelerator Design and Programming for Evolvable Computing

Zhiru Zhang, Cornell University, United States

Abstract: We are living through a fundamental shift in computing, where performance and efficiency gains increasingly come from specialised accelerators tailored to "hot" domains like AI. Yet as accelerator-centric computing proliferates, it continues to build atop a longstanding disconnect between the way we design these systems and the way we program them. This divide slows hardware innovation, complicates the software stack, and makes accelerators far harder to evolve than the rapidly changing applications they are meant to serve.

In this talk, I will present our recent research on closing this gap through a unified hardware-software co-design stack. At the core is a new abstraction that generalises single program multiple data beyond largely independent threads to encompass spatial structure and communication. It offers a single, composable model for expressing both how accelerators are constructed and how they are programmed. I will show how this abstraction is realised in Allo, an open-source, Python-based, MLIR-powered framework to enable concise specifications that map efficiently across FPGA, ASIC, NPU, and GPU platforms. I will conclude with a forward-looking perspective on automated compiler construction, differentiable hardware synthesis, and agentic design automation, and discuss how these directions may help move us toward truly evolvable heterogeneous computing.

Date: Tuesday, 21 April 2026
Time: 13:15 - 14:00 CET

Special Day on “Embracing AI in Education and Research” - Lunchtime Keynote: On My Perfect Life: A Tenured Position While AI Does the Job

Rolf Drechsler, University of Bremen, Germany

Abstract: Artificial Intelligence is reshaping how we explore, create, and teach. Tasks once considered inherently human are now increasingly delegated to systems that appear to reason, learn, and even invent. This development challenges long-standing notions of expertise, authorship, and the role of human judgment in science and education.

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Through this development, AI already influences how research is conducted, published, and taught - often with remarkable efficiency, yet also with opaque mechanisms and uncertain reliability. The enthusiasm surrounding these tools must be balanced by a critical assessment of their capabilities and limitations. What AI systems produce can be impressive, but the results often lack genuine understanding of user intent. The central question is how to preserve creativity, responsibility, and depth of insight in a world where machines can assist with almost everything - except understanding of what they do.

Date: Wednesday, 22 April 2026
Time: 13:15 - 14:00 CET

Special Day on "Open-Source Design Ecosystem" - Lunchtime Keynote: Democratizing Silicon: The Rise of Open-Source EDA and Europe's Strategic Roadmap

Luca Benini, ETHZ, Switzerland and Università di Bologna, Italy

Abstract: In recent years, the paradigm of open source has moved beyond software to transform the landscape of semiconductor design. Open-source Electronic Design Automation (EDA) tools offer a transformative path toward lowering barriers to entry, ensuring technological sovereignty, and accelerating engineering productivity. This talk provides a comprehensive overview of the current state of the open-source hardware ecosystem and its future potential. We will take a deep dive into Europe's strategic investments in these frameworks and explore how fostering a robust open-source toolchain is the essential catalyst for the next generation of open-source chips.

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DATE 2026 About DATE

DATE is a leading international event offering unique networking opportunities to the hardware and electronic systems design community. It brings together designers and design automation users, researchers and vendors, academics and students, as well as specialists in hardware and software design, testing, and manufacturing of electronic circuits and systems.

The **29th edition of the DATE 2026 conference** will be held at the **Palazzo della Gran Guardia** in Verona, Italy, from **20–22 April 2026**. The conference will be chaired by **Valeria Bertacco** from the University of Michigan, USA.

DATE 2026 is structured as an intensive three-day event focused on **in-person interactions**, further strengthening the already close-knit community of hardware and electronic systems designers. The majority of regular research papers will be presented in **technical sessions** featuring short pitch presentations supported by live poster interactions. Additional full-length presentation videos will be available **before, during, and after the conference**. This presentation format ensures that attendees can spend their time meeting, discussing, and exchanging ideas with colleagues—the very essence of what conferences are meant to be.

In addition to **a record number of technical paper presentations**, this year's DATE programme includes a rich variety of events: **Focus Sessions** on timely community topics, **Late Breaking Results sessions** on breakthrough approaches and emerging research directions, **Embedded Workshops**, **Embedded Tutorials**, **Multi-Partner Project sessions**, and the **Young People Programme** to support PhD students in professional networking and career development. The programme also features two **Special Days** on the themes of *"Embracing AI in Education and Research"* and *"Open-Source Design Ecosystem"*.

Verona, one of Italy's most celebrated historic cities, offers a distinctive blend of Roman heritage, medieval charm, and elegant urban life along the banks of the Adige River. Recognised as a **UNESCO World Heritage Site**, Verona preserves over two millennia of history in an exceptional urban fabric, including Roman ruins, fortified walls, Romanesque and Renaissance architecture, and the renowned **Piazza Bra** at the city's heart. Internationally famed as the city of Romeo and Juliet, Verona is also a hub of music, architecture, gastronomy, and wine, shaped as much by its monuments as by its longstanding traditions of opera and hospitality.

A defining symbol of Verona is the **Arena**, one of the best-preserved Roman amphitheatres in the world and the venue for one of the most renowned open-air opera festivals. The seamless integration of ancient heritage and living cultural traditions gives the city a distinctive atmosphere, where major international events take place in dialogue with history. For conference participants, Verona combines the charm of an intimate, walkable historic centre with the cultural richness of a major European destination, providing an inspiring setting for scientific exchange and professional networking.



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DATE 2026 will be hosted at the Palazzo della Gran Guardia, a landmark building overlooking Piazza Bra and standing directly opposite the Arena. Originally conceived in the early seventeenth century to provide a covered space for military reviews, the palace's construction began in 1610 based on a design by **Domenico Curtoni** and was completed in the nineteenth century. Today, it serves as a prestigious congress and exhibition venue in the heart of Verona. The venue combines historic character with practical event infrastructure, including a **700-seat auditorium**, a **conference hall**, approximately **900 m² of interconnected rooms on the upper floor**, and a covered **loggiato**. Its central location and iconic architecture make the Palazzo della Gran Guardia the ideal home for an internationally renowned conference such as DATE.

Join us in celebrating another exciting edition of the DATE conference—the leading scientific event in Design, Automation, and Test of microelectronics and embedded systems for the global academic and industrial research communities in hardware and system design.

Updated information about the conference is available online at: https://www.date-conference.com/



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DATE 2027 Call for papers

Design, Automation and Test in Europe Conference
The European Event for Electronic System Design & Test

Scope of the Event

The 30th DATE conference is the main European event bringing together designers and design automation users, researchers and vendors as well as specialists in hardware and software design, test and manufacturing of electronic circuits and systems. DATE puts strong emphasis on both technology and systems, covering ICs/SoCs, emerging technologies, embedded systems and embedded software.

Structure of the Event

The multi-day event consists of a conference with keynote talks, regular papers, panels, hot-topic sessions, tutorials, workshops, special focus days and a track for executives. The organisation of user group meetings, fringe meetings, a Young People Programme, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design automation, design and test communities. Special space will also be allocated for multi-partner innovative research projects to show their results. More details will be available on the DATE website: http://www.date-conference.com.

Areas of Interest

Within the scope of the conference, the main areas of interest are: design automation, design tools and hardware architectures for electronic and embedded systems; test and dependability at system, chip, circuit and device level for analogue and digital electronics; modelling, analysis, design and deployment of embedded software and cyber-physical systems; application design and industrial design experiences. Topics of interest include, but are not restricted to:

- System-level design methodologies and high-level synthesis
- System simulation and validation
- Formal methods and verification
- Power-efficiency and Smart Energy Systems for Sustainable Computing
- Smart Society and Digital Wellness
- Secure Systems, Circuits and Architectures
- Autonomous Systems and Smart Industry

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- Design and test for analogue and mixed-signal circuits and systems, and MEMS
- Design and test of hardware security primitives
- Design and test of secure systems
- Network on chip and on-chip communication
- Architectural and microarchitectural design
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- Approximate computing
- Reconfigurable systems
- Logical analysis and design
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- Design Automation for Quantum Computing
- Applications of Emerging Technologies
- Applications of Artificial Intelligence Systems
- Applications of Emerging Technologies
- Modelling and mitigation of defects, faults, variability, and reliability
- Test generation, test architectures, design for test, and diagnosis
- Dependability and system-level test
- Embedded software architecture, compilers and tool chains
- Real-time, dependable and privacy-enhanced systems
- Machine learning solutions for embedded and cyber-physical systems
- Design methodologies for machine learning architectures
- Design modelling and verification for embedded and cyber-physical systems

Submission of Papers

All papers must be registered by Sunday, 13 September 2026 AoE (title, abstract and co-authors), the final submission of the paper to be submitted by Sunday, 20 September 2026 AoE (firm deadline) via:
http://www.date-conference.com

Chairs

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