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A Low Power and High Reliability Nonvolatile SRAM Using In-Plane VGSOT-MRAM with Pre-Charge Restore Scheme

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***Abstract*—Conventional magnetic nonvolatile-static random access memory (MNV-SRAM) suffers from large store current, which leads to low area and energy efficiency, severely limiting their development and application. This paper proposes a 10T-2MTJ NV-SRAM cell based on the in-plane voltage-gated spin-orbit torque magnetic tunnel junction (VGSOT-MTJ), which enables field-free deterministic magnetization switching and reduces the required store current by leveraging the voltage-controlled magnetic anisotropy (VCMA) effect to assist the store operation. Thereby, the proposed design achieves the smallest SRAM cell area compared to prior works, due to the relaxed transistor drive strength requirement. On the other hand, existing NV-SRAM restore schemes exhibit a substantial deterioration in restore error ratio (RSER) with increasing MTJ resistance. Targeting the high resistance characteristics of VGSOT-MTJ, we innovatively propose a pre-charge restore scheme with sensitive transistor isolation. Simulation results demonstrate that the proposed design achieves the lowest read and write energy in SRAM mode, with store energy 1.58× to 2.48× lower than other in-plane MTJ-based designs. And the proposed restore scheme significantly improves restore reliability with over 98.7% RSER enhancement, and shows superior robustness across different MTJ resistances and tunnel magnetoresistance ratio (TMR) conditions.**

***Index Terms*—Nonvolatile-SRAM (NV-SRAM), voltage-controlled magnetic anisotropy (VCMA), in-plane magnetic anisotropy (IMA), voltage-gated SOT (VGSOT).**

I. Introduction

DRIVEN by the rapid advancement of Internet of Things (IoT) and edge computing technologies, wearable and embedded devices exhibit surging demand for low-power memory. This trend prioritizes ultra-low standby power consumption, making deep sleep mode with power-off memory highly desirable. However, the reliability of data recovery after power-off has become a critical concern, particularly in applications such as aerospace systems, where unexpected power failures or radiation-induced data corruption require highly robust preservation [1]. Nonvolatile SRAM (NV-SRAM) emerges as one of the most promising solutions to address these challenges [2]–[5]. By integrating SRAM with emerging nonvolatile memories, such as resistive random access memory (RRAM) [4], phase-change memory (PCM) [5], magnetic random access memory (MRAM) [2], [3], NV-SRAM preserves SRAM high-speed characteristics while enabling nonvolatile data storage, thereby enhancing reliability. Among nonvolatile memories, MRAM stands out as a compelling candidate for NV-SRAM due to its low power consumption, exceptional endurance, superior scalability, and good CMOS compatibility [6]–[11].

In NV-SRAM, the write current for the MTJ must be supplied by SRAM transistors, while the size of these transistors directly affects SRAM performance. Owing to its advantages in high speed, low write voltage requirement, and immunity to read-write disturbance, spin-orbit torque (SOT) MRAM is more suitable for NV-SRAM than conventional spin-transfer torque (STT) MRAM [12]. Among mainstream SOT-MRAM, the in-plane magnetic anisotropy (IMA) SOT-MTJ enables intrinsically field-free deterministic switching driven solely by the SOT current, offering a critical advantage for practical applications [11], [13], [14]. Although SOT-MTJ offers improved performance, its write current requirement still imposes certain constraints on SRAM transistor sizing. This inherent trade-off constitutes a major challenge in SOT-NV-SRAM design. To overcome these limitations, researchers have developed a voltage-gated SOT (VGSOT) mechanism [15], [16]. By applying a bias voltage across the MTJ, the voltage-controlled magnetic anisotropy (VCMA) effect reduces switching current and improves the switching speed, enabling high-speed, low-power backup operations at fJ/bit level.

But high resistance of in-plane VGSOT-MTJ constitutes a fundamental constraint in NV-SRAM applications. When the MTJ resistance (R_{MTJ}) significantly exceeds the MOS transistor on-state resistance (kΩ level), this orders-of-magnitude disparity severely degrades the sensing margin, leading to unacceptably high restore error rates (RSER). Addressing these challenges, we present a novel 10T-2M MNV-SRAM cell employing in-plane VGSOT-MTJ, as shown in Fig. 1. The main contributions of this work are listed as follows:

1) We optimize the compact model for the in-plane VGSOT-MTJ, incorporating both IMA and VCMA effects. By applying a negative voltage bias across the MTJ, the write current and the switching speed is improved. This approach reduces the SRAM cell area and energy overhead caused by driving the

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MTJ, thereby enhancing overall performance of the SRAM.

2) We propose a 10T-2M NV-SRAM cell with an optimized MTJ write path, achieving the smallest write current requirement and the most compact write transistor size among all compared designs. It reduces store energy by 1.58× to 2.48× compared to other in-plane MTJ-based designs [12], [17].

3) We propose a pre-charge restore scheme with sensitive transistors isolation that overcomes the limited sensing margin of high-resistance VGSOT-MTJs. The proposed restore scheme maintains 100% reading accuracy for $R_{MTJ} = 10$ kΩ to 500 kΩ and for tunnel magnetoresistance ratio (TMR) ≥ 2.

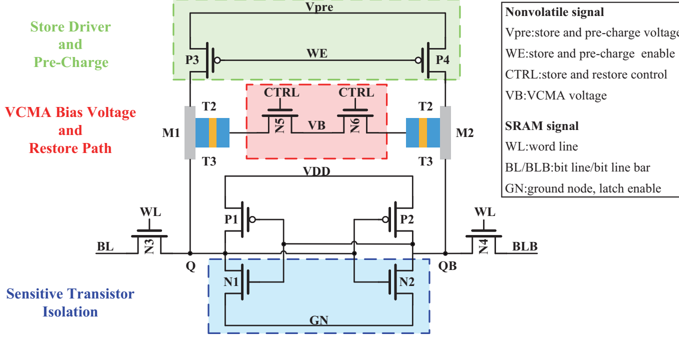


Fig. 1. Schematic of the proposed 10T-2M NV-SRAM based on in-plane VGSOT-MTJ.

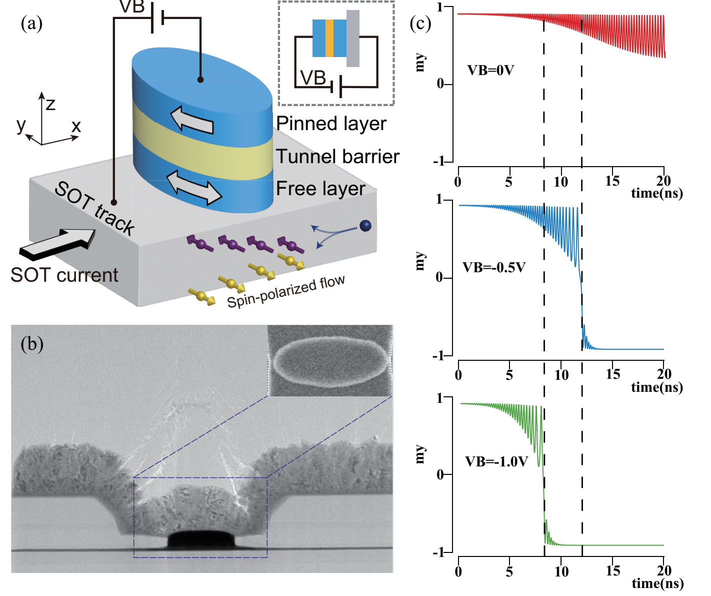


Fig. 2. (a) Structure of the in-plane VGSOT-MTJ. (b) TEM image of a single in-plane SOT-MTJ and the inset shows the great morphology of the elliptical MTJ. (c) Effect of the bias voltage across the VGSOT-MTJ on the switching speed under a constant SOT current.

II. The VGSOT-MTJ Device

The conventional SOT-MTJ constitutes a three-terminal device comprising a sandwich structure (pinned layer/tunnel barrier/free layer) with an underlying SOT track. Structure of the in-plane VGSOT-MTJ and TEM image of the in-plane SOT-MTJ are shown in Fig. 2(a) and (b), respectively. The pinned layer maintains a fixed magnetization direction. Current flowing in the SOT track switches the magnetization of free layer and sets the MTJ to a low-resistance (R_P) or high-resistance (R_{AP}) state. SOT-MTJs provide superior write/read performance and enhanced reliability through physically separated read and write paths, which eliminate read-disturbance and prevent device breakdown. The magnetization dynamics of the free layer can be described by the modified Landau-Lifshitz-Gilbert (LLG) equation as follows [18]:

$$\begin{aligned}\frac{\partial \vec{m}}{\partial t} &= -\gamma\mu_0(\vec{m}\times\vec{H}_{\text{eff}}) + \alpha(\vec{m}\times\frac{\partial \vec{m}}{\partial t}) \\ &\quad - \frac{\gamma\hbar\theta J_{SOT}}{2eM_S t_{FL}}\left(\vec{m}\times(\vec{m}\times\vec{\sigma})\right)\end{aligned} \tag{1}$$

where $\vec{m} = (m_x, m_y, m_z)$ is the magnetization vector of the free layer. $\vec{\sigma}$ is the spin-polarization direction of SOT. J_{SOT} is the SOT current density. γ is the gyromagnetic ratio (1.76×10^{11} rad/(s·T)). μ_0 is the vacuum permeability. $\hbar$ is the reduced Planck constant. VCMA effect primarily modulates the z-component of the effective magnetic field $\vec{H}_{\text{eff}}$, which is given below [18]:

$$\begin{aligned} H_{\text{eff},z} &= \frac{2K_u m_z}{\mu_0 M_S} - \frac{2\xi V_B m_z}{\mu_0 M_S t_{FL} t_{OX}} - M_S N_z m_z \\ H_{\text{eff},x} &= -M_S N_x m_x, \quad H_{\text{eff},y} = -M_S N_y m_y \end{aligned} \tag{2}$$

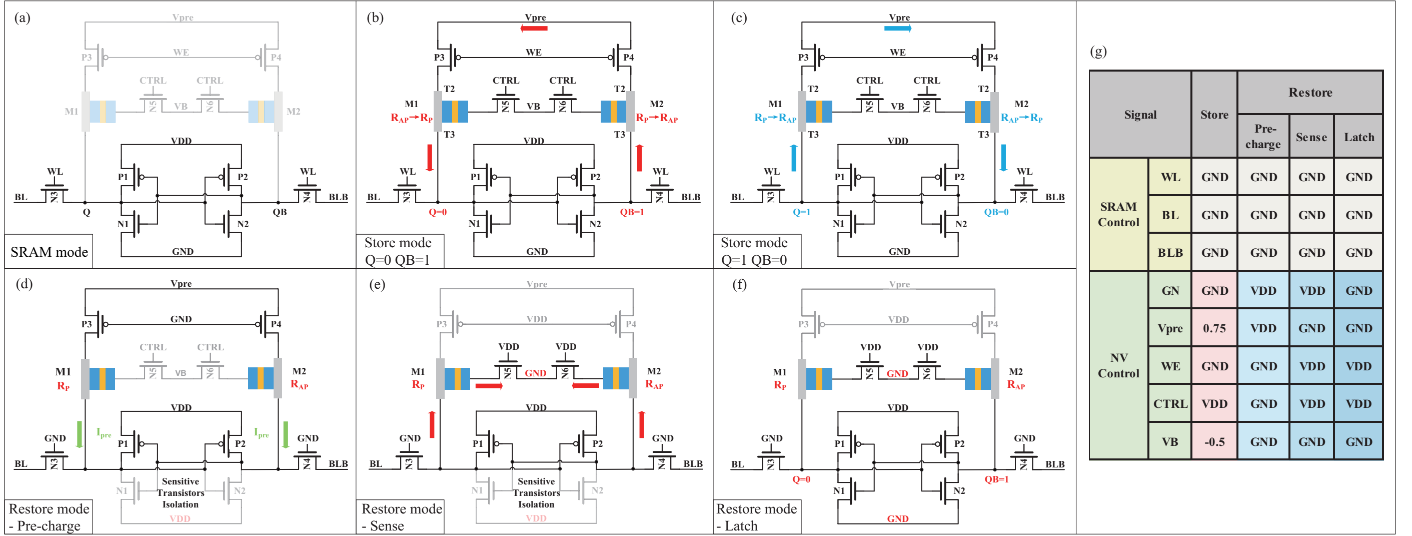
where N_z, N_x and N_y are the demagnetization factors, determined by the shape of the MTJ.

To reduce the SOT switching current in in-plane MTJ, a negative VCMA voltage (V_B) is applied across the MTJ to decrease the switching current and improve write speed [16], [19], as shown in Fig. 2(c). Therefore, employing VCMA-assist scheme in NV-SRAM store operation delivers two critical advantages: 1) It reduces the SOT current required for MTJ switching, which enhances the backup speed while lowering power consumption. 2) It significantly relaxes the constraints on transistor size imposed by MTJ writing, leading to improved memory density while maintaining read/write performance in SRAM mode.

Notably, VGSOT-MTJ devices usually adopt a thick MgO barrier to secure a sufficient VCMA coefficient ξ, high endurance, and minimized STT effect interference [20]. Consequently, VGSOT-MTJs exhibit a high resistance, typically on the order of hundreds of kΩ to the MΩ range [16], [19], which is orders of magnitude higher than the on-resistance of transistors (<10 kΩ), thus severely degrading the RSER.

III. The Proposed In-plane VGSOT-MTJ Based 10T-2M NV-SRAM

To address the aforementioned challenges, we propose a 10T-2M NV-SRAM, as illustrated in Fig. 1 and Fig. 3. The pull-up transistors P1-P2 and the pull-down transistors N1-N2 form cross-coupled inverters. N3-N4 are pass gate transistors. P3-P4 are the store and pre-charge control transistors. N5-N6 are VCMA control transistors. The proposed MNV-SRAM supports four operating modes, which are controlled by the signals detailed in Fig. 3(g). SRAM control signals (WL, BL, BLB) manage standard memory access, while dedicated



Signal		Store	Restore		
			Pre-charge	Sense	Latch
SRAM Control	WL	GND	GND	GND	GND
	BL	GND	GND	GND	GND
	BLB	GND	GND	GND	GND
NV Control	GN	GND	VDD	VDD	GND
	Vpre	0.75	VDD	GND	GND
	WE	GND	GND	VDD	VDD
	CTRL	VDD	GND	VDD	VDD
	VB	-0.5	GND	GND	GND

Fig. 3. Schematic of the proposed 10T-2M NV-SRAM under different operating modes: (a) SRAM mode, (b) store mode under "Q=0, QB=1", (c) store mode under "Q=1, QB=0", and (d) pre-charge phase, (e) sense phase, as well as (f) latch phase in restore mode. (g) Control signal of the proposed MNV-SRAM cell.

nonvolatile control signals (Vpre, WE, CTRL, VB) govern NV functions. GN is set to VDD during the pre-charge and sense phases and to GND in all other phases.

A. SRAM Mode

Fig. 3(a) shows the circuit configuration in this mode, CTRL and WE are both held inactive, thus completely isolating the two VGSOT-MTJs from the 6T-SRAM, the MNV-SRAM cell operates identically to a standard 6T-SRAM cell.

B. Store Mode

The proposed NV-SRAM architecture implements transient data storage in MTJs before power-off. VB is biased to a negative voltage. Although both MTJs share the same top-electrode voltage (VB), the absence of Vpre results in different effective VCMA voltages due to write path voltage division. To mitigate this, applying Vpre aligns their switching speeds more closely, thereby shortening the overall switching time. Store mode activation requires WE = GND and CTRL = VDD, turning on P3-P4 and N5-N6. As shown in Fig. 3(b) and (c), differential voltages between Q and QB generate directional current through the SOT track: When Q=0 and QB=1, current flows along the path QB→M2(T3→T2)→P4→P3→M1(T2→T3)→Q, switching MTJs (M1, M2) to (R_P, R_{AP}) states. Conversely, if Q=1 and QB=0, I_{SOT} flowing from node Q to QB will be generated, thereby switching MTJs (M1, M2) to (R_{AP}, R_P) states respectively.

C. Standby Mode

After store mode and power-off, the nonvolatile MTJs retain runtime data, effectively eliminating static power consumption while preserving the integrity of the data stored in NV-SRAM.

D. Restore Mode

When the system is powered on again, data in the MTJs must be restored to the SRAM. The entire restore mode can be divided into three phases: pre-charge, sense, and latch.

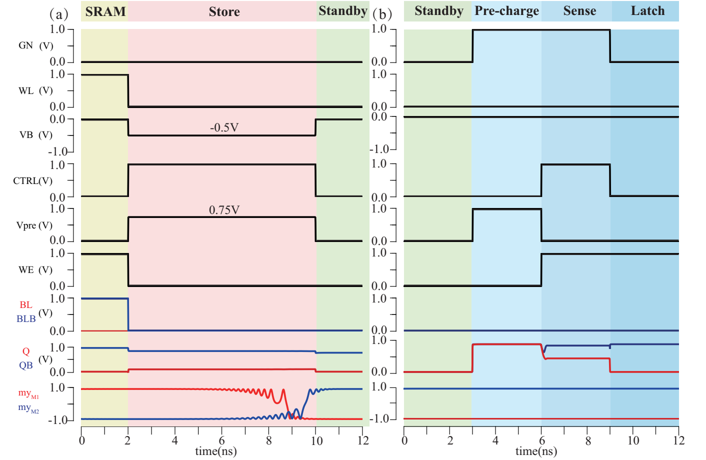


Fig. 4. (a) Store mode and (b) restore mode transient simulation waveforms of a complete operating cycle for the proposed 10T-2M NV-SRAM.

1) Pre-charge: Vpre is set to VDD for precharging. GN is biased to VDD to keep N1 and N2 in the near-cutoff region, thereby eliminating their impact on read performance. CTRL and WE are set to GND, causing P3-P4 to turn on while N3-N6 remain off. Consequently, Q and QB are driven to VDD, as shown in Fig 3(d). Due to the small parasitic capacitance within the cell, the initial pre-charge phase generates only a current pulse flowing through the SOT track, with a width below 10 ps and an average amplitude under 15 µA. Given that the VCMA voltage across the MTJ is zero, this combination ensures the MTJ is immune to write disturbance. The in-cell pre-charge scheme is implemented by reusing the write transistors P3 and P4, which guarantees sufficient precharging and reduces area overhead. Moreover, it renders the restore operation immune to residual charge on Q and QB.

2) Sense: Set WE and CTRL to VDD while keeping other signals unchanged. This turns off P3-P4 and activates N5-N6. With VB = GND, Q and QB begin discharging, as shown

in Fig. 3(e). The complementary states of the two MTJs result in different discharge speeds across the two branches. The two PMOS transistors (P1,P2) serve a latching function. Since the signal does not reach full swing, the PMOS are effectively connected in series with the VGSOT-MTJs, which provides excellent resistance adaptability. In contrast, if NMOS transistors (N1,N2) were to participate in the sense operation, their parallel connection with the VGSOT-MTJs would yield a total resistance significantly lower than that of the MTJ itself, which would effectively eliminate the resistance difference between the two branches. As a result, the difference in discharge speed between the two branches would be greatly weakened. Therefore, the proposed restore scheme necessitates the electrical isolation of the NMOS transistors.

3) Latch: The substantial voltage margin between Q and QB, established through prior pre-charge and sense operations, enables a highly reliable restore operation via latching. As shown in Fig. 3(f), after the voltages at nodes Q and QB stabilize, GN is set to GND to enable the cross-coupled inverters. Once either node voltage drops below the inverter switching threshold voltage, the cross-coupled inverters latch the complementary voltages, converting the MTJ resistance states into digital data stored in the SRAM. By delaying the falling edge of the GN until the voltage difference between the Q and QB stabilizes, the cross-coupled inverters are enabled to latch data more reliably, thus significantly enhancing the robustness of the restore operation.

TABLE I
DEVICE PARAMETERS USED IN SIMULATIONS

Symbol	Parameter	Value	Unit
-	IMA-MTJ (I-MTJ) area	$150\times60\times\pi/4$	nm^2
-	PMA-MTJ (P-MTJ) area	$60\times60\times\pi/4$	nm^2
t_{OX}	MgO barrier thickness	1.3	nm
t_{FL}	Free layer thickness for I-MTJ	1.4	nm
t_{FL}	Free layer thickness for P-MTJ	1.1	nm
t_{SOT}	SOT track thickness	3 [14]	nm
-	IMA-SOT track area	150×60	nm^2
-	PMA-SOT track area	60×60	nm^2
M_S	Saturation magnetization for I-MTJ	8.7×10^5	A/m
M_S	Saturation magnetization for P-MTJ	6.25×10^5	A/m
H_K	Effective anisotropy field for P-MTJ	1.1×10^5	A/m
B_x	Amplitude of in-plane field for P-MTJ	5	mT
TMR_0	TMR with 0V bias	200%	-
V_h	Voltage bias when $TMR=TMR_0/2$	0.8 [6]	V
ρ	SOT track resistivity	160 [14]	μΩ·cm
K_u	Anisotropy energy density	2.5×10^5	J/m^3
ξ	VCMA coefficient	100 [16], [21]	fJ/(V·m)
θ	Spin hall angle	0.6 [14]	-
α	Gilbert damping constant	0.02	-
P	Spin polarization	0.62	-

IV. SIMULATION

Based on the proposed in-plane VGSOT-MTJ model and a CMOS 28 nm design kit, we evaluate the performance of the proposed NV-SRAM design. The MTJ model is built upon the perpendicular magnetic anisotropy (PMA) model [18]. Key device parameters are listed in Table I. Exhaustive functional simulations verify nonvolatile operation of the proposed NV-SRAM cell. Fig.4 presents the transient waveforms of the store and restore operations. A sufficiently long standby period is intentionally omitted between Fig.4 (a) and (b) to avoid interference from the residual charge at the SRAM nodes during restore operation: 1) During data-intensive operations, the NV-SRAM stores data in volatile latch, maintaining identical performance to conventional SRAM. 2) Before power-off, data from SRAM nodes (Q=0, QB=1) is written to MTJs (M1, M2), programming their resistance states as (R_P, R_{AP}) respectively. 3) In standby mode, NV-SRAM provides non-volatile data retention with virtually zero static power consumption. 4) Upon power-on, the SRAM circuit functions as a pre-charge sense amplifier (PCSA) to read MTJ resistance states, recovering the original data to SRAM.

A. SRAM Performance Analysis

The nonvolatile functionality should be integrated into the SRAM without significantly increasing its area or degrading its performance. Table II compares the write and read performances of the proposed design with available literature. Since the designs being compared employ different types of MTJ, a fair comparison is ensured by unifying the thermal stability factor of all MTJ devices to 32 [22]. This configuration achieves a performance trade-off between high-speed access and data retention capability in MRAM. The corresponding formula for calculating the thermal stability factor of the I-MTJ is given below [23]:

$$\Delta_{\mathrm{IMA}} = \frac{\mu_0 \pi M_S^2 t_{FL}^2 w(AR-1)}{4k_{\mathrm{B}}T} \tag{3}$$

where k_B is the Boltzmann constant. w and AR represent width and aspect ratio of the free layer, respectively. For the P-MTJ, the thermal stability factor is given by [24]:

$$\Delta_{\mathrm{PMA}} = \frac{\mu_0 H_k M_S V_{FL}}{2k_{\mathrm{B}}T} \tag{4}$$

$$H_{\mathrm{k}} = \frac{2K_{\mathrm{u}}}{\mu_0 M_S} - (N_z - N_x) M_S \tag{5}$$

where V_{FL} is the volume of the free layer. H_k was set to 1.1×10^5 A/m to achieve $\Delta = 32$.

In all designs investigated in this work, the transistors in 6T-SRAM adopt identical β ratio ($(W/L)_{\text{pull down}}/(W/L)_{\text{pass gate}}$) and γ ratio ($(W/L)_{\text{pull up}}/(W/L)_{\text{pass gate}}$). The channel width of the pull up transistors (W_{pu}) are specified in Table II. All transistors in the nonvolatile circuit feature a width of 120 nm. Simulation results show that under the same thermal stability barrier, the IMA device requires a lower critical switching current but exhibits slower switching speed [24]. The introduction of the VCMA effect further reduces the switching current and improves the speed. The proposed design achieves the smallest transistor size among existing NV-SRAM designs. The SRAM write and read performance is summarized in Table II. The proposed design achieves the lowest energy consumption and write latency.

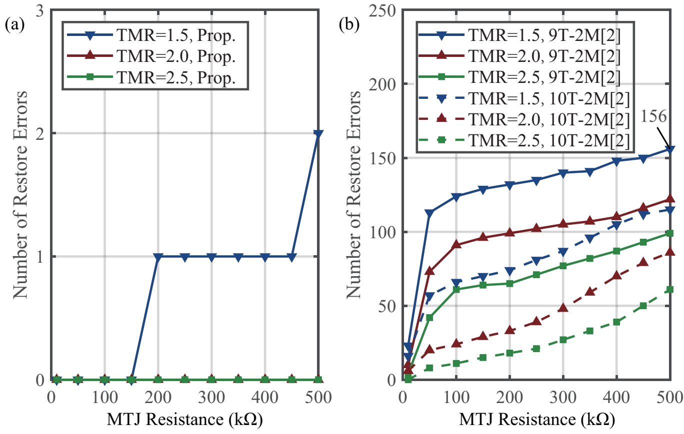


Fig. 5. Number of restore errors from 1000-run Monte Carlo simulations for (a) the proposed 10T–2M NV-SRAM and (b) two reference designs (9T–2M and 10T–2M) [2] based on VGSOT-MTJ.

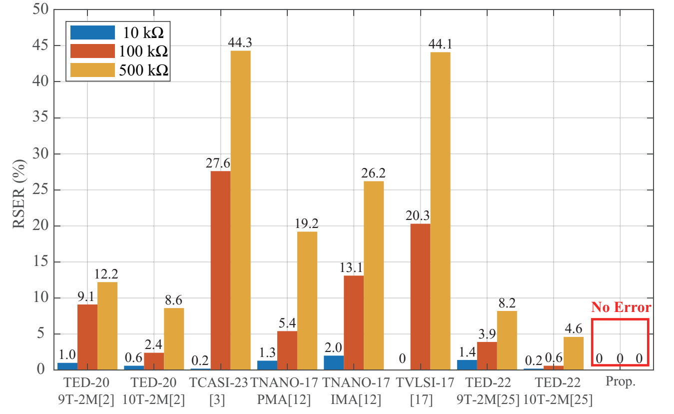


Fig. 6. RSER comparison among the proposed 10T-2M NV-SRAM and other MNV-SRAM cells at different MTJ resistance values.

Compared to the 11T–2M design using STT+SOT MTJ [12], which consumes the most power, our design reduces write energy by more than 3.65×. In read operations, although the proposed architecture exhibits a somewhat longer read latency, it reduces read energy by more than 3.76×. Overall, the proposed design offers a significant improvement in energy efficiency for both write and read operations, and the reduction in transistor size leads to a decreased area overhead, making it highly suitable for low-power embedded memory applications.

B. Reliability Analysis

RSER quantifies the probability of data backup failure caused by process variation from devices and transistors, which directly impacts reliability and system performance. The Monte Carlo simulations of 1000 samples are performed with MTJ process variations of 5% (1σ).

The proposed pre-charge restore scheme is compared with conventional discharge restore scheme utilizing VGSOT MTJ [2]. Their RSER performance under different MTJ resistance and TMR values is illustrated in Fig. 5. The conventional restore scheme achieves favorable read performance when the MTJ resistance is low; however, as R_{MTJ} increases, the RSER rises significantly. In contrast, the proposed design employs pre-charge restore scheme, which maintains 100% reading accuracy across a parameter range of R_{MTJ}= 10 kΩ to 500 kΩ and TMR ≥ 2. Even under the worst case with R_{MTJ} = 500 kΩ and TMR = 1.5, the RSER remains at 0.2%, representing a 98.7% reduction compare to the discharge restore scheme. Thus, without adding any peripheral circuitry, our scheme achieves extremely high restore reliability solely through sensitive transistor isolation.

To demonstrate superior read performance and robustness across the MTJ resistance of the proposed structure, we compare our design with 8 prior designs from [2], [3], [12], [17], [25], and analyze the RSER across different resistance levels (R_{MTJ}=10 kΩ, 100 kΩ, 500 kΩ; TMR=2), as shown in Fig. 6. On all resistance scales, our design achieves 0% RSER. In contrast, all previous work exhibits substantial deterioration in RSER with increasing MTJ resistance. Furthermore, even under an ultra-high resistance of R_{MTJ}=5 MΩ with TMR=2,

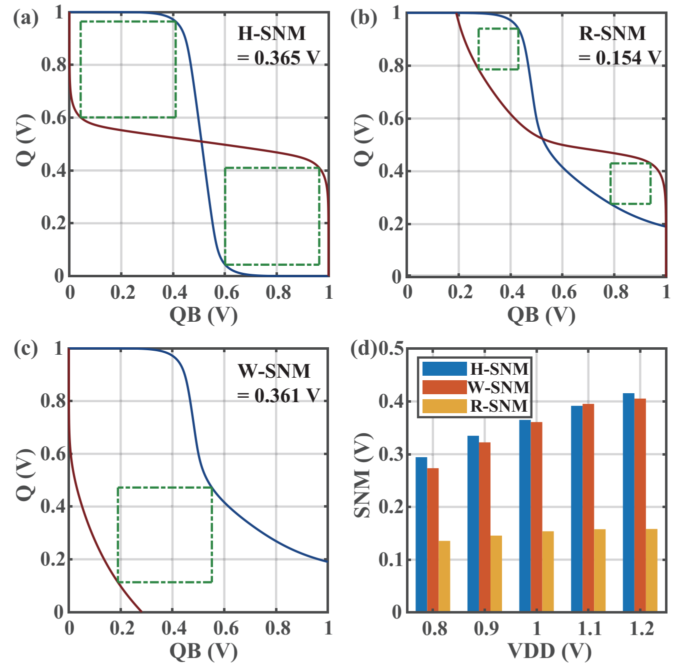


Fig. 7. (a) H-SNM, (b) R-SNM, (c) W-SNM, and (d) SNM at different VDD levels for the proposed 10T-2M NV-SRAM.

the proposed scheme achieves a low RSER of only 0.4%. The simulation results demonstrate that, compared to prior designs, this approach effectively overcomes the technical limitations of insufficient read margin and high RSER caused by the high resistance of VGSOT-MTJs. It exhibits high restore reliability across a wide range of MTJ resistance values, demonstrating significant robustness advantages.

C. Stability Analysis

SRAM stability is quantified via butterfly curve of static noise margins (SNM). The noise margins of the storage cell are visually demonstrated by plotting the voltage transfer characteristics (VTC) curves of its two cross-coupled inverters [26]. Fig. 7(a), (b), (c) present the H-SNM, R-SNM, W-SNM of the proposed NV-SRAM, respectively. During SRAM mode operation, isolation between the NV element and the data

TABLE II
COMPARISON WITH PRIOR MNV-SRAM DESIGNS

	TED-20 [2]	**TED-20 [2]**	**TCASI-23 [3]**	**TNANO-17 [12]**	**TNANO-17 [12]**	**TVLSI-17 [17]**	**TED-22 [25]**	**TED-22 [25]**	**This Work**
Design	9T-2M	10T-2M	8T-2M	11T-2M	11T-2M	8T-2M	9T-2M	10T-2M	10T-2M
Method	VGSOT	VGSOT	STT+SOT	STT+SOT	SOT	SOT	STT+SOT	STT+SOT	VGSOT
Type	PMA	PMA	PMA	PMA	IMA	IMA	PMA	PMA	IMA
Field-free	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Wpu(nm)	140	270	370	530	160	160	240	460	**120**
Write Latency(ps)	137	163	178	213	141	142	158	201	134
Write Energy(fJ)	2.75	4.73	5.8	8.91	3.04	2.98	4.25	7.7	**2.44**
Read Latency(ps)	224	200	211	178	216	225	205	184	230
Read Energy(fJ)	10.2	18.06	24.11	33.78	11.41	11.41	16.24	29.55	**8.98**
H-SNM(mV)	364.1	361.3	360.2	359	363.7	363.7	361.7	359.5	365
R-SNM(mV)	150.8	140.4	135.9	131.3	148.8	150.7	141.9	133.1	154
W-SNM(mV)	363.9	373.6	375	375.3	368.3	365.1	371.8	375.5	360.9
Store Latency(ns)	1.2	1.45	2	2	9.8	9.3	2	2	6.9
Store Current(μA)	17.7	29.4	102.6/29.5*	35.1/9.2*	25.2	29.7	32.7/8.8*	33.7/9.1*	**16.5**
Store Energy(fJ/bit)	23.49	47.13	88.45	44.81	247.352	386.9	54.66	91.55	155.7
Restore Latency(ns)	1**	1**	1**	1**	1**	1**	1**	1**	1.3**
Restore Energy(fJ/bit)	2.03	2.15	64.08	20.59	19.04	128.04	50.55	55.44	**11.84**

* SOT current / STT current. ** The ramp-up time of VDD is 1 ns during restore mode

storage nodes enables performance parity with conventional SRAM architectures.

Table II compares the stability of the proposed structure with available literature in terms of hold, read, and write SNM. The stability of the SRAM is strongly correlated with the ratios β and γ. With fixed β and γ across all designs, the proposed structure demonstrates the highest H-SNM and R-SNM, while the W-SNM exceeds 30% of the supply voltage, indicating superior stability. Furthermore, the SNM of the proposed design was simulated under different VDD, with the results shown in Fig. 7(d), confirming that the incorporation of nonvolatile functionality does not compromise SRAM performance.

D. Power Analysis

The comparison of store and restore latency and power consumption between the proposed design and prior work is summarized in Table II. The proposed design consumes 11.84 fJ/bit in restore mode, which is second only to the VGSOT based designs and significantly lower than other compared designs. Furthermore, the VGSOT based designs [2] exhibit a significantly higher RSER compared to the proposed design. Thus, our design achieves an excellent balance between reliability and power consumption. In terms of store power consumption, compared to IMA-MTJ-based NV-SRAM designs without the VCMA effect [12], [17], the store energy of the proposed design is reduced by approximately 1.58× and 2.48×, respectively. Compared to the designs based on VGSOT-MTJ and SOT-STT-MTJ [2], [12], [25], the proposed design enables field-free deterministic switching, which reduces process complexity. Although the inherent long switching time of the IMA device leads to higher store power consumption, the primary energy consumption in NV-SRAM still comes from read and write operations in SRAM mode. Therefore, our design exhibits significantly lower total power consumption compared to other SOT-NV-SRAM. Notably, our design achieves the lowest per-bit store current of merely 16.5 μA among all compared designs. Since the store operation is a highly parallel process, this reduction in current significantly increases the number of cells that can be backed up simultaneously, thereby shortening the overall backup time.

V. Conclusion

In this paper, we have proposed a 10T-2M nonvolatile SRAM cell based on in-plane VGSOT-MTJs. By employing a VGSOT-assisted store mechanism and a pre-charge restore scheme, the structure significantly improves restore reliability while maintaining low power consumption. The store energy is decreased by 1.58× to 2.48× compared to prior IMA-MTJ-based NV-SRAM designs. The pre-charge restore scheme demonstrats excellent read reliability across a wide range of MTJ resistances, achieving a RSER reduction of over 98.7% at $R_{MTJ} = 500$ kΩ compared to conventional dis-charge restore schemes. The proposed design achieves the smallest transistor size, resulting in the lowest read and write power consumption among all compared SOT-NV-SRAM architectures. These advancements make the proposed NV-SRAM as an ideal solution for energy-efficient and highly reliable nonvolatile memory applications in next generation computing systems.

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