

# Architecture, Design and Technology Co-optimization for 3D ICs with Advanced BSPDN Considering Power & Thermal Integrity Impact

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**Abstract**—This paper presents a comprehensive power and thermal integrity analysis of a commercial IP based 7nm 3D CPU with a much larger SRAM area compared to its logic section. We systematically investigate the impact of different 3D stacking architectures—Memory-on-Logic (MoL) and Logic-on-Memory (LoM)—combined with both front-side and back-side power delivery networks (FSPDN/BSPDN). A key contribution is a novel lightweight IR drop modeling tool developed in-house, which enables super fast and highly accurate power integrity estimation at early physical design stages—far before signoff—significantly reducing design iteration time caused by IR violations. This tool also fills a critical gap in commercial EDA support for advanced 3D integration and BSPDN evaluation. Using this tool alongside multi-physics thermal simulations, we compare four 3D design scenarios. Results show that the MoL architecture with BSPDN achieves an optimal balance between power and thermal integrity: it reduces worst-case IR drop in the logic die to just one-fourth of the 2D reference, and lowers peak temperature by over 15 °C compared to a LoM counterpart. Further improvements, 50% in IR drop decrease and 14°C temperature reduction, are attainable through TSV optimization and high-thermal-conductivity material integration. This study provides essential 3D architecture, design and technology cooptimization methodologies for future high-performance 3D CPUs of advanced technology nodes.

**Keywords**—3D Integration, Power Integrity, Thermal Integrity, Backside Power Delivery Network (BSPDN), Memory-on-Logic (MoL), Design-Technology Co-Optimization (DTCO), 7nm Technology Node

## I. INTRODUCTION

Over the past few decades, the semiconductor industry has relied on planar scaling to improve chip performance. However, as transistor dimensions approach physical limits, this method faces significant challenges. The slowdown of Moore's Law has compelled the industry to seek new technological pathways, particularly for artificial intelligence (AI) and high-performance computing (HPC) applications [1]. In this context, three-dimensional integrated circuit (3D IC) technology has emerged as a key direction for the post-Moore era, achieving high-density integration by vertically stacking multiple dies using through-silicon vias (TSVs) [2]. The rise of AI and large models has further spurred the development of full-chip stacking technology [3], creating unprecedented demand for on-chip cache capacity. Static Random-Access Memory (SRAM), a core cache component, directly determines computational efficiency. At nodes below 5 nanometers, scaling logic circuits is generally easier than scaling SRAM [4], prompting designers to explore vertically stacking SRAM and logic (e.g., Memory-on-Logic or Logic-on-Memory) to maximize area utilization and cache capacity.

While 3D IC offers performance and integration advantages, it also introduces severe challenges in Power Integrity (PI) and Thermal Management. To address power delivery challenges, Backside Power Delivery Network (BSPDN) technology has been proposed [5]. Compared to traditional Frontside PDN (FSPDN), BSPDN moves power

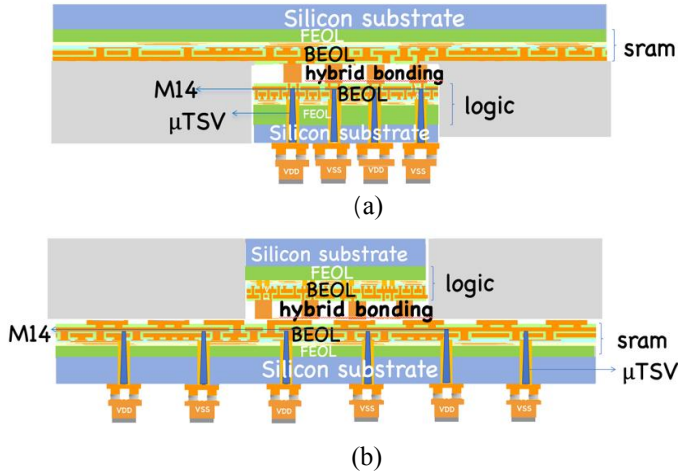


Fig. 1. 3D Memory-on-Logic (MoL) (a) and Logic-on-Memory (LoM) (b) stacking with FSPDN. Hybrid bonding is assumed for 3D integration. The power is delivered to the top die and bottom dies via u-TSV in the top metal layer of the bottom die before reaching hybrid bonding.

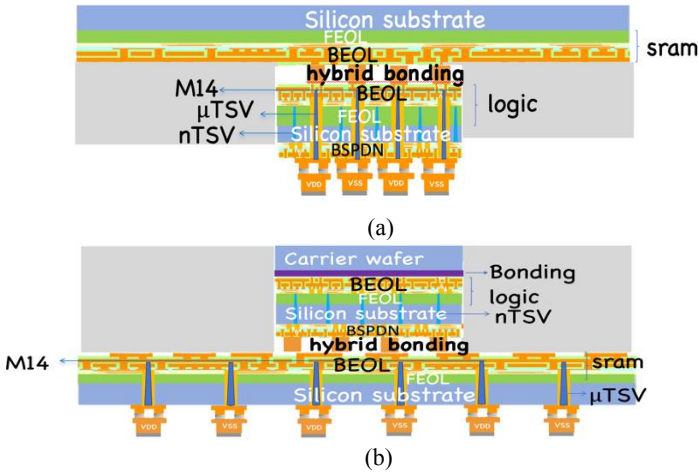


Fig. 2. 3D Memory-on-Logic (MoL) (a) and Logic-on-Memory (LoM) (b) stacking with BSPDN. Hybrid bonding is also assumed for the 3D integration. For the top die, the power is delivered via u-TSV to the top metal layer of the bottom die before reaching hybrid bonding. For bottom die, however, the power is favorably supplied from the BSPDN via buried power rail (BPR).

routing to the wafer backside, freeing frontside routing resources, shortening interconnects, and reducing resistance and power loss. In this work, we for the first time evaluate the power and thermal integrity of a 7nm CPU with SRAM area significantly larger than logic, across various 2D and 3D design configurations. We apply both FSPDN and BSPDN to 3D chips with Logic-on-Memory (LoM) and Memory-on-Logic (MoL) stacking, resulting in four design types (Fig. 1 & 2). Default  $\mu$ TSV counts are 6 for SRAM and 4 for logic dies.

A key contribution is a novel in-house modeling tool based on [6], enabling ultra-fast and accurate power integrity estimation early in physical design—after standard cell placement but well before signoff—significantly reducing iteration time due to IR violations. In contrast, commercial tools like RedHawk require a complete design at signoff, leading to slower cycles. Furthermore, current commercial EDA tools lack dedicated support for 3D power delivery

networks (especially BSPDN) and stacked dies with unequal areas. Our tool addresses this critical gap. To validate accuracy, we designed a 2D control chip and compared IR drop results with commercial tools, confirming precision. For thermal simulation, we used Ansys-based tools [7]. Integrating our tool with thermal simulations, we compared four 3D design scenarios and derived their electrical-thermal performance.

## II. IN-HOUSE IR DROP MODEL

### A. Model Introduction

The core of the model is an abstracted circuit analysis representation of the chip's power delivery network. It is fundamentally constructed from three essential components: current sources, a resistor network, and voltage sources. Specifically:

- Current sources model the dynamic switching currents and leakage currents generated by standard cells or functional modules across the chip.
- The resistor network accurately characterizes the parasitic resistance present in the power delivery metals (e.g., power grids, vias) spanning from the power pads (PADs) to each individual standard cell.
- The voltage sources define the initial supply voltage, such as that provided at the chip's peripheral power pads.

The entire chip grid is discretized into a SPICE-compatible or equivalent circuit netlist. The model then leverages a simulator to solve Kirchhoff's Voltage and Current Laws (KVL/KCL), computing the voltage at each node within the power delivery network. The ultimate objective is to precisely locate and quantify voltage drops (IR Drop) resulting from current flow through the resistive network. This ensures the chip is designed to avoid timing failures or functional errors caused by localized voltage insufficiency.

### B. Model accuracy verification

In order to compare with the results from commercial tools, we designed a 2D control case. The physical design of the 2D chip, an ARM processor with 8Mbit SRAM, is shown in Fig. 3. An "H" type floorplan was applied for symmetry and timing optimization. After placement, we obtained the power density map for the logic section (Fig. 4). The PDN parameters from the physical design are listed in Table. 1.

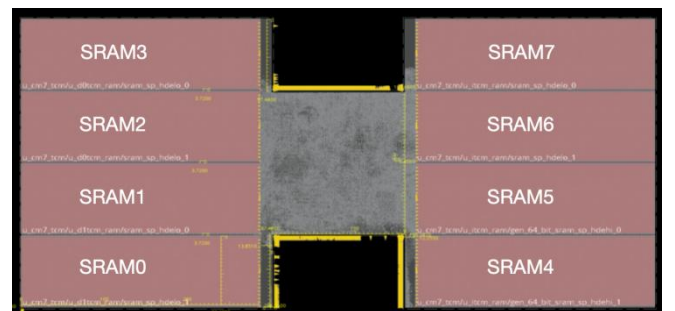


Fig. 3. Floorplan with 8Mb SRAM capacity based on 7nm ARM core design.

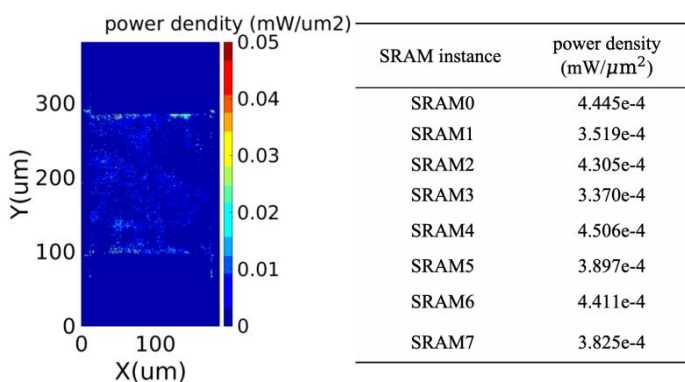


Fig. 4. Obtained power density map for the logic part (left figure) and the eight SRAM macros (right table, assuming uniform power for SRAM and hence average power density is applied for IR drop modelling). The average power density for logic is  $1.81\text{W}/\text{mm}^2$  which is around 5 times the SRAM one.

metal \ value	width(μm)	pitch(μm)	r_line(ohm/μm)	c_line(fF/μm)
metal0	0.06	0.48	16.00	0.2544
metal1	0.068	10.944	10.00	0.2797
metal14	0.5	9.6	0.03288	0.2035
metal15	0.5	10.944	0.03288	0.2035
bpr	0.03	0.48	23.00	0.145
bsmetal1	0.2	4.2	0.91101	0.145
bsmetal2	0.5	3.6	0.06488	0.145
bsmetal3	2.0	20	0.0039	0.145

Table. 1. FSPDN and BSPDN metal layer geometrical and electrical parameters.

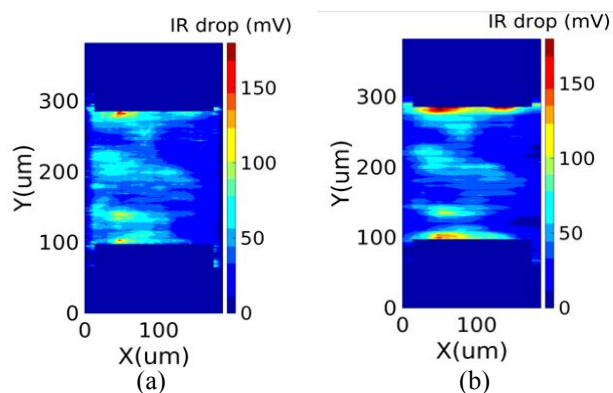


Fig. 5. Logic IR drop results obtained from the Cadence EDA tool (a) and from the in-house model (b).

We performed simulations using both our model and Cadence Voltus, obtaining IR drop results to validate our model's accuracy. **Fig. 5** and **Fig. 6** show the IR drop results from both methods. For more intuitive comparison, the cumulative probability distribution curve of IR drop is plotted in **Fig. 7**.

The figure shows that our PDN model aligns closely with the standard tool, indicating excellent consistency. For smaller IR drop values, our model exhibits a minor deviation, mainly because the standard tool extracts values only at cell grid points. In cell-free regions, data absence or interpolation can cause local distortion, sometimes assessing IR drop as zero, which affects the tool's accuracy. In contrast, our

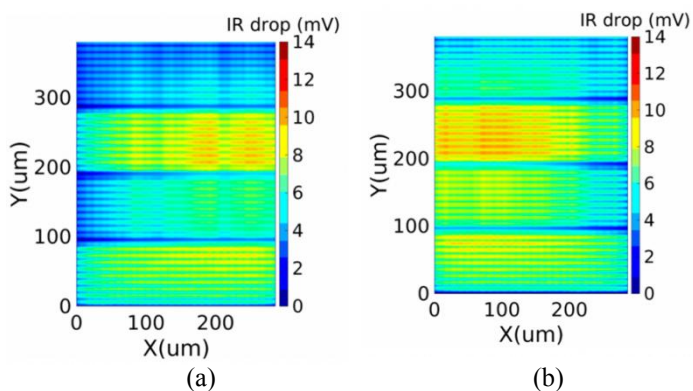


Fig. 6. The applied eight SRAM macros IR drop results in the 2D reference case. (a) shows the SRAM on the left side, (b) shows the SRAM on the right side.

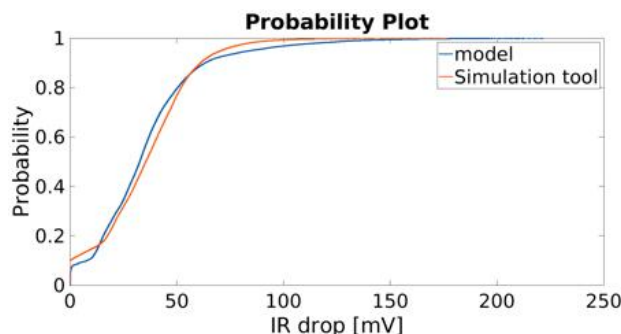


Fig. 7. Cumulative probability distribution curves of IR drop from the model simulation result and that of the commercial EDA tool Cadence Voltus

PDN model uses more comprehensive grid-based modeling, providing a more accurate IR drop distribution.

In the mid-range IR drop values, a slight discrepancy of about 2 – 3 mV exists. This divergence stems primarily from two factors: first, the standard tool incorporates SRAM power characteristics, which may indirectly influence logic IR drop distribution; second, in regions without cell grid points, the tool may use interpolation or approximation due to lack of direct data, causing local distortions.

Nonetheless, both methods maintain high overall consistency in trends, validating the reliability of our PDN model for IR drop analysis.

### C. IR drop simulation for 3D design

Based on the calibrated 2D model, the results of the 3D model can provide predictive support for 3D physical design. The target chip floorplan for the 3D design is illustrated in **Fig. 1** and **Fig. 2**.

The 3D design partitions the Logic module and the Static Random-Access Memory (SRAM) module into two separate layers. In **Fig. 1(a)** and **Fig. 2(a)**, the Logic part is located on the lower die, whereas in **Fig. 1(b)** and **Fig. 2(b)**, it is placed on the upper die. Concurrently, the floorplan of the Logic section is modified to a rectangular shape. In configurations **Fig. 1(a)(b)** and **Fig. 2(a)**, the dies adopt a Face-to-Face (F2F) structure, interconnected at the top level of the BEOL through hybrid bonding to facilitate power delivery. In contrast, configuration **Fig. 2(b)** utilizes a Face-to-Back structure, where the BEOL of the bottom die is connected to the Backside Metal layer of the top die via hybrid bonding[8].

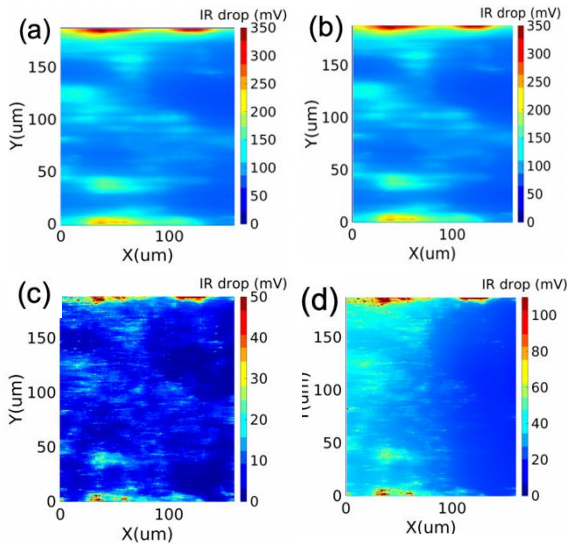


Fig. 8. IR drop heat map for the four different die stacking and PDN structures. (a) (b) (c) (d) are MoL-FSPDN, LoM-FSPDN, MoL-BSPDN, LoM-BSPDN combinations correspondingly.

Design\IR drop(mV)	Average	98% Percentile	Worst
2D logic	35.72	95.24	221.25
2D left SRAM	8.15	10.47	10.97
2D right SRAM	8.70	10.80	11.28
3D FSPDN MoL logic/SRAM	104.81/59.36	220.22/62.71	369.63/63.30
3D FSPDN LoM logic/SRAM	103.12/56.46	217.15/59.78	366.92/60.35
3D BSPDN MoL logic/SRAM	7.40/59.36	25.36/62.71	93.91/63.30
3D BSPDN LoM logic/SRAM	88.24/56.46	96.67/59.78	154.89/60.35

Tab. 2. Displayed the IR drop values for the 2D and 3D CPUs of various PDN and stacking structures.

In all four cases, power is supplied from the backside of the bottom die, delivered through  $\mu$ TSVs that penetrate the substrate and connect to the M14 layer of the bottom die.

For all four 3D designs, we maintained consistent PDN fundamental parameters (as listed in **Table. 1**), and the input power density map for the logic section was derived from the 2D physical design. A significantly smaller IR drop is observed in the SRAM part compared with the logic counterpart. Hence, in the 3D stacking design, the optimization focus for IR drop is on the logic part by applying the BSPDN to it, while the FSPDN is applied to the SRAM design. Consequently, we will pay greater attention to the IR drop results of the logic part. We further extended the model to our 3D structural designs, and the corresponding IR drop results are presented in **Fig. 8** and **Table. 2**, respectively.

### III. THERMAL EVALUATION FRAMEWORK

#### A. 2D chip thermal model

For chip thermal performance assessment, we employed Finite Element Analysis (FEA) for thermal simulations. It is

widely recognized that full-chip thermal modeling, particularly for large-scale designs, demands substantial time and computational resources. To address this challenge, we adopted a simplified yet accurate modeling approach: The multilayer complex structure (including BEOL, BSPDN, and substrate with nano Through-Silicon Vias (nTSV) and Buried Power Rail) was abstracted by assigning each layer an effective anisotropic thermal conductivity defined as  $[K_{xx}, K_{yy}, K_{zz}]$ . The thermal conductivity components for each layer were derived from Fourier's Law.

To evaluate the thermal resistance of BEOL structures in the x, y, and z directions, we first established a 2D local thermal evaluation model for the chip. As illustrated in **Fig.9(a)**, a  $3\mu\text{m} \times 3\mu\text{m}$  BEOL structure was modeled in the local thermal evaluation framework. The thermal conductivity data for each metal wire and via layer were configured based on the experimental and modeling studies by Lofrano et al. [9]. This work systematically validated the thermal conductivity characteristics of copper interconnects at nanoscale dimensions through experimental measurements coupled with 3D finite element modeling, providing critical reference data for nanoscale copper interconnects.

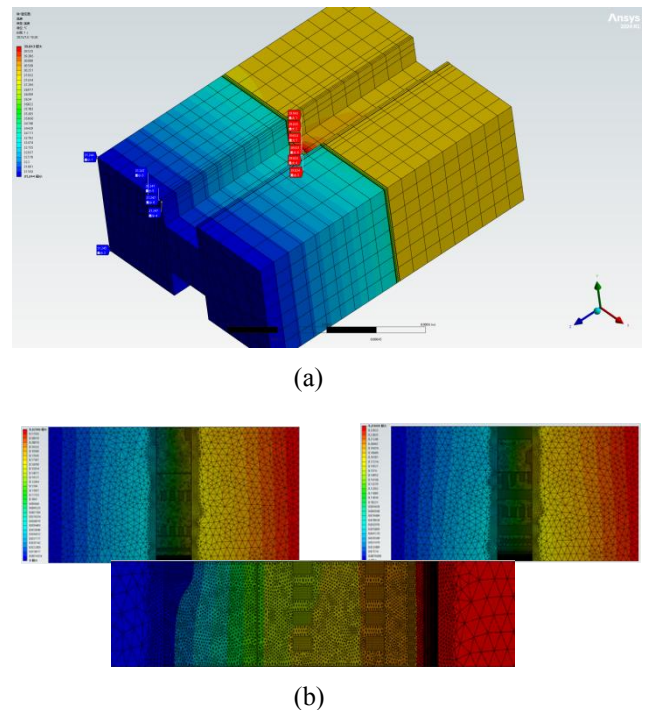


Fig. 9. The built thermal global model (a) and local models (b) for the 2D reference design.

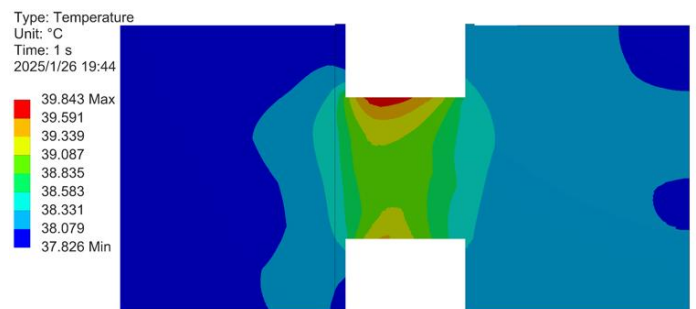


Fig. 10. Simulated temperature distribution in the 2D design FEOL.

Subsequently, we developed a 2D global thermal model for the chip. As shown in **Fig. 9(b)**, this model integrated equivalent thermal conductivity parameters obtained from the local evaluation model. By preserving primary heat conduction paths and adopting a hierarchical parameterization approach, the global thermal evaluation model structure was simplified to accelerate computational efficiency.

The temperature distribution results for the reference 2D design are presented in **Fig. 10**.

### B. 3D chip thermal model

Based on the calibrated 2D model, we meticulously extended it to the four distinct 3D structures incorporating either FSPDN or BSPDN as detailed in **Fig. 1** and **Fig. 2** [10]. For each 3D configuration, corresponding local thermal evaluation models were developed to determine thermal conductivity parameters of metal interconnects and vias, enabling global thermal model construction. The introduction of TSV structures in 3D stacking necessitated recalibration of thermal parameters. Spatially distributed heat flux derived from power maps was applied to the FEOL layer surfaces of logic modules. Thermal boundary conditions included: bottom surface with equivalent heat transfer coefficient of  $20 \text{ W/m}^2\cdot\text{K}$  [11] simulating package thermal resistance, and lateral surfaces with a convection coefficient of  $20 \text{ W/m}^2\cdot\text{K}$ ; top surface with forced convection coefficient of  $80,000 \text{ W/m}^2\cdot\text{K}$  [12] emulating direct liquid cooling; and ambient temperature maintained at  $22^\circ\text{C}$ .

Temperature distribution results for the 3D designs are presented in **Fig. 11** and **Table. 3**, quantitatively characterizing thermal behavior across configurations.

## IV. RESULTS AND ANALYSIS

### A. Analysis of IR drop results

**Table. 2** summarizes the IR drop data for 2D and 3D CPUs across various PDN and stacking architectures. This study focuses on the 98th percentile values to objectively evaluate IR drop performance. The results show that the 3D BSPDN architecture, particularly in the Memory-on-Logic (MoL) configuration, offers significant advantages in IR drop control.

Compared to the conventional 2D benchmark (98th percentile:  $95.24 \text{ mV}$ ), BSPDN-MoL reduces the logic IR drop to  $25.36 \text{ mV}$ —only about 26.6% of the 2D value, corresponding to an improvement of over three-quarters. Against the 3D FSPDN logic part ( $220.22 \text{ mV}$ ), BSPDN-MoL lowers the 98th percentile to just 11.5%, achieving nearly an order-of-magnitude improvement.

Even in the Logic-on-Memory (LoM) configuration, BSPDN reduces logic IR drop to  $96.67 \text{ mV}$ , which is significantly lower than all FSPDN schemes ( $\sim 217 \text{ mV}$ ) at only 44.5% of the latter, and still outperforms the 2D design. Meanwhile, SRAM IR drop under BSPDN remains stable across configurations, with 98th percentile values around  $60 \text{ mV}$ , comparable to FSPDN schemes. To mitigate the increased IR drop in stacked memory dies, increasing  $\mu\text{TSV}$  density proves effective—experimental data indicate that quadrupling  $\mu\text{TSV}$  count can reduce SRAM IR drop by 50%, as detailed in Section C.

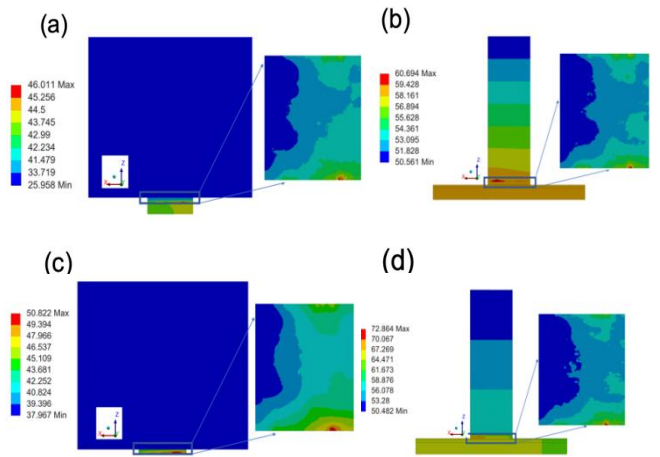


Fig. 11. Thermal heat maps for the four different die stacking and PDN structures. (a) (b) (c) (d) are MoL-FSPDN, LoM-FSPDN, MoL-BSPDN, LoM-BSPDN combinations correspondingly.

Design	Average Temperature( $^\circ\text{C}$ )	Worst Temperature( $^\circ\text{C}$ )
2D logic	38.191	39.843
3D FSPDN MoL	43.321	46.001
3D FSPDN LoM	58.742	60.694
3D BSPDN MoL	41.464	50.822
3D BSPDN LoM	64.535	72.864

Tab. 3. The temperature results for the 2D and 3D CPUs of various PDN and stacking structures are presented in the table above.

In summary, the BSPDN-MoL architecture demonstrates exceptional IR drop control, reducing voltage drop to a fraction of conventional 2D and 3D FSPDN schemes, thereby offering an excellent power integrity solution for high-density 3D integrated systems.

### B. Thermal result analysis

The IR drop data for both 2D and 3D CPUs under various PDNs and stacking architectures are summarized in **Table. 3**. In the case of Memory-on-Logic (MoL) stacking, the top die exhibits a larger heat dissipation area, resulting in a notable reduction of over  $15^\circ\text{C}$  in the maximum temperature of the logic chip, as clearly shown in **Fig. 11**. Compared to the FSPDN, the MoL configuration with BSPDN shows an approximately  $4^\circ\text{C}$  higher temperature. This elevated temperature in BSPDN is attributed to substrate thinning and the BEOL layers acting as a thermal block.

### C. Power and Thermal DTCO

Based on the above analysis and comparison, it is concluded that for the studied CPU design with a significantly larger SRAM die area compared to the logic die area, the MoL configuration with BSPDN represents the optimal choice when considering both power delivery and thermal integrity. To further improve the IR drop in the SRAM die—since BSPDN is not applied to the SRAM—increasing the number of power-delivery TSVs is of critical importance. Therefore, taking the 3D FSPDN MoL configuration (**Fig. 1(a)**) as an example, we attempted to

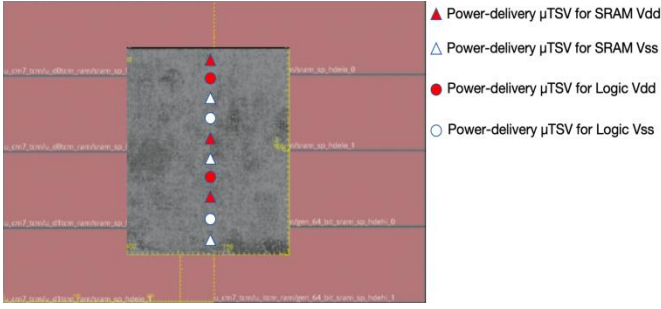


Fig. 12. Distribution diagram of 10 TSVs

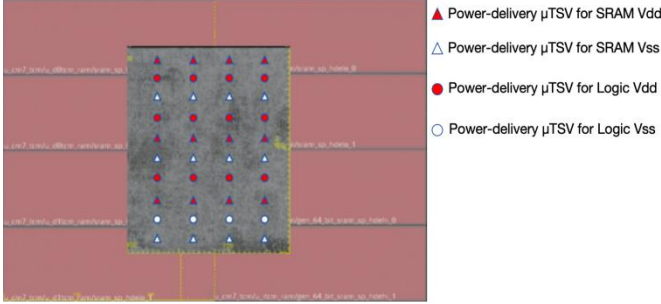


Fig. 13. Distribution diagram of 40 TSVs

increase the number of TSVs and re-evaluated its performance. Compared to the baseline case with 10 TSVs (layout shown in **Fig. 12**), a total of 40 TSVs—20 for Logic (10 for VDD and 10 for VSS) and 20 for SRAM (10 for VDD and 10 for VSS)—were deployed in the layout illustrated in **Fig. 13**. The IR drop simulation results for the SRAM die are presented in **Fig. 14**. The simulations demonstrate that increasing the number of  $\mu$ TSVs can significantly reduce the IR drop. Quadrupling the number of  $\mu$ TSVs reduces the IR drop in the SRAM by 50%. Furthermore, it is observed that due to the central placement of the TSVs, regions closer to the TSVs exhibit relatively lower IR drop owing to shorter power delivery paths, whereas peripheral regions show higher IR drop as a result of longer current paths. Consequently, the IR drop distribution exhibits a distinct pattern—lower in the center and higher at the edges. In terms of thermal simulation, to further reduce the temperature of the logic die in the BSPDN-based MoL configuration, the use of highly thermally conductive materials that also provide electrical isolation would be highly beneficial. For instance, by adopting dummy silicon instead of the thermally isolating conditions assumed previously, the logic die temperature can also be significantly reduced by approximately 14°C.

## V. CONCLUSION

This paper presents a comprehensive study of 3D CPU architectures for designs with larger SRAM die area than logic die, evaluating Memory-on-Logic (MoL) and Logic-on-Memory (LoM) stacking with both Frontside and Backside Power Delivery Networks (FSPDN/BSPDN). A key contribution is an in-house, lightweight IR drop modeling tool, which enables high-accuracy, early-stage

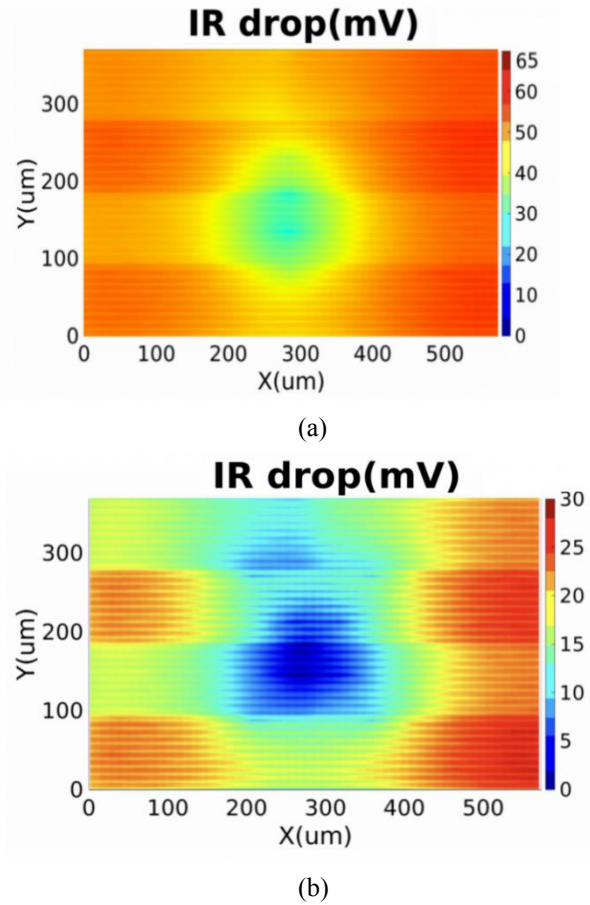


Fig. 14. SRAM macro IR drop results for different numbers of TSVs. (a) presented the results of 10 TSVs, (b) presented the results of 40 TSVs.

power integrity analysis and addresses a critical gap in commercial EDA support for 3D and BSPDN evaluation.

Through architecture, design, and technology co-optimization (DTCO), we demonstrate that the MoL stacking structure with BSPDN achieves the optimal balance between power and thermal integrity. This configuration reduces the worst-case IR drop in the logic die to one-fourth of the 2D reference and lowers peak temperature by over 15 °C compared to the LoM counterpart. Further DTCO measures — quadrupling  $\mu$  TSV count and using high-thermal-conductivity die fill — yield an additional 50% SRAM IR drop reduction and a 14 °C logic temperature decrease.

In summary, this work provides essential methodologies for 3D co-optimization. The findings and analysis framework offer a valuable guide for designing future high-performance 3D CPUs at advanced nodes, where managing power and thermal integrity is critical.

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