

High-Performance and High-Density NAND-Like SOT-MRAM for FinFET Technology Nodes

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Abstract—This paper proposes a comprehensive optimization framework for NAND-like spintronics memory (NAND-SPIN) in advanced FinFET technology nodes. At bit-cell structure level, we propose a NAND-SPIN-GND design which is configured with a grounded bit line (BL) to minimize the parasitic resistance in both read and write paths, thereby decreasing read latency by 35.0% and write energy by 27.3%. At device and layout level, a short-circuiting bottom electrode (SBE) design is proposed, which shorts non-contributing spin-orbit torque (SOT) segments by the BEs, reducing read latency by up to 41.4% and write energy by 55.8%. In addition, a compact capacitance symmetric source line (SL)-type reference scheme is introduced to address the inherent capacitance asymmetry in conventional SL-type reference scheme, resulting in a 48.6% reduction in read latency compared to the conventional word line (WL)-type reference scheme.

Index Terms—NAND-SPIN, STT-MRAM, SOT-MRAM, bit-cell, high performance, high density.

I. INTRODUCTION

Recently, NAND-like spintronics memory (NAND-SPIN) has been presented to address the write asymmetry inherent in spin-transfer torque magnetic random-access memory (STT-MRAM) by integrating efficient spin-orbit torque (SOT) erase with STT program operations to enable high-density and low-power memory [1]–[7]. However, as the fabrication process continues to scale down, particularly toward the FinFET technology node, increased parasitic effects lead to significant performance degradation in NAND-SPIN [8], [9]. To mitigate these issues, we propose a systematic optimization approach covering bit-cell and array design, device and layout optimization, as well as sensing and reference schemes.

II. HIGH-PERFORMANCE NAND-SPIN DESIGN

A. NAND-SPIN-GND bit-cell design

NAND-SPIN integrates multiple MTJs on a single SOT layer for reducing transistors as shown in Fig. 1(a). The SOT current first erases all MTJs to the anti-parallel (AP) state, and then the STT current programs selected MTJs to the parallel (P) state [3]. Both currents flow from SL to BL, mitigating degeneration effects and lowering write voltage requirements. Fully leveraging this, the SL read mode is adopted [10], and hence the BL remains at a low potential. Therefore, we further propose a novel NAND-SPIN-GND structure (Fig. 1(b)), in which multiple BLs share a single GND line connected to the global GND grid, greatly reducing BL parasitic resistance, and eliminates the BL control switches and drivers.

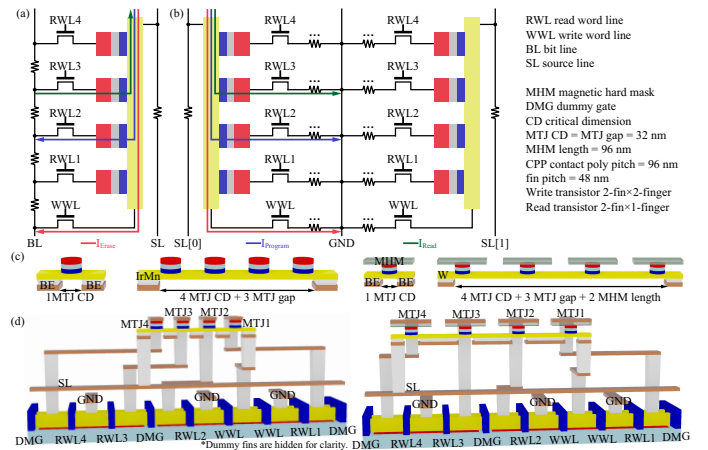


Fig. 1. Schematics of (a) conventional and (b) proposed NAND-SPIN structures. (c) Device layout of standard SOT-MRAM and NAND-SPIN. (d) 3D layout of NAND-SPIN-GND structure with SBE design.

B. SBE layout design

Two mainstream SOT material IrMn and W for NAND-SPIN are considered. The SOT erase requires assistance of magnetic field [2]. The IrMn can intrinsically provide exchange bias, while W has a superior spin Hall angle and resistivity, but necessitates the MHM to generate the field [11]–[13]. For IrMn-based NAND-SPIN with 5-transistor-4-MTJ (5T4J) cell structure, SOT length includes 4 MTJs and 3 gaps, 7 times that of single MTJ, and the situation is further exacerbated for W, while the MHM increases SOT length to 13 times as shown in Fig. 1(c) [14]–[16]. Therefore, a short-circuiting bottom electrode (SBE) layout design is proposed to introduce BEs beneath the gaps, as shown in Fig. 1(d), and reduce SOT resistance by 42.9% and 69.2% for IrMn and W, respectively. It not only enhances the performance but also alleviates the constraints on the number of MTJs integrated on SOT layer.

C. Symmetric SL-type reference scheme

The mainstream reference schemes are SL and WL types [10], [17]–[19]. The WL-type scheme has lower hardware overhead, but this advantage is diminished in NAND-SPIN because a complete NAND-SPIN reference row (4 or 8 data rows) must be configured [20]. Moreover, its drawback of fixed reference location becomes pronounced under FinFET process

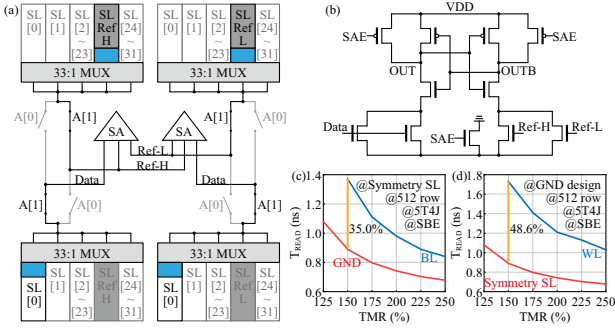


Fig. 2. (a) The proposed capacitance symmetric SL-type reference scheme and (b) the adopted SA [21]. Read latency comparisons for different (c) NAND-SPIN structures and (d) reference schemes.

TABLE I
PARAMETERS UTILIZED IN THE SIMULATIONS

Symbol	Parameter	Value	Unit
-	MTJ/SOT CD	32	nm
-	Free layer thickness	1	nm
-	SOT thickness (IrMn/W)	3 [22]/4.5 [12]	nm
ρ_{SOT}	SOT track resistivity (IrMn/W)	278 [22]/80 [12]	$\mu\Omega\cdot\text{cm}$
θ_{SH}	Spin Hall angle (IrMn/W)	0.25 [22]/0.6 [12]	-
P	Spin polarization	0.62	-
C_P	STT asymmetric factor	0.28 [23]	-
α	Damping constant	0.02	-
M_S	Saturation magnetization	1×10^6	A/m
B_x	Amplitude of magnetic field	20	mT
H_K	Effective anisotropy field	2.64×10^5	A/m
RA	Resistance area product	5 [3]	$\Omega \cdot \mu\text{m}^2$
$TMR(0)$	TMR with zero voltage bias	150%	-
-	Parasitic resistance	31.68 [24]	$\Omega/\mu\text{m}$
-	Parasitic capacitance	0.28 [24]	fF/ μm

technology. In contrast, the SL-type reference scheme incurs no additional hardware overhead when applied to NAND-SPIN, as the data and reference cells own equal location, thereby achieving higher read reliability. The proposed capacitance symmetric SL scheme with two sub-arrays further addresses the mismatch between the data and reference branches as shown in Fig. 2. When the lower sub-array is accessed, the selected SL and MUXs are pre-charged and dis-charged to generate the data signal. Simultaneously, two reference cells at equal location in the upper sub-array are activated to produce high and low reference signals. Both the data and reference inputs of the sense amplifier (SA) load the same number of MUXs, achieving near-ideal capacitance symmetry. The proposed design introduces almost no additional area overhead and significantly outperforms previous more complex approach [19].

III. SIMULATION AND DISCUSSION

The performance simulation is conducted under the 14 nm FinFET node ($V_{DD} = 0.8V$), with critical device parameters provided in Table I. A variation-aware evaluation approach is adopted, with the relative standard deviation of MTJ resistance and critical current set to 5% (1σ). Read voltage is 0.4 V and the standard deviation of SA offset voltage is 5 mV [10]. All results are obtained from 10000 Monte Carlo simulations, with the cell failure probability (P_{FC}) upper-bounded at 4×10^{-6} . The NAND-SPIN cell and array size are set to 5T4J and 512 rows by default, and the 256-row configuration is also considered since some designs cannot meet the requirements.

As shown in Fig. 2(c), compared with the conventional NAND-SPIN retaining the BL, the proposed NAND-SPIN-

TABLE II
PERFORMANCE COMPARISON

Memory Type	STT MRAM [8] ^a	SOT MRAM [16] ^{ab}	NAND SPIN BL [3]	NAND SPIN GND	NAND SPIN GND	NAND SPIN GND	NAND SPIN GND	NAND SPIN GND
Cell structure	1T1J	2T1J	5T4J	5T4J	9T8J	5T4J	5T4J	5T4J
SOT material	-	W	W	W	W	IrMn	IrMn	W
BE layout	-	-	SBE	SBE	SBE	OBE	SBE	OBE
Bit-cell area ($\mu\text{m}^2/\text{bit}$)	0.0207	0.0414	0.0276	0.0276	0.0242	0.0276	0.0276	0.0276
	1 \times	2 \times	1.33 \times	1.33 \times	1.17 \times	1.33 \times	1.33 \times	1.33 \times
T_{WRITE}	5 ns	1 ns	SOT erase 1 ns, STT program 5 ns					
E_{WRITE} (fJ/bit)	512	437.1	225.6	183.6	133.4	111.0	251.1	152.1
	256	370.8	140.8	132.8	110.4	97.5	249.8	122.3
T_{READ} (ns)	512	0.92	1.08 ^c	1.37	0.89	0.89	1.52	1.07
	256	0.74	0.87	0.86	0.74	0.76	1.15	0.83
E_{READ} (fJ/bit)	512	25.5	25.5	31.9	31.9	27.9	31.9	31.9
	256	17.5	17.5	20.7	20.7	18.7	20.7	20.7

^aTransistors are 2-fin \times 1-finger with 3-fin pitch \times 1.5 CPP on area [8].

^b1WL2BL design is adopted for high read performance [16].

^cCannot meet the yield requirement under this configuration.

^dAdopt the proposed symmetric SL-type reference scheme.

^eAdopt the BL read mode for avoiding shunt current issue [25].

GND design can reduce the read latency by 35.0%. As shown in Fig. 2(d), the proposed symmetric SL-type reference scheme achieves a 48.6% reduction in latency compared to the conventional WL-type one [18]. The SBE layout design also reduces the read-path resistance, specifically, the W-based NAND-SPIN with the SBE layout shows a 41.4% reduction in latency compared to the IrMn-based NAND-SPIN with the conventional open-circuit BE (OBE) layout.

The NAND-SPIN-GND structure and SBE layout significantly reduce the write-path resistance. As shown in Table II, the NAND-SPIN-GND design lowers write energy by 27.3%. The IrMn-OBE design fails to achieve reliable write operations in a 512-row configuration, in comparison, under a 256-row configuration, the W-SBE design reduces write energy by 55.8%. The W-SBE NAND-SPIN enables a more compact 9T8J structure that, despite requiring a higher write voltage, achieves superior overall write energy efficiency thanks to the inherent SOT erase power-sharing characteristic of NAND-SPIN.

IV. CONCLUSION

This paper presents a comprehensive optimization framework for NAND-SPIN targeting advanced FinFET technology nodes. The proposed NAND-SPIN-GND architecture eliminates the parasitic resistance of the BL. Furthermore, the proposed SBE layout design significantly reduces the resistance of the SOT layer. Notably, W-based NAND-SPIN-GND with SBE enables a compact 9T8J configuration while maintaining excellent performance. Finally, the proposed symmetric SL-type reference scheme addresses both capacitance imbalance and parasitic resistance mismatch with minimal circuit overhead. In summary, the proposed optimization framework substantially enhances the speed, energy, and scalability of NAND-SPIN, positioning it as a promising candidate for future high-density, low-power memory in deeply scaled process nodes.

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