

SFQ-Based CJoin Gate Implementation for Ultra-Low-Power Brownian Logic Circuits

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Abstract—The increasing energy consumption of data centers has highlighted the urgent need for ultra-low-power computing solutions. Single Flux Quantum (SFQ) circuits, which utilize superconducting Josephson junctions, offer promising advantages in terms of speed and energy efficiency; however, their power consumption has been limited by the need for noise suppression mechanisms. To address this, we propose the practical SFQ Brownian Logic Circuits (SBLCs), which exploit thermal noise for stochastic signal propagation, significantly reducing static power consumption. Especially, we address the three challenges: susceptibility to manufacturing variations, the absence of an actual CJoin gate implementation, which is essential for processing, and a lack of demonstrated practical advantages. This paper evaluates the robustness of SBLCs to manufacturing variations, proposes the first SFQ-based CJoin gate implementation, and demonstrates a Ripple Carry Adder (RCA) with a 3167x improvement in energy efficiency compared to traditional SFQ and CMOS circuits, confirming the superiority of SBLCs for future computing systems.

Index Terms—single flux quantum, superconducting circuits, Brownian circuits, ultra-low-power computing

I. INTRODUCTION

In recent years, the demand for large-scale computing has increased significantly with the advancement of deep learning. According to projections released by the International Energy Agency (IEA), the electricity consumption of data centers is expected to reach approximately 945 TWh by 2030, effectively doubling from the 2024 level [1]. Consequently, while reducing power consumption and enhancing performance in large-scale computing systems have become critical demands, achieving these goals through conventional scaling strategies has proven challenging. To address this issue, extensive research efforts have been directed toward novel device technologies as potential solutions.

Single Flux Quantum (SFQ) circuits [2], leveraging superconducting Josephson junctions (JJs), have emerged as a promising alternative to CMOS technology due to their inherently high operating speeds and low energy consumption [3]–[12]. Despite these advantages, current SFQ technologies still allocate over 90% of their total power consumption to static energy required for noise suppression mechanisms. This critical analysis reveals that transcending traditional noise

suppression paradigms is an essential prerequisite for realizing next-generation ultra-low-power computing systems that are unconstrained by current thermodynamic limitations.

To this end, a class of logic circuits called SFQ Brownian Logic Circuits (SBLCs), which utilize thermal noise for stochastic signal propagation, has been proposed [13]. Unlike conventional SFQ circuits that suppress noise, SBLCs are designed to operate with noise aggressively, enabling ultra-low-power computing by leveraging stochastic dynamics. In particular, the low-loss nature of SFQ circuits, where the intrinsic noise level and switching drive are comparable, makes it suitable to physically implement such noise-driven concepts. Inspired by Brownian circuit (BC) concepts, SBLCs significantly reduce static power and eliminate the need for bias currents traditionally used for noise mitigation.

However, SBLCs are still in early conceptual development stages, facing critical design challenges. First, SBLCs fundamentally rely on the ideal random walk of signals for computation, yet manufacturing variations in SFQ circuits inevitably result in critical current (I_c) variations, potentially disrupting uniform signal propagation probabilities. This poses a significant threat to the foundational integrity of the computational concept. Second, a concrete SFQ implementation of the reversible CJoin gate, which is central to the computational principle, has not yet been realized. Moving SBLCs beyond theoretical computational principles necessitates the development of such fundamental gates. Third, it is essential to demonstrate the advantages of SBLCs through arithmetic circuits clearly. This validation step is crucial to confirm the feasibility and practical benefits of SBLC-based systems.

The contributions of this paper directly address these challenges and are summarized as follows:

- We evaluate the robustness of SBLCs against manufacturing variations, explicitly focusing on the impact of I_c variations, thereby confirming their stable operational feasibility.
- We propose the first practical SFQ-based implementation of the CJoin gate, enabling basic computational functionality crucial for SBLCs.
- We demonstrate the practical applicability and advantages of SBLCs through a detailed case study of a Ripple Carry Adder (RCA). Our results show that SBLC-based RCA significantly outperforms traditional SFQ implementations in terms of energy reduction (3167x).

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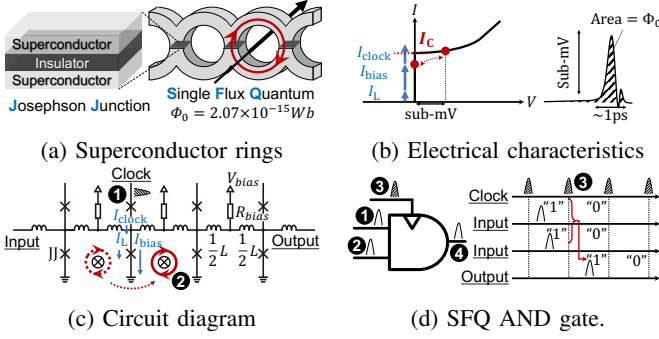


Fig. 1: SFQ fundamentals: device and logic gates.

II. BACKGROUNDS AND LIMITATIONS

A. Basic SFQ Devices and Circuits

As shown in Fig. 1(a), SFQ devices consist of superconducting loops with JJs, where quantized magnetic flux quanta act as logic signals: presence denotes “1” and absence “0”. The electrical characteristics of JJs are illustrated in Fig. 1(b). When the current exceeds the I_c , the junction switches, producing a voltage pulse (sub-mV) that generates single flux quantum ($\Phi_0 = 2.07 \times 10^{-15} Wb$), enabling SFQ transfer through the circuit.

In conventional SFQ circuits, JJs carry three types of current. The first is the circulating current (I_L) induced when an SFQ resides in the superconducting loop. Its magnitude is approximately $I_L \approx \Phi_0/L$, where L is the loop inductance and Φ_0 is the flux quantum. The second is the bias current (I_{bias}), an external supply that drives JJ switching. To reduce the influence of noise, SFQ circuits raise I_c , thereby increasing the energy barrier for SFQ transfer. The third is the clock current (I_{clock}), which triggers JJ switching at a desired timing. In the D flip-flop (Fig. 1(c)), output SFQ pulse (2) is generated only when a clock pulse (1) is applied. In SFQ circuits, gates are synchronized by clock pulses. For instance, in the AND gate (Fig. 1(d)), inputs (1 and 2) produce an output (4) only after the clock pulse (3) arrives. Consequently, the combined currents I_L , I_{bias} , and I_{clock} must be engineered to exceed I_c to enable controlled switching with noise immunity.

Bias current energy injection is also needed during SFQ duplication at branching points, where signal paths either split or merge. As shown in Fig. 2, a single input SFQ pulse duplicates into two outputs (a), while two input pulses merge into one output (b). Without bias current, the total energy of duplicated SFQ pulses cannot exceed that of the original. Thus, the energy of two output pulses is divided from the single input pulse. The external energy supplied by the bias current is required to maintain thermodynamic consistency during duplication.

SFQ devices operate at higher frequencies and consume significantly less power than CMOS circuits. Their power consumption includes static power from bias current and dynamic power from JJ switching, as expressed in Eq. (1).

$$P_{total} = (V_{bias} I_{bias} \times N_{JJ}) + (I_c \Phi_0 \times N_{activeJJ/s}) \quad (1)$$

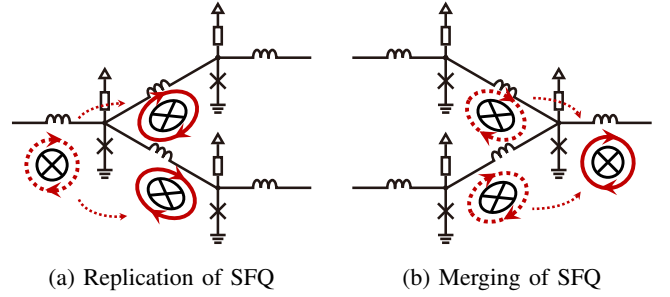


Fig. 2: Replication and Merging of SFQ

where the first term on the right-hand side is static power, and the second term is dynamic power. In static power, V_{bias} and I_{bias} are the bias voltage and current, respectively, and N_{JJ} is the number of JJs in the circuit. In SFQ circuits, bias current is continuously supplied to the JJ (Fig. 1(c)) and consumes power even when the JJ does not switch. Dynamic power is consumed only during JJ switching; otherwise, JJs remain in the zero-voltage state (Fig. 1(b)) and no energy is used. When the JJ switches, the current exceeds I_c and generates an SFQ pulse, leading to dynamic power consumption. $N_{activeJJ/s}$ is the number of activated JJs per second in the target circuit.

Further power reduction in conventional SFQ circuits is fundamentally limited since about 95% of total consumption is static power, mainly due to bias currents needed for operation and noise suppression, as observed in SFQ processors and AI accelerators [3], [4], [9]. Additionally, about 25% of the total JJ count (N_{JJ}) in these circuits is dedicated solely to clock signal routing [9], which further contributes to increased power consumption. From another perspective, the dynamic power consumption in SFQ circuits scales proportionally with the I_c as shown in Eq. (1). A relatively high I_c (around 100 μA) is typically needed for reliable switching against noise, as demonstrated in arithmetic circuits [5], [6], processors [7], [8], [10] and systems [9], [11], [12], where a sufficiently high I_c was essential to ensure accurate operation. Therefore, although bias currents and high I_c are essential for precise operation, they fundamentally limit power reduction, posing challenges for ultra-low-power SFQ computing.

B. SFQ Brownian Logic Circuits

BC is a theoretical computing model where computation arises from stochastic exploration of a circuit by indivisible tokens representing states [14]. Unlike traditional approaches, BC leverages variability and noise as computational resources, avoiding power use to suppress thermal noise. This makes BC promising for overcoming conventional noise limits. Since signal propagation in BC is stochastic and direction-independent, conventional deterministic operators do not apply. Universality is achieved with a small set of primitives (Hub, CJoin, Ratchet) and their connections [15]. Fig. 3(a)-(c) shows gates, while Fig. 3(d) illustrates tokens randomly moving along the line.

Hub gate: A three-terminal reversible junction where all terminals act as bidirectional ports in Fig. 3(a). When a token enters one port, it exits randomly from one of the other two, serving as a probabilistic splitter/merger to guide tokens during

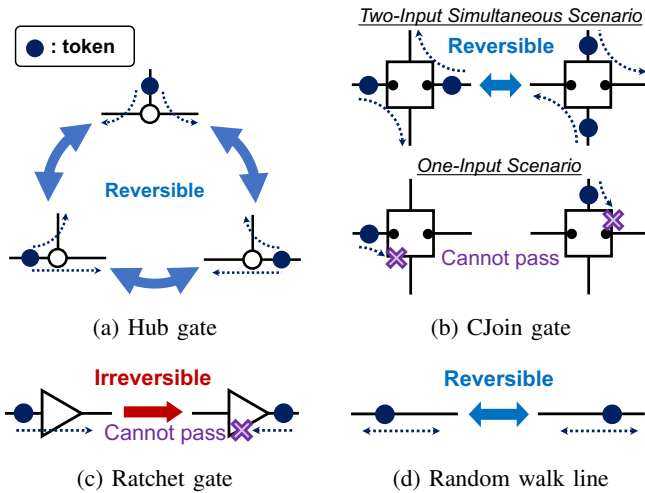


Fig. 3: Symbols for BC Universal gate set

computation. It acts as a three-way intersection for random-walking tokens.

CJoin gate: A four-terminal reversible element composed of two cooperating lines in Fig. 3(b). It transmits only when each input line carries one token, allowing both tokens to proceed together on the merged line. If only one token is present, it diffuses until the other arrives, so no signal passes. Encodes coincidence needed to form minterms and to realize logic by random walks. It is a “meet” point: progress occurs only when two tokens arrive as a pair; otherwise, nothing passes.

Ratchet gate: A two-terminal irreversible element that introduces directionality in Fig. 3(c). Allows tokens to move forward but blocks backward motion, preserving their number. It prevents backflow and speeds convergence, functioning like a valve. In practice, attaching Ratchets to output ports traps tokens once the correct result is reached.

All primitives conserve the number of tokens; Hub and CJoin are reversible, while Ratchet deliberately introduces directionality without creating or annihilating tokens.

SFQ devices align well with BC for two main reasons. First, an SFQ pulse naturally serves as a token. Second, thermal noise perturbs the switching current that governs SFQ transfer, rather than the quantized area of the pulse itself. By reducing the I_c toward the noise scale and minimizing the JJ switching energy, one may dispense with static bias and instead harness noise to drive stochastic operations. In fact, simulation results demonstrate that probabilistic signal transmission of SFQ in the random walk line is feasible by designing the superconducting ring so that it reaches I_c only through noise and I_L [13].

However, despite this conceptual compatibility, the present state of BC remains largely theoretical. Prior SFQ work [13] examines only the random-walk substrate, that is, stochastic token motion, without realizing the BC universal primitives (Hub/CJoin/Ratchet) or their interconnection semantics in SFQ. As a result, essential building blocks required for a complete SFQ instantiation of BC are still missing.

Accordingly, SBLCs remain at an early stage and face

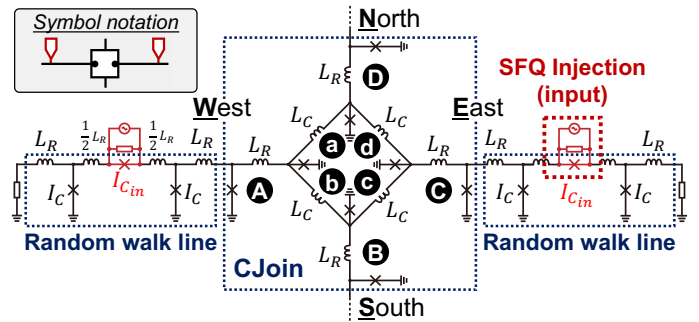


Fig. 4: Proposed circuit schematic of SFQ CJoin gate.

several open challenges before practical implementation. Foremost, the selection and control of I_c in SBLCs. Typical fabrication spreads of approximately $\pm 10\%$ in I_c are common [16]; how such variations perturb transition probabilities, and thus the correctness and convergence of BC-style computation, has not yet been quantified. Equally critical is that concrete device-level designs of the BC primitives, especially the CJoin gate that is central to computation in BC, have yet to be specified, validated, and composed. These gaps indicate that, while BC offers an attractive energy/noise tradeoff, its realization in SFQ technology will require both the invention of missing primitives and a principled treatment of device-level variability. As a concrete step in this direction, we evaluate the robustness of the random-walk signal propagation, which remains statistically stable, and propose the first device-level realization of the CJoin gate. Building on these components, we introduce an SBLC realization of a Ripple-Carry Adder (RCA) and evaluate its behavior and efficiency, thereby foreshadowing demonstrable advantages over conventional baselines.

III. PROPOSED CJOIN GATE AND CIRCUITS FOR SBLCS

A. SFQ CJoin gate

The SFQ CJoin gate is a reversible gate essential for SBLC calculations. Our design uses four SFQ rings, each with four JJs, exploiting energy splitting and recombination of SFQs at branching points. Two conditions enable the JJs switching: (1) SFQ presence in an adjacent ring of the random-walk circuit, causing energy splitting, and (2) SFQs present in two neighboring rings in the gate, causing energy recombination. The gate handles two input patterns: a single terminal input or two tokens from diagonally opposite terminals.

When one SFQ pulse is input from a terminal and the input JJ switches, the SFQ pulse splits into two adjacent superconducting rings. For example, with input from terminal West (W) in Fig. 4, the SFQ splits from **A** into **a** and **b**. At this time, only the input side JJ meets the switching condition, the presence of SFQs in two neighboring rings in the gate, causing the pulse to return to the input terminal. Therefore, the SFQ CJoin gate acts as a dead end in this case.

When SFQs are input from diagonally opposed terminals and the two input JJs switch, the SFQ pulses branch into two adjacent superconducting rings. For example, inputs from terminals W and East (E) or North (N) and South (S) in Fig. 4

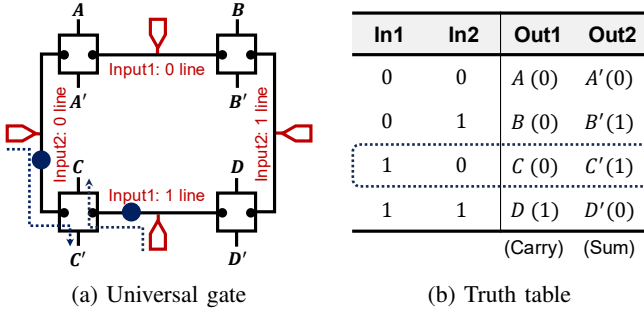


Fig. 5: Arbitrary operation with CJoins

cause SFQs to split from two rings (A and C, or B and D) into four rings (a, b, c and d), filling all four superconducting rings of the SFQ CJoin gate. Consequently, all four JJs in the SFQ CJoin gate meet the switching condition due to SFQ presence in adjacent rings in the gate, so the outputs are unrestricted. However, since SFQ energy recombines at the output, SFQs in the two rings adjacent to the output JJ disappear, and the output always appears at a diagonal pair of terminals—either W and E or N and S.

The splitting and recombination of energy occurring in the CJoin gate may seem like SFQ replication or merging, but they differ fundamentally. Unlike the replication and merging, which change energy and require external input or cause dissipation, splitting and recombination conserve energy. This is achieved by tuning the gate’s superconducting loop inductance to about twice that of the surrounding circuit, halving the I_L and SFQ energy during splitting. This careful tuning allows both processes to coexist in the gate.

By employing four SFQ CJoin gates as designed in this work, a universal gate can be constructed as illustrated in Fig. 5(a). Although the universal gate has four input terminals and eight outputs, dual-rail encoding reduces the effective logical inputs to two. This encoding uses two complementary lines: a signal on the “1 line” means logical “1”, on the “0 line” means logical “0”, and signals on both lines indicate an error. Within this universal gate, two signals enter through the four input terminals due to the dual-rail format, and the corresponding output signals appear from a specific pair of two terminals out of the eight output terminals. The truth table in Fig. 5(b) shows a one-to-one match between input patterns and output pairs. The dual-rail encoding scheme permits independent assignment of logical values to each of the eight output terminals. For instance, designating logic “0” to terminals A, A', B, C, and D', and logic “1” to terminals B', C', and D yields output patterns corresponding exactly to those of a half adder. Consequently, this universal gate can be functionally equivalent to a half adder.

B. SBLC Ripple-Carry Adder

This section explains how an N -bit ripple-carry adder (RCA) is composed from the SBLC primitives introduced earlier, namely random-walk lines, Hub, CJoin, and Ratchet gates. Once a single SBLC full-adder (FA) stage is available, an N -bit RCA is obtained by cascading N identical stages (top of Fig. 6), same as CMOS technology. Regarding full-adder

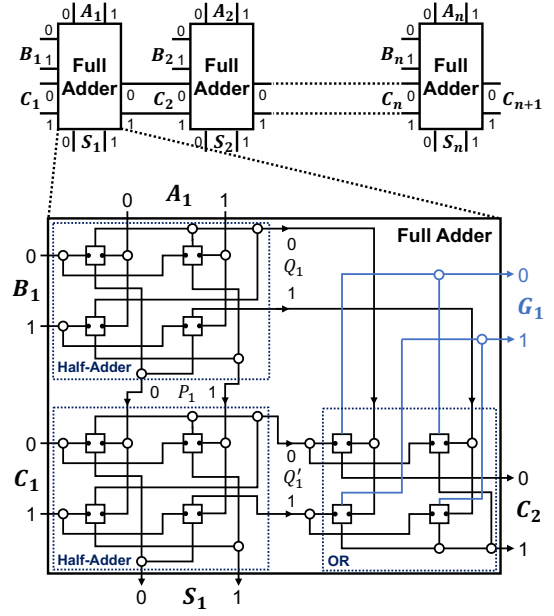


Fig. 6: SBLCs Ripple-Carry Adder

TABLE I: Parameter list

| Parameter | Symbol | Unit | Value |
|--|--------------|---------------|-------|
| Critical current of JJ | I_c | μA | 2.15 |
| Critical current of JJ (SFQ injection) | $I_{c_{in}}$ | μA | 400 |
| Inductance (Random walk line section) | L_R | pH | 360 |
| Inductance (CJoin gate section) | L_C | pH | 720 |

construction, the stage i receives (A_i, B_i, C_i) and emits (S_i, C_{i+1}) . The sum network implements $S_i = A_i \oplus B_i \oplus C_i$ by chaining two Half-Adders (HAs): the upper HA forms $P_i = A_i \oplus B_i$, and the lower HA maps $S_i = P_i \oplus C_i$. The carry network implements $C_i = Q_i \vee Q'_i = (A_i \wedge B_i) \vee (P_i \wedge C_i)$ by chaining two HAs and a OR logic gate.

Each HA and OR gate is constructed using the aforementioned Universal gate. By appropriately merging and connecting these outputs, an FA is realized. Fig. 6 shows an example built entirely with reversible gates. However, since the connections of each Universal gate serve only for signal merging and transmission, they can be replaced with conventional SFQ JTL. Furthermore, since JTL possesses unidirectionality, it also functions as a Ratchet gate. That is, using the universal gate in Fig. 5(a), the merging section can instantiate the entire RCA using existing SFQ wiring. Additionally, the blue path G_i in Fig. 6 represents a pass-through token to maintain reversibility at stage boundaries. Since RCA is an irreversible function, G_i can be omitted in implementations for arithmetic purposes, and the implementation in this paper follows this approach.

IV. EVALUATIONS

A. Experimental setup

This section describes the three experiments conducted in this study. First, we analyze the impact of I_c fabrication variations on the random walk circuit by investigating whether the SFQ position distribution still follows a normal distribution despite manufacturing variability. We use Jsim [17], which

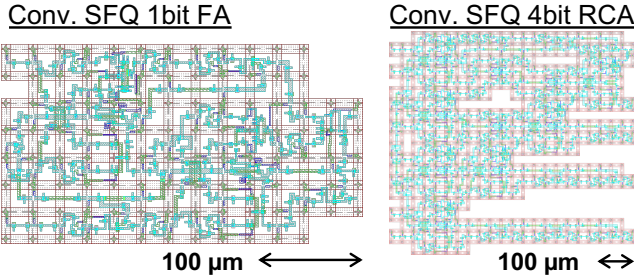


Fig. 7: Layouts of conventional SFQ RCAs

is a SPICE-based superconducting circuit simulator, as in previous studies [13], and employ JJs with critical current density (J_c) conforming to the AIST ADP2 process [18], while shrinking their area to reduce I_c . This experiment uses a circuit derived from the Random walk line in Fig. 4, increasing superconducting ring connections and centering the SFQ input. Parameters summarized in Table I ensure the I_L forms a significant portion of I_c because noise current is minimal and unstable. The dominant noise source in SFQ circuits is Josephson noise from the JJ [19], primarily caused by the shunt resistor parallel to the JJ. The noise current's standard deviation is estimated by about $1 \mu\text{A}$ ($\approx \sqrt{4k_B T \Delta f / R_s}$), where k_B is the Boltzmann constant, T is the temperature (4.2 K), Δf is the bandwidth (700 GHz) and R_s is the shunt resistor (184 Ω). We examine I_c variation from $\pm 0\%$ to $\pm 20\%$ in 1% increments. Ten random patterns are generated per variation level to avoid bias in the distribution of variations. For each circuit, the SFQ's final position after 10,000 ps is measured 1,000 times to build a distribution, which is then tested for normality using the Shapiro-Wilk test [20] to verify SFQ random walk behavior.

Second, we verify the fundamental functionality of the SFQ CJoin gate designed using the circuit in Fig. 4, following the parameters in Table I. We also use the SPICE-based simulator, Josim [21], which offers fast simulation with a large circuit. Note that the inductance of the superconducting rings in the CJoin gate (L_C) is twice that of the random walk section (L_R), allowing bias-current-free operation. We inject SFQs into terminals W and E to measure their behavior in the CJoin gate, observing the operation over a 5 μs simulation time. This process is repeated 1000 times to check for any SFQ behavior violating the defined operation of the SFQ CJoin gate.

Finally, we evaluate the proposed SBLC RCA by combining a token-level Monte Carlo simulation with an SFQ device-level energy/latency estimation. At the Monte Carlo simulation, tokens (SFQs) diffuse on the gate-level netlist built from the universal gate set. A trial begins with tokens placed on the dual-rail input ports and ends when all of them arrive at the outputs. The simulator records the number of token moves (steps) required to reach a terminal state.

Device-level timing and energy are then obtained from the step count (N_{step}). One token move corresponds to exactly one JJ switching event in the underlying random walk wiring, so the operation latency and energy are given from Eq. (2).

$$\text{Latency} = N_{\text{step}} t_{\text{sw}}, \quad \text{Energy} = N_{\text{step}} I_c \Phi_0 \quad (2)$$

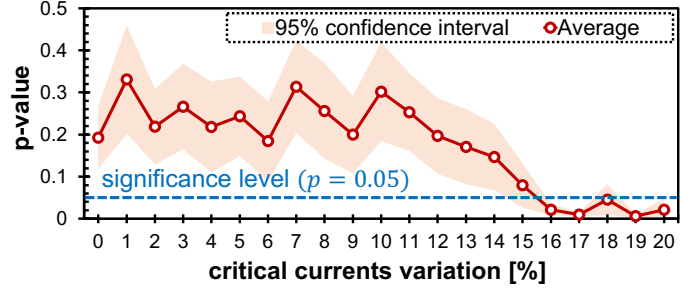


Fig. 8: Impact of I_c fabrication variations

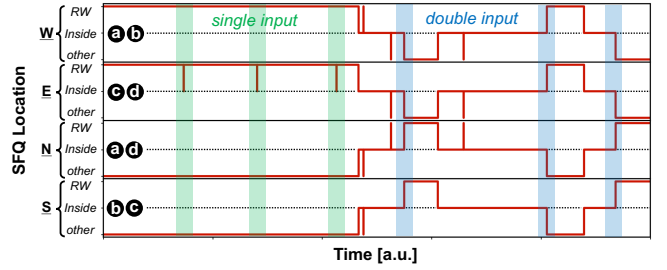


Fig. 9: SFQ location in the CJoin gate

where JJ switching delay is $t_{\text{sw}}=1.4$ ps. For the SBLC runs we use parameters in the table I, yielding $I_c \Phi_0 \approx 4.45 \times 10^{-21}$ J. The SBLCs energy is dynamic only because no static bias is supplied. These assumptions are consistent with the power formulation in Sec. II-A. We report side-by-side results for conventional SFQ implementations synthesized for the AIST ADP2 1.0 μm (10 kA/cm²) process [18], layouts shown in Fig. 7, and a 16 nm CMOS reference [22].

B. Resistance of manufacturing variation

The results are presented in Fig. 8, where the line graph indicates the mean transition of the p-values, and the light red shaded area represents the 95% confidence interval of the p-values. From these results, it can be observed that the confidence interval of the p-values for variations in the range of 0 to $\pm 14\%$ exceeds the significance level of 0.05, indicating that the distribution can be regarded as a normal distribution. Therefore, it is confirmed that fabrication variations within the range of 0 to $\pm 14\%$ do not critically affect the functionality of the random walk circuit. Furthermore, since typical fabrication spreads are within $\pm 10\%$ [16] in I_c , it is demonstrated that the impact of fabrication variations on the random walk circuit is not critical.

C. Functional verification for SFQ CJoin gate

Fig. 9 illustrates one set of results, categorizing SFQ positions at each terminal into three regions: the RW section (including rings A to D), inside the gate (the two rings adjacent to each terminal among a to d), and elsewhere, thereby showing SFQ migration. The regions marked in green indicate where a single SFQ enters the gate; in these cases, the SFQ quickly returns to the RW section after entering, confirming that the gate acts as a dead end. The blue regions show where the SFQ presence switches terminals, demonstrating back-and-forth movement of SFQs between the paired

TABLE II: Performance evaluations: Latency, Energy, and EDP.

| Circuit | CMOS (16 nm) | | | Conventional SFQ (1 μm) | | | Proposed SBLC (1 μm) | | |
|-----------|--------------|-------------|-----------|-------------------------------------|-------------|-----------|----------------------------------|-------------|-------------|
| | Lat. [ps] | Energy [aJ] | EDP [rJs] | Lat. [ps] | Energy [aJ] | EDP [rJs] | Lat. [ps] | Energy [aJ] | EDP [rJs] |
| 1 bit FA | 248.5 | 278.3 | 69.2 | 33.0 | 2122 | 70.0 | 542 | 1.70 | 0.93 |
| 2 bit RCA | 278.4 | 871.3 | 373.8 | 49.7 | 8699 | 432 | 1086 | 3.45 | 3.75 |
| 3 bit RCA | 708.2 | 1520 | 1077 | 66.4 | 15255 | 1013 | 1625 | 5.17 | 8.39 |
| 4 bit RCA | 938.1 | 2495 | 2341 | 83.1 | 21822 | 1813 | 2167 | 6.89 | 14.9 |

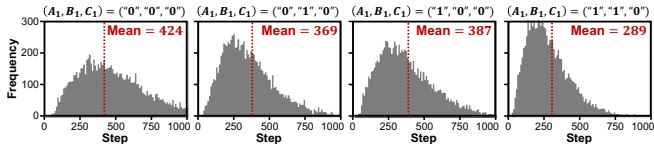


Fig. 10: Histograms of step count for RCA

terminals W and E, and N and S via the gate. Simultaneously, no violations of SFQ behavior are observed in any of the 1000 tests. These results show the functional correctness and operational stability of the SFQ CJoin gate.

D. Performance Evaluations for SBLC-RCA

Fig. 10 shows the token-level Monte-Carlo results for the 1 bit FA as histograms of the step count over representative input combinations. SBLC computation converges to a deterministic Boolean output for each input, while the random walk makes the completion step count stochastic. The distributions are unimodal with a sharp mode at small and a long right tail. Cases that generate long carry chains shift the histogram to the right and increase variance. As the bit width grows, both the mean and spread of step count increase roughly in proportion to the number of full-adder stages, consistent with ripple propagation across stages. For performance comparisons, we use the mean value ($=N_{\text{step}}$) and map it to latency and energy using the model in Sec. IV-A.

Table II demonstrates the latency, energy, and EDP for 1 bit FA and 2–4 bit RCAs. The SBLC energy scales nearly linearly with bit-width (1.7 aJ \rightarrow 6.89 aJ from 1 bit to 4 bit), reflecting the conservation of tokens and the absence of duplication bias. In contrast, conventional SFQ energy grows rapidly with width because of active duplication and clocking. As expected for random-walk search, SBLC latency is higher than deterministic SFQ/CMOS, but the energy reduction dominates the energy-delay product. Relative to conventional SFQ, the SBLC energy is reduced by $1248\times$ (1 bit), $2521\times$ (2 bit), $2951\times$ (3 bit), and $3167\times$ (4 bit). The results demonstrate the central promise of SBLCs. By eliminating static bias and harnessing noise to drive token motion, SBLC arithmetic achieves orders-of-magnitude lower energy while maintaining acceptable latency thanks to high-speed JJ dynamics.

V. RELATED WORKS

ERSFQ: The Energy-Efficient Rapid Single Flux Quantum (ERSFQ) circuit replaces resistor-based bias currents in conventional RSFQ circuits with superconducting inductors and JJs [23], reducing static power consumption during idle periods to nearly zero and enabling ultra-low-power logic operation [24], [25]. Owing to the elimination of static power

dissipation, the total energy consumption of this circuit can be reduced by two orders of magnitude compared to RSFQ circuits. [26]. However, these studies focus exclusively on the reduction of static power consumption; as the number of JJs employed increases, the dynamic power consumption correspondingly increases.

HFQ: Half Flux Quantum (HFQ) circuits leverage π -phase shifters and $0-\pi$ JJs ($0-\pi$ SQUIDS) to use HFQ ($\Phi_0/2$) as the logical unit instead of SFQ (Φ_0) employed in conventional SFQ circuits [27]. This flux reduction lowers the circulating current and I_c , primarily reducing dynamic power during JJ switching. Various low-power HFQ circuit designs [28]–[30], including static power reduction methods like LVHFQ, have been proposed [31]. These studies reduce dynamic power consumption, but the reduction is much smaller than that of SBLCs. In addition, since reversible logic operations are not possible, energy dissipation still occurs due to the fundamental computational principles.

AQFP: Adiabatic Quantum Flux Parametron (AQFP) is a superconducting circuit enabling ultra-low-energy computation through adiabatic state transitions [32]. Reversible gates based on AQFP, called reversible quantum-flux-parametrons (RQFP), have been proposed [33], and computing systems utilizing RQFP have also been developed [34]. Numerous circuit-level innovations and system architectures have also been explored [35]–[38]. While both AQFP and SBLCs support low-power reversible computing, adiabatic switching of AQFP creates an inherent trade-off between switching energy and time. In contrast, SBLCs allow high-speed switching without such constraints, preserving the fast switching typical of SFQ circuits. Additionally, the presence or absence of a clock distinguishes AQFP from SBLCs.

VI. CONCLUSIONS

This work proposes and evaluates key components for SBLCs, demonstrating their practicality through case studies. We found that manufacturing variations in I_c do not critically affect random walk circuits used as interconnects, confirming the robustness of SFQ random walk behavior. We introduced the CJoin gate for SFQ devices, enabling universal gate design for SBLC computation. Finally, we built RCA based on SBLCs, achieving a $3167\times$ energy efficiency improvement over conventional RSFQ circuits, highlighting the advantage of SBLCs in low-power operation. Future work will focus on bounding the computation time, implementing the Hub/Ratchet gates for full universality, and scaling arithmetic circuits to larger bit-widths. These highlight SBLCs as a promising direction for future low-power computing systems.

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