

# Antiferromagnetic Tunnel Junctions (AFMTJs) for In-Memory Computing: Modeling and Case Study

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**Abstract**—Antiferromagnetic Tunnel Junctions (AFMTJs) enable picosecond switching and femtojoule writes through ultrafast sublattice dynamics. We present the first end-to-end AFMTJ simulation framework integrating multi-sublattice Landau-Lifshitz-Gilbert (LLG) dynamics with circuit-level modeling. SPICE-based simulations show that AFMTJs achieve  $\sim 8\times$  lower write latency and  $\sim 9\times$  lower write energy than conventional MTJs. When integrated into an in-memory computing architecture, AFMTJs deliver  $17.5\times$  average speedup and nearly  $20\times$  energy savings versus a CPU baseline—significantly outperforming MTJ-based IMC. These results establish AFMTJs as a compelling primitive for scalable, low-power computing.

## I. INTRODUCTION

Von Neumann architectures create performance bottlenecks from data movement between separate processing and memory units. *In-memory computing (IMC)* addresses this "memory wall" by enabling computation directly within memory arrays, minimizing data movement and its associated costs [1]. However, realizing IMC's potential requires memory technologies that offer high speed, low energy, and high density.

Antiferromagnetic Tunnel Junctions (AFMTJs) [2] are emerging spintronic devices that provide picosecond-scale switching [3], low write energy [4], high packing density for near-terahertz IMC architectures, and robustness against external magnetic fields due to near-zero net magnetization. Unlike conventional Magnetic Tunnel Junctions (MTJs), which switch via net magnetization toggling, AFMTJs switch through reorientation of antiparallel magnetic sublattices (Fig. 1), enabling sub-100 ps switching far exceeding the nanosecond-scale dynamics of MTJs (Table I).

Despite their promise, AFMTJs remain unexplored in computing architectures. Prior work has focused on physical characterization [?], [2], [4], [7], [14] without demonstrating dynamic models integrated into circuit-level simulations or functional architectures.

This paper makes three main contributions: (1) We develop the first compact AFMTJ model for in-memory computing, capturing dual-sublattice Landau-Lifshitz-Gilbert dynamics and inter-sublattice exchange coupling; (2) We validate our model against experimental tunneling magnetoresistance (TMR) and switching characteristics; (3) We demonstrate system-level IMC gains of  $17.5\times$  average speedup and  $\sim 20\times$  energy savings over a CPU baseline, significantly outperforming MTJ-based alternatives. This work lays a foundation for

TABLE I: Comparison of MTJ and AFMTJ characteristics.

Property	MTJ	AFMTJ
Sublattice Structure	Single ferromagnetic (FM) layer	Two antiparallel AFM sublattices
TMR Ratio	80–120% [5], [6]	Up to 500% [2]
Switching Time	1–2 ns [5]	10–100 ps [2], [7]
Write Energy	300 fJ [8]	20–100 fJ [this work]
Field Sensitivity	High	Low (inherent robustness due to zero net magnetization)

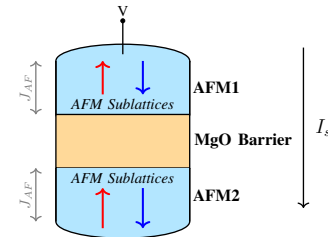


Fig. 1: AFMTJ device structure. Each AFM layer contains two oppositely aligned sublattices coupled by inter-sublattice exchange ( $J_{AF}$ ). Applied voltage drives spin-polarized current across the MgO barrier, enabling switching and readout.

future architectural exploration of AFMTJ-based systems for ultrafast, energy-efficient, and scalable in-memory computing.

## II. AFMTJ DEVICE MODEL

We extend the UMN MTJ SPICE framework [9] to capture the dual-sublattice AFMTJ physics<sup>1</sup>. Each cell instantiates two dynamically coupled magnetization vectors,  $\mathbf{M}_1$  and  $\mathbf{M}_2$ , evolving under modified Landau-Lifshitz-Gilbert [10] equations:

$$\frac{d\mathbf{M}_i}{dt} = -\gamma\mathbf{M}_i \times \mathbf{H}_{\text{eff},i} + \alpha\mathbf{M}_i \times \frac{d\mathbf{M}_i}{dt} + \boldsymbol{\tau}_{\text{STT},i} + \boldsymbol{\tau}_{\text{ex},i}$$

where  $\mathbf{H}_{\text{eff},i}$  includes the demagnetizing, anisotropy, thermal, and inter-sublattice exchange fields. The exchange torque terms  $\boldsymbol{\tau}_{\text{ex},i} = -J_{AF}\mathbf{M}_1 \times \mathbf{M}_2$  couple the sublattices, enabling mutual dynamic feedback. An adaptive fourth-order Runge-Kutta integrator (0.1 ps base step) evolves all six magnetization components.

<sup>1</sup>Our AFMTJ SPICE model is available at: [https://github.com/yousufc890/AFMTJ\\_Model](https://github.com/yousufc890/AFMTJ_Model)

TABLE II: AFMTJ Parameters Used

Parameter	Value	Description
P0	0.8	Polarization Factor
$\alpha$	0.01	Damping Factor
Ms0	600 emu/cm <sup>3</sup>	Saturation Magnetization
$J_{AF}$	5e-3	Inter-sublattice Exchange Coupling Constant
lx, ly	45nm	Lateral dimensions of free layer
lz	0.45nm	Thickness of free layer

Values were selected based on known properties of AFM materials. AFMTJ cell dimensions were kept consistent with the original UMN MTJ model [7], [9], [12], [14]–[17].

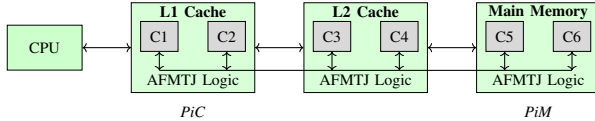


Fig. 2: High-level system architecture showing hierarchical AFMTJ-based in-memory compute. AFMTJ subarrays (C1–C6) serve as both memory (data) and compute (logic) blocks within L1, L2, and main memory, enabling processing in cache (PiC) and processing in memory (PiM).

### A. Validation and Comparison

We validated our model against fabricated AFMTJs [11]–[13], achieving comparable TMR values ( $\sim 80\%$ ) and picosecond switching dynamics. Table I summarizes key differences from conventional MTJs and Table II summarizes the key material parameters used in this work.

## III. AFMTJ-BASED IN-MEMORY COMPUTING ARCHITECTURE

### A. System Integration

To explore AFMTJ’s system-level benefits, we integrate it into a hierarchical IMC architecture [18] to replace MTJs. Fig. 2 illustrates the hierarchical IMC architecture, wherein AFMTJ subarrays embedded at L1, L2, and main memory serve as both non-volatile storage and fine-grained logic operators (XOR, NAND). Multi-row activation and charge sharing implement bit-line computing, with sense amplifiers resolving logic outcomes from magnetization-dependent current differentials.

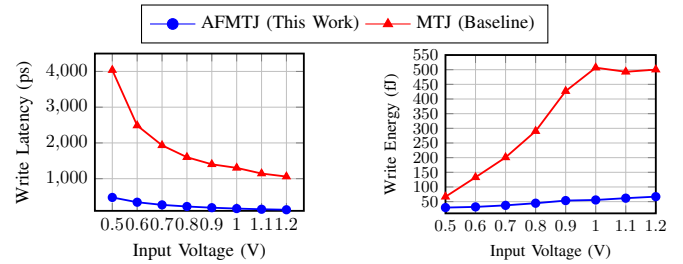
### B. Cell Operations

The AFMTJ cells support three modes: *write* (a spin-polarized current alters magnetization); *read* (the TMR is sensed through the tunnel barrier to resolve the stored state); and *logic* (conditional voltage pulses on multiple rows drive in-place Boolean operations such as NAND or XOR). A lightweight controller orchestrates the operations, exploiting AFMTJ’s picosecond switching for pipelined execution.

## IV. EVALUATION

### A. Experimental Setup

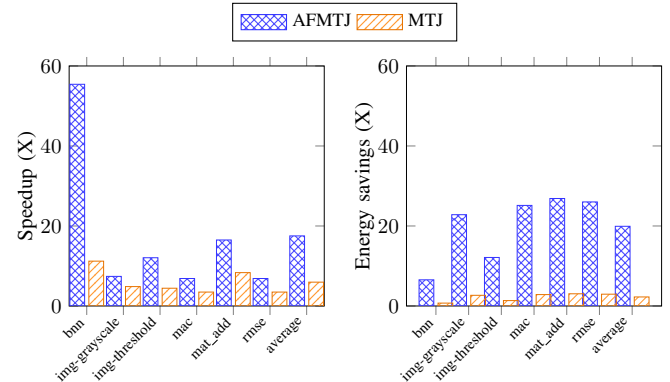
We used Synopsys HSPICE for device simulations. To explore AFMTJ as a drop-in replacement for MTJ in a system-level evaluation, we used the calibrated AFMTJ and a baseline MTJ [9] in an identical IMC hierarchy. The baseline CPU is a 2 GHz ARM Cortex-A72 with 32 KB L1, 1 MB L2, and 8 GB main memory. Workloads include binarized neural network (*bnn*), image grayscale (*img-grayscale*), image thresholding



(a) Write Latency

(b) Write Energy

Fig. 3: Write (a) latency and (b) energy comparison of AFMTJ vs. MTJ across input voltages.



(a) Latency

(b) Energy

Fig. 4: System-level (a) latency speedup and (b) energy savings of AFMTJ- and MTJ-based hierarchical IMC architecture versus the CPU baseline across workloads.

(*img-threshold*), multiply accumulate (*mac*), matrix addition (*mat\_add*), and root mean square error (*rmse*).

### B. Device-Level Results

Fig. 3 shows performance across input voltages. At 1.0 V, AFMTJ achieves 164 ps write latency (vs.  $\sim 1400$  ps for MTJ) and 55.7 fJ write energy (vs.  $\sim 480$  fJ), representing  $\sim 8\times$  and  $\sim 9\times$  improvements, respectively. Switching latency drops from 65 ps at 0.5 V to 20 ps at 1.2 V.

### C. System-Level Results

Fig. 4 summarizes the performance of AFMTJ- and MTJ-based IMC architectures against the CPU baseline. AFMTJ-based IMC achieves **17.5 $\times$  average speedup** and **19.9 $\times$  average energy savings**, compared to  $6\times$  and  $2.3\times$  for MTJ-based IMC. Write-intensive workloads (*bnn*: 55.4 $\times$ ; *mat\_add*: 16.5 $\times$ ) show the largest gains.

## V. CONCLUSION

We presented the first SPICE-based AFMTJ simulation framework capturing dual-sublattice dynamics and demonstrated its integration into in-memory computing. AFMTJs achieve  $\sim 8\times$  lower write latency and  $\sim 9\times$  lower energy than MTJs at the device level, translating to 17.5 $\times$  speedup and  $\sim 20\times$  energy savings at the system level. Future work includes compact Verilog-A models, fabrication validation, and architecture-level studies targeting edge AI, real-time signal processing, and other high-impact applications.

## ACKNOWLEDGMENT

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