

Late Breaking Results:

ADC-FIST: ADC-Free In/Near-Sensor Stochastic Object TrackingMehran Moghadam*, Sepehr Tabrizchi[†], Ali Shafiee Sarvestani[†], Sercan Aygun[‡], Arman Roohi[†], and M. Hassan Najafi**Case Western Reserve University, [†]University of Illinois Chicago, [‡]University of Louisiana at Lafayette

{moghadam, najafi}@case.edu, {stabr, ashaf25, aroohi}@uic.edu, sercan.aygun@louisiana.edu

Abstract—In/Near-sensor computing is a promising approach for efficient vision processing; however, conventional approaches often rely on power-hungry analog-to-digital converters (ADCs) and complex computational circuits. We introduce **ADC-FIST**, a novel framework that eliminates ADCs by leveraging stochastic computing (SC). Our approach replaces traditional ADCs with lightweight analog-to-bit-stream converters and simple logic gates for object tracking. **ADC-FIST** achieves comparable accuracy to conventional binary approaches while reducing power consumption and area by 89% and 88%, respectively. It enables efficient, always-on object detection and tracking, demonstrating the potential of ADC-free SC designs for resource-constrained vision systems.

I. INTRODUCTION AND MOTIVATION

The increasing demand for intelligent sensor networks and Internet of Things (IoT) devices has sparked significant interest in processing data directly within sensors, leading to the emergence of *In-sensor processing* (ISP) as a promising paradigm. ISP moves computational tasks closer to the data source by integrating processing capabilities directly within the sensing element. This dramatically reduces data movement and enables real-time decision-making at the edge while significantly lowering power consumption and bandwidth requirements in sensor networks. ISP enables sophisticated applications such as real-time event detection, continuous object tracking, and next-generation visionary sensing. However, these applications require complex signal processing and pattern recognition to be performed at the sensor level, fundamentally changing how sensor data is collected, processed, and transmitted. To realize these advanced capabilities, ISP must operate within stringent constraints of power, memory, and physical space, where traditional computing approaches primarily based on conventional binary radix computing often prove inadequate. Analog-to-digital conversion (ADC) is particularly an important challenge as it consumes significant power and energy. Maintaining sensing accuracy while enabling low power and energy computations demands innovative solutions, driving researchers to explore alternative computing paradigms. *Stochastic computing* (SC) [1]–[3] has emerged as a promising alternative, particularly for resource-constrained environments. By representing data through probability streams and performing complex computations using simple logic gates (e.g., multiplication via an AND gate), SC enables efficient, low-cost computations. This emerging approach provides inherent error tolerance and enables progressive refinement of results, making it particularly attractive for sensor applications where approximate results are often acceptable, and hardware simplicity is crucial. Previous work has integrated SC with neural networks for near-sensor computations, relying on expensive analog to stochastic converters and primarily targeting image classification tasks [4], [5]. In contrast, the design we propose in this work distinguishes itself by using a cost-efficient stochastic conversion unit and targeting event detection and object tracking tasks.

To enable advanced computations in sensors, particularly for low-energy object tracking, we introduce **ADC-FIST**, a novel framework that seamlessly integrates ISP with SC. **ADC-FIST** provides an efficient approach to optimizing both sensing and processing while maintaining system performance under stringent resource constraints. The inherent error resilience of SC aligns well with the high noise susceptibility of sensor data, while its low-complexity hardware architecture makes it an ideal solution for power- and area-constrained

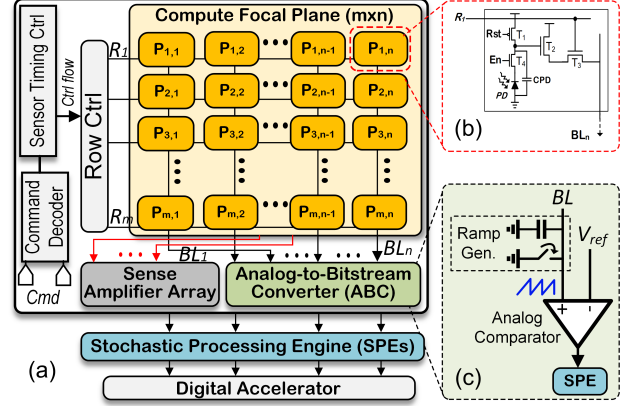


Fig. 1. (a) General overview of the **ADC-FIST** architecture, (b) pixel structure, and (c) analog-to-bitstream converter structure.

sensor devices. **ADC-FIST** enables robust and energy-efficient in-sensor data processing with minimal computational overhead.

II. **ADC-FIST** ARCHITECTURE

Fig. 1 provides a general overview of **ADC-FIST**, an event-based image sensor designed for low-energy object tracking. The **ADC-FIST** sensor consists of a pixel array, an analog-to-bitstream converter (ABC), a stochastic processing engine (SPE), and a sense amplifier array (SPA) for background subtraction. **ADC-FIST** operates in two distinct modes: *Event Detection Engine (EDE)* and *Object Tracking Engine (OTE)*. Each engine can be active or operate in different modes. In *EDE*, only the central pixels within each region of the pixel array are activated and connected to the SPA. In this mode, the two most significant bits of each pixel are read and compared with the previously stored pixel array in memory. In *OTE*, the pixels are connected to the ABC and SPE units. To optimize efficiency, **ADC-FIST** limits the Regions of Interest (ROI) to eight in the horizontal direction, effectively reducing the number of ABC and SPE units. Instead of relying on traditional, power-intensive ADC units, **ADC-FIST** employs a low-cost ABC unit, substantially lowering area and power costs. The object-tracking computations are performed in the SC domain, reducing computational complexity while enabling dynamic precision control, leading to further reductions in power and energy consumption. The following sections detail the main components of **ADC-FIST**:

1. Pixel Array: The pixel array absorbs ambient light and converts it into analog voltages using pixels (Fig. 1(b)). Traditional designs employ either a rolling shutter (row-by-row readout) or a global shutter (simultaneous readout). In **ADC-FIST**, the pixel-array architecture is modified to support both event detection and in-sensor computation. In event detection mode, the pixel array is divided into regions of size 9×9 boxes, with only one pixel from each box being read, as illustrated in Fig. 1(a) (red lines). To enhance efficiency, we connect these central pixels to a separate V_{DD} to keep them always-on, while the remaining pixels are turned off during event detection mode. Upon detecting an event, the system activates the relevant ROIs and initiates object tracking by applying the Gabor algorithm [6] to these areas. The pixel array is partitioned into 32×16 regions, each with 64×64 pixels.

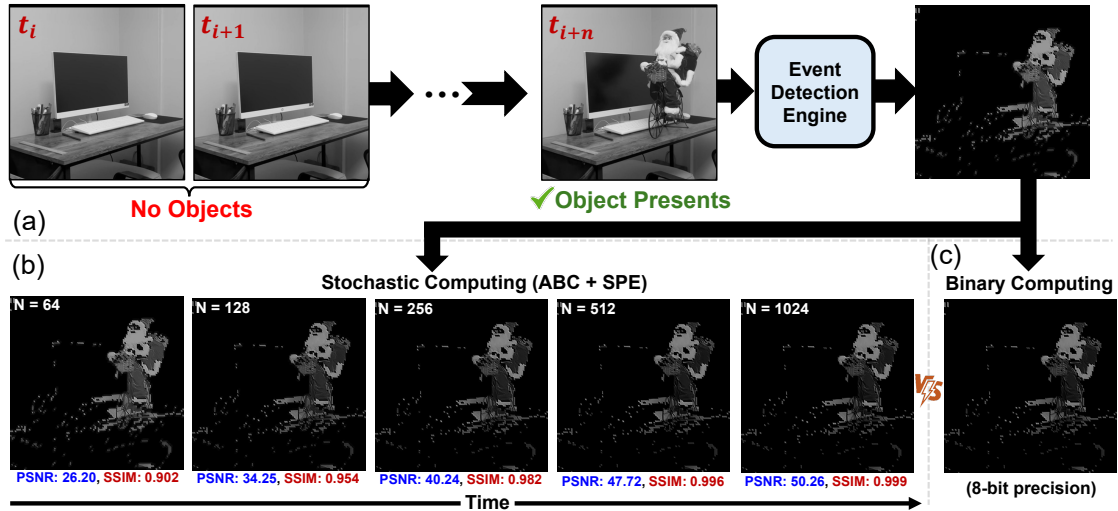


Fig. 2. The overall flow of **ADC-FIST**. (a) Object detected in the EDE, (b) Conversions and computations in SC domain, and (c) Binary computation.

To minimize overhead and power consumption, at most eight ROIs can be activated in the horizontal direction. For example, $ROI_{(1,1)}$ and $ROI_{(1,9)}$ share a vertical bus, as depicted in Fig. 1(a).

2. Analog-to-Bitstream Converter (ABC): The ABC component in **ADC-FIST** is a low-cost pulse-width modulator converting the sensed analog input into periodic pulse signals. Periodic pulse signals can be used as the input to SC circuits with the data value encoded with duty cycle and accuracy controlled by the frequency or the period of pulses [7]. Fig. 1(c) shows the circuit design of the input converter used in our system consisting of a ramp generator and an analog comparator. The analog input from the sensing circuit controls the duty cycle and the frequency of the reset signal in the ramp generator determines the frequency of the generated pulses.

3. Stochastic Processing Engine (SPE): The logic design of the SPE in **ADC-FIST** is significantly simpler than its conventional binary counterpart. In this module, each ROI is convolved with a 9×9 Gabor filter [8] to enhance object features. Similar to the convolution design developed in [9], we implement the convolution operation using an array of AND gates to perform multiplication operations, followed by an accumulator that counts the number of '1's with positive and negative components accumulated separately. Because the ABC generates periodic pulse signals, each pulse train is sampled at the system clock to produce a binary sequence before accumulation, ensuring that the '1'-count corresponds to the duty-cycle-encoded input value. The results of positive and negative accumulation are subtracted using a binary subtractor. Multiplication operations are the most costly part in convolution operations, and implementing them with simple AND gates significantly reduces the area and power costs.

III. PROOF-OF-CONCEPT: EDE

Fig. 2 demonstrates the overall flow of the **ADC-FIST** framework where the *EDE* captures the target object and forwards the detected ROIs to the *OPE* for further processing. At this stage, each sensed pixel value is first converted to a stochastic signal using the ABC unit. The detected object frame is then convolved with Gabor filters using SC-based computational elements, i.e., SPE. We evaluated the SPE unit's output by varying the bit-stream length (N) and measuring the peak signal-to-noise ratio (PSNR-in *db*) and structural similarity index measure (SSIM) for each output frame. As can be seen in Fig. 2, the output quality improves as the bit-stream length increases. With a clock frequency of 1GHz (for a target accuracy rate of less than 1% mean absolute error), convolving with the Gabor filter takes $64ns$ with the proposed design when $N=64$, which can achieve an acceptable

TABLE I
COMPARISON BETWEEN DIFFERENT EVENT-DRIVEN DESIGNS

Design	Power		Area	Delay	Multi Precision	NVM
	Pixel_Array	EDE Comp./Sense				
ADC-FIST	0.11	0.14	0.045	0.12	6.67	Yes
NSP [10]*	1	1	1	1	1	No
NeSe [11]	0.185	0.33	1	0.73	1	No

*NSP is regarded as the baseline. The reported results are measured using Synopsys HSPICE and Design Compiler in 65nm technology.

quality of SSIM=0.902. Considering the low-cost design of the SC-based convolution, **ADC-FIST** processes 8×2^{12} pixels in parallel.

To ensure a fair comparison with prior works, Table I reports the synthesis results using the same image sensor size and EDE resolution, with all data normalized based on the NSP design [10]. For prior works, we assume they utilize SAR-ADC to read pixel values. In [10], a smaller box size is employed, leading to higher power consumption and memory usage in their design. In contrast, NeSe [11] utilizes Magnetic RAM (MRAM) to store and compare previous pixel values, which increases energy consumption. However, due to the smaller box size in [10], the EDE still consumes more power in this design. By eliminating the ADC, exploiting SC, and employing a larger box size, **ADC-FIST** reduces area requirements. However, compared to other designs, it operates at a lower speed due to its reliance on SC and implementing an object tracking algorithm. Nevertheless, **ADC-FIST** offers several advantages, including support for multi-precision computing and eliminating nonvolatile memory (NVM) demands, further reducing power consumption.

IV. CONCLUSIONS

ADC-FIST enhances in/near-sensor vision processing by substituting traditional, power-intensive ADCs with efficient stochastic computing units. This approach achieves a significant reduction in power consumption and physical footprint, with decreases of 89% and 88% in power and area, respectively. Importantly, it maintains detection accuracy within 2% of conventional methods, with an SSIM greater than 0.98. Moreover, **ADC-FIST** operates at frame rates that are seven times higher than standard architectures, thereby demonstrating the feasibility of ADC-free architectures for energy-constrained vision applications.

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