Late Breaking Results: CHESSY: Coupled Hybrid Emulation with SystemC-FPGA Synchronization

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***Abstract*—The growing complexity of cyber-physical systems (CPSs) calls for early prototyping tools that combine accuracy, speed, and usability. Virtual Platforms (VPs) provide fast functional simulation, but hybrid co-emulation solutions, in which key digital components are deployed on FPGA, become necessary when accurate timing modelling is required and RTL simulation is too costly. However, existing hybrid emulation tools are mostly proprietary, and rely on vendor-specific FPGA features. To address this gap, we introduce an open-source framework that connects SystemC-based VPs with FPGA emulation, enabling full-system co-emulation of digital and non-digital components. The FPGA accelerates the execution of main digital subsystems, while a wrapper coordinates timing and communication with the VP through JTAG, maintaining synchronization with simulated peripherals. Evaluations using a RISC-V SoC, with an example in the biosignals processing domain, show up to 2500× speedup compared to RTL simulation, while maintaining less than 2× total simulation time relative to pure FPGA emulation.**

***Index Terms*—FPGA, SystemC, hybrid emulation**

I. Introduction and Background

Early prototyping helps shortening time-to-market and reducing costs of Cyber-Physical Systems (CPS) design [1]. A key challenge lies in accurately modeling interactions between digital systems and their surrounding environment (e.g., sensors, actuators, power sources) within a unified framework. Standard approaches rely on high-level SW Virtual Platforms (VPs) such as QEMU or Renode, which enable fast, functional simulation and facilitate multi-domain full-system modeling through frameworks like SystemC AMS [2]–[8]. However, pure SW VPs trade timing fidelity for speed and require separately maintained high-level abstractions of each component.

Conversely, FPGA emulation executes the actual RTL code of digital blocks with cycle accuracy, without incurring the huge costs of RTL simulation. However, it complicates the modelling of interactions with components not available at RTL, or non-digital [9]. VP-FPGA hybrid co-emulation frameworks [10] address this duality by combining a SW VP with FPGA-accelerated modelling of key digital blocks (e.g., processors), but existing implementations either are proprietary/not openly available [11]–[15], rely on vendor-specific features [16], [17] or require RTL instrumentation (e.g., transactors), as for SCE-MI [10] and others [14], [17]–[19].

To address these limitations, we propose **CHESSY** (Coupled Hybrid Emulation via SystemC–FPGA Synchronization), a *fully open-source*, flexible, hybrid prototyping framework that combines FPGA-accelerated RTL execution with loosely timed SystemC models [20]. CHESSY leverages JTAG for VP-FPGA communication and timing synchronization, through lightweight Board Support Package (BSP) stubs, thus being *FPGA-agnostic and requiring no changes to firmware or RTL*

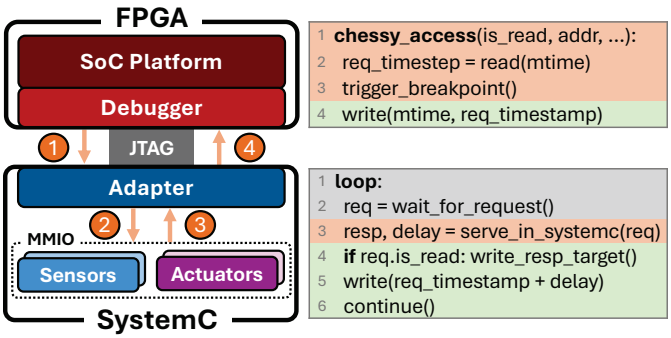

Fig. 1. Overview of CHESSY. The background shades in the pseudocode (right) indicate the timestamp observed by the corresponding hardware (left): *gray* = previous request, *orange* = current request, *green* = current request + simulated peripheral delay.

[13]. The result is a portable and transparent co-emulation environment that bridges cycle-accurate RTL execution of key digital modules with high-level simulation of the rest of the system, including non-digital components.

We demonstrate CHESSY on a RISC-V System-on-Chip [21], [22] for a biosignal-based robot control use case. The results show that we achieve more than three orders of magnitude speedup over RTL simulation while maintaining a total simulation time of less than 2× that of pure FPGA emulation. CHESSY is available at https://github.com/eml-eda/chessy.

II. Methodology

Figure 1 illustrates CHESSY, which connects a SystemC VP to an FPGA-based target through a debugger-mediated link.

The FPGA runs an unmodified design containing a processor and (a subset of) its fully-digital on-chip peripherals, while SystemC, running on the host, simulates the rest of the Memory-Mapped I/O (MMIO) peripherals, especially those interacting with the external world, such as sensors and actuators. A host-side adapter links the two environments by intercepting I/O requests at dedicated breakpoints and maintaining time synchronized through controlled updates to the FPGA's timer registers (e.g., `mtime`). This lets the software running on the FPGA perceive realistic peripheral latencies, even though the latter are simulated on the host.

Figure 1 captures this process: ① whenever the FPGA wishes to communicate with a simulated device, it issues a `SystemCRequest` via a wrapper function `chessy_access`; ② this request is intercepted by the host adapter, a SystemC module, that dispatches it to the appropriate peripheral; ③ the peripheral SystemC model computes the response, after a specified `simulated_delay`; finally, ④ the adapter returns the result to the FPGA and updates timer

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registers accordingly. The only FPGA-side requirement to realize this behavior is a debugger server accessible through standard physical connections such as JTAG, providing basic breakpoint handling and memory/register access. This avoids RTL modifications, reduces hardware integration effort, and keeps the framework portable across FPGA vendors, processor models, debuggers, phy links, and simulation environments.

A. Communication and synchronization details

CHESSY synchronizes FPGA and VP executions at each interaction (e.g., a read/write request from the FPGA-emulated core to a peripheral virtualized in SystemC). This minimizes synchronization overheads while maintaining timing accuracy equal to the resolution of the timer register present in the FPGA-emulated system (a requirement of our approach). Namely, the interaction works as follows.

The `chessy_access` function is implemented as a SW stub running on the FPGA, and it packages each communication request into a transaction structure containing operation type (`is_read`), target address (`addr`), data pointer (`data_ptr`), transfer size (`size_bytes`), and local timestamp (`timestamp_us`, read from `mtime`). When the request is ready, a breakpoint notifies the host.

On the host, the adapter controls the debugger to monitor for breakpoints on `chessy_access`, and reads the request transaction data structure; for write operations, it fetches the payload from the FPGA memory pointed to by `data_ptr`; for read operations, it prepares to write the response back after processing. Data transfer occurs over JTAG via the GDB `restore` (write) and `dump` (read) commands.

Next, the SystemC global simulation time is advanced until `timestamp_us`. The adapter then encapsulates the request into a high-level `SystemCRequest` and forwards it to the appropriate SystemC peripheral, determined by the target address. Peripheral models compute the functional response and advance the simulated time to model the peripheral's latency.

When a read reply is ready, the adapter writes the result into FPGA memory and advances time (`mtime`) to `timestamp_us` + `simulated_delay`, ensuring that the FPGA's perception of time reflects the simulated behavior.

III. Results

To validate the proposed approach, we emulated the RISC-V-based Astral platform [21] on a AMD VCU118 FPGA, connected to a Linux workstation running the MESSY [20] SystemC-VP for peripherals simulation. The workstation is equipped with a quad-core CPU, 32GB of RAM, an RV64 GNU GCC / GDB toolchain, and an RTL simulator (Siemens QuestaSim 2022.3) for baseline comparisons.

The simulation time overhead introduced by CHESSY was evaluated against a pure FPGA setup (i.e., without VP communication), using a periodic read–compute–write benchmark with a configurable delay to emulate a generic CPS workload. The benchmark was run while sweeping the computation-to-I/O ratio by varying: **(i)** the data transfer size, from a few bytes up to several kilobytes, and **(ii)** the computation delay, from zero to millions of cycles, thereby controlling the access frequency to VP-simulated models. The results, reported on the left side of Fig. 2, show that the overhead is nearly insensitive

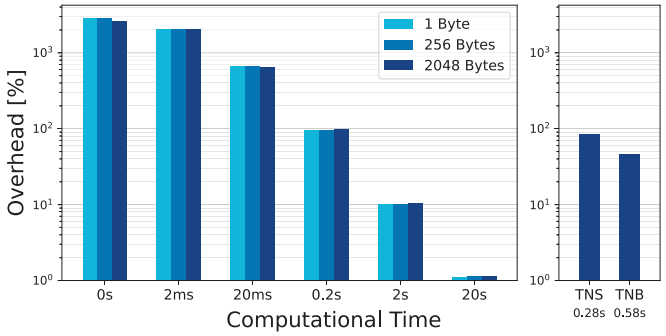

Fig. 2. Simulation time overhead [%] for different transfer sizes and interaction intervals. The two rightmost bars show overheads for 14 M (TNS) and 28 M (TNB) cycle variants of TempoNet (280 ms and 560 ms at 50 MHz).

to transfer size, with relative variation always below 4%, since data exchanges are implemented as host memory dump/restore operations. The total overhead clearly depends on the frequency of FPGA-VP interactions, but reduces to acceptable values for compute-intensive workloads, which are those that necessitate FPGA-acceleration in the first place. On average, each access incurs a nearly constant overhead of less than 100 ms.

We then assessed CHESSY's effectiveness on a realistic biomedical use case, including an Electromyography (EMG) sensor and a robotic arm, both modeled in SystemC, connected to the RISC-V SoC mapped on the FPGA. The application SW reads EMG data, performs gesture recognition via the TempoNet Neural Network (using either a small $\approx$ 4k-parameter / 14 M-cycles variant or a larger $\approx$ 9k-parameter / 28 M-cycles variant), and sends commands to the robotic arm [23]. As with the synthetic benchmark, we measure the average overhead relative to an FPGA-only baseline, reported on the right side of Fig. 2. The 14 M-cycle network exhibits an overhead of about 86%, which reduces to 47% for the 28 M-cycle one. Hence, for realistic applications with similar compute-to-access ratios, the total time remains below $2\times$ that of pure FPGA execution.

Larger and more compute-intensive workloads, common in modern embedded ML, benefit even more: the relative overhead drops to nearly 1% for workloads longer than 20 s. For extremely access-intensive use cases, the protocol remains usable, although simulation may become up to $30\times$ slower. Overall, CHESSY adds modest performance overhead, especially for compute-bound applications, while retaining practical efficiency even in I/O-heavy scenarios.

Finally, to relate CHESSY's performance to a traditional cycle-accurate RTL simulation, the biomedical workload was also executed on QuestaSim. As expected, the FPGA-accelerated setup (including the HIL-based CHESSY protocol) achieves speedups greater than $2500\times$ over RTL.

IV. Conclusions

We presented CHESSY, an open-source, FPGA-agnostic hybrid prototyping framework that does not require RTL modifications. Through a lightweight JTAG-based mechanism, it allows FPGA-emulated hardware to interact with SystemC-modeled peripherals while preserving realistic timing behavior. Experiments show that CHESSY provides over three orders of magnitude speedup compared to RTL simulation, with total execution time remaining within $2\times$ that of pure FPGA emulation for realistic applications.

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