

Late Breaking Results: A Power-Efficient RISC-V Baseband System-on-Chip for Multi-Standard Integrated Sensing and Communications

Limin Jiang*, Yi Shi[†], Yihao Shen*, Yintao Liu*, Siyi Xu*, Qingyu Deng*, Xiaoxiao Chen*, Qianli Wang*, Shan Cao*, Zhiyuan Jiang*, and Sheng Zhou[†]
 *School of Information and Communication Engineering, Shanghai University, Shanghai, China
[†]Department of Electronic Engineering, Tsinghua University, Beijing, China
 jiangzhiyuan@shu.edu.cn

Abstract—We present *Ishtar*, a power-efficient RISC-V baseband system-on-chip (SoC) tailored for multi-standard integrated sensing and communications (ISAC) in low-altitude wireless networks (LAWNs). *Ishtar* integrates a hierarchical scheduling scheme and a system-level power-gating architecture that dynamically controls power domains to balance performance and energy efficiency. It supports dynamic task scheduling across heterogeneous protocols using a domain-specific, graph-based representation. Implemented in 40 nm technology and running at 300 MHz, *Ishtar* achieves better normalized efficiency than state-of-the-art SDR SoCs, delivering real-time multi-standard sniffing under stringent power and area constraints.

Index Terms—SDR, RISC-V, SoC, power-gating, integrated sensing and communications, low-altitude wireless networks

I. INTRODUCTION

Low-altitude wireless networks (LAWNs) have emerged as critical infrastructure that enables communication among unmanned aerial vehicles (UAVs), basestations, and ground users [1], [2]. Effective operation of LAWNs requires continuous channel measurements and sensing (i.e., sniffing) across heterogeneous links such as 4G, 5G, and satellite networks, operating in diverse and dynamic environments (as shown in Fig. 1). These scenarios impose stringent demands on radio flexibility and processing capability. Software-defined radio (SDR) architectures provide the necessary reconfigurability, but their hardware implementations face tight constraints on power and area efficiency. Commercial off-the-shelf (COTS) solutions such as Sora [3] and Aerial [4] suffer from both power and weight limitations, making them impractical for airborne platforms. Multicore solutions, including Mempool-based designs [5]–[8], offer core-level parallelism but face challenges in meeting multi-protocol adaptability, power optimization, and fast waveform processing. Meanwhile, digital signal processors (DSPs) such as Ceva [9], [10], Prabhu et al. [11] and Tomahawk2 [12] integrate specialized hardware accelerators, but exploiting these accelerators often demands significant hardware expertise and programming effort, increasing development complexity.

In this work, we propose *Ishtar*, a power-efficient SDR system-on-chip (SoC) designed for multi-standard integrated sensing and communications (ISAC). *Ishtar* employs a hierarchical scheduling scheme and programmable power-gating to balance performance and energy efficiency. With our in-house protocol implementation, *Ishtar* supports dynamic task scheduling and protocol-specific acceleration across heterogeneous communication standards, enabling real-time sniffing and analysis in LAWNs.

This work was supported in part by the National Natural Science Foundation of China (NSFC) under Grants 62271300, in part by the Shanghai Municipal Science and Technology Commission under grants 25DP1501502, 24DP1501100 and 24DP1500600. Available open-source protocol implementation: <https://acelab-shu.github.io/ACE-Echo/>.

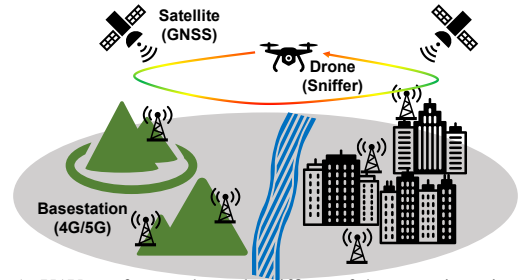


Fig. 1. A UAV performs channel sniffing of base stations in urban and mountainous areas with assistance from satellite localization.

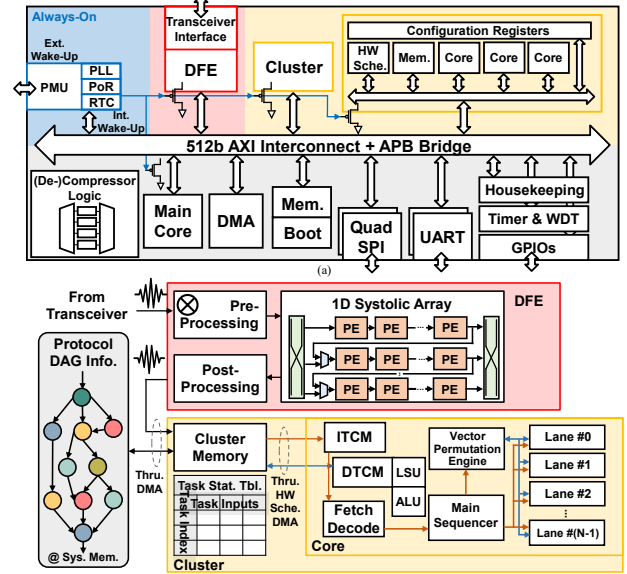


Fig. 2. Overview of *Ishtar*. (a) System architecture overview. (b) Data processing flow and detailed structure of the DFE and cluster domains.

II. IMPLEMENTATION

System Architecture: As shown in Fig. 2(a), *Ishtar* is partitioned into four power domains to minimize dynamic power consumption in low voltage threshold components. The always-on (AON) domain manages the remaining three domains and contains the power management unit (PMU), which controls the sequencing of power switches and isolation signals. During sleep mode, the system can be awakened by external signals or an internal real-time clock (RTC) interrupt. The DFE domain handles baseband signal processing from the transceiver, featuring multiple multiply-accumulate (MAC)-based processing elements (PEs) to meet the stringent real-time requirements of instantaneous tasks such as synchronization. The cluster domain comprises several computing clusters responsible for ISAC; each cluster processes one physical channel defined in

TABLE I
IMPLEMENTATION RESULTS AND FEATURES OF THE PROPOSED DESIGN
COMPARED WITH STATE-OF-THE-ART SDR SoCs

	Ishtar	Heart-Stream [8]	DXT501 [14]	Prabhu [11]	Tomahawk2 [12]
Tech. (nm)	40	12	28	28	65
Freq. (MHz)	300	800	800	290	445
Area (mm ²)	31	5	48	2.2	36
Voltage (V)	1.1	0.8	0.9	1.0	1.2
Power (W)	0.0005 AON + 0.26 Sys + 2.92 Core + 0.74 DFE	1.15	3	0.18	0.76
Peak Perf.	142.9 Core GOPS + 94.4 DFE GOPS	410 GFLOPS	102.4 GOPS	N/A	105 GOPS
Norm. Eff.*	1.95	3.39	0.24	N/A	12.06
Program Model	RISC-V HW Sche. SIMD	RISC-V SPMD SIMD	ASIP HW Acc.	RISC-V ASIP VLIW	RISC HW Acc. VLIW
Power Opt.	✓	✗	✓	✓	✓
DFE	✓	✗	✓	✓	✗
Task Sche.	✓	✗	✗	✗	✓

* Efficiency normalized to 40 nm and 1.1 V, with scaling factor $\left(\frac{Tech_{Ishtar}}{Tech_{Ours}}\right)^2 \left(\frac{V_{Ishtar}}{V_{Ours}}\right)^2$. The unit is Performance per mm² per W.

the communication protocol. Within each cluster, the hardware scheduler maps individual protocol modules onto dedicated cores for parallel execution [13]. The remaining components form the system domain, which provides the minimal functionality required for proper system operation. The main core features a 1 KiB instruction cache and an 8 KiB data cache, supporting the RV32IM instruction set architecture. Moreover, Ishtar is test-ready, incorporating scan flip-flops, compression and de-compression logic, and memory built-in self-test (MBIST) structures for compression mode testing.

Processing Dataflow: Fig. 2(b) illustrates the procedure for channel status tracking. Before execution, the protocol specifications of physical channels are condensed into dependency acyclic graphs (DAGs) using a domain specific language (DSL) [13], which explicitly defines data dependencies among modules (i.e., tasks). Each task is implemented in C with vector intrinsics [15] targeting the cores [16] within the cluster, and the DAGs are stored in system or flash memory. Next, the DFE processes the incoming baseband signals. The signals first pass through a mixer for frequency-offset compensation, followed by a cascaded systolic array [17] that performs filtering and correlation to identify synchronization signals across different protocols. The post-processing stage detects peaks and generates a synchronization flag. The compensated baseband signals and the DAG information are transferred to the cluster memory via direct memory access (DMA) programmed by the main core. The hardware scheduler then analyzes the DAG and converts the dependencies into a task status table, which tracks the input readiness of each task. Once all inputs are available, the scheduler selects an idle core and triggers its internal DMA to transfer the corresponding code and data into the tightly coupled memory (TCM). Each core implements an RV32IM processor with a custom vector extension optimized for baseband processing, featuring multiple parallel lanes for intra-lane computation and a permutation engine for inter-lane operations. The computed results are written back to system memory through dual DMAs.

III. RESULTS

Ishtar is synthesized using the SMIC 40 nm process and implemented at 300 MHz with Cadence Innovus. The current version of Ishtar instantiates a single computing cluster comprising two cores, one of which features vector processing capabilities (64 lanes). Power analysis is performed using Ansys RedHawk. All protocol implementations follow the specifications defined in [18]–[21]. Functional and latency evaluations are conducted using Synopsys VCS.

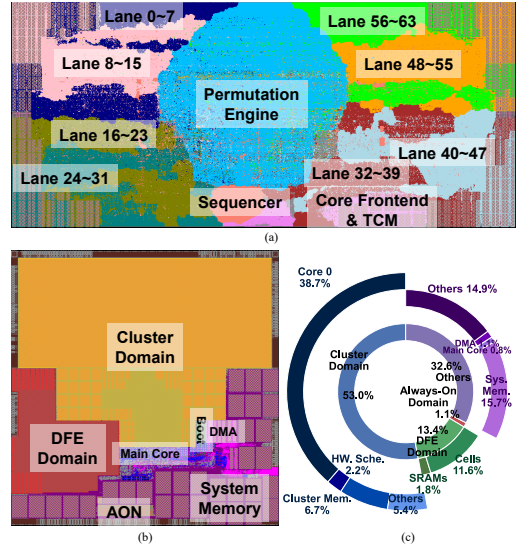


Fig. 3. Floorplan details of Ishtar. (a) Floorplan of the vector extension core. (b) Floorplan of the complete SoC. (c) Area breakdown of Ishtar.

TABLE II
LATENCY OF PHYSICAL CHANNELS ACROSS DIFFERENT CELLULAR GENERATIONS (W/O CODE OPTIMIZATIONS, 50 MS SENSING INTERVAL)

Physical Channels	Gen.	Latency (us)	Norm. Eff.
Broadcast	4G	864.18	24.66
Control Format Indicator	4G	115.25	28.69
Downlink Control	4G	4707.56	14.31
Downlink Shared	4G	7940.43	10.58
Broadcast	5G	3618.39	16.24
Downlink Control	5G	1775.30	21.05
Downlink Shared	5G	17494.58	5.97

Comparison with State-of-the-Arts: Table I summarizes the implementation results and key features of Ishtar compared with other SDR SoCs. Ishtar achieves superior normalized efficiency, primarily attributed to its high-performance components – including both the DFE and the vector extension core – as well as its low power consumption. Moreover, Ishtar simplifies the programming model: the hardware scheduler operates transparently to the programmer, requiring only minimal configuration effort.

Implementation Details: Fig. 3 illustrates the implementation details of Ishtar. The cluster and DFE domains dominate the overall floorplan, occupying 66.4% of the total chip area. The AON domain accounts for only 1.1%, consuming minimal power during sleep mode. The floorplanning of the vector extension core presents a particular challenge due to the permutation engine, which requires interconnections with all 64 lanes. To ensure balanced routing density and timing closure, cell and module padding techniques are applied to adjust the placement density between the central and peripheral regions.

Physical Channel Latency: Table II presents the latency of various protocols executed on Ishtar under a 50 ms interval. Ishtar demonstrates strong efficiency owing to its power-gating strategy. The measured latencies are in the millisecond range, primarily constrained by computationally intensive algorithms such as channel decoding and equalization.

IV. CONCLUSION

This work introduces Ishtar, a RISC-V baseband SoC optimized for multi-standard ISAC in LAWNs. The hierarchical scheduling and power-gated architecture jointly enable scalable performance with minimized power overhead. Experimental results demonstrate efficiency gains and flexible programmability over existing SDR SoCs, validating Ishtar as a practical foundation for low-power, real-time multi-standard channel sensing in future UAV and edge communication platforms.

REFERENCES

- [1] J. Wu, Y. Yang, W. Yuan, W. Liu, J. Wang, T. Mao, L. Zhou, Y. Cui, F. Liu, G. Sun, *et al.*, “Low-altitude wireless networks: A comprehensive survey,” *arXiv preprint arXiv:2509.11607*, 2025.
- [2] Z. Sheng, X. Bowen, S. Daohong, F. Wei, J. Zhiyuan, and N. Zhisheng, “Agile coverage for low-altitude aerial intelligent networks: A blended hyper-cellular solution,” *China Communications*, vol. 22, no. 9, pp. 22–36, 2025.
- [3] K. Tan, H. Liu, J. Zhang, Y. Zhang, J. Fang, and G. M. Voelker, “Sora: High-performance software radio using general-purpose multi-core processors,” *Communications of the ACM*, vol. 54, no. 1, pp. 99–107, 2011.
- [4] A. Kelkar and C. Dick, “NVIDIA Aerial GPU hosted AI-on-5G,” in *2021 IEEE 4th 5G World Forum (5GWF)*, pp. 64–69, IEEE, 2021.
- [5] Y. Zhang, M. Bertuletti, C. Zhang, S. Riedel, D. Shen, B. Wang, A. V. Coralli, and L. Benini, “TeraPool: A physical design aware, 1024 RISC-V cores shared-11-memory scaled-up cluster design with high bandwidth main memory link,” *IEEE Transactions on Computers*, 2025.
- [6] Y. Zhang, M. Bertuletti, S. Riedel, M. Cavalcante, A. Vanelli-Coralli, and L. Benini, “TeraPool-SDR: An 1.89 TOPS 1024 RV-Cores 4MiB shared-L1 cluster for next-generation open-source software-defined radios,” in *Proc. ACM Great Lakes Symp. VLSI (GLVLSI)*, pp. 86–91, 2024.
- [7] M. Bertuletti, Y. Zhang, A. Vanelli-Coralli, and L. Benini, “A 66-Gb/s/5.5-W RISC-V many-core cluster for 5G+ software-defined radio uplinks,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2025.
- [8] Y. Zhang, M. Bertuletti, S. Mazzola, S. Riedel, and L. Benini, “A 410GFLOP/s, 64 RISC-V cores, 204.8 GBps shared-memory cluster in 12nm FinFET with systolic execution support for efficient B5G/6G AI-enhanced O-RAN,” in *2025 IEEE European Solid-State Electronics Research Conference (ESSERC)*, pp. 401–404, 2025.
- [9] CEVA Inc., “Baseband platform IP for 5G RAN ASICs.” [Online]. Available: <https://www.ceva-ip.com/wp-content/uploads/PentaG-RAN-17724.pdf>.
- [10] CEVA Inc., “Integrative baseband IP platform for cellular IoT.” [Online]. Available: <https://www.ceva-ip.com/wp-content/uploads/PentaG-product-note-2025.pdf>.
- [11] H. Prabhu, L. Liu, F. Sheikh, and O. Edfors, “A 1070 pJ/b 169 Mb/s quad-core digital baseband SoC for distributed and cooperative massive MIMO in 28 nm FD-SOI,” in *2021 Symposium on VLSI Circuits*, pp. 1–2, IEEE, 2021.
- [12] B. Noethen, O. Arnold, E. P. Adeva, T. Seifert, E. Fischer, S. Kunze, E. Matúš, G. Fettweis, H. Eisenreich, G. Ellguth, *et al.*, “10.7 A 105GOPS 36mm² heterogeneous SDR MPSoC with energy-aware dynamic scheduling and iterative detection-decoding for 4G in 65nm CMOS,” in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 188–189, IEEE, 2014.
- [13] L. Jiang, Y. Shi, S. Xu, S. Cao, and Z. Jiang, “A hybrid hardware-software scheduling scheme for heterogeneous many-core systems,” *IEEE Embedded Systems Letters*, pp. 1–1, 2025.
- [14] Y. Chen, L. Liu, X. Feng, and J. Shi, “DXT501: An SDR-based baseband MP-SoC for multi-protocol industrial wireless communication,” in *2022 IEEE Symposium in Low-Power and High-Speed Chips (COOL CHIPS)*, pp. 1–6, IEEE, 2022.
- [15] L. Jiang, S. Xu, Y. Liu, Y. Shen, Y. Shi, S. Cao, and Z. Jiang, “An arbitrary register grouping scheme for RISC-V vector extension: Compilation support and hardware implementation,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 1–1, 2025.
- [16] L. Jiang, Y. Shi, Y. Shen, S. Cao, Z. Jiang, and S. Zhou, “Unlimited vector processing for wireless baseband based on RISC-V extension,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 33, no. 12, pp. 3423–3436, 2025.
- [17] B. Ruan, L. Jiang, S. Cao, and Z. Jiang, “Dynamically configurable FIR filters based on serial MACs and systolic arrays,” in *2024 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, IEEE, 2024.
- [18] ETSI, “LTE; Evolved Universal Terrestrial Radio Access (E-UTRA); Physical channels and modulation (3GPP TS 36.211 version 14.15.0 Release 14),” 2020. [Online]. Available: https://www.etsi.org/deliver/etsi_ts/136200_136299/136211/14.15.00_60/ts_136211v141500p.pdf.
- [19] ETSI, “LTE; Evolved Universal Terrestrial Radio Access (E-UTRA); Multiplexing and channel coding (3GPP TS 36.212 version 14.16.0 Release 14),” 2021. [Online]. Available: https://www.etsi.org/deliver/etsi_ts/136200_136299/136212/14.16.00_60/ts_136212v141600p.pdf.
- [20] ETSI, “5G; NR; Physical channels and modulation (3GPP TS 38.211 version 15.10.0 Release 15),” 2022. [Online]. Available: https://www.etsi.org/deliver/etsi_ts/138200_138299/138211/15.10.0_60/ts_138211v151000p.pdf.
- [21] ETSI, “5G; NR; Multiplexing and channel coding (3GPP TS 38.212 version 15.13.0 Release 15),” 2022. [Online]. Available: https://www.etsi.org/deliver/etsi_ts/138200_138299/138212/15.13.0_60/ts_138212v151300p.pdf.