

Drafting and Multi-Input Switching in Digital Dynamic Timing Simulation for Multi-Input Gates

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Abstract—Trace-history-dependent effects such as drafting and multi-input switching are poorly modeled in static timing analysis, yet do not justify excessive transistor-level analog simulations. We present a closed-form analytic delay model for fast digital dynamic timing analysis of interconnected NOR gates, which captures both effects. Our delay formulas are derived from a thresholded hybrid gate model based on non-constant-coefficient differential equations, which can be analytically parametrized via a few characteristic gate delay values. By utilizing our formulas in the discrete-event simulator-based *Involution Tool*, we show that accurate circuit simulation can be done at roughly inertial-delay cost. The significantly improved timing prediction accuracy of our delay model is demonstrated by two representative benchmark circuits.

Index Terms—Dynamic timing analysis, multi-input switching, drafting, thresholded hybrid models, discrete-event simulation, gate-level circuit verification.

I. INTRODUCTION AND OVERVIEW

Modern digital designs in advanced technologies exhibit increasingly tight timing margins and strong sensitivity to power, voltage, and temperature (PVT) variations. Industrial design flows therefore rely on static timing analysis (STA) [1], [2], which is extremely fast but based on worst-case corner delay analysis. Trace-history-dependent phenomena like (i) *drafting*: delay dependence on the time since the last output transition, and (ii) *multi-input switching* (MIS, “Charlie effect”) [3]–[5]: delay dependence on the relative arrival times of multiple inputs are either ignored or lumped into guardbands. Both (i) and (ii) can significantly affect circuit delays in deeply scaled technologies, however.

To analyze timing violations suspected by STA, designers have to resort to analog simulations, e.g., using *SPICE* [6], which accurately capture drafting and MIS but are far too slow for large designs. *Digital dynamic timing analysis* (DDTA) based on discrete-event simulation offers a faster alternative: it propagates digital events through a netlist using gate delay models. However, state-of-the-art DDTA uses inertial delays [7] or single-history models such as DDM and IDM [8]–[10], which at most cover drafting only. MIS-aware timing models have only been developed for STA and often rely on empirical macromodels or computationally intensive ODE evaluations [4], [5], [11]–[15].

Our recent work on *thresholded hybrid models* for digital gates [16]–[18] revealed that gate-level behavior can be accurately described by mode-switched ordinary differential equations (ODEs) driven by digital inputs, with digital outputs obtained by thresholding internal analog signals. For 2-input NOR/NAND gates, in particular, this yields closed-form MIS-aware delay formulas [16], [18], [19]. These models are not yet suitable for being used in DDTA, however, since they ignore drafting and lack the embedding in a circuit simulation algorithm.

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Contributions. Our paper (see [20] for the full version) provides the following contributions:

- 1) We derive closed-form delay formulas for interconnected NOR gates that account for *both* drafting and MIS, by starting from the thresholded hybrid ODE model presented in [18].
- 2) We show how to analytically parametrize the model using six characteristic delay values (three for rising and falling transitions each), without any need for waveform fitting.
- 3) We design an event-driven simulation algorithm for MIS- and drafting-aware DDTA that uses our delay formulas, and implement it in the publicly available *Involution Tool* [21]–[23].
- 4) We evaluate our model’s timing prediction accuracy on a 50-stage cross-coupled NOR chain and on a NOR-equivalent `c_17_slack` circuit from the ISCAS benchmark [24], demonstrating superior accuracy over state-of-the-art delay models with negligible run-time overhead.

II. HYBRID DELAY MODEL WITH MIS AND DRAFTING

Our analysis starts from the MIS-aware first-order thresholded hybrid models for interconnected NOR, NAND and C gates presented in [18]. Transistors are replaced by time-varying resistors here, resembling the Shichman-Hodges model [25], [26], and are switched on/off according to the digital inputs $(A, B) \in \{0, 1\}^2$. Applying Kirchhoff’s laws to the resulting voltage divider, augmented with an effective load capacitance and an optional serial resistor representing the interconnect, yields a first-order ODE with piecewise time-varying coefficients for the output voltage $V_{out}(t)$, which is finally digitized via thresholding at $V_{DD}/2$. Closed-form trajectories for this ODE were used to derive MIS-aware delay formulas $\delta(\Delta)$. Since drafting was ignored in [18], the derivations were based on trajectories that start from perfectly saturated voltage levels (0 or V_{DD}).

To incorporate drafting, one needs delay formulas $\delta(T, \Delta)$ that also depend on arbitrary previous-output-to-input delay T , which correspond to arbitrary trajectory starting voltages V_{int} . This is highly nontrivial because any number of intermediate input transitions might change the slope of $V_{out}(t)$ without crossing the threshold.

We addressed this problem by introducing the notion of *virtual transitions*. Every input transition, whether it causes an output change or not, is associated with a real or virtual output transition. Informally, such a transition is virtual if the next input transition occurs soon enough to prevent the output trajectory from *actually* reaching $V_{DD}/2$. Nevertheless, we hypothetically let the trajectory continue until it hits $V_{DD}/2$ and declare it a virtual transition. This effectively creates a one-to-one relation between input transitions and (real/virtual) output transitions and thus makes the previous-output-to-input delay T and the input separation time Δ well-defined.

For a 2-input NOR gate, there are eight combinations of previous and current input states. We group them into Cases (a)–(h), such as $(0, 0) \rightarrow (1, 0)$, $(1, 1) \rightarrow (0, 1)$, etc. For each case i , we derive:

- a closed-form trajectory $V_{out}^{(i)}(t, V_{int}, \Delta)$, and

- a delay function $\delta_{(i)}^{\uparrow/\downarrow}(V_{int}, \Delta)$ that schedules the output transition. For example, for Case (g) (i.e., $(0, 1) \rightarrow (0, 0)$), we obtain the piecewise analytic approximation

$$\delta_{(g)}^{\uparrow}(V_{int}, \Delta) \approx \begin{cases} \delta_0(V_{int}) - \frac{\alpha_1}{\alpha_1 + \alpha_2} \Delta + \delta_{\min} & 0 \leq \Delta < \frac{(\alpha_1 + \alpha_2)(\delta_0(V_{int}) - \delta_{\infty}(V_{int}))}{\alpha_1} \\ \delta_{\infty}(V_{int}) + \delta_{\min} & \Delta \geq \frac{(\alpha_1 + \alpha_2)(\delta_0(V_{int}) - \delta_{\infty}(V_{int}))}{\alpha_1} \end{cases},$$

$$\begin{cases} V_{int} \leq \frac{V_{DD}}{2} \\ -2RC_3 \log\left(\frac{V_{DD}}{2(V_{DD} - V_{int})}\right) + \delta_{\min}, & V_{int} > \frac{V_{DD}}{2} \end{cases} \quad (1)$$

where α_1, α_2 and R are the resistance parameters of the serial pMOS transistors in the NOR gate, δ_{\min} represents a pure delay, and C_3 is the effective load capacitance. In [18], we showed that all these model parameters (except the load capacitance and pure delay) can be computed analytically from six characteristic gate delay values (three for rising and falling transitions each, for $\Delta = 0, \Delta = \infty$ and $\Delta = -\infty$).

The extremal quantities $\delta_0(V_{int})$ and $\delta_{\infty}(V_{int})$ arising in Eq. (1) can be explicitly expressed in terms of the Lambert W function [27] and the model parameters. For example, we obtain

$$\delta_0(V_{int}) = -\frac{\alpha_1 + \alpha_2}{2R} \left[1 + W_{-1} \left(\left(-e \cdot \left(\frac{2(V_{DD} - V_{int})}{V_{DD}} \right)^{\frac{4R^2 C_3}{\alpha_1 + \alpha_2}} \right) - 1 \right) \right].$$

III. EVENT-DRIVEN SIMULATION AND TOOL INTEGRATION

In order to be able to employ our delay formulas in DDTA, we provide an event-driven simulation algorithm. For each NOR gate in a circuit, our simulator maintains: (i) the time and type of the last (real or virtual) output transition, (ii) the current internal voltage V_{int} , (iii) the most recent transition times at both inputs (to compute T and Δ), and (iv) a flag distinguishing real from virtual transitions.

Whenever an input transition occurs at time t_{cur} , the algorithm:

- 1) identifies the corresponding case $(i) \in \{a, \dots, h\}$ from the current input mode,
- 2) computes the candidate delay $d = \delta_{(i)}^{\uparrow/\downarrow}(V_{int}, \Delta)$ and schedules a potential output transition at $t_o = t_{cur} + d$,
- 3) looks ahead to the next input event at time t_{next} : if $t_o - d_{\min} \notin (t_{cur}, t_{next})$ or the analog trajectory does not cross $V_{DD}/2$ in this interval, the transition remains *virtual* and is dropped at the digital level (transition cancellation); otherwise it is committed as a real output transition,
- 4) updates T and evaluates the corresponding trajectory $V_{out}^{(i)}(t, V_{int}, \Delta)$ at $t = T + d_{\min}$ to obtain the new V_{int} .

This algorithm covers both “classical” cancellations (two close opposite transitions on the same input) and cancellations triggered by transitions on different inputs, which constitute MIS scenarios. We implemented this algorithm in the *Involution Tool* [21], [22], which is built on top of Questa and VHDL VITAL.

IV. EXPERIMENTAL RESULTS

We briefly report on two benchmarks synthesized in the Nanagate Open Cell Library with FreePDK15TM 15 nm FinFET models ($V_{DD} = 0.8V$) [28]. For both circuits, the characteristic delay values of all the constituent NOR gates were determined via *SPICE* simulations. They are used to parametrize two alternative delay models used for comparison purposes in the *InvTool*: (i) an IDM channel [10], and (ii) standard inertial delay channels. Moreover, they are of course also used to parametrize (iii) the delay formulas of our model, as sketched in Section II.

For our experimental evaluation of the modeling accuracy, we compared the three delay models (i)–(iii) against a “golden reference”

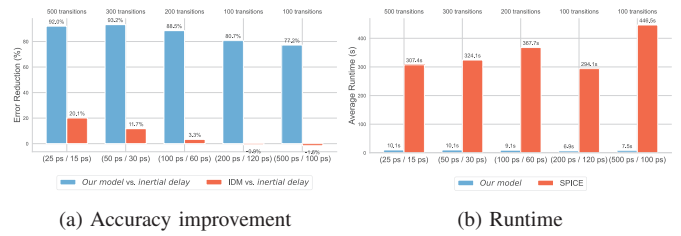


Fig. 1: Cross-coupled 50-stage NOR chain: average ADT improvement over inertial delays (left) and average runtime (right) for our hybrid model and IDM, normalized to inertial delays.

obtained by discretizing the *SPICE* output waveforms, under identical input stimuli fed into our circuits under test. As our accuracy metric, we use the absolute (i.e., unsigned) *area under the deviation trace* (ADT) between the reference trace and the trace generated by the respective model. Note that positive and negative contributions correspond to leading and trailing transitions, respectively.

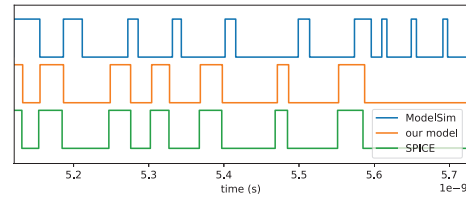


Fig. 2: Example waveform at one output of stage 50 of our NOR chain circuit.

Cross-coupled NOR chain: Our first benchmark circuit consists of three parallel chains of 50 stages of 3 cross-coupled 2-input NOR gates. We stimulate the three primary inputs with Gaussian-distributed transition times (various μ, σ), running 30 simulations per configuration and averaging the ADT. Fig. 1 (left) shows that our model consistently and significantly reduces ADT compared to inertial delays and IDM across all input distributions. Moreover, as revealed by Fig. 2 for stage 50, inertial delays suffer from large temporal shifts and numerous spurious glitches at deep stages, whereas our model faithfully follows the reference trace.

Fig. 1 (right) demonstrates that the runtime remains comparable to inertial and IDM-based DDTA, while all DDTA variants are orders of magnitude faster than the analog simulation.

c_17_slack NOR: As our second benchmark circuit, we take the *c_17_slack* circuit from [21], where all NAND gates are replaced by functionally equivalent NOR gates and characterized individually. Using the same input stimuli as in [21] with $N = 2000$ transitions, our model achieves an ADT improvement of 20.8% over standard inertial delays, comparable to the enhanced ExpChannel-IDM in [21]. This indicates that, for small circuits, the lack of MIS support in IDM does not constitute a major deficiency. In deeply cascaded multi-input structures like our NOR chain, however, our model significantly outperforms IDM due to its MIS awareness.

V. CONCLUSIONS AND OUTLOOK

We presented a hybrid delay model for 2-input NOR gates that provides closed-form, MIS- and drafting-aware delay functions and trajectories suitable for fast DDTA. The model can be parametrized using a handful of characteristic delay values, seamlessly integrates into our *Involution Tool*, and substantially improves accuracy over inertial and IDM-based DDTA without sacrificing speed. Ongoing work is devoted to employing our delay formulas in novel approaches for symbolic timing analysis [29], in the spirit of INSTA [29], [30].

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