

SINA: A Circuit Schematic Image-to-Netlist Generator Using Artificial Intelligence

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Abstract—Current methods for converting circuit schematic images into machine-readable netlists struggle with component recognition and connectivity inference. In this paper, we present SINA, an open-source, fully automated circuit schematic image-to-netlist generator. SINA integrates deep learning for accurate component detection, Connected-Component Labeling (CCL) for precise connectivity extraction, and Optical Character Recognition (OCR) for component reference designator retrieval, while employing a Vision-Language Model (VLM) for reliable reference designator assignments. In our experiments, SINA achieves 96.47% overall netlist-generation accuracy, which is 2.72x higher than the state-of-the-art approaches.

Index Terms—Automated netlist generator, open source, component detection, CCL, OCR, VLM.

I. INTRODUCTION

Recent advances in Artificial Intelligence (AI) have reshaped circuit design workflows, especially with the adoption of Large Language Models (LLMs) [1]. Although LLMs have shown strong performance in digital circuit generation [2], their use in analog and mixed-signal design remains limited due to the absence of machine-readable representations of existing circuit knowledge [3], [4]. Circuit schematics appearing in research manuscripts, textbooks, and websites capture substantial, validated circuit design information, yet they are not directly interpretable by Electronic Design Automation (EDA) tools. Unlocking this visual information for reuse and for building datasets that support circuit-focused AI models requires converting schematic images into machine-readable netlists [5].

Current EDA workflows still depend on manually transcribing schematic images into netlists, a process that is slow, error-prone, and difficult to scale [6]. Although several tools have attempted to automate this step, existing image-to-netlist methods continue to struggle with persistent limitations: inaccurate component recognition, unreliable connectivity inference, and weak reference designator extraction and assignment: [7]–[9]. These limitations hinder the creation of large, high-quality netlist datasets and restrict the capabilities of AI-driven EDA systems.

In this paper, we introduce SINA, an open-source [10] and fully automated pipeline for converting schematic images into SPICE-compatible netlists. SINA is designed to operate robustly across diverse schematic styles. To address the key shortcomings of existing methods, SINA integrates a YOLO-based [11] detector for component recognition, applies Connected-Component Labeling (CCL) [12] for reliable connectivity inference, and combines Optical Character Recogni-

tion (OCR) with a Vision-Language Model (VLM) for accurate reference designator extraction and assignment.

II. PROPOSED FRAMEWORK

SINA is a fully automated pipeline that takes circuit schematic images as input and converts them into SPICE-compatible netlists. As illustrated in Fig. 1, the framework consists of four main stages: component detection, connectivity inference, reference designator (label) extraction & assignment, and final netlist generation.

A. Component Detection

SINA uses a YOLOv11-based object detection model [11] to identify circuit components, returning bounding boxes, component types, and unique component identifiers, as shown in Fig. 2(b). To enhance reliability, SINA includes an independent VLM-based verification step using GPT-4o [13]. The VLM analyzes the schematic. Its predictions of component types and counts are compared against YOLO's detections to compute a concordance-based confidence score. Any mismatches between the two systems are flagged for users review.

B. Connectivity Inference

SINA infers electrical connectivity by determining which component terminals share a common circuit node. After component detection, the detected components are masked using their bounding boxes, leaving only the wiring of the circuit visible. The resulting image is processed using CCL [12], which segments the wiring into distinct connected regions. Regions that correspond to artifacts such as small stubs, loops, or gaps are filtered out, and only those that connect to two or more components are retained. This is consistent with the definition of an electrical net [14]. Electrically equivalent nodes (*e.g.* multiple ground symbols) are merged into a single node, as shown in Fig. 2(c). Component-to-node relationships are then established by identifying intersection points between component positions and node regions, determining which terminals connect to which nodes, as illustrated in Fig. 2(d). This stage produces the complete component-to-node mapping required for netlist generation.

C. Reference Designator Extraction and Assignment

SINA employs EasyOCR [15] to extract textual annotations from the schematic, enabling the identification of reference designators and component values. The OCR-extracted text is mapped to detected components based on spatial proximity,

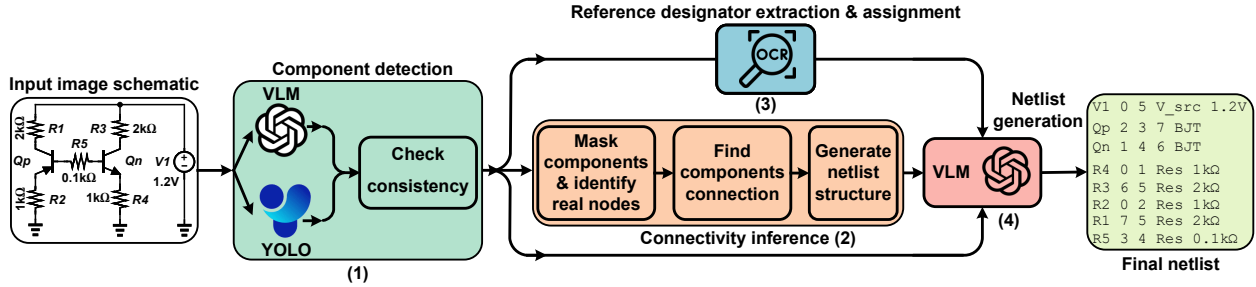


Fig. 1. The proposed SINA's workflow.

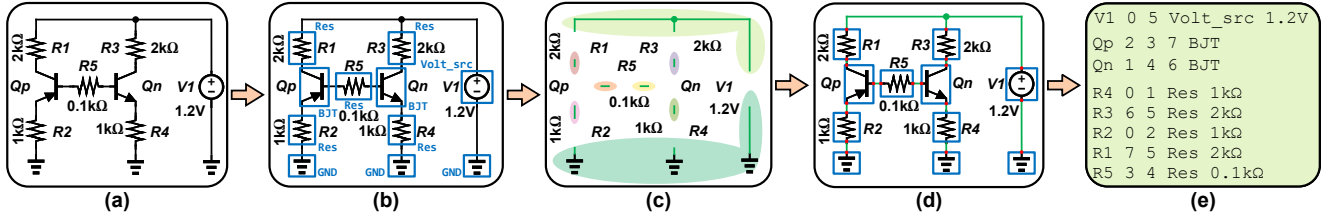


Fig. 2. An example of SINA's pipeline. (a) The original circuit schematic image. (b) The detection model output with identified components and their bounding boxes. (c) Removing components and clustering nodes. (d) Nodes and their connections to the components. (e) The final generated netlist.

TABLE I
SINA'S COMPONENT DETECTION PERFORMANCE EVALUATION.

Precision	Recall	F1 Score	Weighted Mean Average Precision
94%	99%	96.47%	98%

TABLE II
PERFORMANCE COMPARISON BETWEEN SINA AND MASALA-CHAI [3] ON 40 TEST SCHEMATICS.

Method	Text Extraction	Component Detection F1 Score	Circuit Structure	Overall Accuracy
SINA	97.55%	99.6%	99.3%	96.47%
[3]	95.09%	62.4%	59.8%	35.5%

providing essential context for the next stage, where GPT-4o assigns final component designators and values. By separating text extraction from semantic interpretation, SINA leverages each tool's strengths: the OCR for dependable text detection and VLMs for contextual reasoning.

D. Netlist Generation

As shown in Fig. 2(e), a VLM (GPT-4o) generates the SPICE-compatible netlist using three inputs: the OCR-extracted reference designators, the component-to-node connectivity mappings, and the original schematic image for visual context. With this information, the model assigns final reference designators and values to each component, and produces the final netlist that reflects the circuit's schematic structure and parameters.

III. EVALUATION

To evaluate the performance of SINA, we construct an open-source benchmark containing schematics that span a broad

range of styles, complexities, and component counts. Our object detection model is fine-tuned on a custom dataset of more than 700 annotated schematics, drawn from diverse sources such as research manuscripts, scanned textbooks, and hand-drawn sketches. To increase robustness across varied visual conditions, we apply data augmentation techniques including scaling, brightness jitter, and flipping [16].

We assess the component detection model performance using a benchmark of 75 schematics containing more than 1,000 components across 10 distinct types. The benchmark includes a mix of computer-generated, scanned, and hand-drawn schematics, covering a broad range of styles and component layouts. The component detection model achieves an F1 score of 96.47%, as shown in Table I.

For overall netlist generation performance, we compare SINA with Masala-CHAI [3], the only available open-source netlist generation framework for this task, using a curated set of 40 schematics. These test circuits are selected to ensure a fair comparison, including only component types supported by both systems. As shown in Table II, SINA outperforms Masala-CHAI across all evaluation metrics, with an overall accuracy that is **2.72x** higher.

IV. CONCLUSION

This paper introduced SINA, a fully automated and open-source pipeline for converting circuit schematic images into SPICE-compatible netlists. SINA combines a YOLOv11-based model for component detection, CCL for connectivity inference, OCR for text extraction, and a VLM for resolving reference designator assignments. In our evaluation, SINA achieves 96.47% netlist-generation accuracy, representing a 2.72x improvement compared to the state-of-the-art approaches.

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