

# Non-volatile Spintronic Flip-Flops with Checkpoint Preservation Supported in RISC-V Platform

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**Abstract**—Due to ambient energy’s inherent instability, intermittent computing is essential for task completion. This work comprehensively explores the spintronic flip-flop implementation in the open-source RISC-V platform. Magnetic tunnel junction (MTJ) has great potential for non-volatile flip-flop (NV-FF) implementation because of its high density, low read and write energy consumption, and compatibility with CMOS process. To the best of the authors’ knowledge, the checkpoint preservation is firstly supported in this work. The proposed non-volatile differential sampling latch (NV-DSL) achieves 7.39 fJ/bit data transfer energy consumption. The phased write strategy reduces write energy by 24.3%. A generalized NV-FF design methodology is further established, achieving a 68.88% area reduction. The power consumption of proposed non-volatile RISC-V processor is reduced by nearly 75%. When performing atomic tasks, the energy consumption and latency are reduced by 61.4% and 43.87%, respectively, compared with the cache scheme.

**Index Terms**—STT-MTJ, RISC-V platform, NV-DSL, NV-FF, checkpoint preservation.

## I. INTRODUCTION

EDGE computing devices have found widespread applications in various domains such as smart logistics, industrial automation, and wearable devices [1]–[3]. The inherent instability of ambient energy necessitates intermittent computing to ensure task completion, while frequent system state preservation and recovery incur significant energy and latency overheads [4]. To accommodate the dynamic nature of energy harvest [5], [6], intermittent computing systems employ incremental computation strategies, utilizing available energy to progressively advance the compute process and compensate for frequent power interruptions [7], [8].

One of the pivotal design aspects of edge intermittent computing processors lies in data preservation during power interruptions. The traditional macro-level data preservation method is shown in Fig. 1(a). This process requires the occupancy of data between the CPU, cache and external memory, resulting in significant latency and energy consumption. To address this issue, hybrid caches based on non-volatile memory (NVM) are proposed, as shown in Fig. 1(b). Compared with conventional methods, this approach significantly reduces time and energy [9]–[11]. The bit-level data preservation scheme shown in Fig. 1(c) forms internal registers with specialized storage circuits. This method achieves bit-level data retention, offering theoretically the lowest save/restore time and energy overhead

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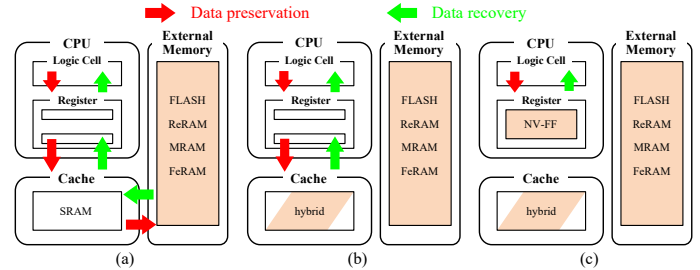


Fig. 1. (a) Macro-level data preservation using external NVM. (b) Macro-level data preservation using non-volatile hybrid cache. (c) Bit-level data preservation using NV-FF.

[12]–[14]. Relevant research efforts primarily focused on the design of non-volatile flip-flop (NV-FF) utilizing various types of NVMs. Spin transfer torque-magnetic tunnel junction (STT-MTJ) is a promising candidate device due to the advantages of mature technology, fast access speed, high endurance and the compatibility with CMOS process [15]–[19]. Nevertheless, the slower read/write speeds of non-volatile memory may adversely affect computational circuit performance. By integrating proactive checkpoint strategies, intermittent computing systems can flexibly and reliably execute failure atomic sections.

The main contributions of this paper are listed as follows:

The bottom-up design methodology in non-volatile RISC-V (NV-RISC-V) platform is proposed. In unit and circuit levels, the non-volatile differential sampling latch (NV-DSL) realizes bit-level data read, write, storage and transfer, achieving 7.39 fJ/bit data transfer power and 24.3% write energy reduction. A generalized NV-FF design method is established based on the NV-DSL. Three types of NV-FF are proposed and the area of non-volatile master-slave flip-flop (NV-MSFF) is  $4.9 \mu\text{m}^2$ , resulting in a 68.88% area reduction.

In architecture level, a single-cycle processor based on the RISC-V integer instruction set is implemented, achieving  $9.04 \mu\text{W}$  average power consumption at 50 ms intervals during Embench tasks, representing a 74.97% improvement. In terms of task type supported, the checkpoint preservation is firstly supported in this work for performing atomic tasks.

## II. MTJ-BASED NV-FF IMPLEMENTATION

### A. Bottom-up Design Methodology

Fig. 2 demonstrates the design methodology of MTJ based NV-FF in RISC-V platform from bottom-level function cell to top-level applications. Our design process is primarily divided into four progressive layers:

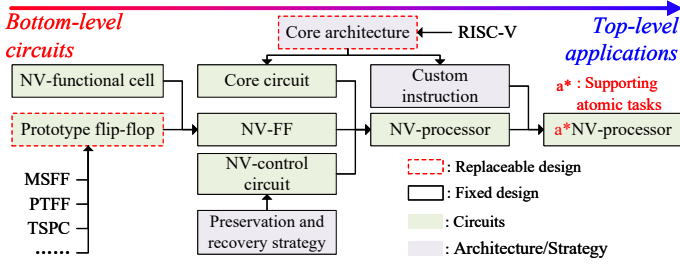


Fig. 2. Bottom-up design methodology of NV-RISC-V processor.

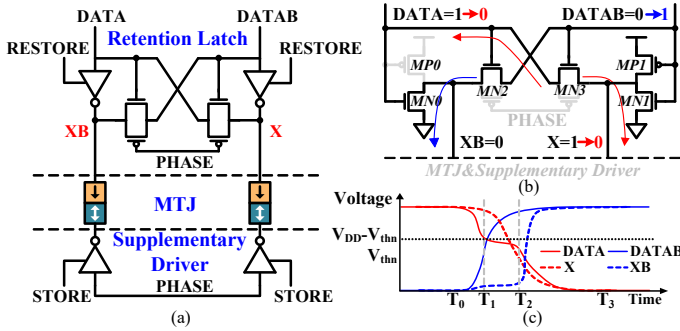


Fig. 3. (a) Schematic of proposed NV-DSL. (b) Data transfer process. (c) Data transfer diagram.

TABLE I  
DRIVE CAPABILITY AND OPERATING MODE OF NV-DSL

Restore	Store	Phase	Capacity	Operation mode
0	1	X	no	non-volatile read
1	0	1	weak	data transfer
1	0	0	strong	temporary storage
1	1	X	strong	non-volatile write

Unit level: A differential sampling latch is designed for temporary data storage. The non-volatile unit is written/read after the power supply is interrupted/restored. The data update and non-volatile writing are decoupled, eliminating the contradiction between circuit operation speed and writing duration.

Circuit level: A general NV-FF design method is proposed and applied to master-slave, pulse-triggered and true single-phase clocking structure. The non-volatile functions can be involved into standard design process of prototype flip-flops.

Architecture level one (Reactive): SW/HW co-design was explored within the terminal processor. We integrate the customized NV-MSFF in the RISC-V platform, the processor supports non-atomic task save and recovery.

Architecture level two (Proactive): Based on the NV-RISC-V platform, a bit-level data saving instruction for executing atomic tasks is proposed to avoid frequent access from core to cache, reducing the power consumption and delay overhead of data preservation and recovery.

### B. Non-volatile differential sampling latch

Conventional NV-FFs require the application of clock gating during the data preservation phase to maintain data integrity, leading to the issue of task progress suspension. In this work,

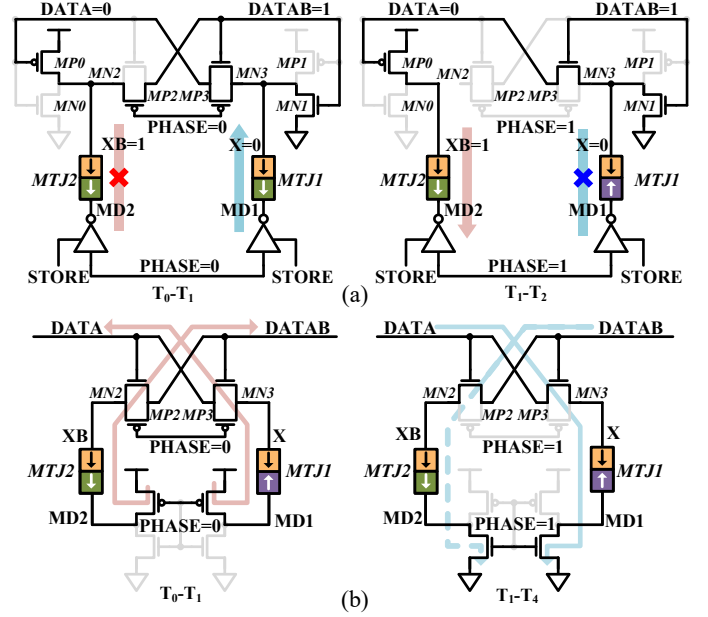


Fig. 4. Non-volatile (a) write and (b) read process of NV-DSL.

the NV-DSL with different drive capacities is proposed to address this problem. The schematic is shown in Fig. 3(a).

Table I summarizes control signals and the corresponding operation modes. In no drive mode, the cross-coupled circuit structure is repurposed as a read amplifier, enabling non-volatile read operations. In weak drive mode, data in the latch can be easily modified by external signals, thereby facilitating data transfer. In strong drive mode, the latch is allowed to stably store data or work in conjunction with supplementary driver to perform non-volatile write operations.

Fig. 3(b) and (c) show the simplified circuit and operational waveform in data transfer mode. During  $T_0$ - $T_1$ , the upper latch rapidly pulls the DATA node low while gradually charging the DATAB node. At  $T_1$ , the DATAB voltage exceeds the NMOS threshold voltage, turning on MN1/MN3. Throughout  $T_1$ - $T_2$ , DATAB continues rising beyond the inverter threshold voltage, triggering discharge at node X. By  $T_2$ , MN2 turns off and DATAB is pulled high, while node X is pulled low. This establishes a ground path for DATA, ultimately toggling XB high. At  $T_3$ , the PHASE signal transitions low, initiating internal positive feedback to complete the data transfer.

The NV-DSL write process comprises two stages, as shown in Fig. 4(a). During the first stage ( $T_0$ - $T_1$ , PHASE=0), write current flows through MTJ1, switching it to P state while the state of MTJ2 remains unchanged. Subsequently, during the second stage ( $T_1$ - $T_2$ , PHASE=1), NV-DSL enters weak drive mode, leaving node DATAB floating at a high voltage; current then flows through MTJ2 and switches the state. Fig. 4(b) illustrates the circuit path states during its read operation, divided into four stages similarly to a conventional sense amplifier. The first stage (PHASE=0) is the pre-charge phase, during which the supplementary driver pulls up nodes X and XB while transistors MP2/MP3 pre-charge nodes DATA/DATAB. Stages two through four constitute the voltage difference development phase (PHASE=1), where the supplementary driver discharges

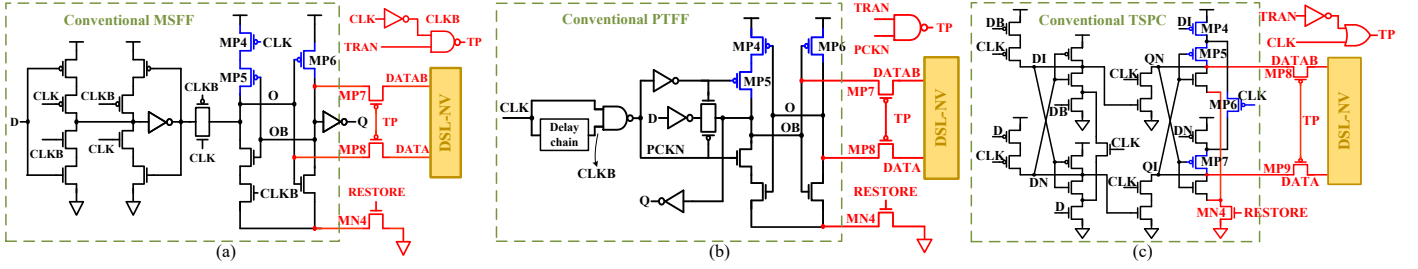


Fig. 5. Schematic of generalized NV-FF (a) NV-MSFF (b) NV-PTFF (c) NV-TSPC.

nodes XB/X through MTJ1/MTJ2; concurrently, MN2/MN3 act as a cross-coupled pair, amplifying the voltage difference between DATA and DATAB to near rail-to-rail levels.

### C. Generalized NV-FF design

The circuit structure of existed NV-FF lacks versatility and cannot be used for prototype flip-flops of different principles [20], [21]. The general NV-FF design method builds upon the proposed NV-DSL, incorporating circuit and corresponding non-volatile timing design. The modifications incorporate PMOS data-transfer switches and a transistor gated by RESTORE signal in the prototype flip-flop.

Derived from the prototype MSFF, the NV-MSFF in Fig. 5(a) incorporates an NV-DSL, PMOS transistors MP7 and MP8, and a gated transistor MN4. The PMOS transistors prevent excessive voltage drop at nodes DATA/DATAB in the NV-DSL transfer stage and ensure the accurate transfer of the voltage levels from data nodes O and OB to the NV-DSL. MN4 operates during the NV-DSL non-volatile read phase when RESTORE is low, enabling MP4, MP5, and MP6 to further amplify the voltage difference between DATA and DATAB.

Using the proposed generalized design methodology, NV-PTFF and NV-TSPC circuits are also implemented by incorporating NV-DSL, data-transfer switches, and the gated transistor MN4, as shown in Fig. 5(b) and (c). In the operational principle of NV-PTFF, during data readout, the CLK is set to low, which consequently sets the PCKN signal to high. This activates the latch structure and the gate-drain cross-coupled transistors MP4, MP5 and MP6 amplify the data voltage from the NV-DSL to a valid logic level. The NV-TSPC design additionally includes a dedicated pair of PMOS transistors with gate-drain cross-coupled connections during the clock's low-level period [22] and differs in the way to generate the transfer pulse signal.

The three cases discussed above elucidate nonvolatile design methodology based on different prototype flip-flops. This approach imposes only one core circuit requirement: the presence of a valid gate-drain cross-coupled PMOS pair during the clock's low phase. Although not all flip-flops inherently meet this requirement, the advancement of process nodes and the increasing demands for tolerance to process variations and circuit noise have challenged the reliability of dynamic logic. Consequently, static logic-based flip-flops are now favored, ensuring the continued prevalence of latch structures within flip-flop designs. For prototype flip-flops of different operating principles, the primary design effort for nonvolatile integration lies in the analysis and design of the TP signal, aiming to

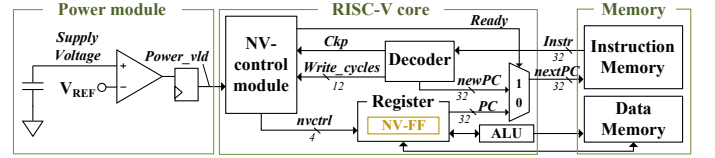


Fig. 6. The architecture of processor in NV-RISC-V platform.

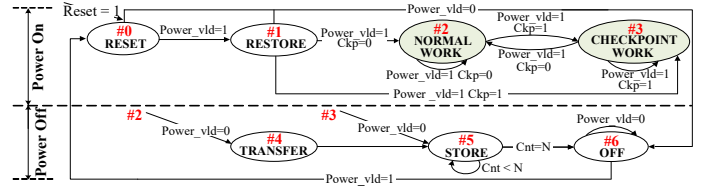


Fig. 7. The state transition diagram of non-volatile control module.

TABLE II  
OUTPUT SIGNAL TABLE OF NON-VOLATILE CONTROL MODULE

	TRAN	RESTORE	STORE	PHASE	READY
RESET	1	0	1	0	0
RESTORE	1	0	1	1	0
NORMAL WORK	Ckp	1	0	Ckp	1
CHECKPOINT WORK	$\overline{\text{Ckp}}$	1	0	$\overline{\text{Ckp}}$	1
TRANSFER	1	1	0	1	0
STORE	0	1	1	0/1	0
OFF	0	0	0	0	0

minimize the impact of the nonvolatile function on the normal operating timing of the flip-flop. This design methodology for NV-FFs is significantly expediting the design process.

### III. THE PROPOSED PROCESSOR ON RISC-V PLATFORM

In a single-cycle kernel, the operation state of the processor core can be uniquely determined by the register stack, instruction and program counter (PC) registers. By combining the NV-FFs presented in previous sections, the aforementioned registers can be implemented to enable bit-level data preservation in the processor core. This strategy avoids frequent access instructions to remove data from core to memory, thereby reducing latency and energy overhead.

The architecture of proposed processor in NV-RISC-V platform is shown in Fig. 6, including power supply, processor core and memory modules. Once the capacitor voltage which is charged by external power exceeds the reference voltage  $V_{ref}$ , the power valid signal (Power\_vld) is pulled high. The non-volatile control module then uses a 4-bit control signal to stage-wise read non-volatile data. Upon completion, a ready

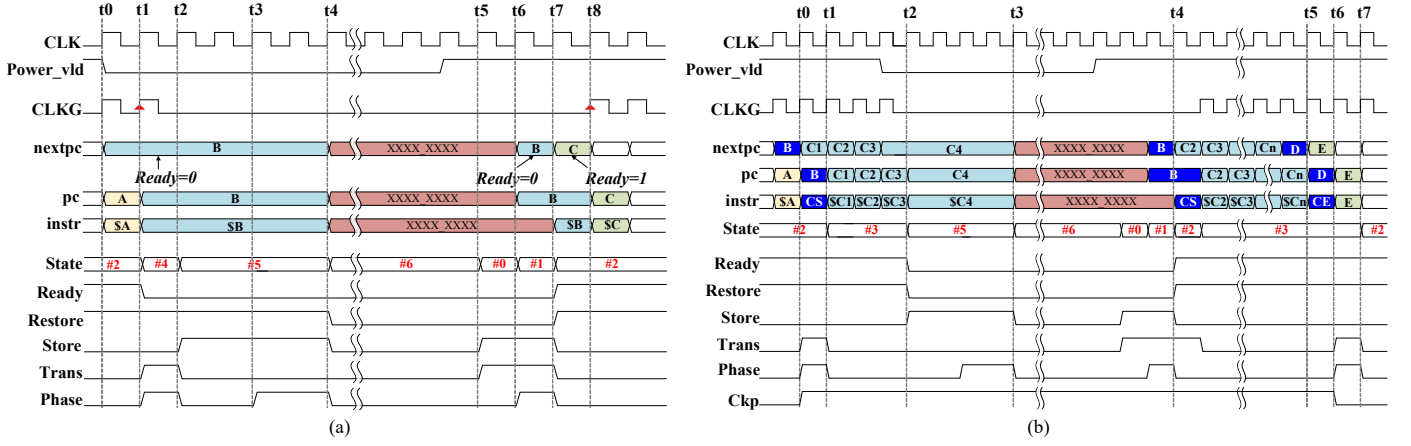


Fig. 8. Timing diagram of (a) non-atomic tasks (b) atomic tasks before and after power-off.

signal (READY) is provided, indicating that the processor core can begin executing subsequent tasks. The architecture supports proactive and reactive data preservation strategies. For proactive preservation, the processor core initiates a checkpoint signal (Ckp) based on atomic operations. For reactive preservation, when supply voltage drops below  $V_{ref}$ , the non-volatile control module automatically saves critical data to NV-FFs, halts task execution, and preserves system state.

Fig. 7 illustrates the state transitions of the non-volatile control module. The 4-bit *nvctrl* signal corresponds to the TRAN, RESTORE, STORE, and PHASE signals, controlling data transfer, write, and read operations. The RESET phase is the initial phase upon each power restoration. During this phase, the non-volatile readout circuit within the NV-DSL performs pre-charging. In the RESTORE phase, data is read from the NVMs into the register to establish valid logic levels. The NORMAL WORK phase is the conventional operation of the processor core. The core should remain in this phase for extended periods under stable power supply conditions. When the core processes atomic tasks, the CHECKPOINT WORK phase is entered. Data is transferred to NV-DSL during the TRANSFER phase, but non-volatile writing does not occur. In the STORE phase, the core performs non-volatile write operations. It persists for N clock cycles to write the complementary states into the two MTJ cells. During this phase, the external power supply has already dropped below the reference voltage, and the energy is supplied by energy storage elements such as capacitors. Upon completion of writing, the system enters the OFF phase and the external supply is terminated. The correlation between the 4-bit *nvctrl* signal and the different states of the control module is detailed in Table II.

The critical distinction between atomic and non-atomic tasks lies in whether the checkpoint preservation is required. Non-atomic tasks do not need to save checkpoint. [23]–[25] The processor directly transfers instruction address B and content \$B to the NV-DSL at t1 when power-off as shown in Fig. 8(a). At t2, the low-level READY signal gates the clock, resulting in CLKG being held low. Simultaneously, the non-volatile control module enters the STORE phase, initiating the process of writing the data latched in the NV-DSL into the MTJ. At t3, the

Phase signal toggles, commencing the write operation for the complementary MTJ cell. At t4, the non-volatile write operation is completed, the power supply is completely cut off, and the state preservation for the non-atomic operation is finished. Following power restoration, the system enters the initial RESET phase, during which the NV-DSL begins precharging. At t6, the non-volatile control module transitions into the RESTORE phase. The non-volatile data is read back into the register, and the next instruction address restored is still that of \$. At t7, the instruction memory fetches the corresponding instruction content, \$B, based on the instruction address from the final moment of the previous cycle. Simultaneously, the READY signal is asserted high, and the instruction address updates to that of the next instruction, C. Between t7 and t8, the non-volatile core executes instruction \$B. Finally, at the rising edge of CLKG at t8, the execution result of instruction \$B is committed, thereby completing the final instruction that was interrupted by the prior power loss.

The primary difference between atomic tasks and non-atomic tasks lies in the preservation of checkpoints. In the atomic task, we use two custom RISC-V instructions CKPSTART (CS) and CKPEND (CE) to indicate the start and end of the atomic task, as shown in Fig. 8(b). At t1 time, the kernel starts to execute the first instruction C1 of the atomic task, and the non-volatile control module enters the checkpoint work phase (#3). At t2 time, the power supply is interrupted, and the state is #3, so it will not carry out new data transfer and directly enter the non-volatile write phase (#5) and write the state data before instruction CS execution. At t4 time, the core power supply is restored, and the non-volatile data readout is completed. The core re-executes CS, which asserts the Ckp signal high. Simultaneously, because the register signal Ckp\_r had a non-volatily stored value of '0' before the power loss, the non-volatile control module resumes the Normal Work phase (#2). After the CS instruction is re-executed, the module re-enters the Checkpoint Work phase (#3). At t5 time, the core commits the final instruction Cn of the atomic task and fetches the next instruction CE. The operation of the CE instruction de-asserts the Ckp signal is synchronous with the clock. Consequently, at t6 time, the Ckp signal is de-asserted low, indicating the

TABLE III  
PHYSICAL PARAMETERS OF STT-MTJ

Parameters	Description	STT-MTJ
Tox	MTJ Oxide Layer Thickness	0.85nm
Tsl	MTJ Free Layer Thickness	1.3nm
CD	MTJ Critical Dimension	40nm
Rp	MTJ Resistance	3.98kohm
TMR	Tunneling Magnetoresistance Ratio	200%
$\alpha$	Gilbert Damping Coefficient	0.025
$\gamma$	Gyromagnetic Constant	$1.76 \times 10^7$ Hz/Oe
P	Electron Polarization Ratio	0.52
Hk	Perpendicular Effective Anisotropy Field	1734Oe
Ms	Saturation Magnetization of Free Layer	15800Oe

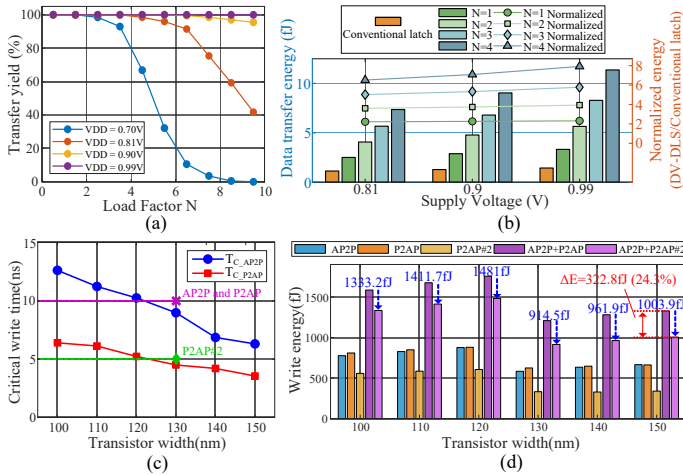


Fig. 9. (a) Variation of data transfer yield with load factor N under different supply voltages. (b) Data transfer power comparison between NV-DSL and conventional latches. (c) The critical write time dependent on transistor width. (d) The write energy dependent on transistor width.

completion of the atomic task's execution. At  $t_7$  time, the kernel executes the first instruction E after the atomic task. The non-volatile control module samples the low-level Ckp signal and returns to the normal working phase.

#### IV. SIMULATION RESULTS

The proposed MTJ based bit-level data retention circuits are simulated using 28-nm CMOS process, MTJ VerilogA compact model and NV-RISC-V platform. The physical parameters of STT-MTJ are shown in Table III [26], [27]. The post-simulation results and layout are shown as follows.

##### A. Evaluation of NV-DSL

Fig. 9(a) shows the impact of supply voltage and load factor N on data transfer yield. N is defined as the normalized ratio of the transistor size of load latch to that of driver latch. At supply voltages ranging from 0.81V to 0.99V, NV-DSL can achieve a data transfer yield more than  $3\sigma$  for N less than 4. A comparison of the data transfer energy is shown in Fig. 9(b). As N increases, the normalized data transfer energy of NV-DSL relative to conventional data transfer also increases. It can be argued that the NV-DSL trades off data transfer

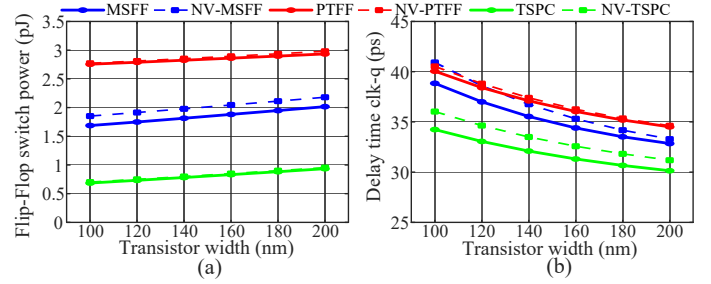


Fig. 10. The relationship between transistor width and (a) flip-flop switching power (b) delay time clk-q.

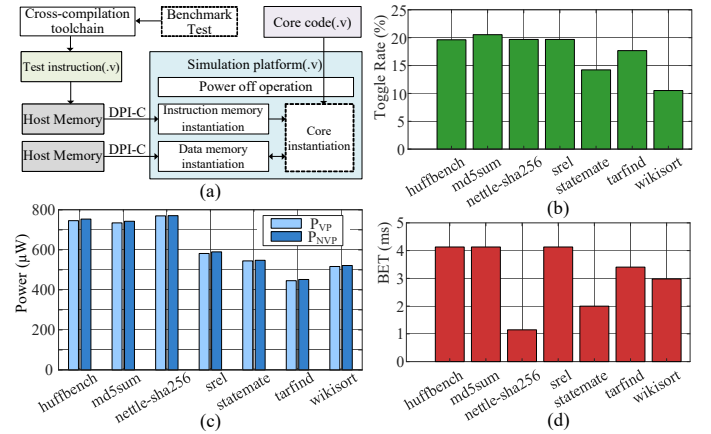


Fig. 11. (a) Core simulation process and platform. (b) Toggle rate of different tasks. (c) Comparison of power consumption of NVP and VP in different tasks. (d) BET of different tasks.

energy consumption for stable data transfer capability when the load factor N exceeds 1. The non-volatile write functionality requirements can already be met with N less than 2, while the data transfer energy consumption can be controlled within 4 times that of conventional latch. As shown in Fig. 9(c), the critical write time decreases as the write transistor size increases. AP2P and P2AP represent the write energy under actual write time. P2AP#2 represents the write energy with independently controlled write time. As shown in Fig. 9(d), when the driver transistor width is 150nm, the write energy of P2AP#2 compared to P2AP is reduced by 322.8fJ, resulting in a write energy reduction of 24.3%.

##### B. Evaluation of Generalized NV-FF

Fig. 10(a) and (b) show the switching energy and clk-q delay of the prototype flip-flop and NV-FF at different data transfer transistor sizes. The additional power consumption introduced by NV-DSL is primarily due to the continuous toggling of the inverted clock signal when generating the data transfer signal TP. Therefore, NV-MSFF has more increased flip energy consumption. NV-TSPC and NV-PLFF reduce the additional energy cost by optimizing the TP generation logic. Among these, TSPC benefits from its true single-phase clock design, resulting in the lowest energy consumption. In terms of clk-q delay, the addition of the RESTORE signal gate control transistor in the prototype flip-flop introduces additional delay. As transistor size increases, the clock-to-output delay

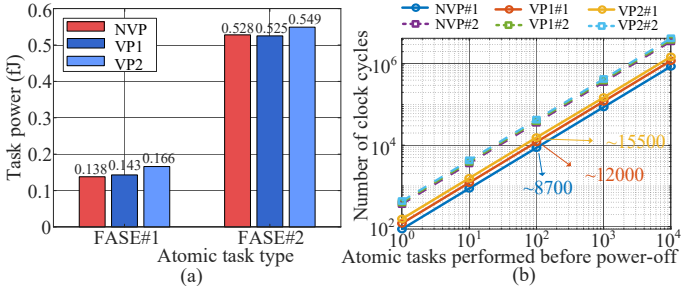


Fig. 12. Comparison of (a) energy consumption (b) time cost between NVP and VP to perform atomic tasks.

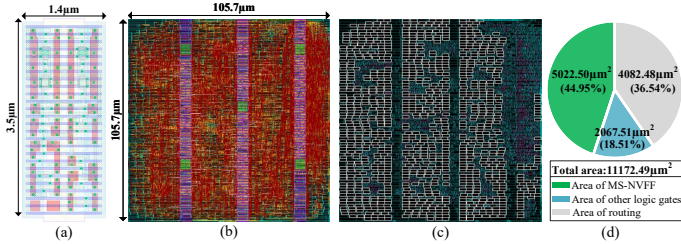


Fig. 13. (a) Layout of NV-MSFF. (b) Layout of the processor. (c) Distribution of NV-MSFF in the layout. (d) Area proportion of each part.

decreases, but the flip power consumption of flip-flops rises. Compared to their prototype counterparts, the non-volatile flip-flops do indeed result in performance degradation. The Energy-delay product (EDP) of NV-MSFF shows an average relative increase of 12.4% compared to MSFF, while NV-PLFF and NV-TSPC demonstrate an average EDP increase of 1.8% and 6.6% compared to the prototype flip-flops, respectively.

### C. Evaluation of NV-RISC-V processor

The kernel simulation flow and platform are shown in Fig. 11(a). The processor core can execute benchmark test code to evaluate the correctness of core implementation, as well as the overhead and benefits of the proposed data-saving scheme. Fig. 11(c) compares the power consumption of the proposed non-volatile and conventional volatile processor for different tasks. Fig. 11(b) and (d) respectively compare the toggle rates and break-even time (BET) for different tasks. The average power consumption of the processor core varies, leading to different break-even times for the NV-RISC-V processor compared to the volatile processor. The NVP demonstrates a minimum power consumption of  $452\mu\text{W}$  when executing tarfind, while reaching a maximum power consumption of  $771\mu\text{W}$  during nettle-sha256. If tasks are run at 50 ms intervals [9], the average power consumption of the non-volatile processor core ranges from a minimum of  $9.04\mu\text{W}$  to a maximum of  $15.42\mu\text{W}$ . This represents a reduction of up to 74.97% and at least 67.29% compared to existing STT-MTJ-based nv-processors.

Fig. 12 compares the energy and time consumption of non-volatile processor (NVP) and volatile processor (VP) in atomic tasks. The number of instructions in the FASE#1 task is fewer than that in FASE#2, so the energy consumption of executing on-site protection instructions by VP accounts for a significant proportion overall. NVP with the proposed checkpoint instructions achieves up to 16.9% power reduction

TABLE IV  
PERFORMANCE COMPARISON WITH EXISTING NV-FF

	JSSC'19 [12]	TVLSI'23 [28]	TVLSI'23 [29]	TCAS-I'24 [30]	This work
Process	40nm	40nm	28nm	10nm	<b>28nm</b>
Voltage(V)	1.1	1.1-2.2	0.4	0.4	<b>0.9</b>
NV-Type	STT-MTJ	STT-MTJ	STT-MTJ	FEFET	<b>STT-MTJ</b>
Data Delay Time(ps)	88	N/A	N/A	176	<b>85.8</b>
Area( $\mu\text{m}^2$ )	18.96	N/A	180	N/A	<b>4.9</b>
Non-volatile Write Time	2.39ns	30ns (short write) / 100ns (long write)	5ns	N/A	<b>128ps (transfer) / 15ns (write)</b>
Non-volatile Write Energy (fJ/bit)	866.38	22900	190	$\sim 0$	<b>7.39 (transfer) / 914.5 (write)</b>
Non-volatile Read Time	0.12ns	N/A	2.5ns	1 clock circle	<b>2 clock circles</b>
Non-volatile Read Energy (fJ/bit)	8.19	N/A	32.3	0.626	<b>6.02</b>
Preservation Strategy	Reactive	Reactive	Reactive	Reactive	<b>Proactive /Reactive</b>
Checkpoint Preservation Supporting	No	No	No	No	<b>Yes</b>

compared to VP2. When considering the power consumption of data migration to the volatile cache, the power is reduced by 61.4%. When executing 100 atomic tasks, NVP achieves a 43.87% reduction in execution time over VP2.

Fig. 13(a) shows the layout of proposed NV-MSFF, which area is  $4.9\mu\text{m}^2$ , achieving a 68.88% area reduction compared to existing MTJ-based NV-FFs. The entire area of the processor is  $11172.49\mu\text{m}^2$  as shown in Fig. 13(b). Fig. 13(c) and (d) respectively illustrate the distribution of NV-MSFF within the processor and the area breakdown.

Table IV shows the performance comparison with other NV-FFs in recent years. The proposed NV-FF has a lower power consumption, a reduced area and a negligible transfer time. This work enables active checkpoint state saving, which is the first implementation within the surveyed range. At the hardware circuit level, the design supports atomic tasks, and in scenarios with frequent saves, it uses data transfer instead of data saving, significantly reducing the non-volatile write overhead.

## V. CONCLUSION

In this work, we propose spintronic NV-FFs with checkpoint preservation and deploy them on RISC-V platform. In unit and circuit levels, a generalized design method is proposed, accelerating the design process and achieving a 68.88% area reduction. The NV-DSL achieves 7.39 fJ/bit data transfer energy. The phased write strategy reduces energy by 24.3%. In architecture level, a single-cycle processor based on the RISC-V platform is implemented, achieving  $9.04\mu\text{W}$  average power consumption at 50 ms intervals during Embench tasks, representing a 74.97% improvement. For atomic tasks, custom instruction set expansion reduced energy by 61.4% and latency by 43.87% over the cache storage scheme.

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