

Consolidating ML-driven Early IR-drop Mitigation for Fast and Reliable IR-drop Closure

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Abstract—This work proposes a new methodology of ML (machine-learning) driven early i.e., pre-layout IR-drop mitigation to make a fast and reliable IR-drop convergence at post-layout. Our methodology is intended to facilitate two important issues that the conventional IR-drop mitigation flow has not fully and effectively taken into account. Those issues are (1) *how we can relieve the burden of excessive use of metal resources for robust power delivery network (PDN)* and (2) *how we can reduce the iteration count of the very slow process of layout simulation followed by incremental IR-drop mitigation at the post-layout optimization stage*. Precisely, to make our early IR-drop mitigation method accurate and reliable, we devise two core components: (1) *IR-drop cost formulation* to be used at the global placement through comprehensive analysis of the sources of IR-drop and (2) *post-layout IR-drop prediction at placement by developing GNN (graph neural network) based prediction model*. Through experiments with benchmark circuits, it is shown that using our early IR-drop mitigation method is able to reduce IR-drop violations by 25.7% on average and Worst DVD (Dynamic Voltage Drop) by 7.1% on average while maintaining the same or even better chip PPA over that produced by the conventional commercial IR-drop mitigation flow.

I. INTRODUCTION

In principle, the advances in technology scaling are expected to reduce the level of operating voltage as the transistor dimension shrinks. In addition, it has been shown that the power density in modern circuits increases exponentially with technology scaling [1]. Thus, it is desirable to set the voltage level as low as possible, particularly for implementing AI and NPU chips. However, in practice, the operating voltage has not been lowered down to the level theoretically expected since setting such ideal voltage level is most likely to fail in meeting IR-drop constraint or require excessive hardware resources.

Mitigating IR-drop provides two distinct benefits: (1) *Stabilizing circuit operation*: If IR-drop mitigation is poorly made in a local region of circuits, the gates in the local region would have a voltage level that is a full voltage margin lower than that of the initial voltage setting, thereby increasing the gate delay, which is likely to fail in circuit operation. On the other hand, if IR-drop mitigation is well performed in a way to substantially retain the initial voltage, the circuit operation could be much more stable and reliable. (2) *Power saving*: A reduced setting of voltage margin by IR-drop mitigation can allow us to reset the supply voltage to a lower level. This results in saving the amount of dynamic power which quadratically changes with the level of supply voltage. Thus, consolidating IR-drop

mitigation in the design process is highly important in terms of reliable circuit operation as well as power saving.

Lots of IR-drop mitigation methods have been proposed in the literature. These methods can be broadly categorized into three groups:

- *Group 1* (reinforcing PDN (power delivery network)): It typically involves dense power grids and grid merging (e.g., [2]–[4]), which enable effective IR-drop reduction at the cost of increasing the routing resource usage, often leading to congestion and potential timing degradation in highly dense circuits.
- *Group 2* (re-optimizing placement at the post-layout): It attempts IR-drop improvement by re-optimizing placement employing techniques such as cell shifting or decap (decoupling capacitor) insertion, which are usually based on the IR-drop analysis at the post-layout stage, i.e., at the *ECO-power_integrity* stage (e.g., [3]–[7]). However, (*limitation 1*) the ECO-based methods suffer from limited flexibility due to the scarce metal/space resources and insufficient timing margin at this stage. Moreover, (*limitation 2*) it relies heavily on a full-chip IR-drop simulation on detailed layout, which is impractical or a very slow process for large-scale SoCs with billions of transistors. For instance, commercial tools such as Voltus require strict simulation time constraints (e.g., approximately $1000\times$ resolution_per_run).
- *Group 3* (co-optimizing placement and IR-drop mitigation at the pre-layout): It performs IR-drop mitigation at placement by adjusting cell locations (e.g., [8]–[10]). One critical *limitation* of those methods is that they didn't effectively reflect the post-layout cell power profile, resulting in losing the accuracy of IR-drop mitigation, thus, quality degradation.

Our work belongs to *group 3* (i.e., co-optimizing placement and IR-drop mitigation) and overcomes the limitation of the prior methods in *group 3*. To put it another way, we want to fully reap the benefits of *group 2* by effectively resolving limitations 1 and 2 in *group 2* as well as to save the metal resource for PDN construction. The key contribution items of this work are summarized as:

1. *IR-drop cost formulation at placement*: We analyze the sources of IR-drop and the degree of their impacts, based on which we devise a reliable IR-drop cost formulation and integrate it into the conventional optimization objec-

- tives to be used at the placement optimization stage. This overcomes limitation 1 of *group 2*.
2. *Employing GNN-based power prediction model at placement*: We develop an offline-trained GNN (graph neural network) based power prediction model to efficiently and accurately estimate the post-layout power behavior. Using our power prediction model is intended to address limitation 2 of *group 2* as well as the limitation of *group 3*.
 3. *Tightly and seamlessly linking our early IR-drop mitigation framework into a commercial EDA flow*: We build up early IR-drop mitigation module with above items 1 and 2 which can be seamlessly linked into any of commercial EDA flows, so that it can be practically ready to be used in industry. (In this work, we adopt Cadence physical design flow.)

II. MOTIVATION AND OVERALL FRAMEWORK

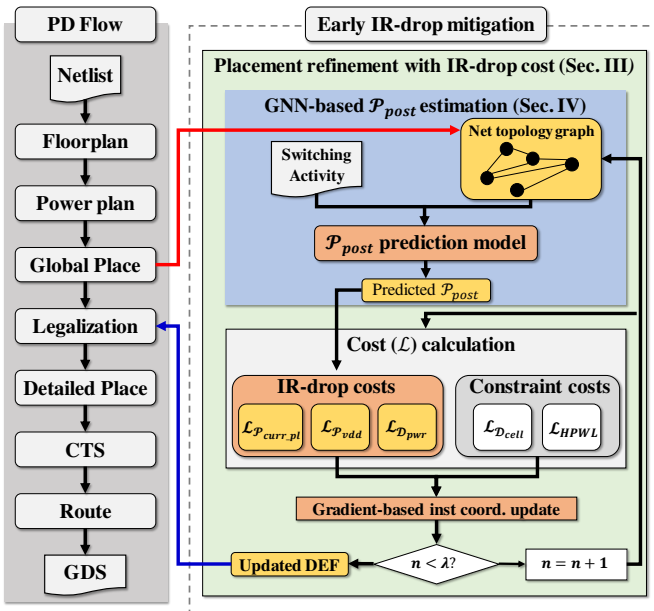


Fig. 1. Our proposed IR-drop mitigation framework.

Fig. 1 shows the overall flow of our proposed framework and how it is seamlessly integrated into the conventional physical design flow. The gray box on the left indicates the conventional design flow while the right side highlights our framework of IR-drop mitigation. Unlike the conventional ECO-based approaches which have tried to mitigate IR-drop at the post-route, our method directly performs IR-drop optimization immediately after the global placement. This choice is motivated by two reasons: (i) *global placement is the last stage where large-scale cell movements are still feasible*, and (ii) *early intervention can be free from the limited flexibility and excessive runtime overhead in ECO-based methods*.

Our framework consists of two main components:

- **Placement refinement engine with IR-drop cost**: After global placement, we refine cell instance locations with a new cost function that specifically considers IR-drop mitigation.

The cost function is formulated in a way to alleviate three primary sources of large IR-drop: (1) *power density imbalance*, (2) *power imbalance on VDD rail*, and (3) *long current paths*. By incorporating those factors into the conventional placement optimization, our method is able to preemptively mitigate IR-drop while preserving routability and timing. (Details on our IR-drop cost formulation will be explained in Sec. III.)

- **Post-layout power prediction model**: All IR-drop mitigation costs are inherently based on the distribution status of cell powers. Thus, accurately estimating cell powers is essential. However, the low correlation between the power measured from commercial tools at global placement and the power measured at post-layout [11] leads to an inaccurate optimization. To reduce this gap, we employ a Graph Neural Network (GNN) based method, trained offline, to predict post-layout cell power directly from early placement features. This ensures that the IR-drop cost is evaluated using realistic power values, thereby enabling reliable and effective optimization. (Details on our power prediction model will be provided in Sec. IV.)

By seamlessly linking these two components into a commercial EDA flow, our framework is able to support IR-drop mitigation at placement through the use of commercial EDA flow and tools, by which we can effectively overcome the limited flexibility in ECO-based methods as well as the inaccuracy issues of prior pre-layout methods.

III. IR-DROP COST FORMULATION

A. Sources of IR-drop

IR-drop arises when current flows through resistive power delivery network. Though the resistance of power rail itself is constant, in a local area, the amount of current momentarily pulled by the cell instances connected to the rail may significantly vary, which implies that power related factors must be optimized for mitigating IR-drop. However, *the conventional placement engines place primary importance on optimizing the metrics of HPWL, cell density, net congestion, and timing, and ignore optimizing IR-drop related objectives*. To address this limitation, we incorporate three new IR-drop related terms in the primary objectives. Those are (1) *minimizing power density*

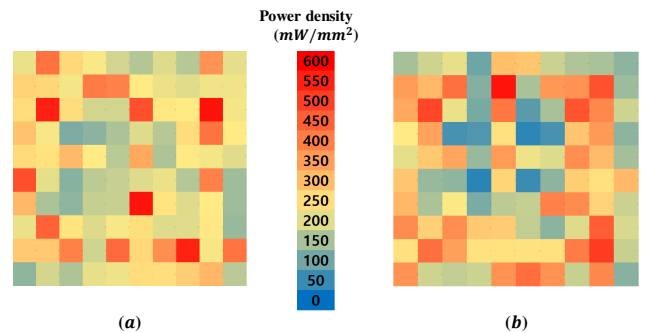


Fig. 2. Power density map of circuit AC97. (a) Power map obtained from vectorless power simulation. (b) Power map obtained from vectored power simulation.

imbalance, (2) minimizing power imbalance on VDD rails, and (3) shortening long current paths.

1. *Power density imbalance*: Since IR-drop is a local effect, power density imbalance causes a high spatial IR-drop variation. For example, Figs. 2(a) and (b) show a power distribution map of post-route layout of circuit AC97 generated by vectorless and vectored power simulation, respectively. It is highly desirable to reduce the peak power density by uniformly distributing the power density across the entire circuit layout as much as possible.

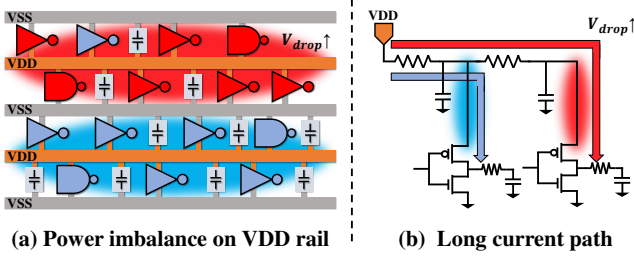


Fig. 3. Illustration of IR-drop aggravating factors. (a) Power delivery imbalance on VDD rail. (b) Long current path with power-hungry cell instance.

2. *Power imbalance on VDD rail*: Existence of VDD rail feeding many power-hungry cell instances causes a drastic IR-drop. As illustrated in Fig. 3(a), the upper VDD rail connected to power-hungry cell instances (i.e., red ones) must deliver more current than that to the lower VDD rail feeding the low-power cells (i.e., blue ones), resulting in a high risk of severe IR-drop at the upper VDD rail [12].
3. *Long current path*: IR-drop also varies according to the resistance on the current path length. Thus, shortening the paths that carry high current would help alleviate IR-drop. Fig. 3(b) illustrates this concept where the cell instance on the left, which is close to the current source, experiences a low resistance, causing a small IR-drop. On the other hand, the cell instance on the right, which is far from the source, undergoes a high IR-drop. Clearly, when power-hungry cells are located far from the current source, resistive losses are accumulated along the current delivery path, causing a significant IR-drop [13], [14].

B. Cost Function Formulation for Mitigating IR-drop

Our IR-drop aware cost function C_{tot} to be minimized in the placement optimization is defined as:

$$C_{tot} = \sum_{C_i \in \mathcal{L}} w_i \cdot C_i, \quad (1)$$

$$\mathcal{L} = \{D_{pwr}, P_{vdd}, P_{curr_pl}, HPWL, D_{cell}\},$$

where \mathcal{L} is the collection of placement cost terms and w_i is a weighting factor of cost $C_i \in \mathcal{L}$.

HPWL and D_{cell} are classical objectives that have been widely employed in analytic placement [15] while the remaining three terms are newly introduced to directly address the major sources of IR-drop. Precisely, \mathcal{D} denotes a density term: D_{cell} for cell density and D_{pwr} for power density. Similarly, \mathcal{P}

denotes a power-related term: P_{vdd} represents the row-by-row imbalance on power-hungry cell instances along VDD rails, and P_{curr_pl} accounts for current path length awareness by encouraging power-hungry cell instances to be placed close to the power sources. The interaction among these terms enables IR-drop aware placement as follows:

- D_{pwr} : A power density regularizer that penalizes non-uniform power distribution. This term suppresses the formation of IR-drop hotspots caused by **power density imbalance**.
- P_{vdd} : A row-level constraint that discourages gathering of power-hungry cell instances along the same VDD rail. This directly mitigates **power imbalance across VDD rails**.
- P_{curr_pl} : A current path length aware term that encourages power-hungry cells to be placed close to power sources while guiding low-power cells far away. This addresses the problem of **long current paths**.
- HPWL: A smooth approximation on net wirelength, which is used to shorten interconnects and improve timing closure.
- D_{cell} : A traditional cell density regularizer that ensures uniform spreading of cells across the placement region. This term alleviates congestion overhead and preserves sufficient routing resources.

(1) **Formulation of D_{pwr}** : It indicates the variance of grid-based power density in placement. We formally defined it as:

$$D_{pwr} = Var\{\hat{D}_{g_j}\}_{g_j \in M}, \quad (2)$$

$$\hat{D}_{g_j} = \frac{\sum_{cell_i \in U} P_{cell_i} \cdot exp(dist(cell_i, g_j))}{\sum_{cell_i \in U} P_{cell_i}} \quad (3)$$

in which M and U are respectively the set of grids and cell instances in the placement. $dist(cell_i, g_j)$ returns the Manhattan distance between the centers of grid g_j and instance $cell_i$, and P_{cell_i} is the power number of $cell_i$.

Minimizing D_{pwr} in Eq.2 suppresses and flattens the grid regions with high power concentration that are unfavorable to IR-drop. For example, as illustrated in Fig. 4(a), the power-hungry cell instances initially gathered in a local region are

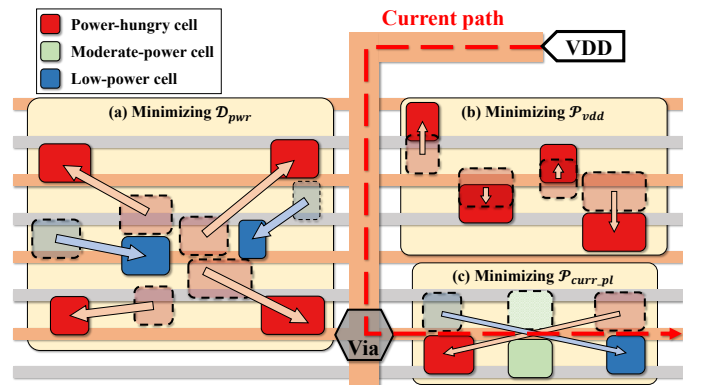


Fig. 4. Impact of cost function terms on cell placement.

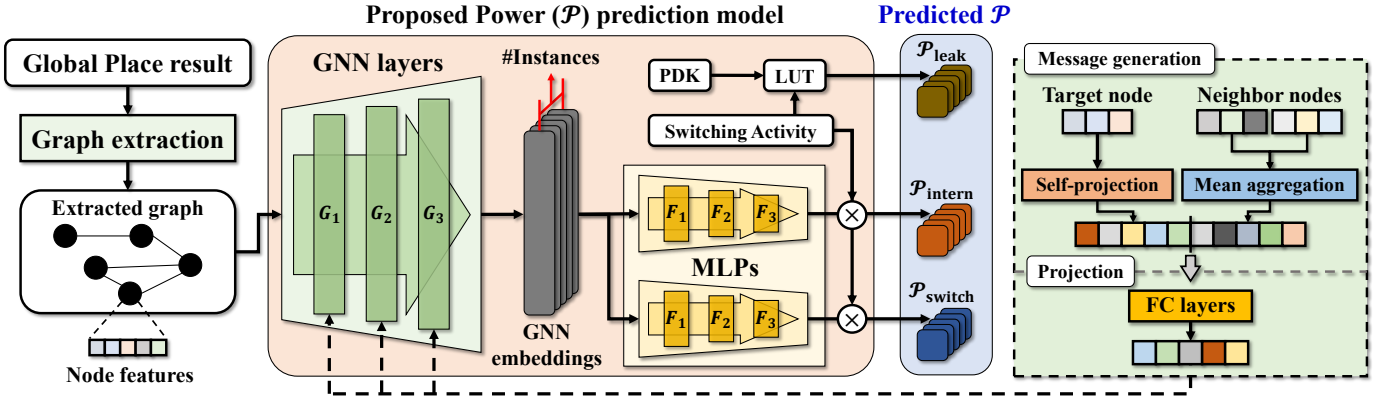


Fig. 5. Proposed architecture of cell power prediction model.

spread out by minimizing \mathcal{D}_{pwr} while the low-power cells are placed in between the power-hungry cells, thereby balancing the overall power density distribution.

(2) **Formulation of \mathcal{P}_{vdd} :** It enforces row-level power uniformity, ensuring that power-hungry cell instances are not overly fed to a common VDD rail. We formally define it as:

$$\mathcal{P}_{vdd} = \text{Var}\{\hat{P}_{row_j}\}_{row_j \in R}, \quad (4)$$

$$\hat{P}_{row_j} = \frac{\sum_{cell_i \in U} P_{cell_i} \cdot \exp\left(-\frac{(y_{cell_i} - y_{row_j})^2}{\rho}\right)}{\sum_{cell_i \in U} P_{cell_i}} \quad (5)$$

where R is the set of VDD rails. y_{cell_i} and y_{row_j} respectively denote the y -coordinate position of $cell_i$ and row_j .

As illustrated in Fig. 4(b), minimizing \mathcal{P}_{vdd} enables the power-hungry cells clustered on one VDD rail to redistribute them toward nearby rails, achieving a balanced current demand.

(3) **Formulation of \mathcal{P}_{curr_pl} :** It enforces power-hungry cell instance to have a short current path, as illustrated in Fig. 4(c) where the power-hungry cell is moved to the location that makes its current path shorten. We formally define it as:

$$\mathcal{P}_{curr_pl} = \sum_{cell_i \in U, l_i \in Layers} \frac{(d_{x_i}^2 + d_{y_i}^2) \cdot P_{cell_i}}{w(l_i)} \quad (6)$$

where x_i and y_i are the x - and y -coordinates of placement location of $cell_i$ and $w(l_i)$ is a weighting factor on metal layer l_i that reflects the contribution of l_i to PDN. The smoothed distances d_{x_i} and d_{y_i} are computed by:

$$d_{x_i} = -\frac{1}{\alpha} \log \sum_{x_j \in VDD_x} \exp\left(-\alpha \sqrt{(x_i - x_j)^2 + \varepsilon}\right), \quad (7)$$

$$d_{y_i} = -\frac{1}{\alpha} \log \sum_{y_j \in VDD_y} \exp\left(-\alpha \sqrt{(y_i - y_j)^2 + \varepsilon}\right), \quad (8)$$

in which VDD_x (VDD_y) indicates all horizontal (vertical) coordinates of vertical (horizontal) power rails. α is a smoothing term that makes the smoothed distance be similar to the original value, and ε is a minimal term that prevents the gradient vanishing due to the square root used for smoothed absolute function.

Both α and ρ are hyperparameters in our framework. We also use this smoothed distance function in computing HPWL term.

IV. GNN-BASED POWER PREDICTION MODEL

A. Model Architecture

The architecture of our proposed cell power prediction model is shown in Fig. 5. To extract placement features, first, we construct a graph representation on the global placement result as follows:

1. We extract all cell instances and arcs from the input circuit. Let $U = \{cell_1, cell_2, \dots\}$ be the set of all extracted cell instances and $A = \{arc_1, arc_2, \dots\}$ be the set of all extracted arcs.
2. We construct an undirected graph $G = (V, E)$ such that $|V| = |U|$ where each node $v_j \in V$ corresponds to a distinct instance $cell_j \in U$. Likewise, $|A| = |E|$ where each edge $e_k \in E$ corresponds to distinct arc $arc_k \in A$.
3. We assign the features listed in Table I to every node.

TABLE I
NODE FEATURES USED IN OUR GNN MODEL.

#	Feature name	Dim	Feature explanation
1	Position	2	Coordinate of instance normalized by the core area
2	\mathcal{P}_{intern}	1	Tool estimated internal power in global placement stage
3	\mathcal{P}_{switch}	1	Tool estimated switching power in global placement stage
4	Fanout	1	Fanout of instance
5	Cell type	1	Cell type index in liberty file
6	Input Cap	1	Sum of input pin capacitance
7	Max. Output Cap	1	Maximum output load capacitance
8	Worst slack	1	Worst slack of cell

Starting from the extracted graph shown on the left side in Fig. 5, we compute node embeddings, one for each cell instance, using three-hop GraphSAGE [16] layers. The produced embeddings are then processed by two separate multi-layer perceptrons (MLP), as shown in the middle in Fig. 5, each predicting P_{intern_i} and P_{switch_i} of $cell_i$. ReLU activation function is then applied at the ends of the FC layers except the last one. On the other hand, P_{leak_i} is estimated from the PDK using the cell instance information. Then, P_{cell_i} , which is to be used in our cost formulations in Eqs. 3, 5, 6 is computed by

$$P_{cell_i} = P_{leak_i} + P_{intern_i} + P_{switch_i}. \quad (9)$$

Note that since training is performed at the cell-level, the total number of training samples is equal to the number of cell instances across all training designs. Thus, our approach

is able to easily acquire a sufficient training dataset from a few designs.

B. Integrating our GNN Prediction Model into Placement Optimization Engine

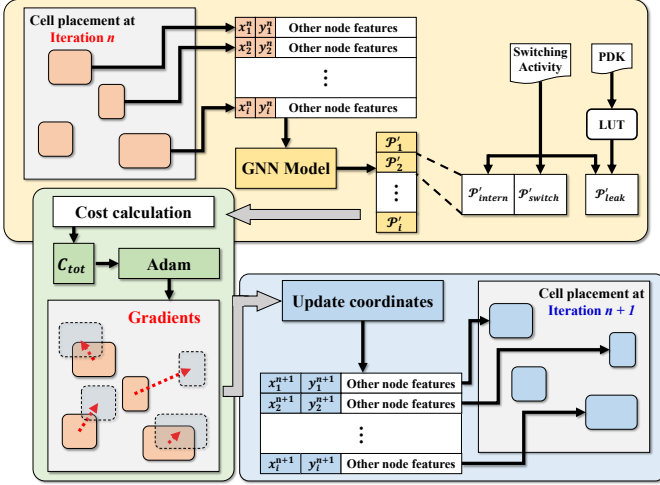


Fig. 6. Linking our GNN model to IR-drop aware placement optimization.

Once our GNN model is trained offline, it is integrated into our IR-drop aware placement optimization flow, as illustrated in Fig. 6. At each iteration of placement refinement, every cell instance position (x, y) is updated. The cell position updating procedure proceeds as follows:

1. Each iteration begins with the prediction of post-layout power components on every cell instance (i.e., P_{leak_i} , P_{intern_i} , P_{switch_i}) by using our GNN-based prediction model with updated node features of cell instances.
2. Using the predicted post-layout powers, the IR-drop mitigation cost is computed according to the placement cost formulation C_{tot} in Eq.1.
3. The gradient of each instance with respect to the cost function is then calculated using the Adam optimizer [17].
4. Finally, each cell instance coordinate (x, y) is updated based on the computed gradients.

These four steps (1–4) are repeated until the iteration count reaches upper bound Γ , which was set to 100 in this work.

By exploiting our GNN based power predictor rather than using an inaccurate early-stage estimation provided by commercial tools, our framework is able to perform much more reliable IR-drop mitigation. In fact, as revealed in the experiments, our proposed early IR-drop mitigation method is able to well minimize altogether the three dominant IR-drop sources namely (1) *power density imbalance*, (2) *power imbalance across VDD rails*, and (3) *long current paths* by using cost function C_{tot} in Eq.1 with accurate power estimation.

V. EXPERIMENTAL RESULTS

All experiments are performed on a server equipped with an AMD Ryzen 3970X processor (2.2GHz) and 128GB of memory. Seven benchmark designs from OpenCores [18] are evaluated in our study. These designs are implemented using

ASAP7 PDK [19] which is 7nm FinFET technology node. The clock frequency (f_{clk}) and chip utilization ($Util.$) set for each design are specified in Table II.

TABLE II
SUMMARY OF BENCHMARKS USED IN OUR STUDY AND **IR-drop unaware** CONVENTIONAL PD FLOW (**Org**) FOR COMPARISON.

Benchmarks	f_{clk} (GHz)	Util. (%)	#cells	IR-drop unaware conventional PD flow result (Org)				
				#viol.	Worst DVD (mV)	f_{eff} (GHz)	Power (mW)	Area (μm^2)
SPI	1.43	60	1,952	489	164.17	1.44	0.59	3,116
SHA256	1.67	60	9,590	5,197	172.77	1.66	4.44	16,633
AC97	1.67	80	7,992	1,568	139.62	1.67	5.54	17,321
AES_CIPHER	1.67	60	14,773	6,923	156.57	1.66	2.30	18,173
WB_CONMAX	1.25	50	20,998	1,793	134.39	1.28	3.04	28,119
DES3	1.67	60	51,160	5,729	112.03	1.66	29.57	89,629
AES128	1.67	60	130,614	46,043	136.67	1.66	35.13	196,525

In the implementation flow, we used Synopsys Design Compiler [20] for logic synthesis and Cadence Innovus [21] for floorplanning, placement, clock tree synthesis, and routing. We carried out simulation and analysis using Cadence Xcelium [22] by generating testbench vectors on benchmark circuits. Then, we used Cadence Voltus [23] for dynamic vectored power rail analysis at the post-layout stage.

In our framework, hyperparameter α in Eq.7 and ρ in Eq.8 was set to 20 and ρ in Eq.5 to the length of the diagonal on the grid for each design. The GNN layers in Fig. 5 progressively expand the node embedding dimension from 10 to 128: G_1 maps 10-dimensional node features to 32, G_2 to 64, and G_3 to 128. Subsequently, the FC layers compress the embeddings to produce a single power prediction: F_1 reduces 128 to 64, F_2 to 32, and F_3 to 1. The post-layout power prediction model was trained for 1,000 epochs using a learning rate of 0.001.

A. Assessment on Accuracy of Power Prediction

We trained our GNN-based power prediction model using six benchmark designs (SPI, SHA256, AC97, AES_CIPHER, WB_CONMAX, and DES3). For evaluation, we employed a leave-one-out strategy where the model was trained on the remaining circuits excluding the target circuit, and then tested on the excluded circuit.

TABLE III
COMPARISON OF EARLY POWER PREDICTION ERRORS (RMSE) BY COMMERCIAL TOOL [21] AND OURS USING GNN WITH RESPECT TO THE POWER AT POST-ROUTE.

Benchmarks	P_{intern}		P_{switch}	
	Innovus [21]	Ours	Innovus [21]	Ours
SPI	42.32	13.09	42.46	36.83
SHA256	31.70	27.20	55.13	50.81
AC97	55.14	2.78	46.42	5.81
AES_CIPHER	50.18	40.80	113.70	118.32
WB_CONMAX	19.81	9.86	38.63	33.40
DES3	13.76	7.65	76.54	70.63
Average	35.49	16.90	62.15	52.63

Table III shows a comparison of post-layout power prediction error (RMSE: Root Mean Square Error) between the commercial tool [21] and our GNN-based model at the global placement stage. Our power prediction model reduces the internal power error by an average of 52.4% (from 35.49 to 16.9) and the switching power error by 15.3% (from 62.15 to 52.63) over the commercial tool. This improvement justifies the construction of our IR-drop mitigation cost formulation on a more accurate power basis.

TABLE IV

IR-DROP AND PPA COMPARISON FOR IMPLEMENTATION BY A COMMERCIAL TOOL WITH IR-DROP MITIGATION FLOW (ECO) [7] & OUR FLOW (OURS).

Benchmarks	Conventional IR-drop mitigation flow (ECO) [7]						Early IR-drop mitigation flow (Ours)											
	#viol.	Worst DVD (mV)	Power (mW)	f_{eff} (GHz)	Area (μm^2)	Runtime (min)	#viol.		Worst DVD		Power		f_{eff}		Area		Runtime	
							Raw	Ratio	Raw	Ratio	Raw	Ratio	Raw	Ratio	Raw	Ratio	Raw	Ratio
SPI	498	149.91	0.59	1.44	3,116	20.2	334	0.67	139.71	0.93	0.59	1.01	1.44	1.00	3,095	0.99	7.7	0.38
SHA256	5,197	163.21	4.44	1.66	16,633	23.5	4,344	0.84	156.35	0.96	4.48	1.01	1.64	0.99	16,746	1.01	11.7	0.50
AC97	1,299	135.91	5.62	1.50	17,321	23.1	564	0.43	122.54	0.90	5.56	0.99	1.67	1.11	17,305	1.00	10.9	0.47
AES_CIPHER	6,924	155.47	2.30	1.66	18,173	27.0	5,355	0.77	136.62	0.88	2.33	1.01	1.66	1.00	18,278	1.01	12.1	0.45
WB_CONMAX	1,793	134.39	3.04	1.28	28,119	61.5	1,009	0.56	129.20	0.96	3.05	1.00	1.28	1.01	28,131	1.00	18.0	0.29
DES3	6,386	112.95	29.76	1.58	89,629	73.6	448	0.07	106.92	0.95	29.61	0.99	1.66	1.05	89,644	1.00	66.8	0.91
AES128	46,689	138.20	35.32	1.57	196,525	427.7	39,058	0.84	128.18	0.93	35.35	1.00	1.66	1.06	196,202	1.00	191.4	0.45
Average	9,827	141.43	11.58	1.53	52,788	93.8	7,302	0.74	131.36	0.93	11.57	1.00	1.57	1.03	52,772	1.00	45.5	0.49

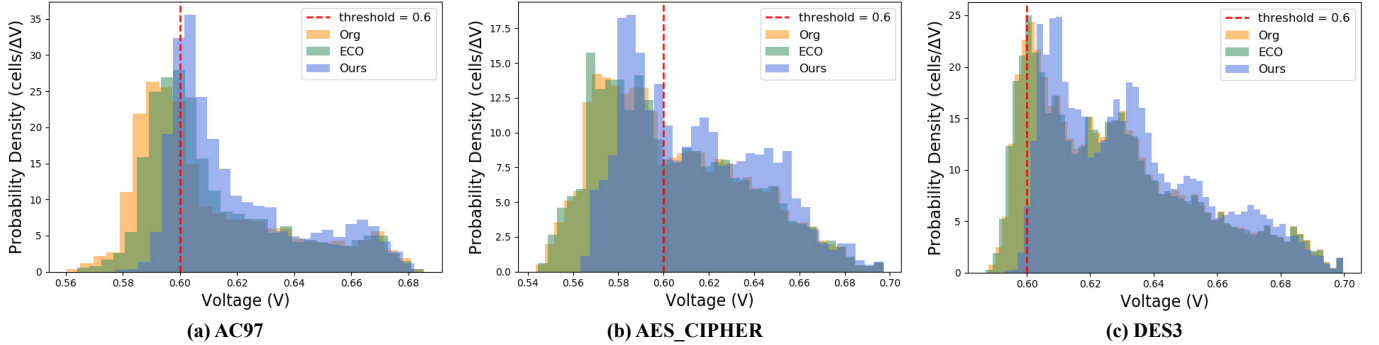


Fig. 7. Probability density distribution of cell-level Effective Instance Voltage (EIV).

B. Assessment on Effectiveness of IR-drop Mitigation

Table II includes baseline implementations (**Org**) which are obtained from the conventional Innovus physical design (PD) flow that prioritizes PPA without considering IR-drop mitigation. Table IV shows a comparison of IR-drop measures and PPA of the implementations produced by a commercial IR-drop aware PD flow (**ECO**) in [7] and our proposed flow (**Ours**). For **ECO**, the results were generated by applying the placement optimization method in [7], involving four iterations of IR-drop mitigation during placement, followed by routing to obtain a final set of post-optimized outcomes, which are shown in Table IV.

Note that both Ours and ECO used the same switching-activity file and all physical design flow settings were identical. We take the power data from the vectorless Innovus power report while we obtain the performance data by calculating the effective clock frequency $f_{eff} = \frac{1}{t_{clk} - t_{wns}}$ where $t_{clk} = 1/f_{clk}$ in Table IV and t_{wns} is the worst negative slack value at post-route.

Overall, our early IR-drop mitigation flow consistently improves IR-drop metrics: using 100mV as the pass/fail threshold, our flow is able to reduce the number of IR-drop violations (#viol.) by 25.7% on average in comparison with that by a state-of-the-art commercial IR-drop mitigation flow. In addition, it reduces the worst IR-drop, measured by Worst Dynamic Voltage Drop (DVD), by 7.1% on average. More importantly, these gains are achieved with no degradation in design PPA and **Ours** requires significantly less runtime (Runtime) compared to the **ECO** flow.

Finally, Fig. 7 shows histograms of Effective Instance Voltage (EIV) for circuits AC97, AES_CIPHER, and DES3. The **ECO**-based IR-drop aware placement optimization [7]

primarily targets the most vulnerable cell instances identified by simulation. As a result, it can marginally improve the worst EIV, resulting in a slight distribution shift from the distribution of **Org**, as shown in Fig. 7. In contrast, **Ours** integrates an IR-drop cost into the global placement (early) step, so that the IR-drop mitigation can be performed more extensively over all cell instances, which results in the histograms exhibiting a further right-shift than that of **ECO**, decreasing the standard deviation of EIV by 9% on average.

VI. CONCLUSION

This work proposed a new design methodology of early IR-drop mitigation. Three distinct contributions were (1) *a comprehensive IR-drop cost formulation* to be used at the global placement through a precise analysis of the sources of IR-drop and (2) *a development of ML (machine-learning) driven post-layout IR-drop prediction model*. In addition, our IR-drop mitigation flow was (3) *seamlessly linked into a state-of-the-art commercial EDA flow*. In summary, our early IR-drop mitigation flow was able to reduce the number of IR-drop violations and the worst IR-drop by 25.7% and 7.1%, respectively over that of conventional early IR-drop flow, even with identical or improved design PPAs.

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