

# Optimal Compilation of Syndrome Extraction Circuits for General Quantum LDPC Codes

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**Abstract**—Quantum error correcting codes (QECC) are essential for constructing large-scale quantum computers that deliver faithful results. As strong competitors to the conventional surface code, quantum low-density parity-check (qLDPC) codes are emerging rapidly: they offer high encoding rates while maintaining reasonable physical-qubit connectivity requirements. Despite the existence of numerous code constructions, a notable gap persists between these designs—some of which remain purely theoretical—and their circuit-level deployment.

In this work, we propose Auto-Stabilizer-Check (ASC), a universal compilation framework that generates depth-optimal syndrome extraction circuits for arbitrary qLDPC codes. ASC leverages the sparsity of parity-check matrices and exploits the commutativity of X and Z stabilizer measurement subroutines to search for optimal compilation schemes. By iteratively invoking an SMT solver, ASC returns a depth-optimal solution if a satisfying assignment is found, and a near-optimal solution in cases of solver timeouts. Notably, ASC provides the first definitive answer to one of IBM’s open problems: for all instances of bivariate bicycle (BB) code reported in their work, our compiler certifies that no depth-6 syndrome extraction circuit exists.

Furthermore, by integrating ASC with an end-to-end evaluation framework—one that assesses different compilation settings under a circuit-level noise model—ASC reduces circuit depth by approximately 50% and achieves an average 7x-8x suppression of the logical error rate for general qLDPC codes, compared with as-soon-as-possible (ASAP) and coloration-based scheduling. ASC thus substantially reduces manual design overhead and demonstrates its strong potential to serve as a key component in accelerating hardware deployment of qLDPC codes.

**Index Terms**—quantum computing, quantum error correction

## I. INTRODUCTION

Quantum computing harnesses the unique principles of quantum mechanics and holds the potential to deliver significant speedups for various hard problems [1]–[4]. While there is no “free lunch” in quantum computer development—given the inherently noisy environment and the fragility of qubits—quantum error correction (QEC) enables reliable quantum computing by using redundant physical qubits for logical encoding [5]–[7], thereby enabling the high-fidelity storage and processing of quantum information [8].

Building a robust, fault-tolerant quantum computer depends not only on high-performance QECCs [9]–[12] and efficient decoding architectures [13]–[18], but also on the effective design

of syndrome extraction circuits, which is a compiler optimization task serving as a crucial bridge between code abstraction and physical gate execution. While bespoke and experimentally validated [11], [12], [19], hand-designed syndrome extraction circuits exist for specific codes—such as the depth-4 surface code or depth-7 BB code—these require substantial manual efforts and experience. Consequently, a compiler capable of generating optimal circuits for arbitrary qLDPC codes remains a critical missing piece in the field.

Previous compilers designed for NISQ are not tailored for QEC circuits. Compilers such as Qiskit [20] and TKet [21] utilize peephole optimization based on gate cancellations and commutativity rules within local subcircuits and schedule gate sequences in the as-soon-as-possible (ASAP) approach. However, they cannot lead to non-trivial optimization effects for syndrome extraction circuits, as they only consider local commutativity optimization opportunities. Tremblay et al. [22] observed the commutativity within the same-type stabilizer checks and introduced a coloration-based method to schedule X and Z stabilizer checks of the CSS code separately. However, the applicability of this method is limited: (1) It is only specified for CSS code, rather than general qLDPC codes which may contain both X and Z components in one stabilizer check. (2) Although it gives optimal scheduling for X and Z stabilizer checks separately, the compiled circuit is about 2× deeper than the optimal solution. For example, an X-Z separated scheduling of the surface code leads to a depth-8 circuit, which is 2× compared with the best manually designed depth-4 circuit.

Exploiting the sparsity and structural regularity of qLDPC codes, we show that the general constraints of syndrome extraction circuits can be readily expressed as a satisfiability modulo theories (SMT) problem and solved efficiently using modern SMT solvers. Based on this observation, we propose ASC for compilation and end-to-end evaluation of arbitrary qLDPC codes. In summary, our key contributions are:

- We analyze and derive a set of general rules for the syndrome extraction circuits of arbitrary qLDPC codes, providing the theoretical foundation of our compiler.
- Utilizing the SMT solver, we implement a lightweight

yet efficient compiler based on our general rules. This compiler not only significantly reduces human-design overhead but also, for the first time, resolves an open problem in [12] by providing a definite answer that no depth-6 circuit exists for their listed BB codes.

- We develop a comprehensive compilation and evaluation framework, comprising an SMT-based scheduler, a circuit-level noise simulator, and a decoding pipeline for logical level evaluation. Our evaluation demonstrates that ASC can effectively reduce the depth of syndrome extraction circuits and logical error rates, providing further support for theoretical analysis and experimental demonstration.

We note that recent works [23], [24] explore more comprehensive fault-tolerant circuit compilation frameworks or adopt more advanced techniques such as ancilla bridge. Our work is developed independently and instead focuses on a more concise framework, which enables future integration of constraints from different fault-tolerance considerations or hardware platforms. To facilitate future research, we open-source both our implementation and evaluation data at <https://github.com/iqubit-org/Auto-Stabilizer-Check>.

## II. BACKGROUND

### A. Stabilizer Formalism

The concept of *stabilizer* is fundamental to QEC and a certain class of QECCs—stabilizer codes. Rooted in the mathematical frameworks introduced by Gottesman [25], the stabilizer formalism enables describing and manipulating quantum states and operations via a group-theoretic approach. Herein we briefly introduce the stabilizer formalism:

**Definition 1** (Pauli Group). *The Pauli group  $P_n$  is composed of  $n$ -fold tensor products of  $I, X, Y, Z$ , with the global phase of  $\pm 1$  or  $\pm i$ .*

**Definition 2** (Stabilizer Group). *Let  $S \subseteq P_n$  be a subgroup of the  $n$ -qubit Pauli group that does not contain  $-I$ . The subspace*

$$V_S := \{|\psi\rangle \in \mathcal{H}_{2^n} \mid s|\psi\rangle = |\psi\rangle, \forall s \in S\} \quad (1)$$

*is stabilized by  $S$ , and  $S$  is referred to as the stabilizer group. Accordingly, a stabilizer code  $\mathcal{C}$  is defined as the codespace stabilized by a corresponding stabilizer group.*

**Definition 3** (Normalizer). *The normalizer of a stabilizer group  $S \subseteq P_n$  is defined as*

$$N(S) = \{n \in P_n \mid ns = sn, \forall s \in S\}. \quad (2)$$

Now we can consider all Pauli errors  $E \in P_n$  occurring on stabilizer codes. An error  $E$  is detectable if it anti-commutes with some  $s \in S$  ( $Es = -sE$ ), thus producing a non-zero syndrome measurement outcome. On the other hand, if  $E \in N(S) \setminus S$ ,  $E$  commutes with all  $s \in S$  and acts as a logical operator on the codespace, making it undetectable by any syndrome measurement. The code distance  $d$  is therefore the minimum weight of such operators in  $N(S) \setminus S$ , ensuring errors of weight less than  $\lfloor d/2 \rfloor$  can be corrected.

TABLE I  
STABILIZER GENERATORS OF THE STEANE CODE

$g_1$	X	X	X	X	I	I	I
$g_2$	X	X	I	I	X	X	I
$g_3$	X	I	X	I	X	I	X
$g_4$	Z	Z	Z	Z	I	I	I
$g_5$	Z	Z	I	I	Z	Z	I
$g_6$	Z	I	Z	I	Z	I	Z

### B. Quantum Low-Density Parity-Check Codes

We use the notation  $[[n, k, d]]$  to denote the physical qubit number  $n$ , logical qubit number  $k$  and code distance  $d$  of a stabilizer code. A stabilizer code  $\mathcal{C}$  has  $n - k$  independent generators  $\{g_i\}_{n-k}$ , also known as *stabilizer checks*. For example, the  $[[7, 1, 3]]$  Steane code [26] has the stabilizer generators in Table I, and can be represented as the *Tanner Graph* [27].

This representation naturally leads to the *parity check matrix* formulation of the Steane code

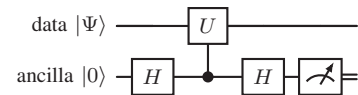
$$H_X = H_Z = \begin{bmatrix} 1 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 1 & 1 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 & 1 \end{bmatrix} \quad (3)$$

where an entry of 1 indicates a non-identity Pauli operator in  $\{g_i\}$ . Since the Steane code is a CSS code, its stabilizer check can be specified by two independent parity-check matrices  $H_X$  and  $H_Z$ . More generally, a stabilizer code can be represented in the *Binary Symplectic Form* (BSF) as a single matrix  $H$  that encodes X, Z or X-Z crossed stabilizers. The shape of  $H$  is  $(m, 2n)$ , denoting  $m$  stabilizer checks on  $n$  data qubits, where  $2n$  is used to represent both X and Z components.

qLDPC codes are also a family of stabilizer codes, with the weight of *stabilizer checks* bounded by a constant [27]. In other words, the Hamming weight of each row and each column in  $H$  is bounded by a constant factor, corresponding to the maximum degree  $\Delta(G)$  of the *Tanner Graph*  $G$ .

### C. Syndrome extraction circuit

Given a stabilizer check  $g \in P_n$  and an  $n$ -qubit state  $|\Psi\rangle$ , syndrome extraction refers to the process of measuring the eigenvalue of  $g$  on  $|\Psi\rangle$ . A standard stabilizer check is performed by the syndrome extraction circuit, also known as a syndrome measurement circuit [11], which is driven from a standard Hadamard test circuit in [28]



that entangles ancilla and data qubits through CX or CZ gates to measure the eigenvalue of  $g$  on  $|\Psi\rangle$ , as depicted in Fig. 1. The syndrome extraction outcomes from ancilla qubits are then decoded to determine the subsequent logical feedback [8], constituting one of the key components of fault-tolerant quantum computing (FTQC). Since quantum systems are inherently subject to noise—including decoherence, gate imperfections, and environmental interference—that accumulates over the course of circuit execution, longer syndrome extraction circuits significantly increase the risk of introducing

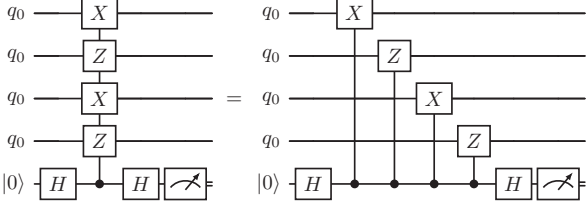


Fig. 1. Illustration of Hadamard test and stabilizer measurement of a given stabilizer generator  $g = XZXZ$  as an example.

additional, uncorrectable errors before error syndromes can be accurately measured. Therefore, optimizing syndrome extraction circuits is crucial for QEC.

### III. GENERAL RULES OF SYNDROME EXTRACTION CIRCUIT FOR QLDPC CODES

Consistent with [11], [12], we define circuit depth as the number of non-overlapping CX (CZ) layers. We exclude single-qubit gates as they are significantly easier to implement and typically introduce negligible error compared to two-qubit gates. This definition motivates the following questions:

- 1) What is the minimum depth required for the syndrome extraction circuit of a general qLDPC code?
- 2) How can we optimize the circuit depth for the syndrome extraction of a general qLDPC code?

#### A. General rules

There are two rules for a syndrome extraction circuit:

- Each qubit can participate in at most one two-qubit gate per TICK, where a TICK represents the minimum time step in our circuit. For example, the stabilizer check  $XZXZ$  in Fig. 1 requires at least 4 TICKs to execute.
- The stabilizer check process must align with  $H$  to ensure correctness of the QEC process. We will show that the CX/CZ gates cannot be performed in an arbitrary order.

#### B. Lower bound

It is obvious that the lower bound of the syndrome extraction circuit equals the maximum degree of the corresponding *Tanner Graph*, namely  $\Delta(G)$ . Taking the Steane code as an example,  $\Delta(G) = 6$ , as data qubit  $q_0$  connects 3 X checks and 3 Z checks, each edge represents a two-qubit gate between  $q_0$  and one ancilla qubit, thus the minimum number of TICKs to execute all two-qubit gates is at least 6.

#### C. X-Z commutativity

As we have mentioned before, an X-Z separated scheduling is far from optimal. Examining the depth-4 syndrome extraction circuit of the surface code [19], we find that there is ample room for optimization. We plot some examples in Fig. 2, where  $a_1$  and  $a_2$  denote two ancilla qubits, corresponding to  $XXXX$  and  $ZZZZ$  stabilizer checks, respectively. It turns out that swapping the order of CX and CZ twice results in a circuit (Fig. 2 (b)) that is equivalent to the circuit in Fig. 2 (a). This equivalence allows more CX and CZ gates to be executed in parallel. In contrast, swapping their order only once yields a

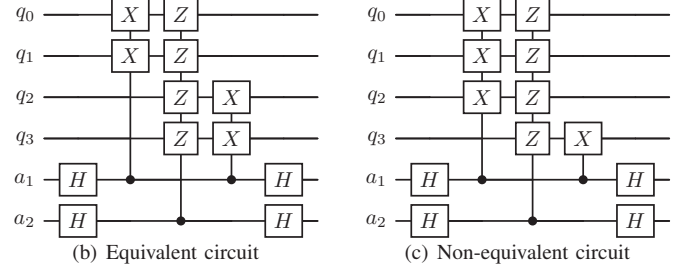
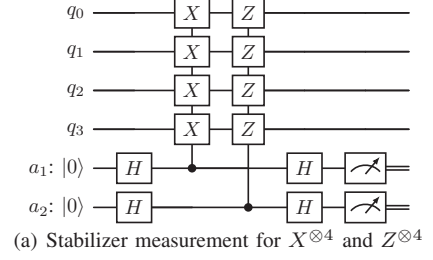


Fig. 2. Examples of equivalent and non-equivalent stabilizer measurement circuits for stabilizer checks  $g_1 = XXXX$  and  $g_2 = ZZZZ$ .

circuit (Fig. 2 (c)) that is inequivalent to the circuit in Fig. 2 (a), owing to their anti-commutativity. This observation motivates the following proposition:

**Proposition 1 (X-Z commutativity).** *For any pair of stabilizer checks, if the parity of the inversion number in the CX-CZ order across their shared data qubits is even, then all corresponding syndrome extraction circuits are equivalent.*

We provide a concise proof sketch here. Suppose  $|\Phi\rangle = \sum_{x=0}^{2^n-1} c_x |x\rangle$  is an  $n$ -qubit stabilizer state on data qubits  $\{q_1 \dots q_n\}$  and  $\sum_{x=0}^{2^n-1} |c_x|^2 = 1$ , where  $c_x \in \mathbb{C}$  are the complex amplitudes associated with each basis state  $|x\rangle$ . Considering two stabilizers checked by ancilla qubits  $a_1, a_2$ , the joint state of these  $n+2$  qubits can be written as:

$$|\Phi\rangle |+\rangle |+\rangle = \frac{1}{2} \sum_{x=0}^{2^n-1} \sum_{y_1=0}^1 \sum_{y_2=0}^1 c_x |x y_1 y_2\rangle \quad (4)$$

where  $x y_1 y_2$  denotes the concatenation of an  $n$ -bit string  $x = x_1 \dots x_n$ , 1-bit strings  $y_1$  and  $y_2$ , thus each basis state in (4) can be viewed as  $|x y_1 y_2\rangle = |x_1 \dots x_n y_1 y_2\rangle$ . Without loss of generality, suppose there exists a CX gate between  $a_1$  and  $q_k$ , a CZ gate between  $a_2$  and  $q_k$ . Consider exchanging the order of this  $CX_{a_1, q_k}$  and  $CZ_{a_2, q_k}$ , which share the data qubit  $q_k$ :

- If CX operates ahead of CZ:

$$|x_1 \dots y_2\rangle \xrightarrow{CX_{a_1, q_k}} |x_1 \dots (x_k \oplus y_1) \dots y_2\rangle \xrightarrow{CZ_{a_2, q_k}} (-1)^{y_2(x_k \oplus y_1)} |x_1 \dots (x_k \oplus y_1) \dots y_2\rangle \quad (5)$$

- If CZ operates ahead of CX:

$$|x_1 \dots y_2\rangle \xrightarrow{CZ_{a_2, q_k}} (-1)^{y_2 x_k} |x_1 \dots y_2\rangle \xrightarrow{CX_{a_1, q_k}} (-1)^{y_2 x_k} |x_1 \dots (x_k \oplus y_1) \dots y_2\rangle \quad (6)$$

Note that (5) and (6) differ only by  $(-1)^{y_1 y_2}$ . Therefore, an even number of CZ-CX order exchanges will cancel out the

accumulated phase  $(-1)^{y_1 y_2}$ , yielding a state equivalent to that obtained from separate stabilizer measurements by  $a_1$  and  $a_2$ . Crucially, Proposition 1 is not limited to the CSS code and applies generally to any type of stabilizer checks, i.e., those involving mixed-X/Z stabilizer generators.

#### D. Formulated constraints

We formulate the fundamental constraints of syndrome extraction circuits as follows:

**Constraint 1.** At each TICK, a qubit may participate in at most one two-qubit gate  $\implies$  unique occupation.

**Constraint 2.** For each  $H[i][j] = 1$ , there must exist exactly one corresponding two-qubit gate  $\implies$  integrality of stabilizer check.

**Constraint 3.** For any stabilizer check pair, the parity of the inversion number in the CZ-CX order over their shared data qubits should be even  $\implies$  correctness of commutativity.

Note that these constraints serve as general rules for constructing and scheduling syndrome measurement circuits of qLDPC codes, not limited to CSS codes. At this point, we have established concise and complete theoretical guidance for our compiler.

## IV. IMPLEMENTATION

Leveraging the constraints formulated in Section III, we propose ASC's framework, which enables global scheduling of all types of stabilizer checks. For most near-term qLDPC codes, the sparsity of the parity-check matrix  $H$  allows it to be efficiently handled by modern SMT solvers. The workflow of ASC is illustrated in Fig. 3, comprising an SMT-based scheduler in the central processing module, a circuit-level noise simulator for evaluation, and an automated circuit filter.

### A. SMT-based scheduler

1) *Definition of variables:* The SMT problem formulation of our scheduling task is built upon the following variables:

**(Boolean Variable)**  $H$  has the shape of  $(m, 2n)$ : the parity-check matrix of the qLDPC code.  $H[i][j] = 1 \vee H[i][j+n] = 1$  represents that the  $i$ -th ancilla qubit has to interact with the  $j$ -th data qubit at some TICK and only once.  $m$  is the number of ancilla qubits (number of stabilizer generators);  $n$  is the number of data qubits.

**(Boolean Variable)**  $A$  has the shape of  $(m, n, T_{max})$ :  $A[i][j][k] = 1$  if the  $i$ -th ancilla qubit has to interact with the  $j$ -th data qubit at TICK  $k$ .  $T_{max}$  will be defined later.

**(Integer Variable)**  $T$  has the shape of  $(m, n)$ : the TICK of each CX/CZ gate. If ancilla qubit  $i$  visits data qubit  $j$  at TICK  $k$ , then  $T[i][j] = k \iff A[i][j][k] = 1$ .

Owing to the low-density parity-check property,  $H$  is an extremely sparse matrix. To further denote the empty positions  $(i, j)$  where no CX/CZ gate is required (namely the zeros in  $H$ ) and avoid the scheduling overhead in advance, we just set  $T[i][j] = -1$  for all  $H[i][j] = 0 \wedge H[i][j+n] = 0$ .

2) *Optimization Goal:* Our goal is to minimize the circuit depth, i.e., the maximum element in  $T$ :

$$\min \max_{i,j} T[i][j] \quad (7)$$

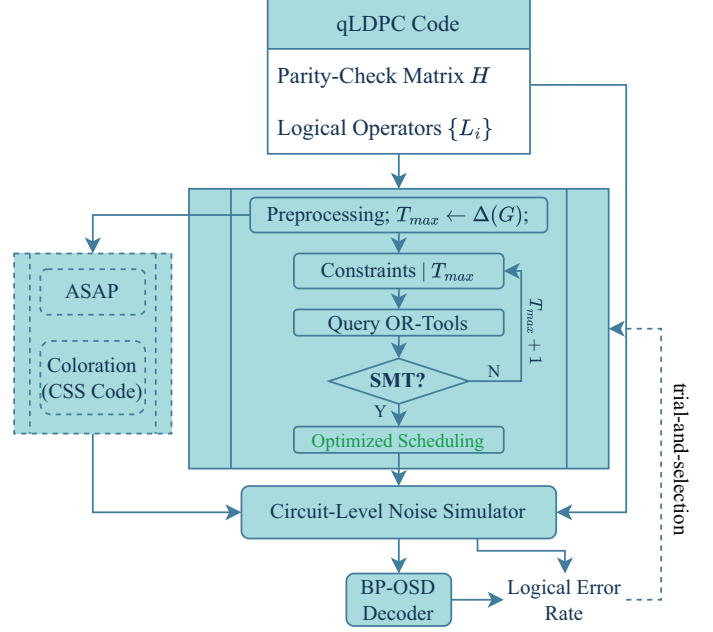


Fig. 3. Workflow of ASC with the evaluation pipeline.

3) *Problem Constraints:* Through this representation, a legal syndrome extraction circuit scheduling must satisfy the following constraints:

- ① Unique occupation of data qubits  $j$  at TICK  $k$ :

$$\forall j, k \quad \sum_i A[i][j][k] \leq 1 \quad (8)$$

- ② Unique occupation of ancilla qubits  $i$  at TICK  $k$ :

$$\forall i, k \quad \sum_j A[i][j][k] \leq 1 \quad (9)$$

- ③ Integrality of stabilizer check:

$$\forall i, j \quad \sum_k A[i][j][k] = H[i][j] \vee H[i][j+n] \quad (10)$$

- ④ Correctness of commutativity for all  $\{g_i, g_j\}$ :

$$\forall i, j \quad \sum_l \mathbb{I}(T[i][l] < T[j][l]) \bmod 2 = 0, l \in \{l \mid (H[i][l] \wedge H[j][l+n]) \oplus (H[i][l+n] \wedge H[j][l]) = 1\} \quad (11)$$

where  $\mathbb{I}(\cdot)$  equals 1 when the condition holds and 0 otherwise. Equations (8)-(9), (10) and (11) completely enforce **Constraints 1, 2** and **3**, respectively.

Instead of directly optimizing the circuit depth in (7), which is usually inefficient, we add one more constraint to confine the search space:

- ⑤ Bound of all TICKS:

$$\forall i, j \quad T[i][j] \leq T_{max} \quad (12)$$

where  $T_{max}$  is a constant to bound all  $T[i][j]$ . We begin with the lower bound established in Section III-B, and then search for satisfiability, similar to the strategy in [29]. We incrementally increase the depth step by step until we reach the estimated

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**Algorithm 1: Optimal X-Z crossed circuit scheduling**

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**Input:** qLDPC check matrices in BSF  $H$ **Output:** CX/CZ scheduling list  $T$  of each TICK

```
1 Initialize:  $T_{max}$ ; Conditions  $C$ ; SMT Solver  $S$  ;
2 for  $T_{max} \leftarrow \Delta(G)$  to  $2\Delta(G)$  do
3   if  $S(C).timeout()$  then
4     continue;
5   if  $S(C) == True$  then
6     return  $T$ ;
7 return False;
```

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upper bound, i.e.,  $2\Delta(G)$ . Once a satisfying assignment is found, the search loop terminates and returns the optimized schedule, as described in Algorithm 1.

### B. Circuit-level noise simulator

To further evaluate the fault-tolerant performance of the circuits generated by the scheduler, we implement a circuit-level noise simulator using Stim [30]. After scheduling all CX and CZ gates, we build up a standard quantum memory experiment circuit following [11], [12]. This circuit includes  $d$  rounds of syndrome extraction (where  $d$  is the code distance), and a final measurement round of all data qubits. The syndrome outcomes are passed to the BP-OSD decoder [31], [32] for decoding, which outputs the *predicted observables* for each logical operator. By comparing these predicted observables with the *actual observables* from the Stim simulator, we compute the logical error rates of the memory experiments—values that reflect the fault-tolerant performance of the circuit.

### C. Automated circuit filter

We also integrate a simple circuit filtering module for selecting the more fault-tolerant circuits automatically: Since the scheduling produced by the SMT solver exhibits a certain degree of randomness, we can run it multiple times and retain the circuit with the lowest logical error rate, as illustrated by the dashed line *trial-and-selection* in Fig. 3. This might be useful for further theoretical or experimental analysis of different circuit variants of a given qLDPC code.

## V. EVALUATION

In this section, we evaluate the effectiveness of ASC over four aspects: (1) its solution to IBM’s open problem regarding the BB code; its ability to (2) reduce circuit depth and (3) improve logical accuracy for general qLDPC codes; and (4) its scalability when applied to larger qLDPC codes.

All experiments are conducted on a dual-socket *Intel Xeon Platinum 8358P* CPU, featuring 32 cores per socket, 2 threads per core, a base frequency of 2.60 GHz, and a maximum frequency of 3.40 GHz. For the SMT solver, we use *OR-Tools*’s CP-SAT from Google [33] with default settings, except that the maximum SMT solving time is set to 2 hours. The circuit-level noise model is the same as [11], where each operation of the circuit is followed by a depolarizing channel with strength  $p$ ,

TABLE II  
DEPTH-OPTIMAL COMPILATION OF IBM’S BB CODES [11]

BB Code	ASAP	Color	ASC	ASC Time
[[72, 12, 6]]	15	12	7	< 1 min
[[90, 8, 10]]	15	12	7	< 1 min
[[108, 8, 10]]	16	12	7	< 5 min
[[144, 12, 12]]	16	12	7	< 5 min
[[288, 12, 18]]	16	12	7	< 5 min
[[360, 12, $\leq 24$ ]]	16	12	7	< 10 min
[[756, 16, $\leq 34$ ]]	16	12	7	< 2 hours

including the reset, measurement, idling and CX/CZ gates. All memory experiments are conducted under  $p = 0.001$ , which is the current hardware noise level.

### A. IBM’s open problem

We first apply ASC to solve one open problem mentioned in [12]. The IBM team manually constructed depth-7 circuits by leveraging code symmetries and further identified up to 935 equivalent depth-7 variants through exhaustive computational search, yet they remained uncertain whether a depth-6 circuit could exist. Notably, ASC generates depth-7 circuits for all these BB code examples within 2 hours without timing out. To our knowledge, this constitutes the first concrete evidence supporting the conjecture that no depth-6 circuits exist for these BB codes.

### B. Reduction of circuit depth

To evaluate the capability of ASC in compiling general qLDPC codes, we select a series of representative examples, including 2 BB codes in [34], 2 GB codes in [31], 2 HGP codes in [35], and 2 Color codes in [36]. We show the compilation results in Table III. Compared with the ASAP scheduling and the coloration-based method, ASC always returns an optimal or near-optimal circuit compilation with depth close to the lower bound  $\Delta(G)$ , which demonstrates the effectiveness of ASC in searching for optimal syndrome extraction circuits for arbitrary qLDPC codes automatically.

### C. Improvement of logical accuracy

We conduct quantum memory experiments for all qLDPC codes in Table III. As shown in Fig. 4, the logical error rates of circuits from ASC achieve a 7x-8x reduction on average, compared with the ASAP or coloration-based methods. This improvement is primarily attributed to the substantial reduction in idling errors resulting from the nearly halved circuit depth.

Focusing on the [[18, 4, 4]] code in [34], we also show how to utilize our filter tool described in Section IV-C to select the circuit with better fault-tolerant performance. As we increase the selection time from 1 to 30 minutes, the corresponding logical error rate of the best selected circuit decreases and gradually converges to optimal, as shown in Fig. 5.

### D. Scalability

In Table III, we find that the compilation time depends not only on the qubit number of a qLDPC code but also on the

TABLE III  
DEPTH-OPTIMAL COMPILATION OF SOME GENERAL QLDPC CODES

Code	Source	Parameters	$\Delta(G)$	Manual	ASAP	Color	ASC	ASC Time
BB Code I	[34]	[[18, 4, 4]]	6	7 [34]	12	12	<b>7</b>	< 1 min
BB Code II	[34]	[[36, 4, 6]]	6	7 [34]	12	12	<b>7</b>	< 10 min
GB Code I	[31]	[[48, 6, 8]]	8	<i>unknown</i>	21	16	<b>9</b>	(< 2.1 hours) Timeout
GB Code II	[31]	[[126, 2, 12]]	4	<i>unknown</i>	8	8	<b>4</b>	< 1 min
HGP Code I	[35]	[[52, 4, 4]]	6	10 [35]	12	12	<b>7</b>	< 5 min
HGP Code II	[35]	[[65, 9, 4]]	6	10 [35]	12	12	<b>7</b>	< 11 min
Color Code I	[36]	[[19, 1, 5]]	6	<i>unknown</i>	12	12	<b>6</b>	< 1 min
Color Code II	[36]	[[37, 1, 7]]	6	<i>unknown</i>	12	12	<b>6</b>	< 1 min

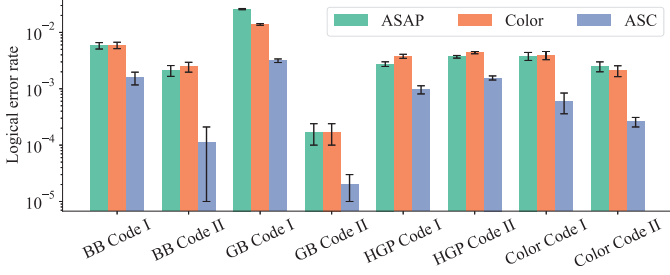


Fig. 4. Logical error rate comparison.

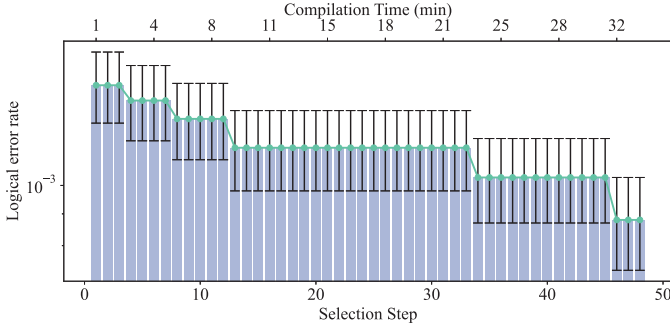


Fig. 5. Improvement of fault-tolerance through the automated circuit filter, with a fixed random seed for noise simulation.

maximum degree of its *Tanner Graph* (denoted  $\Delta(G)$ ). This is because both factors determine the number of SMT constraints. For example, the  $[[48, 6, 8]]$  GB code uses only 48 data qubits yet times out during compilation, due to its large maximum degree  $\Delta(G) = 8$ .

We evaluate the compilation scalability of ASC using the surface code: this code family is itself a subset of qLDPC codes, and its members can be characterized by a code distance  $d$ —all of which admit nearly identical depth-4 optimal syndrome extraction circuits. Fig. 6 illustrates the ASC compilation time against the total number of data qubits  $n = d^2$ , which scales approximately as a power law yet remains relatively low—staying under one minute even when  $d = 21$ . This indicates that ASC exploits the sparsity of qLDPC codes with low degree, namely the low density of their parity-check matrices, to achieve efficient SMT solving. However, like other SMT-based approaches, ASC still faces challenges when scaling to

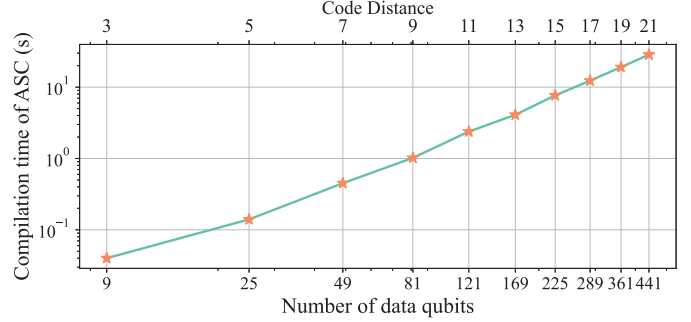


Fig. 6. Compilation time scaling of ASC.

larger codes—whether due to more qubits or a larger Tanner graph maximum degree. Nevertheless, compiling large codes could be addressed in future work by combining ASC with localized divide-and-conquer strategies, such as the ancilla bridge method [37], [38].

## VI. CONCLUSION

In this work, we develop ASC: a lightweight yet efficient compiler and evaluation framework for syndrome extraction circuits in general qLDPC codes, designed around a set of simple rules. For most near-term qLDPC codes, our compiler generates either theoretically optimal or near-optimal solutions within a specified time budget. Via end-to-end evaluations, we demonstrate significant reductions in both circuit depth and logical error rates across a diverse set of qLDPC codes. We further introduce a simple randomized filtering method that automatically produces more fault-tolerant circuits. We anticipate that ASC will serve as a concise, automated qLDPC compilation tool to support both theoretical analysis and experimental demonstrations in quantum error correction.

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