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Soft-Error Resilient MRAM-OTP BCAM for DDR4 STT-MRAM Redundancy Management

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***Abstract*—Memory systems operating in high-radiation environments require robust protection against single-event effects (SEE) damage. While STT-MRAM offers inherent advantages due to its spin-based storage, conventional redundancy repair architectures remain vulnerable due to separated storage and configuration circuits, slow boot performance, and radiation-induced errors in long signal paths. This paper proposes a novel radiation-hardened one-time programmable (OTP) content-addressable memory (CAM) based on magnetic tunnel junctions (MTJs) for efficient column redundancy in STT-MRAM macros. The design incorporates a radiation-hardened-by-design (RHBD) CAM array with built-in self-repair (BISR), featuring complementary OTP MTJ bitcells enabling parallel programming and disturbance-free matching, a soft-error resilient array with dual-node hardened latches and dual match-line sensing, and a DDR4-compatible repair mechanism supporting TMR-Latch-based fast initialization and energy-efficient search with inter-loop termination. The proposed system significantly improves wake-up speed to less than two clock cycles, and reduces power consumption to less than 12fJ, offering a viable solution for 37MeV radiation-tolerant memory systems.**

***Index Terms*—MRAM, OTP, MBIST, Content Addressable Memory, Reliability**

I. Introduction

In high-radiation environments such as space and nuclear reactors, conventional charge-based memories like SRAM and FLASH are highly vulnerable to SEE, as shown in Fig.1(a), including single-event upsets (SEU) and latch-up (SEL), as well as total ionizing dose (TID) effects [1]–[4]. In contrast, magnetic RAM (MRAM) leverages a spin-based storage mechanism through magnetic tunnel junctions (MTJs), which inherently resist radiation-induced upset, while the data stored via electron spin orientation that naturally immune to single-event upsets and tolerant to TID [5], [6]. Although peripheral CMOS circuits still require radiation-hardening-by-design (RHBD) techniques, the intrinsic robustness of MTJs allows MRAM to achieve superior radiation performance with relatively low overhead.

Redundancy repair is an essential yield-enhancement technique in memory manufacturing [7], [8]. The repair process is initiated during post-fabrication testing, where fault locations are identified and a redundancy analysis algorithm allocates redundant elements to replace faulty cells, presented in Fig.1(b), which solution is permanently stored by programming fuse elements, achieving viable yields in high-density memory architectures [9]–[11].However, conventional approaches exhibit

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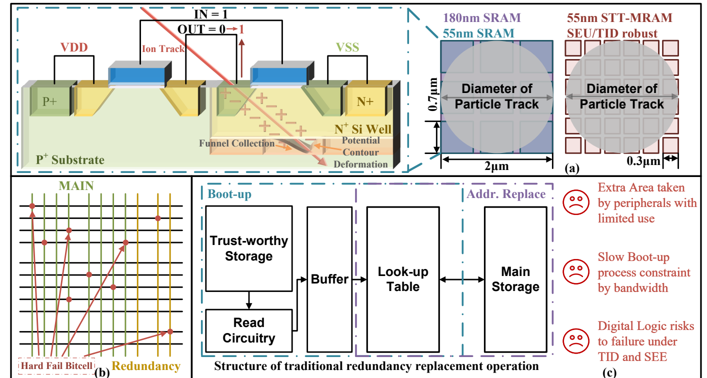

Fig. 1. (a) Radiation-induced failure of memories. (b) Hard failure distribution within the memory. (c) Risks of the traditional approach under radiation.

significant vulnerabilities in radiation-prone environments for STT-MRAM-based storage macros, shown in Fig.1(c). These methods typically decouple reliable non-volatile storage from volatile configuration registers, necessitating separate peripheral circuits for each section and consequently reducing overall storage density. This partitioned architecture further requires bank-level data transfer from fuse arrays to configuration registers during boot-up, substantially increasing system wake-up time. Moreover, the extended physical data transfer path inherently introduces multiple points susceptible to radiation-induced logical errors, compromising reliability under continuous exposure.

To address these challenges, this work proposes an OTP MTJ-based RHBD CAM for column redundancy repair, integrated with a dedicated BISR strategy [12], [13]. The proposed architecture significantly enhances the reliability of STT-MRAM in radiation applications through three key innovations [14]–[16]:

Data Bitcell: A binary CAM cell comprising complementary OTP MTJ elements supporting parallel byte-wise programming, coupled with an in-situ read-disturb-free data matching path;

CAM Array: A soft-error-resilient array design incorporating radiation-hardened double-node latches for local content matching, dual match-line pathways with low-leakage Schmitt triggers, and RHBD matching logic;

System Deployment: A DDR4-compatible macro-level column redundancy mechanism featuring unique hard-fail repair via BISR, TMR-based NV-latch initialization for fast wake-up, and an energy-efficient search strategy with sequence reordering and inter-loop termination.

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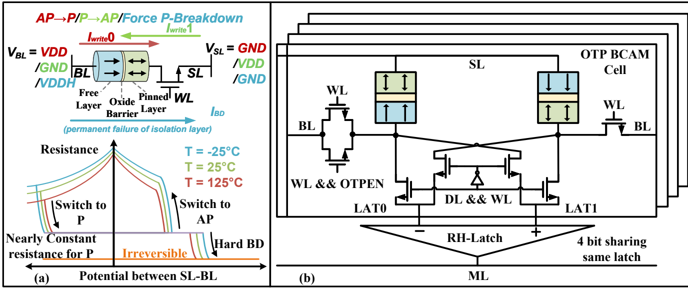


Fig. 2. (a) Mechanism of MRAM switching and hard breakdown. (b) Proposed structure of MRAM OTP-CAM bitcell

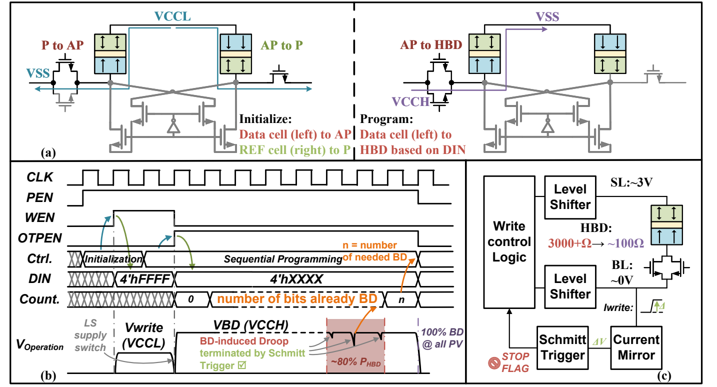


Fig. 3. (a) Programming operation of the proposed complementary cell. (b) Timing control of proposed OTP programming. (c) Self-termination feedback.

II. OTP MRAM-Based Data Bitcell Design

The normal device of STT-MTJ consists of two thicker sections of CoFeB and a thinner film of MgO with a sandwich structure, which refers to the fixed layer, free layer, and oxide barrier [17]–[19]. In an MTJ presented in Fig.2(a), the fixed ferromagnetic layer filters electrons based on their spin, creating a current where the electrons' magnetic moments are predominantly aligned in one direction. This spin-polarized current is then injected into the free layer. When these electrons enter the free layer, they must align their spins with the local magnetization. In the process of transferring their spin angular momentum to the collective magnetization of the free layer, they exert a torque upon the electrons within.

In the proposed design, a breakdown mechanism is utilized for hard failure of the MTJ device, making it an irreversible lower resistance state, which not only provides a larger read margin but also better data retention capability [20]–[24]. Hard breakdown in an STT-MTJ is described as failure of the ultra-thin MgO tunnel barrier, culminating in a permanent short circuit. It is initiated by a high electric field, which promotes Fowler-Nordheim tunneling and generates defects like oxygen vacancies. This increases leakage current via trap-assisted tunneling, creating a feedback loop of Joule heating and further degradation. The culmination is the thermally-assisted formation of a conductive filament through metal ion diffusion or a chain of vacancies that bridges the electrodes. This irreversibly destroys the tunnel barrier, eliminating magnetoresistance and switching capability, and rendering it as a low-value resistor, treated as an OTP cell [25], [26].

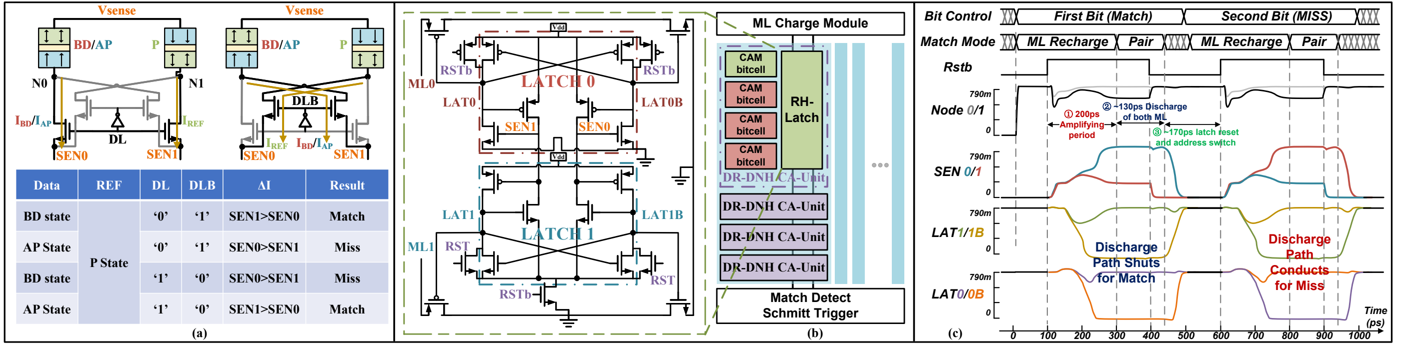
Based on the mechanism of MTJ and its potential as a flexible role as a one-time programmable memory cell or a normal cell, a CAM-oriented cell with a pair of self-referenced MTJ cells and individual read and write paths is proposed as Fig.2(b). The data within the OTP Binary CAM cell can be programmed by different voltages applied across the source line and bit line, while the word line helps enable the access transistors. The matching result is based on the logic in the memory structure, with the proposed discharge path through the reconfigurable path handled by the DL and DLB and sampled by a radiation-hardened latch. Then the result would reflect whether the duplicated match lines discharge simultaneously, which turns out to be the matching result.

Unlike the traditional 2T-2M bitcell structure, the self-reference OTP bitcell took the full advantage of three independent states, shown in Fig.3(a). The default state of the cell is normally operational reprogrammable, with the left cell initialized in P state and the other one set to AP state, representing the "unprogrammed" state. While the designated cells are chosen, they would come through two independent phases of programming. The first step is a state-reversing writing from the original configuration, with the left cell flipped to the AP state and vice versa. The writing path is configured carefully the left and right cells connected by opposite terminals, which naturally form two complementary paths of writing as the voltage is applied to SL or BL. Once the initialization is set, the second step would determine which bit needs to be programmed as BD to present "0". In this stage, the WL signal enables further access transistor activated for the left cell's path and deactivates the right one's path. The OTP programming only happens on the left cell with the higher programming voltage applied.

While the OTP state of post-BD MTJ cells has significantly lower resistance, the parallel programming of OTP becomes troublesome, while the high voltage for breakdown operation would induce significant leakage current through the post-BD cell. The huge droop on SL would reflect an observable disturbance on the power supply and write driver, which results in an insufficient supply for further success breakdowns on parallel paths. Thus, in order to find the balance between the period of OTP programming and the area cost of OTP peripherals, the proposed design introduces a single-end self-terminated write driver, which is achieved by sharing the Schmitt trigger introduced in the later section. Considering the huge droop induced by the programmed cells, each bit-line is connected to a specific current mirror, which replicates the current variation, and then the difference is amplified by the Schmitt trigger, as Fig.3(b). When the BD happens, the output quickly catches the rising intensity of the current and outputs the stop-programming flag, which disconnects the current writing path. Meanwhile, an external counter would continuously collect the number of already breakdown bits with the required amount. The full asynchronous design in Fig.3(b) ensures the proper data is programmed and potentially improves the latency.

III. Radiation Hardened Binary Content Addressable Memory

While research confirms that the MRAM bitcell is intrinsically resilient to SEE, the peripheral circuitry becomes



Data	REF	DL	DLB	ΔI	Result
BD state	P State	‘0’	‘1’	SEN1>SEN0	Match
AP State		‘0’	‘1’	SEN0>SEN1	Miss
BD state		‘1’	‘0’	SEN0>SEN1	Miss
AP State		‘1’	‘0’	SEN1>SEN0	Match

Fig. 4. (a) The sensing scheme based on DL controlled sampling path. (b) Double-node hardened dual-port latch for each four data cells. (c) Timing of Comparing within the proposed DR-DNH CA-Unit

the limiting factor for achieving the required reliability in mission-critical applications where ideally zero errors are permitted. As noted in the Introduction, conventional redundancy repair schemes are often bottlenecked by the lengthy and performance-intensive data transfer and matching process. To address this, the design proposed in this work aims to shorten the critical path significantly by embedding the search operations within the memory array using a dedicated in-situ CAM circuitry, thereby enhancing both repair speed and system robustness against search errors.

The CAM bitcell employs a dual-discharge-path architecture, where each path is governed by a pair of access transistors controlled by complementary data lines, DL and DLB. During operation, the source line is precharged to a reference voltage, establishing a ready state for sensing. Current subsequently flows through either the ipsilateral discharge path enabled when DL is activated, or the contralateral path triggered by DLB, directing the signal toward the differential sensing nodes SEN0 and SEN1. The match or mismatch state is determined by comparing the magnitude of currents at these two nodes. In Fig.4(a), the ”Match” is detected when the current at SEN1 exceeds that at SEN0. This scenario arises under two specific conditions: when a logic “0” provided via DL encounters a breakdown state stored in the cell, or when a logic “1” supplied through DLB coincides with an anti-parallel (AP) state, either of which causes the SEN1 path to discharge more rapidly. Conversely, the SEN0 is greater than SEN1, which indicates a mismatch. This differential sensing mechanism enhances noise margin and enables reliable and low-power matching operation in the presence of device variations and parasitic effects.

In Fig.4, we proposed a Dual-Modular Redundant (DMR) radiation-hardened latch (RH-Latch) designed, inspired by RHSCC-16T SRAM [27], to ensure robust and error-resilient data retention under harsh operating conditions, such as ionizing radiation or SEUs. This latch employs a dual-node hardening architecture, where critical data is stored redundantly in two independent nodes, LAT0/LAT0B and LAT1/LAT1B. Each node is driven by a cross-coupled inverter pair, providing continuous feedback to maintain state integrity.

The sense node SEN0 and SEN1 receive differential current signals from the CAM bitcells and convert them into voltage levels. These voltages are then compared using a current mirror reference, which amplifies the difference to resolve match or mismatch conditions swiftly. For instance, when SEN1 exceeds SEN0, transistor N1 conducts more strongly, pulling LAT1B low, while the lower SEN0 level results in less conduction through N0, keeping LAT0 high. This imbalance triggers a positive feedback loop within the cross-coupled inverters, rapidly driving the nodes to a stable state where LAT1 remains high and LAT1B’s low. Additionally, the use of redundant feedback paths and balanced transistor sizing enhances tolerance to charge sharing and node leakage. The electrical isolation between the two modules prevents fault propagation, and the self-restoring feedback mechanism effectively suppresses single-event transients. This latch not only accelerates decision-making through positive feedback but also significantly improves the reliability of data correctness.

The charge and recharge channel, controlled by complementary signals RST and RSTb, is carefully designed to enable rapid recovery and reset of both latch nodes while balancing power efficiency and operational stability. This module also coordinates the data line transistors with input data signals to ensure precise timing alignment. Operation commences when the match start flag transitions high, initiating precharging of all bitcells and pulling up the source lines. After a deliberately timed interval of 100 ps, the reset flag is set low, triggering the sampling phase through the differential sense amplifiers SEN0 and SEN1. This duration is optimized to allow the match line to settle stably at VDD without excessive energy consumption, thereby minimizing dynamic power dissipation.

As indicated in Fig.4(c), the subsequent discharge period, lasting approximately 130 ps, is tightly controlled to regulate current flow and prevent over-deviation in the match-line driver, further reducing power surges and enhancing signal integrity. A Schmitt trigger circuit samples the falling edge of the discharge waveform, providing noise immunity and generating a stable control signal for DMR logic and flip-flop-based sampling circuits. The reset operation is initiated 300 ps after the previous pull-down event, with latch reset completing within 50 ps. A subsequent 150 ps interval precedes the next comparison cycle, providing essential margin for logic operations such as row switching and match-line recovery. This structured timing strategy not only minimizes power consumption through managed transition times but also ensures robustness against voltage fluctuations and temperature variations, achieving a balance between energy efficiency and operational reliability.

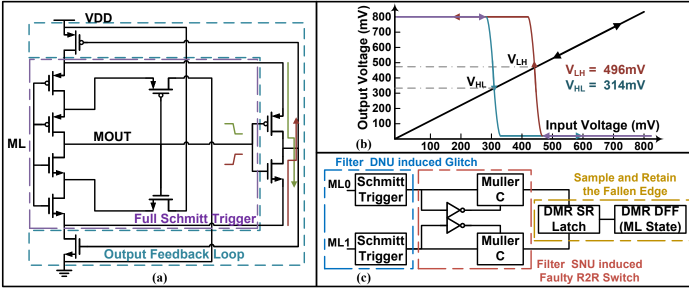


Fig. 5. (a) Schematic of proposed Schmitt Trigger. (b) Hysteresis voltage curve of the proposed structure. (c) Spike-filtering logical circuit for post-processing

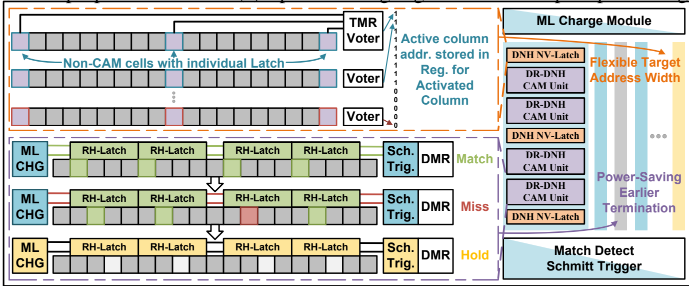


Fig. 6. Locally deployed strategy for fast wake-up and inter-loop termination

In Fig.5(a), the incorporation of a full Schmitt trigger affords substantial performance improvements essential for radiation-hardened CAM subsystems operating under stringent conditions, with benefits spanning power efficiency, switching velocity, noise resilience, and system-level reliability. Central to this performance enhancement is the trigger's sophisticated hysteresis response, meticulously calibrated to operate within a narrow voltage window. The Fig.5(b) shows the feedback mechanism with high efficiency: when the input voltage, such as that originating from a discharging match line, surpasses the high-to-low threshold, the output signal declines and propagates through an embedded feedback inverter. This action promptly disables the upper clamping transistor, effectively isolating the core circuit from VDD. Conversely, during low-to-high transitions, the signal deactivates the lower clamping transistor. This active supply regulation not only reduces leakage current but also enhances switching speed by mitigating parasitic capacitive loadings. Consequently, the trigger demonstrates accelerated signal settling and enhanced transient performance.

Furthermore, the trigger's calibrated hysteresis confers exceptional immunity to noise-induced malfunctions, particularly those arising from distributed noise and SNU events. By rejecting spikes of signal variations within the hysteresis band, the design ensures that only legitimate match/mismatch outcomes are propagated to subsequent stages, as shown in Fig.5(c). Coupled with dual modular redundancy in the latching circuitry, the Schmitt trigger significantly fortifies the system against SEUs, underscoring its suitability for radiation-intensive applications. This design choice proves critical in large-scale CAM arrays wherein numerous match lines operate concurrently, substantially curtailing unwarranted energy dissipation.

IV. Power Optimized on-chip Redundancy Replacement Strategy

In practical redundant array implementations, the number of columns requiring replacement is uncertain and process-dependent, often affected by localized defects and fabrication variability. Although redundancy storage must support at least 20 parts per million (ppm), enabling all columns for comparison is impractical due to the excessive number of latches, which would lead to high static power and area overhead. To address this, the proposed design in Fig.6 employs two key techniques to efficiently eliminate unnecessary comparisons from both unprogrammed columns and already mismatched addresses, significantly reducing dynamic energy consumption.

A double-node hardened latch with a single MTJ pair serves as a flag cell, as DNH-NVLATCH, enhancing robustness against single-event upsets for high-reliability applications. Unlike the standard DR-DNH CAM unit, the DL-controlled configurable path is removed, simplifying control logic, reducing parasitic load, and improving timing margins. These flag cells are programmed into an OTP state when a column is assigned redundant data, ensuring non-volatile storage. During initialization, their states are retrieved via a dedicated sensing circuit to verify programming status. Each column stores identical data across three cells for error resilience, with outputs processed by a triple modular redundancy (TMR) voter for majority-based state decision before match-line precharge. This hierarchical redundancy improves fault tolerance and soft-error resilience, enabling flexible and energy-efficient precharging where only columns with valid redundancies are activated.

For matching, only one of four CAM bitcells is selected per comparison round, avoiding the conventional approach of storing all four results with extra registers and full latch-discharge access, which introduces significant power and delay overhead. An inter-loop termination strategy using distributed Schmitt triggers and gated power logic is introduced: each match line is coupled to a Schmitt trigger for noise-immune sensing. Upon detecting a mismatch, which creates a direct discharge path to VSS, the current column is immediately disabled for subsequent matches, terminating further comparisons. Footer transistors gated by the Schmitt output reduce leakage in inactive columns. This design enhances energy efficiency by limiting switching activity and shortening evaluation time, with Schmitt hysteresis ensuring noise tolerance and preventing false termination. The architecture supports scalable word widths without compromising power efficiency, making it suitable for high-density, low-power CAM designs.

Additionally, a sparsity-aware coding strategy with hash-based slicing dynamically reorders the comparison sequence via DL activation signals. Input addresses are hashed into slices, grouping columns by similarity, then evaluated and ranked by bit-density uniformity. Comparisons start with the densest slices and proceed to sparser ones, combining hash-guided search with sparsity-aware ordering to enable early mismatch detection. This hybrid approach reduces the active search space to under 20 percent of the original set in initial rounds, curtailing latch discharge operations and lowering dynamic energy in subsequent matching phases.

Some studies indicate that STT-MRAM exhibits latency and throughput compatible with contemporary DDR3 and DDR4 standards [28]–[31]. However, manufacturing inconsistencies

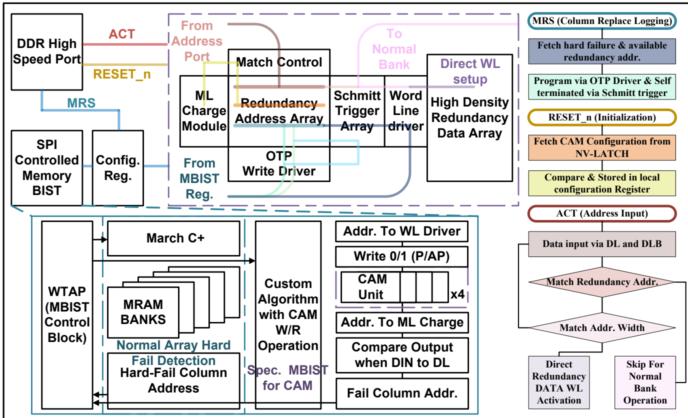
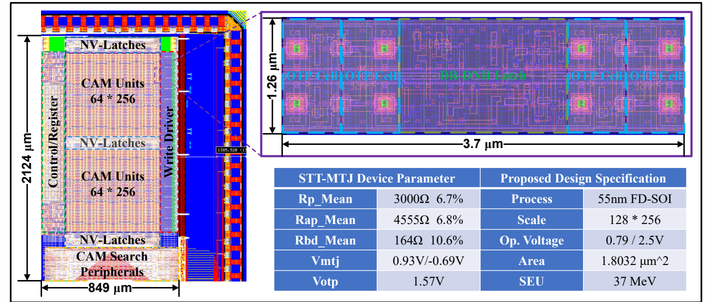


Fig. 7. Built-in Self-Repair assisted redundancy replacement mechanism fulfilling high-speed memory access

impede its adoption in radiation-prone environments. To address this, we propose a radiation-tolerant binary CAM for redundancy management within STT-MRAM macros, enabling efficient address remapping as shown in Fig.7. During post-fabrication testing, built-in self-test (BIST) identifies hard failures in the main array. Detected fault addresses are stored in configuration registers using Mode Register Set (MRS) commands compliant with DDR4 timing parameters such as t_{MOD}. These addresses are then programmed into non-volatile CAM bitcells, while a simultaneous operation configures a DNH NV-Latch as a redundant column indicator. Upon system initialization, a RESETn signal triggers recovery of flag bits from non-volatile storage through TMR logic, completing within the DDR4-specified t_{INIT} period of under 10 ns.

The design improves radiation tolerance through several strategies: critical configuration data is distributed across three independent NV-latch instances during RESETn to minimize single-point failure risk; data paths are shortened between MTJ storage and TMR voter logic to reduce exposure to particle strikes; and DMR comparators combined with Schmitt triggers provide error suppression against transient noise and SEUs. Address matching during ACT commands occurs in parallel across redundant columns, enabling rapid mismatch detection. The redundancy module shares wordline drivers with the primary address decoder to maximize area efficiency. For each ACT command, the CAM array performs concurrent comparisons with stored redundant addresses. Match results are resolved within the DDR4 t_{AA} window, sampled by a Schmitt trigger-based sensing array, and output as a one-hot match vector to the WL driver for redundancy data or a miss signal for bypass.

While conventional 1T1M STT-MRAM arrays require dedicated MBIST for detecting MTJ-specific faults, standard March tests like March C+ must be adapted to accommodate non-volatility and asymmetric write characteristics. This work proposes a customized MBIST algorithm that treats a radiation-hardened latch and CAM bitcell pair as a unified NV-SRAM cell. The test procedure writes complementary values into these structures using BL and SL drivers, then holds DL at "1" to evaluate match conditions with Schmitt triggers detecting mismatches. Deviations from expected responses flag faulty columns for exclusion in subsequent OTP configurations. This



STT-MTJ Device Parameter		Proposed Design Specification	
Rp_Mean	3000Ω 6.7%	Process	55nm FD-SOI
Rap_Mean	4555Ω 6.8%	Scale	128 * 256
Rbd_Mean	164Ω 10.6%	Op. Voltage	0.79 / 2.5V
Vmtj	0.93V/-0.69V	Area	1.8032 µm^2
Votp	1.57V	SEU	37 MeV

Fig. 8. Layout of proposed design and essential parameters

method maintains compatibility with March C+ patterns while adapting to the hybrid BCAM structure, and is orchestrated by a standard Test Access Port controller for at-speed testing within RHBD STT-MRAM architectures.

V. Simulation and Analysis

The proposed design is post-simulated on the 55nm FD-SOI CMOS FEOL and a commercial-verified STT-MRAM BEOL process, shown in Fig.8, with the FD-SOI process helping enhance resilience to both TID effects and SEEs by leveraging its buried oxide (BOX) layer for effective isolation of ionization-induced charges and its ultra-thin body structure for the reduction of sensitive volume [32]–[34]. Thus the following verification would be focus on single event effects based on post-layout simulation. With the sample array achieved in the storage capacity of 32K bits and occupying the area of 1.8032 μm^2, the radiation-emulating faulty injection verifies capable of sustaining 37MeV SEUs.

While radiation effects are challenging to quantify at the circuit level, a widely adopted methodology involves the use of a double-exponential current source to emulate the transient current injection induced by an ionizing particle strike along a specific node [35], [36]. The current waveform is described by:

$$I(t) = I_0 \left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta} \right) \tag{1}$$

where the I_0 is considered as the unified current injected:

$$I_0 = \frac{Q_{\text{inj}}}{\tau_1 - \tau_2} \tag{2}$$

The τ_α and τ_β are considered as the node charge collection time constant and the ion track build-up constant, respectively, treated as the rise and fall time parameters. The polarity of Q_{inj} depends on the type of transistor drain struck (NMOS or PMOS), presented in Fig.9(a). To evaluate the radiation tolerance of the proposed design, single-event transients are injected into critical nodes in Fig.9(b). The OTP memory cell, continuously biased by a sensing voltage, exhibits inherent resilience, allowing any injected transient current to be rapidly suppressed by the low-impedance voltage source. This also ensures stable match-line charging during initialization.

During the sensing phase, fault injections are applied to various nodes within the DMR latches. When a single-node upset is introduced, the match line remains stable without a discharge path to ground being formed, owing to the masking effect of

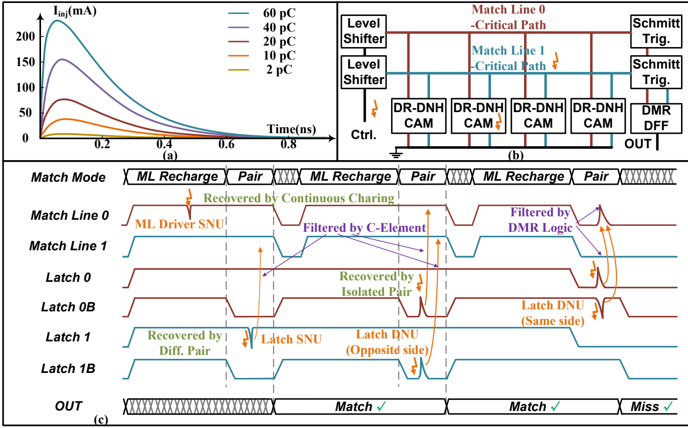


Fig. 9. (a) Output Current of test source under different amounts of charge injection. (b) Sensitive nodes in the proposed design. (c) Single Node and Double Node upset filtering and recovery of the proposed design.

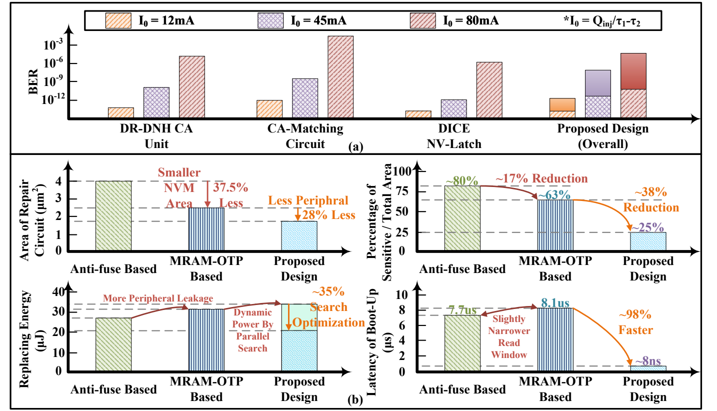


Fig. 10. (a) Search Error Rate under different doses of injection. (b) Comparison between the proposed design and the traditional anti-fuse/OTP structure

the C-element logic. Certain double-node upset scenarios are also mitigated. For instance, when two nodes on the same side of both latches are simultaneously struck, the complementary nodes in each latch help restore the correct state, with previous values preserved by the C-elements. In cases where both output nodes of a single latch are affected, one match line may temporarily fluctuate. Although this perturbation impacts analog sensing, the subsequent digital output, sampled by a radiation-hardened Schmitt trigger and processed by redundant voting logic, effectively suppresses the faulty falling edge, thereby preventing error propagation.

Fig.10(a) presents the fault injection examination of radiation single event by adjusting the current source strength. The SPICE-based Monte-Carlo test is held by a script-controlled simulation randomly choosing the injection node with 10000 runs per case. Fault injection tests are carried out using current sources with amplitudes ranging from $12mA$ to $60mA$ to emulate ion strikes with varying deposited charge. The sub-circuits are working well under $12\mu A$ and are still functional with less than 1 ppm failure under $45\mu A$ injection. The CAM matching circuit with a relatively sensitive node and less protection would fail under the $60\mu A$ case. The proposed design has proven search error rate lower than 10^-8 with $45\mu A$ injectiong which matched up with the fully hardened traditional approach with TMR standard cells and sense amplifiers. Considering the smaller area occupied by proposed design, it would be less likely stroked by larger ions.The comprehensive examination of the proposed design shows the efficiency under various node injection and demonstrates its full functionality even under injection levels equivalent to a 37 MeV single-event strike, confirming its reliability in high-radiation environments.

In Fig.10(b), the proposed architecture is compared with two established redundancy replacement methods, the anti-fuse-based and MRAM-OTP-based implemented with TMR. The results reveal significant advantages across multiple metrics: the proposed circuit reduces area by 28% compared to conventional TMR structures, owing to its compact design and simplified peripheral circuitry. The number of radiation-sensitive nodes is also considerably reduced, with the in-situ comparison helping minimize the extended sensing path. A

TABLE I
PERFORMANCE COMPARISON WITH OTHER CAM DESIGN

	DATE'23 [37]	TCAS2'17 [38]	ISCAS'25 [39]	This Work
Type	SRAM-CAM	STT-TCAM	STT-TCAM	STT-OTP-BCAM
Structure	9T	6T-4M + Latch	6T-4M + 12T Latch	7T-2M + 21T Latch
SER (%)	N/A	6.1	N/A	0.1
Match Energy (fj/bit)	0.66	7.67	6.407	12.51
Sense Latency (ns)	0.55	0.58	0.85	0.5
Rad. Hardened Design	NO	NO	YES	YES

25% reduction in dynamic power during parallel search operations is achieved through optimized matching sequences and termination strategies. Furthermore, the design achieves a 98% improvement in startup time, completing initialization within 8 ns for rapid system recovery in radiation-prone applications, without waiting for the excessive reading operation of the traditional approach. Compared with the latest CAM works in Table I, the proposed radiation-hardened design achieves better sensing latency without over-compromising sensing energy.

VI. CONCLUSION

This work has presented a radiation-hardened one-time programmable CAM architecture for redundancy management in STT-MRAM, achieving robust operation under high-radiation conditions while significantly improving power and latency metrics. The proposed design demonstrates a wake-up time of less than two clock cycles and energy consumption below 12fJ per bit, supporting DDR4-compatible memory interfaces. Through the adoption of a TMR flag latch and sparsity-aware hashing search strategy, the active comparison volume is reduced by over 60%, drastically cutting dynamic power. The combination of OTP-based bitcells, dual-node hardened latches, and Schmitt-triggered early termination offers resilience against single-event upsets up to 37MeV, while maintaining 98% faster initialization and 25% lower dynamic power compared to conventional anti-fuse and MRAM-OTP redundancy solutions. These results validate the proposed architecture as an efficient, reliable, and scalable solution for radiation-tolerant memory.

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