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2025 Design, Automation & Test in Europe Conference (DATE)

March 31 – April 2, 2025

Lyon, France

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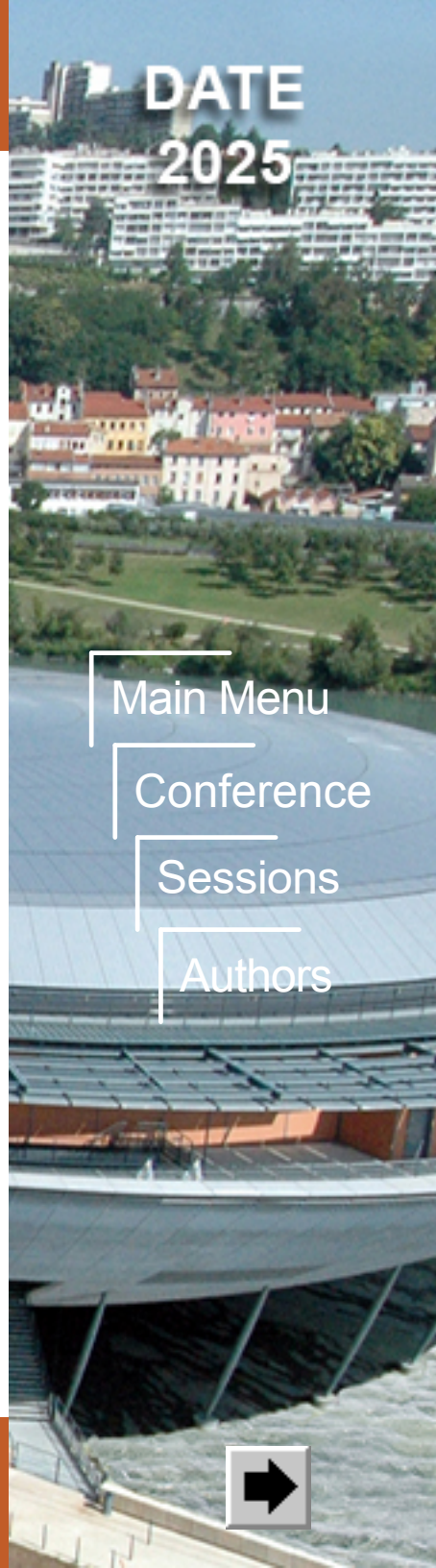
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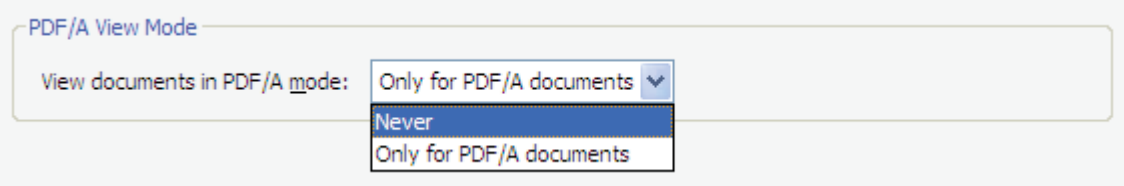
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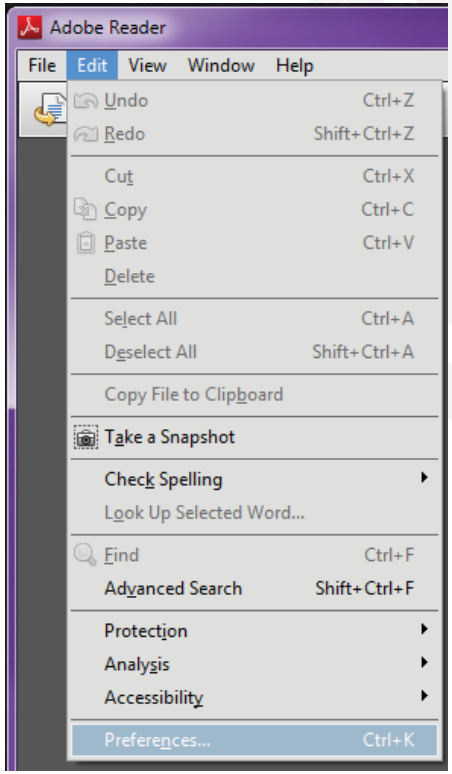


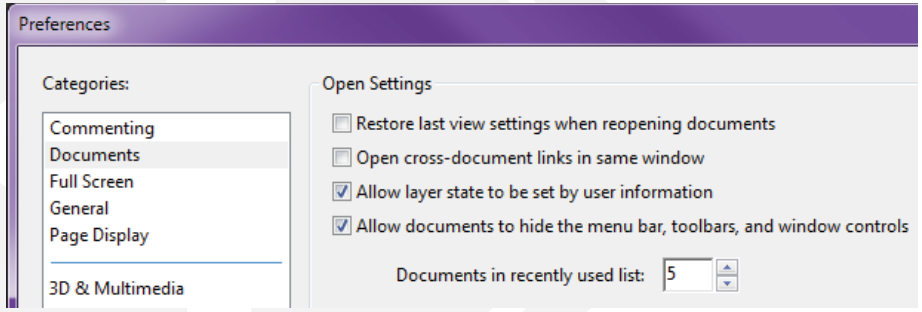
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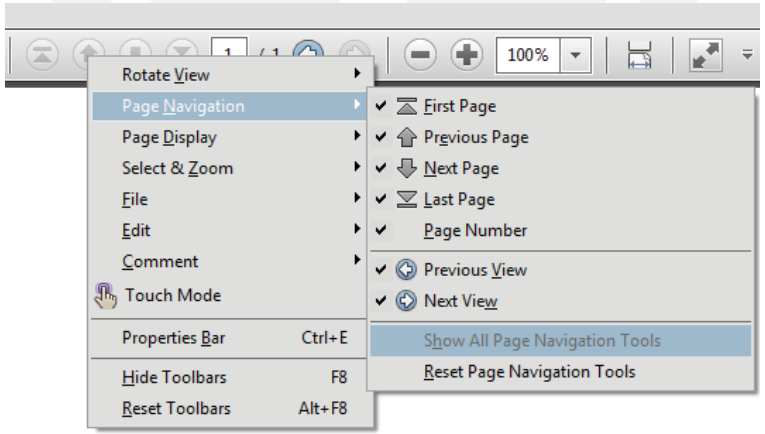
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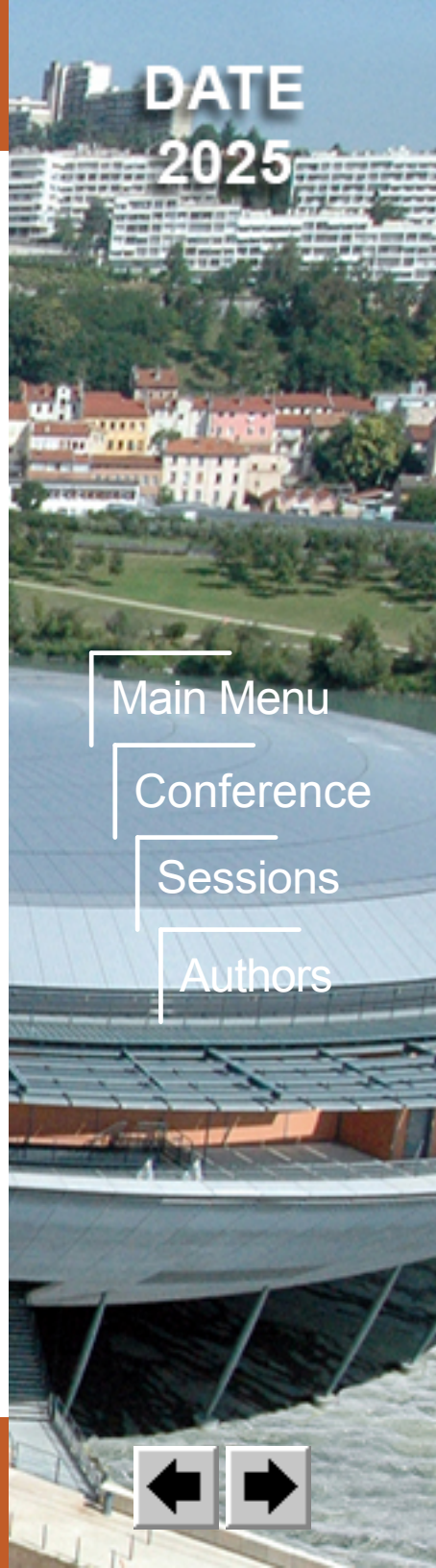
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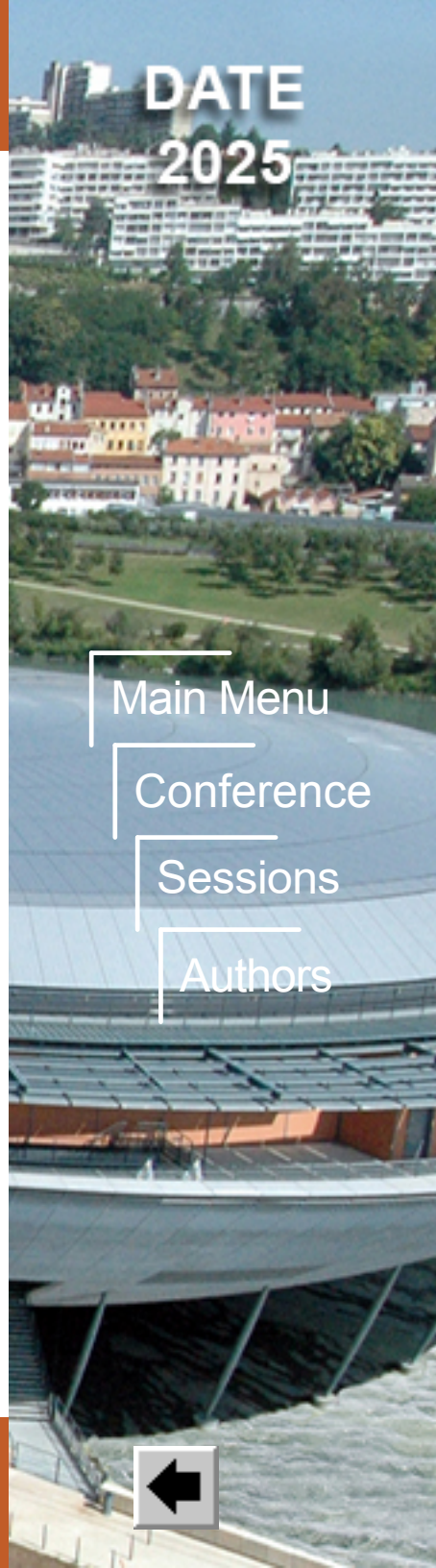
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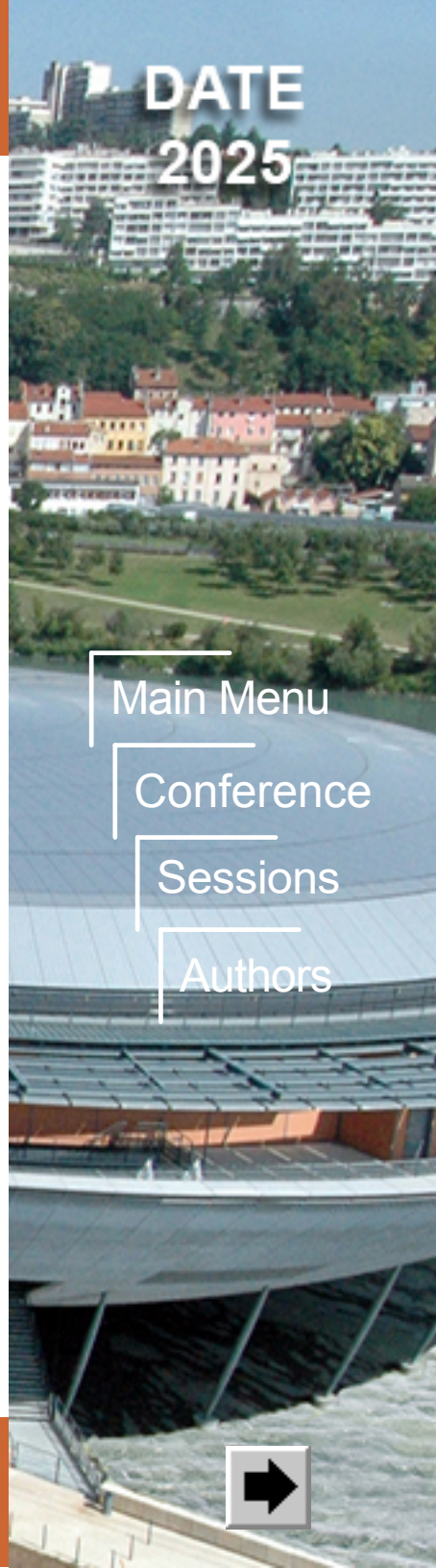
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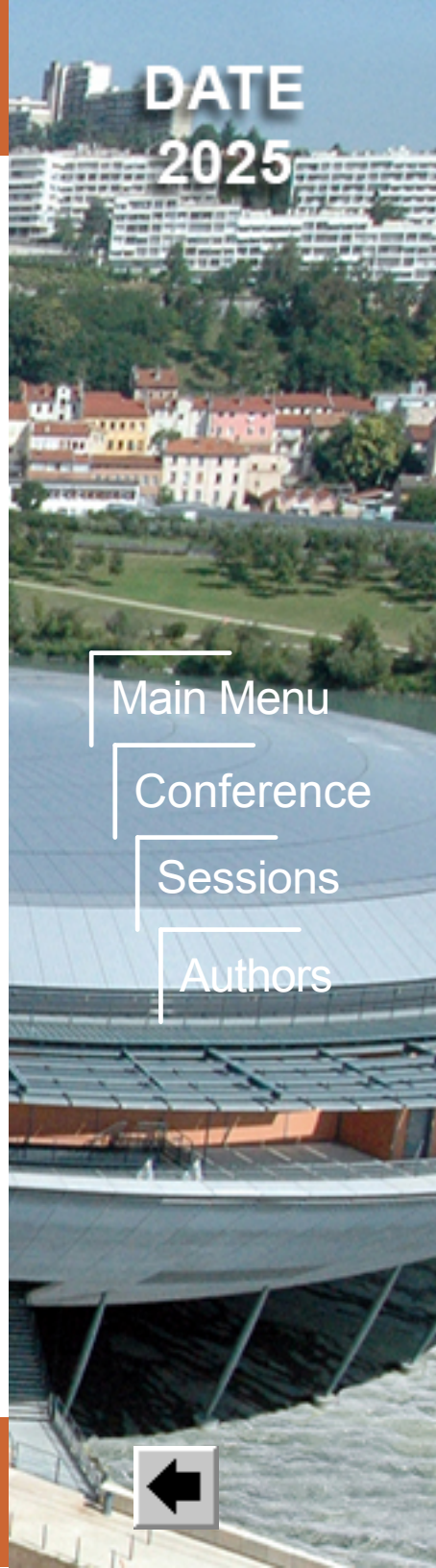
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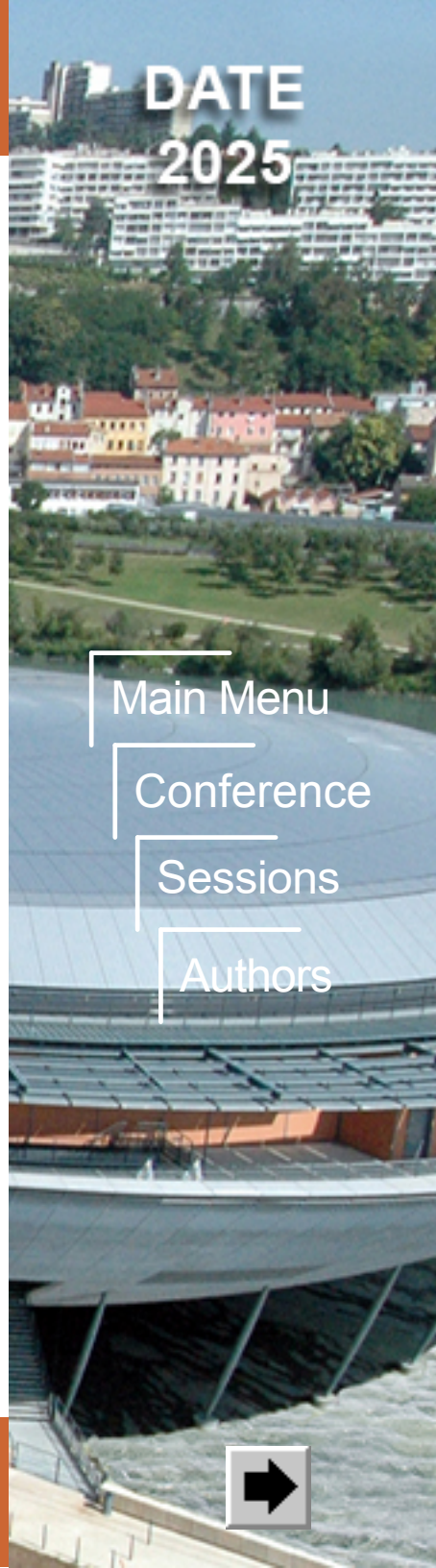
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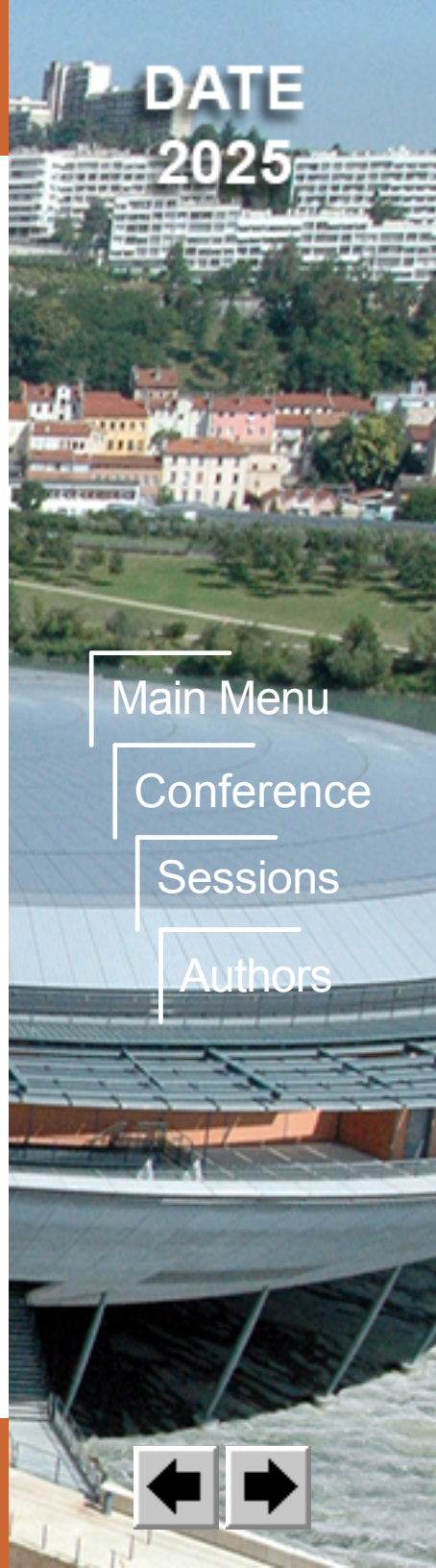
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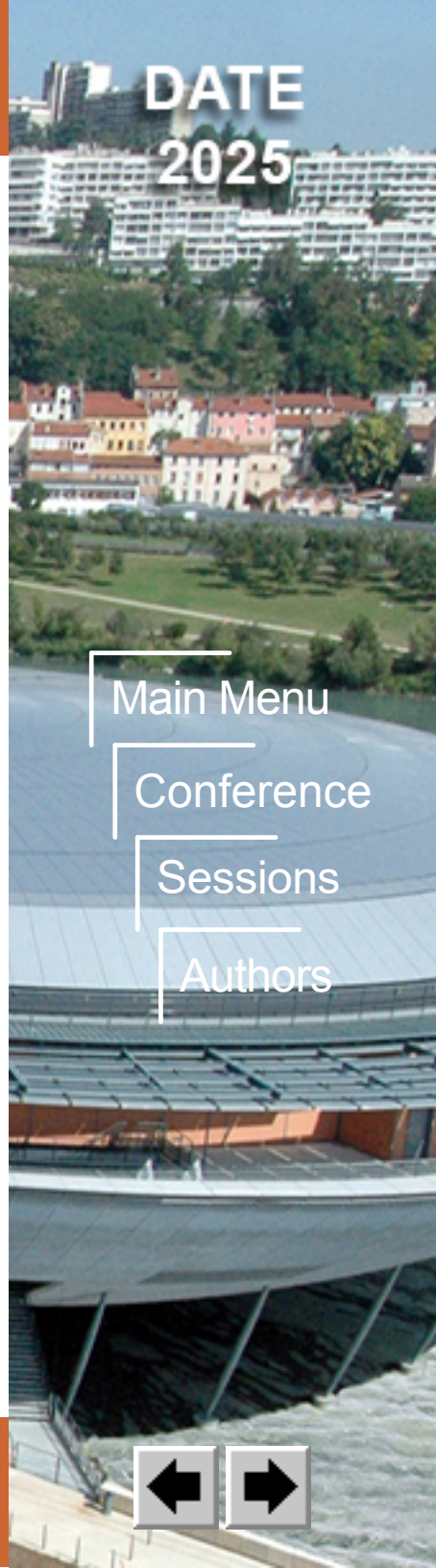
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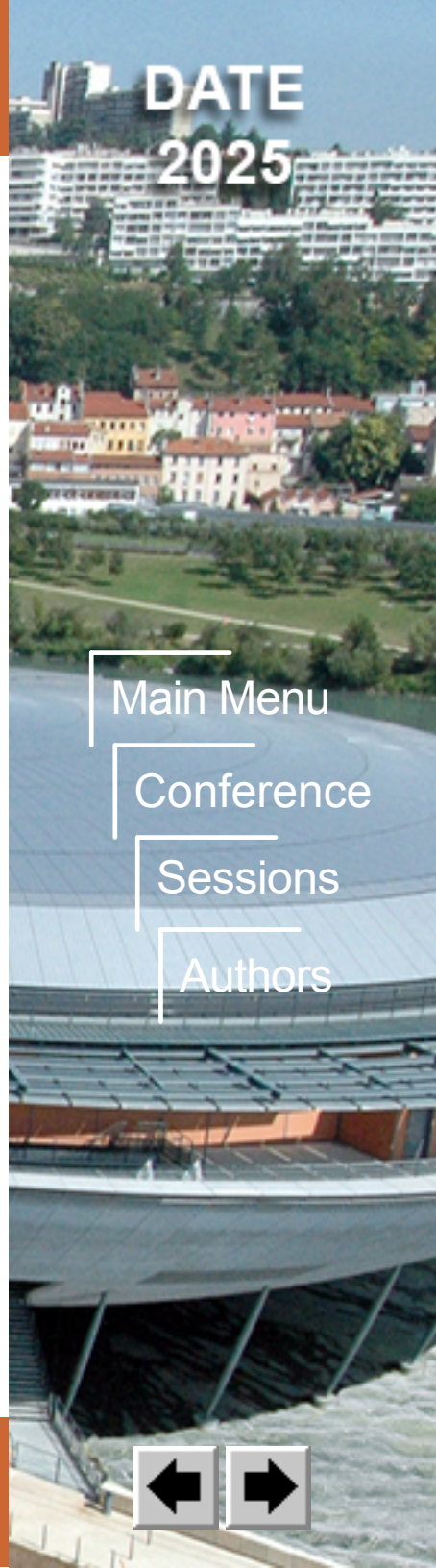
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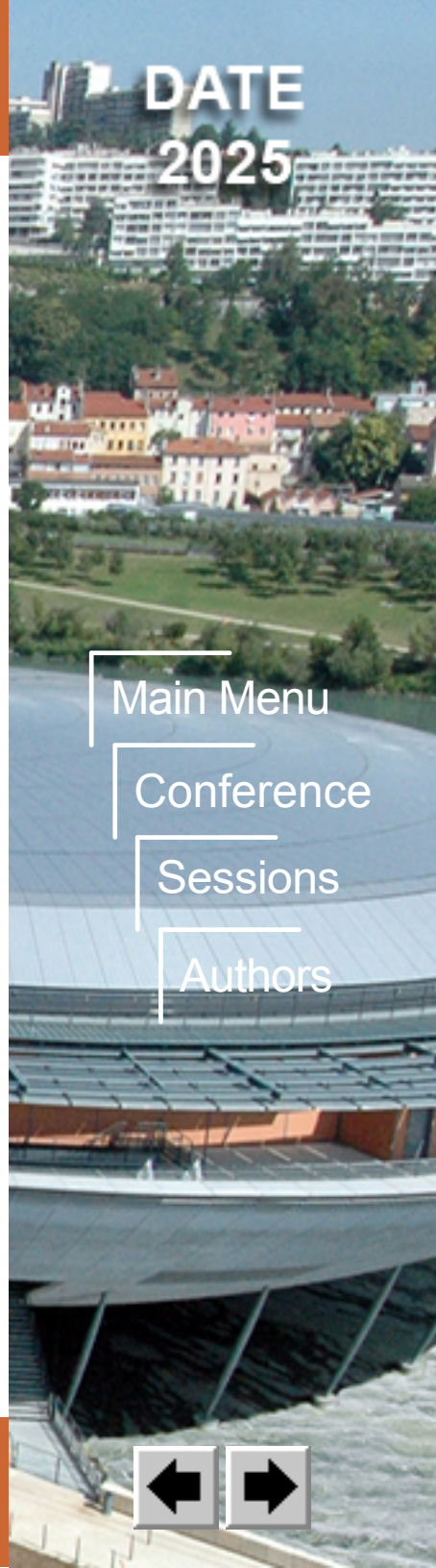
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DATE 2025 Foreword

Dear Colleague,

We proudly present the Advance Programme of the Design, Automation, and Test in Europe conference, DATE 2025. From the 31st of March to 2nd of April 2025, the community meets at the Centre de Congres de Lyon, France for Europe's largest design automation conference to discuss innovative ideas in all aspects of electronic design, automation and test – from system-level hardware and software implementation, right down to integrated circuit design and new electronics devices. We warmly welcome you to this event!

DATE 2025 offers an intensive three-day format, focussing on interaction and further strengthening of our already tight-knit community. The vast majority of regular papers will be presented in technical sessions using short flash-presentations, where the emphasis is on embedded poster-supported live interactions (in addition to common full-length presentation videos available before, during and after the conference). By using this format, we make sure that the attendees can actually spend their time doing what conferences are truly about: meeting, discussing and exchanging ideas.

Main Technical Programme

The main conference programme over the three days of the conference includes **31 Interactive Technical Sessions and 4 Sessions dedicated to the presentation of Best Paper Award candidates.** All sessions are organized in parallel tracks aligned with the four areas of DATE, i.e.,

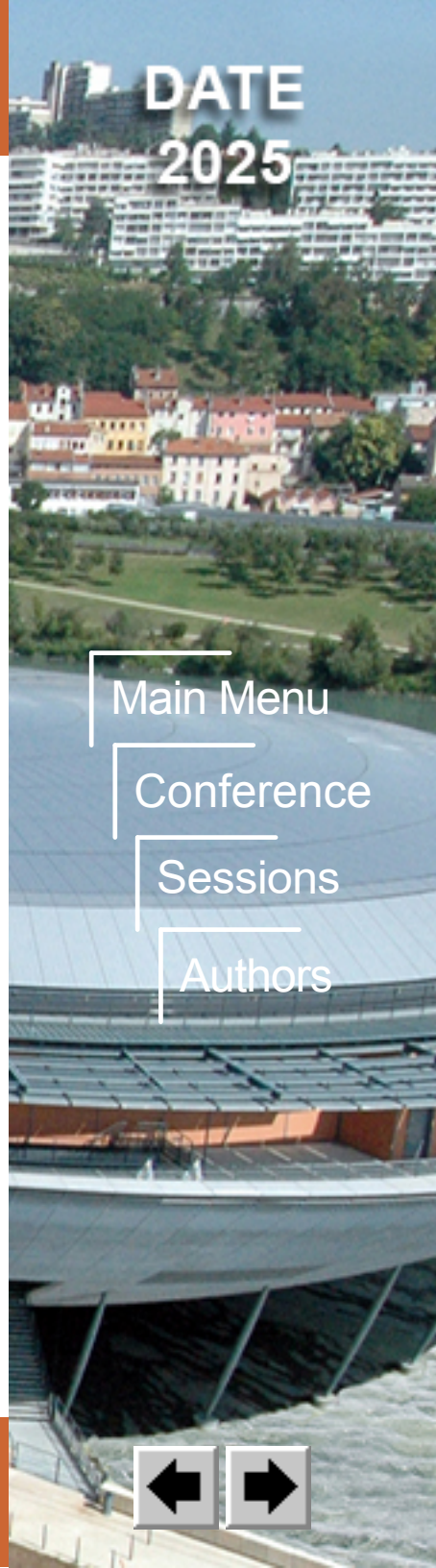
D – Design Methods & Tools,

A – Application Design,

T – Test and Dependability, and

E – Embedded Systems Design.

This year, we observed an unprecedented increase in paper submissions, with 22% more submissions than DATE 2024. Out of a total of 1551 abstract submissions, 1213 full research papers eventually went into review. As always, all these full papers have undergone a rigorous



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review procedure with the help of the 591 members (also a new record) of the Technical Programme Committee, who carried out 4647 reviews (mostly four reviews per submission). As the result of this process, 302 papers (24.8%) were finally selected for regular presentation and 56 additional submissions for presentation as extended abstract. We would like to sincerely thank all members of the Technical Programme Committee for their efforts on this demanding task!

Most importantly, our thanks also belong to all authors and presenters who constitute the very foundation of DATE. Authors from the submitted papers span representatives from the three main world regions: ~30% from Europe-Middle East-Africa, ~19% from the Americas, and 51% from Asia and Oceania. Overall, all submissions involved more than 7490 authors from 52 different countries – a distribution that clearly demonstrates DATE's international character, global reach and impact.

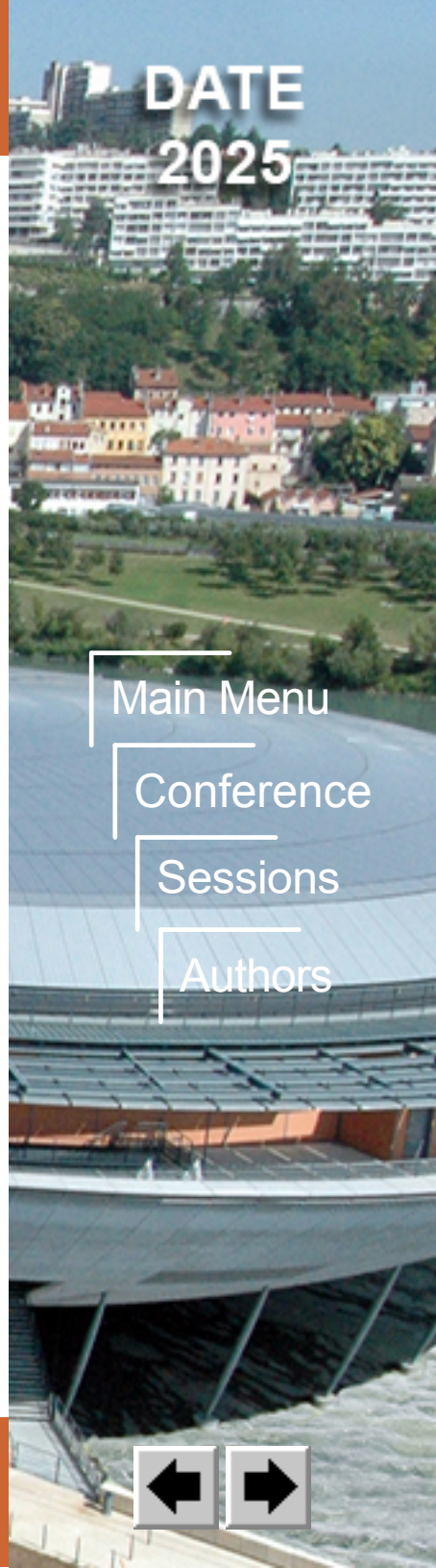
Monday Keynotes

After the Opening Ceremony on Monday, a plenary keynote lecture will be offered by Jean-Rene Lequepeys, CTO of CEA-Leti, FR, on "Towards greener electronics and a 1000X gain in energy efficiency: Co-Optimizing innovative IC architectures, disruptive CMOS technologies and new EDA tools". The presentation will be followed by a second plenary keynote lecture by Prof. Giovanni de Micheli, EPFL, CH on "A vision of systems and technology in a connected Europe". Later on, still on Monday, the IEEE CEDA Lunchtime will a panel commemorating the 20-year celebration of CEDA community. Each keynote talk and panel is also followed by a "Later… with the keynote speakers" session to enable deeper discussion and exchanges between the speakers and the DATE community.

Focus Sessions

In addition, the program offers a range of Focus Sessions on Hot Topics, including

- Specifications Mining in a World of Generative AI: Extensions, Applications, and Pitfalls
- AI-Driven Design Evolution: Benchmarking and Infrastructure for the Next Era of Semiconductors and Photonics
- Design Automation for Physical Computing Systems
- Designing Secure Space Systems
- 3D Integration, Cryogenic Circuits and Superconducting Logic: Emerging Trends Shaping the Future of High-Performance Computing
- Improving Chip Design Enablement for Universities in Europe
- European Startups on AI: Path to Success



- The European Chips Act: Ready to Take-Off
- GenAI-Native EDA: Redefining Verification with Large Language Models

Two **Late Breaking Results** sessions cover novel (orthogonal) research directions and breakthrough results in a variety of DATE subdomains. There will also be three dedicated sessions with presentations covering results and lessons learned from **Multi-Partner projects** addressing the full span of DATE topics. As we did last year, the programme will again feature two consecutive "**Unplugged**" sessions to stimulate brainstorming around the theme of "**Unconventional Computing**": a session format centered on direct exchanges among the participants, to formulate timely challenges as research problems and find inspiration for solution approaches.

Special Days

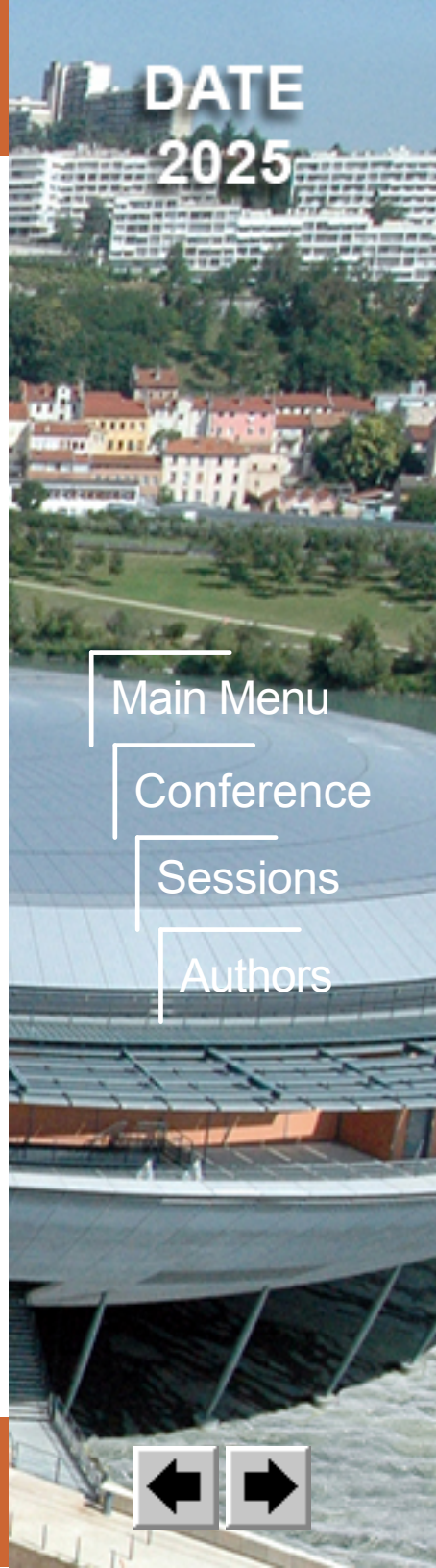
Two Special Days embedded in the programme will focus on areas bringing new challenges to the system design community: **Emerging Computing Paradigms** and **AI and ML Trends**. Each of the Special Days will have a full programme of keynotes and technical presentations.

The Special Day on **Emerging Computing Paradigms** will focus on alternative computing paradigms both from architecture design and technology implementation. There will be two sessions organized by Charlotte Frenkel, TU Delft, NL and John Paul Strachan, Forschungszentrum Juelich, DE. The sessions will feature a series of insightful talks from neuromorphic computing, spintronics neural networks, silicon photonics, quantum computing, cellular automata and probabilistic computing.

The Special Day on **AI and ML Trends** focuses on exploring the latest trends and innovations in Artificial Intelligence (AI) and Machine Learning (ML) in the context of DATE. As AI (and mainly generative AI) is booming, especially since the release of chat-GPT, we expect AI/ML will change the way to approach Design, Automation, and Test. In this context, field experts will present their thoughts on the challenges and opportunities of AI/ML and will engage the audience in an open discussion about the trends that the DATE community should pursue.

This Special Day will highlight the following topics:

- Design of hardware architectures and software, including automatic exploration of large



design spaces, assistance of the human designer, resource selection and optimization
- Verification of hardware architectures, with topics such as performance prediction, (formal) design validation, accelerating simulations thanks to AI-Augmented Surrogate Models
- AI-Accelerated Physical Design and Validation of layout and floorplans New AI accelerators architectures

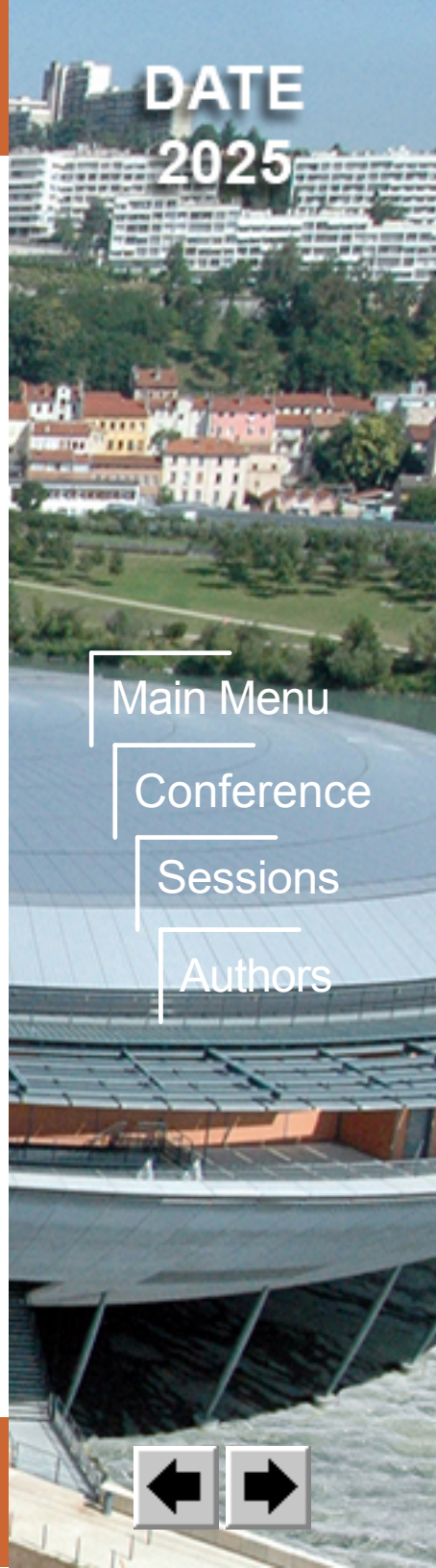
Special Initiative on Autonomous Systems Design

A now traditional Special Initiative on Autonomous Systems Design is held on Monday and Tuesday, consisting of reviewed and invited papers, as well as working sessions on self-governed and self-adaptive systems that are designed to operate in an open and evolving environment, which has not been completely defined at design time. There will be five technical sessions and an embedded workshop. On Tuesday lunchtime there will be a keynote by Yankin Tanurhan, Synopsys, US on "**AI/ML at the forefront of semiconductor evolution: Enhancing design, efficiency and performance**".

Young People Programme

The Young People Programme (YPP), an initiative targeting PhD students with the goal of supporting their career development, will take place on Monday, Tuesday and Wednesday. The programme kicks off on Monday morning with the **Panel on Careers Perspectives** and **Career Fair - University** during which participating companies will introduce themselves and explain their business and working environment. In the afternoon, the students will have the opportunity to attend the **University Fair & Student Teams Fair** to introduce themselves. Next will take place the **Career Fair – Industry** with company presentations. Hereafter, the students can exchange with potential employers from the EDA and microelectronics industries and arrange interviews during the **Speed Dating** session. The **PhD Forum** will close the first day of the conference, and will include 41 selected students who have completed, or are about to complete, their PhD thesis showcasing their work to the academic and industrial community.

On Tuesday, the Young People Programme continues with the **HackTheSilicon DATE** and on Wednesday it will dedicate half day to the **SoC Labs: The academic community for System on Chip development**.



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Workshops

Over the course of the conference, **seven half-day workshops** cover several pressing topics from areas such as:

- Eco-ES: Eco-design and circular economy of Electronic Systems,
- Workshop on Open-Source Design Automation,
- Heterogeneous Integration: from advanced 3D technology to innovative computing architectures,
- Cross-stack explorations of ferroelectric-based logic and memory solutions for at-scale compute workloads,
- Open source solutions for massively parallel integrated circuits,
- Designing sustainable intelligent systems: Integrating carbon footprint reduction, TinyML and RISC-V
- Workshop on NanoSecurity: From nanoelectronics to secure systems

Technical Tutorials

The DATE programme will include three embedded tutorials offered by leading experts in their respective fields. The topics span:

- Agile Hardware Specialization: A toolbox for Agile Chip Front-end Design
- Securing the Future: Designing Built-in-Security Enabled Photonic AI Chip
- Lifecycle Management of Emerging Memories: Why and How?

Finally, the technical programme is complemented by the **Welcome Reception** on Monday evening and the traditional **DATE Party** on Tuesday evening. Both events are unique networking opportunities for the community to meet, discuss and exchange.

For further information, please visit: www.date-conference.com

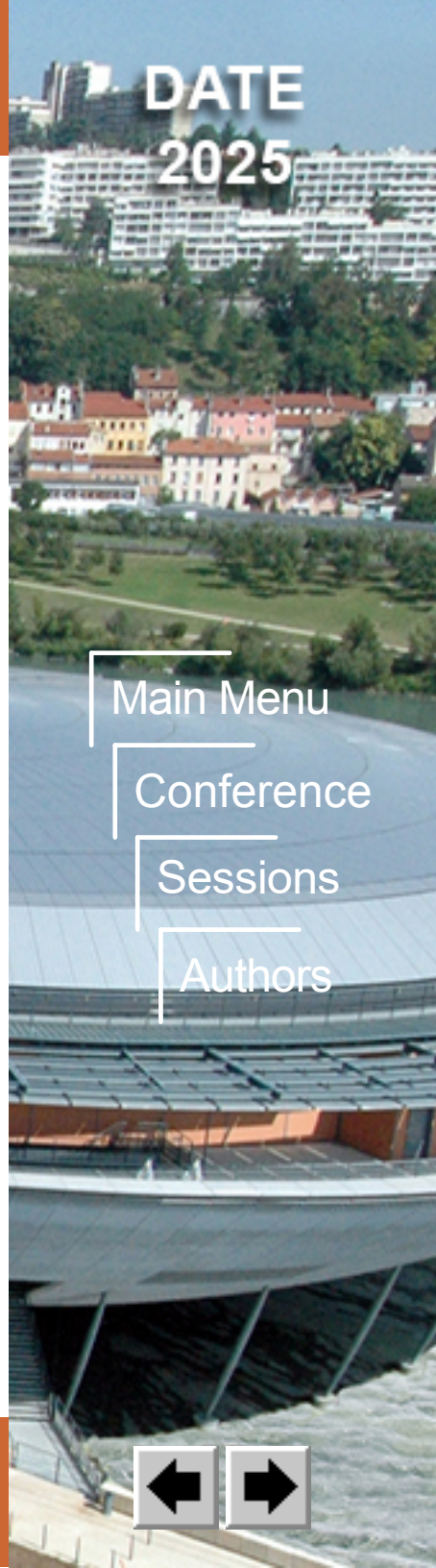
Overall, this year's programme provides a broad, deep and exciting coverage of all the topics our community stands for. We sincerely thank everyone who participated in its organisation and execution. And, of course, we wish you an exciting and memorable DATE 2025 in Lyon, France!



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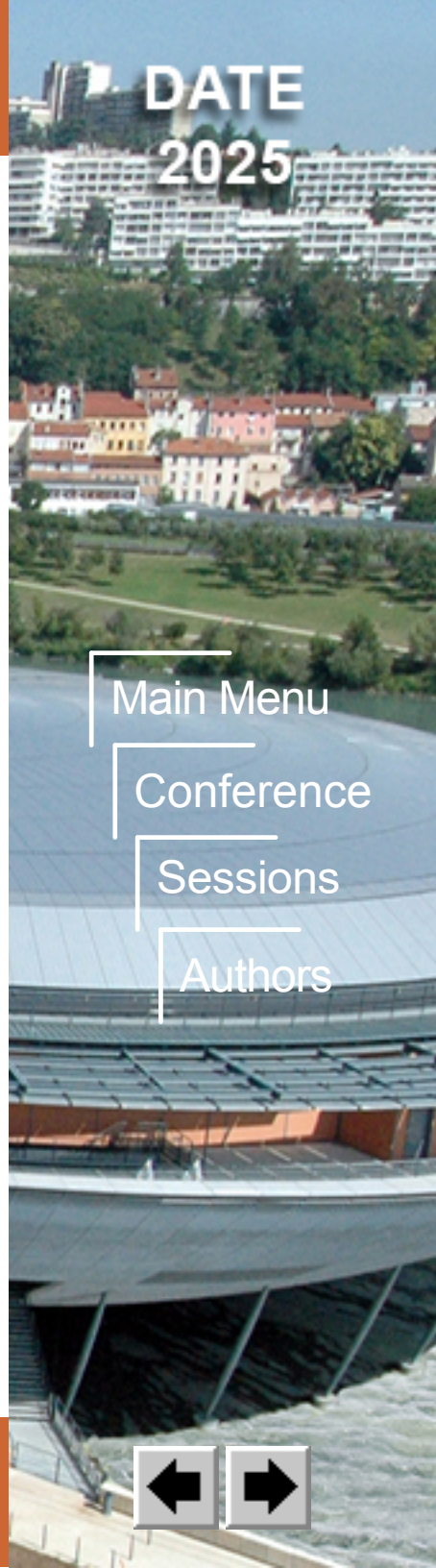
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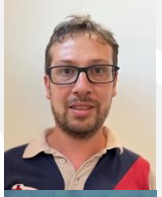
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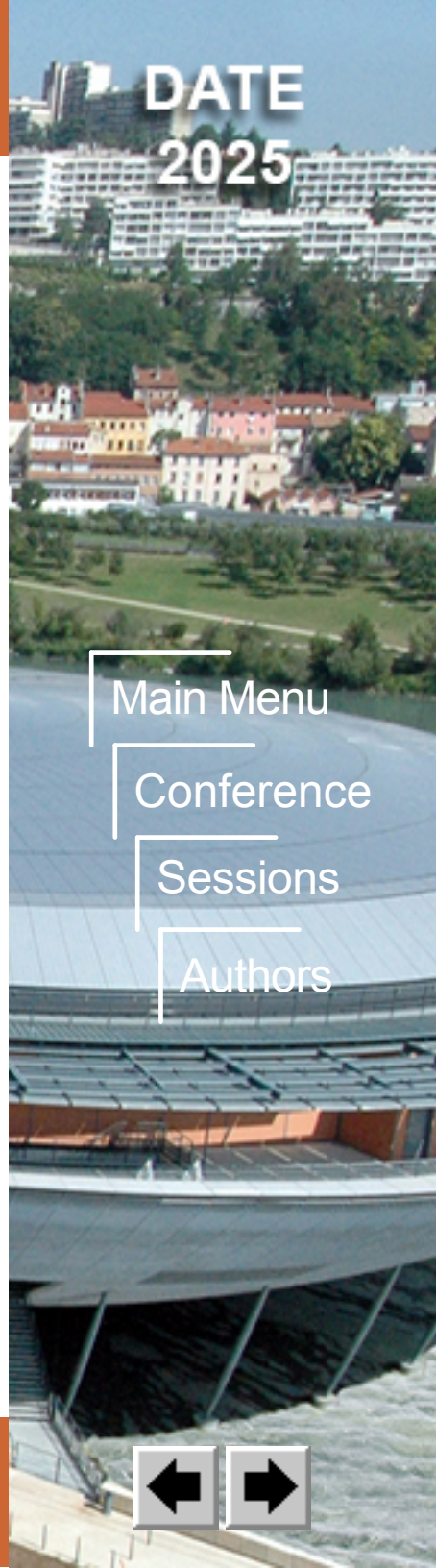
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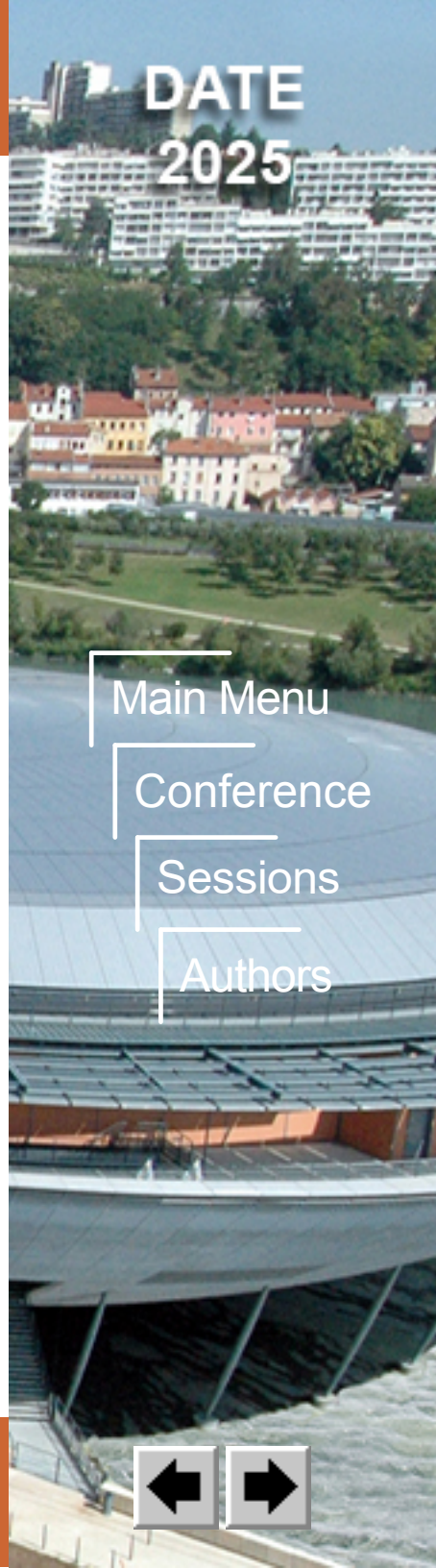
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D2 System Simulation and Validation
Chair: Georg Weissenbacher, TU Wien, AT
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D3 Formal methods and Verification
Chair: Stefano Quer, Politecnico di Torino, IT
Co-Chair: Rolf Drechsler, University of Bremen/DFKI, DE

DT4 Design and Test for Analog and Mixed-Signal Circuits and Systems, and MEMS
Chair: Salvador Mir, CNRS/Univ. Grenoble Alpes/TIMA, FR
Co-Chair: Ricardo Martins, Instituto de Telecomunicações / Instituto Superior Técnico – Universidade de Lisboa, PT

DT5 Design and Test of Hardware Security Primitives
Chair: Mike Hutter, PQShield, AT
Co-Chair: Fatemeh Ganji, Worcester Polytechnic Institute, US

DT6 Design and Test of Secure Systems
Chair: Tobias Schneider, NXP Semiconductors, AT
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D7 Network-on-Chip and On-Chip Communication
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D8 Architectural and Microarchitectural Design
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D11 Reconfigurable Systems
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D12 Logical Analysis and Design
Chair: Tiziano Villa, Dipartimento d'Informatica, Universita' di Verona, IT
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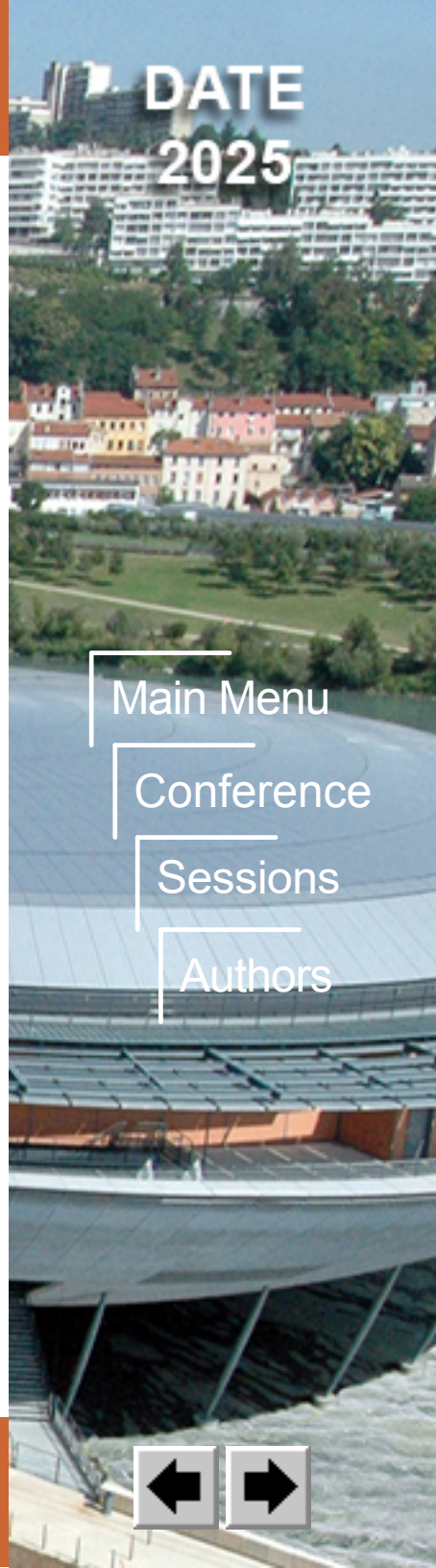
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D15 Emerging Design Technologies for Future Memories
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A4 Autonomous Systems and Smart Industry

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T3 Dependability and System-Level Test

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DT6 Design and Test of Secure Systems

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Chair: Ahmed Rezine, Linköping University, SE
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Chair: Jing Li, New Jersey Institute of Technology, US
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Co-Chair: Irem Boybat, IBM Research Europe - Zurich, CH

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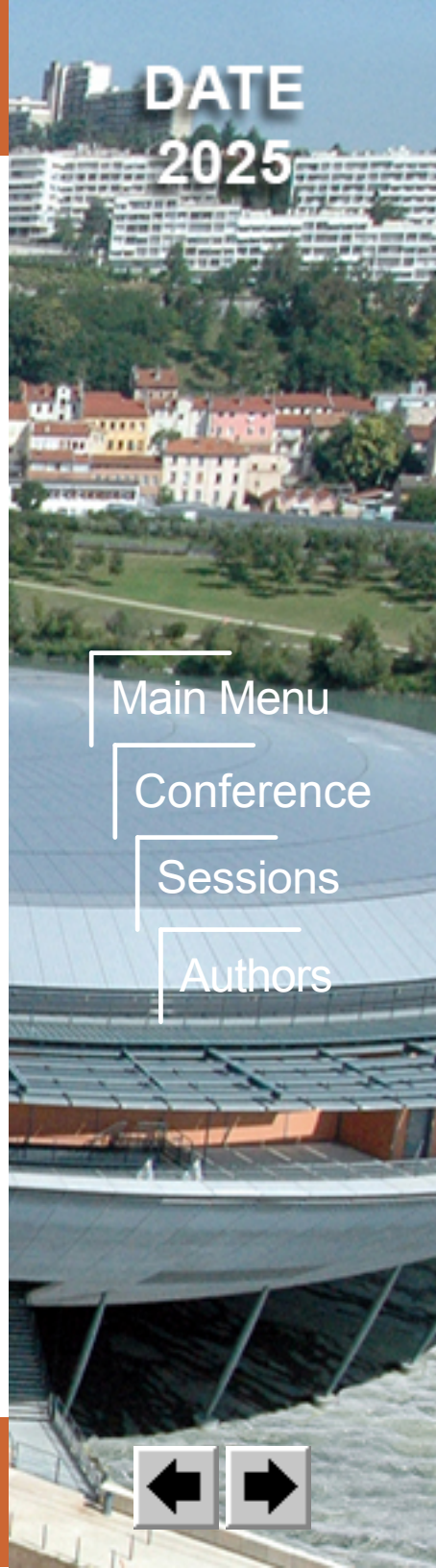
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D3 Formal Methods and Verification

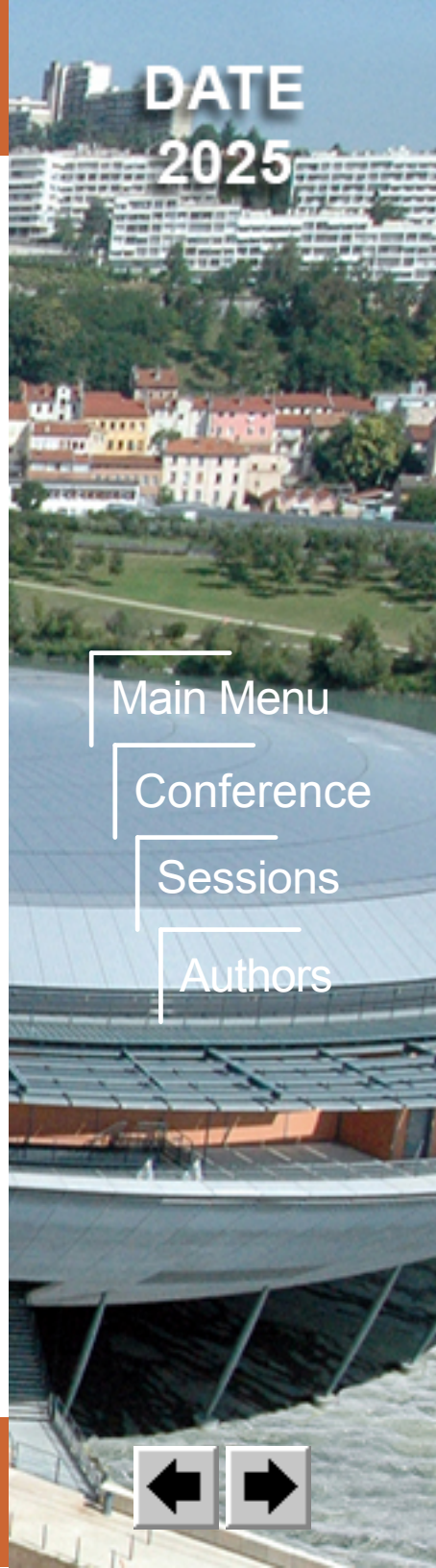
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DT5 Design and Test of Hardware Security Primitives

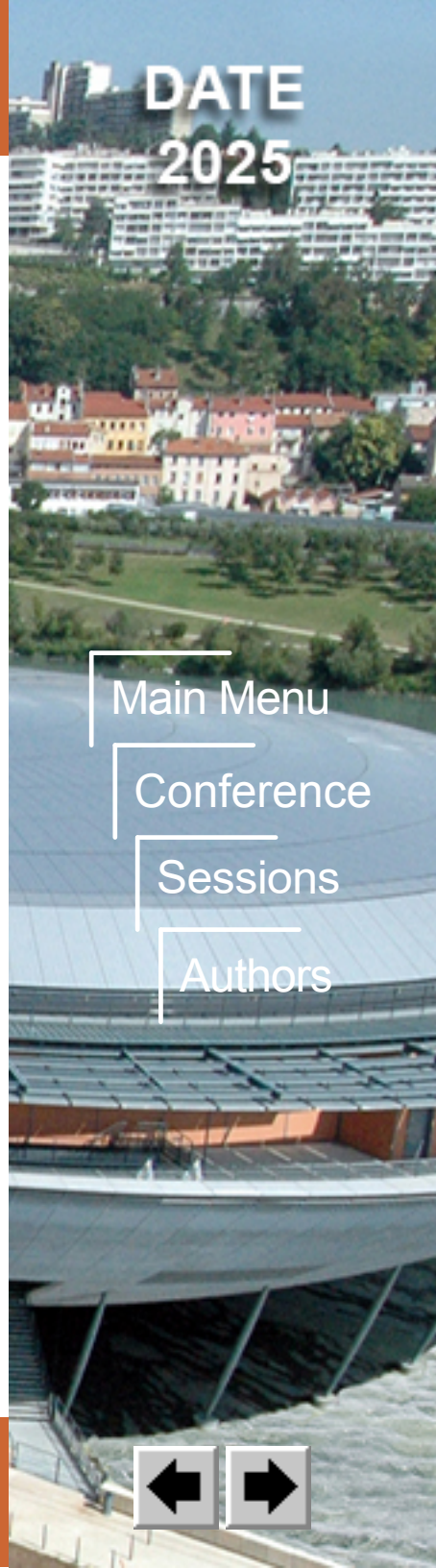
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D8 Architectural and Microarchitectural Design

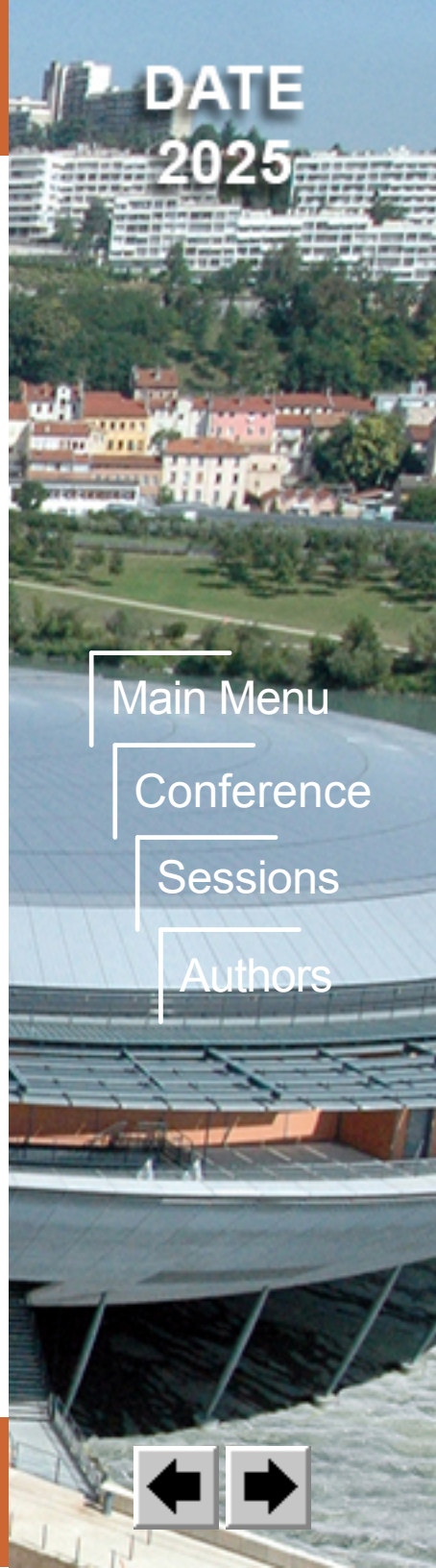
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D10 Approximate Computing

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D11 Reconfigurable Systems

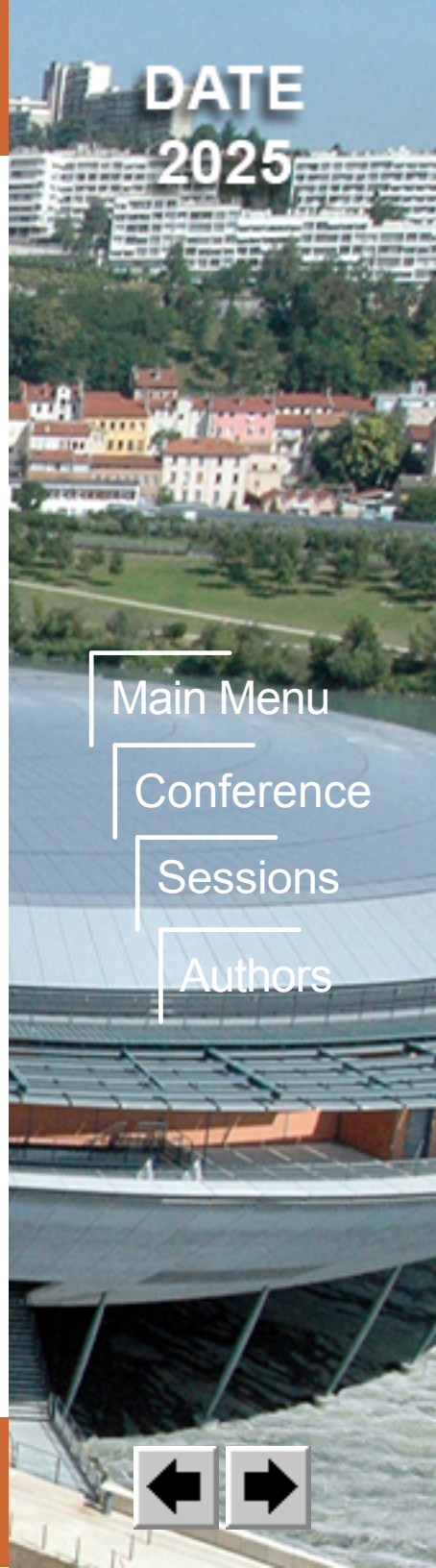
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Sessions
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Conference Information

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Rajeev Murgai, Synopsys India Pvt. Ltd., IN
Andre Reis, UFRGS, BR

D13 Physical Analysis and Design

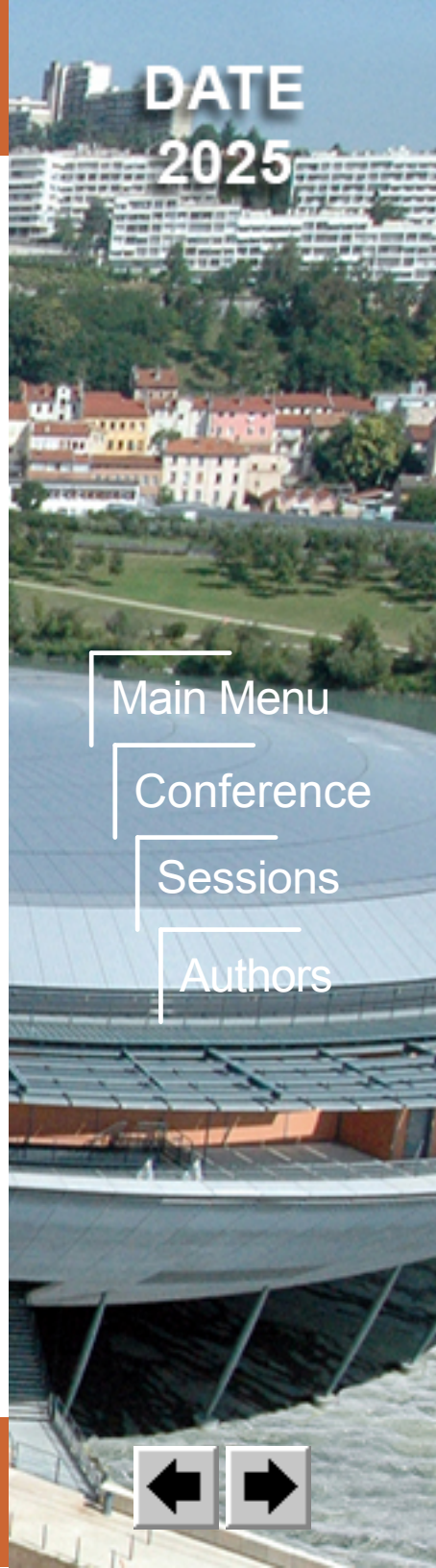
Chair: Matthias Fuegger, CNRS & LMF, ENS Paris-Saclay, FR
Co-Chair: Shao-Yun Fang, National Taiwan University of Science and Technology, TW

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Zhiang Wang, University of California San Diego, US
Zhiyao Xie, Hong Kong University of Science and Technology, HK
Wenjian Yu, Tsinghua University, CN

D14 Emerging Design Technologies for Future Computing

Chair: Michael Niemier, University of Notre Dame, US
Co-Chair: Ari Alastalo, VTT, FI

Ihsen Alouani, CSIT, Queen's University Belfast, UK, GB
Salvatore Amoroso, Synopsys Inc, GB
Giovanni Ansaloni, EPFL, CH
Olivia Chen, Kyushu University, JP
Siddharth Joshi, University of Notre Dame, US
Thomas Kämpfe, Fraunhofer IPMS, DE
Asif Ali Khan, TU Dresden, DE
Lauri Koskinen, University of Oulu, FI
Marko Kosunen, Aalto University, FI
Can Li, The University of Hong Kong, HK
Xueqing Li, Tsinghua University, CN
Yu Li, Harbin Institute of Technology, Shen Zhen, CN
Vasilis Pavlidis, Aristotle University of Thessaloniki, GR
Jean-Michel Portal, Aix-Marseille University, FR
Dayane Reis, University of South Florida, US
Vishnu Unnikrishnan, Tampere University, FI
Pascal Vivet, CEA-Leti, FR
Tony Wu, Meta, US
Bonan Yan, Peking University, CN
Zheyu Yan, Zhejiang University, CN



Conference Information

D15 Emerging Design Technologies for Future Memories

Chair: Rajendra Bishnoi, Delft University of Technology,, NL
Co-Chair: Sonal Shreya, Aarhus University, DK

Harshit Agarwal, IIT Jodhpur, IN
Charles Augustine, NVIDIA, US
Laura Bégon-Lours, ETH Zürich, CH
Erika Covi, University of Groningen, NL
Seema Dhull, Principal Engineer, IN
Deliang Fan, Arizona State University, US
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Farshad Moradi, Aarhus University, DK
Jongsun Park, Korea University, KR
Guillaume Prenat, Spintec, FR
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Xueyan Wang, Beihang University, CN
Tianyao Xiao, Sandia National Laboratories, US
Amirreza Yousefzadeh, University of Twente, NL

D16 Design Automation for Quantum Computing

Chair: Ilia Polian, University of Stuttgart, DE
Co-Chair: Carmen G. Almudever, Technical University of Valencia, ES

Anastasiia Butko, LBNL, US
Edoardo Charbon, EPFL, CH
Andrew W Cross, IBM, US
Sebastian Feld, Delft University of Technology, NL
Francisco Garcia-Herrero, Universidad Complutense de Madrid, ES
Swaroop Ghosh, Pennsylvania State University, US
Edoardo Giusto, University of Naples, Federico II, IT
Lingling Lao, National University of Defense Techonology, CN
Sonia Lopez Alarcon, Rochester Institute of Technology, US
Matthias Möller, Delft University of Technology, NL
Siyuan Niu, Lawrence Berkeley National Lab, US
Leon Riesebos, IonQ, US
Fabio Sebastiano, Delft University of Technology, NL
Yunong Shi, AWS Quantum Technologies, US
Michal Stechy, PsiQuantum, PL
Robert Wille, Technical University of Munich, DE

A1 Power-efficient and Smart Energy Systems for Sustainable Computing

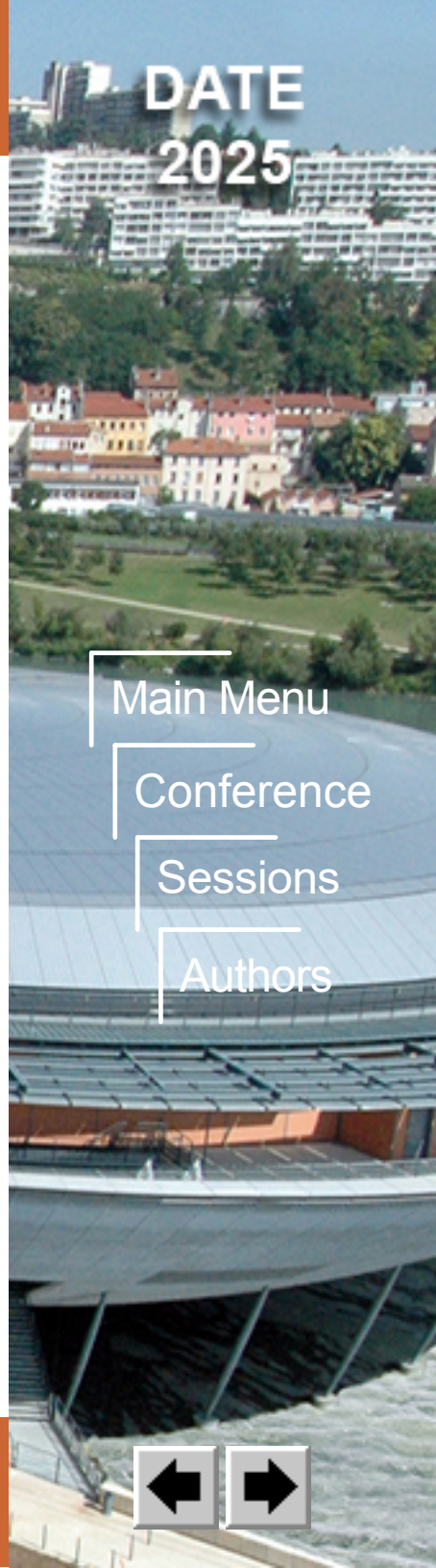
Chair: Semeen Rehman, TU Wien, AT
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David Castells-Rufas, Universitat Autònoma de Barcelona, ES
Kuan-Hsun Chen, University of Twente, NL
César Fuguet, CEA List, FR
Min Li, Huawei Research Europe, BE

A2 Smart Society and Digital Wellness

Chair: Graziano Pravadelli, University of Verona, IT
Co-Chair: Tiziana Margaria, University of Limerick and Lero, IE

Daniela De Venuto, Politecnico di Bari, IT
Florenc Demrozi, Department of Electrical Engineering and Computer Science, University of Stavanger, NO
UmaMaheswari Devi, IBM Research - India, IN
Srinivas Katkoori, University of South Florida, US



Conference Information

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Bo Wang, SUTD, SG
Georgios Zervakis, University of Patras, GR
Sefki Kolozali, University of Essex, GB
Velu Kumaravel, University of Oldenburg, DE
Bo Wen, IBM Research, US
Farhana Zulkernine, School of Computing, Queen's University, CA

A3 Secure Systems, Circuits, and Architectures

Chair: Cedric Marchand, Ecole centrale Lyon, FR
Co-Chair: Mirjana Stojilovic, EPFL, CH

M. Khurram Bhatti, University of Exeter, GB
Noemie Boher, Intrinsic-ID, NL
Luca Cassano, Politecnico di Milano, IT
Julien Francq, Naval Group, FR
Kris Gaj, George Mason University, US
Matthias Hiller, Fraunhofer AISEC, DE
Wei Hu, Northwestern Polytechnical University, CN
Naghmeh Karimi, University of Maryland Baltimore County, US
Cuauhtemoc Mancillas, Cinvestav, MX
Angelos Marnerides, University of Cyprus, CY
Maria Mendez Real, Lab-STICC CNRS UMR 6285, FR
Michael Pehl, Technical University of Munich, DE
Amin Rezaei, California State University, Long Beach, US
Dustin Richmond, University of California, Santa Cruz, US
Ahmad-Reza Sadeghi, Technische Universitaet Darmstadt, DE
Jo Vliegen, ES&S, imec-COSIC, ESAT, KU Leuven, BE
QIAN WANG, University of California Merced, US
Xiaolin Xu, Northeastern University, US

A4 Autonomous Systems and Smart Industry

Chair: Antonio Carlos Schneider Beck, Universidade Federal do Rio Grande do Sul, BR
Co-Chair: Lulu Chan, NXP Semiconductors, NL

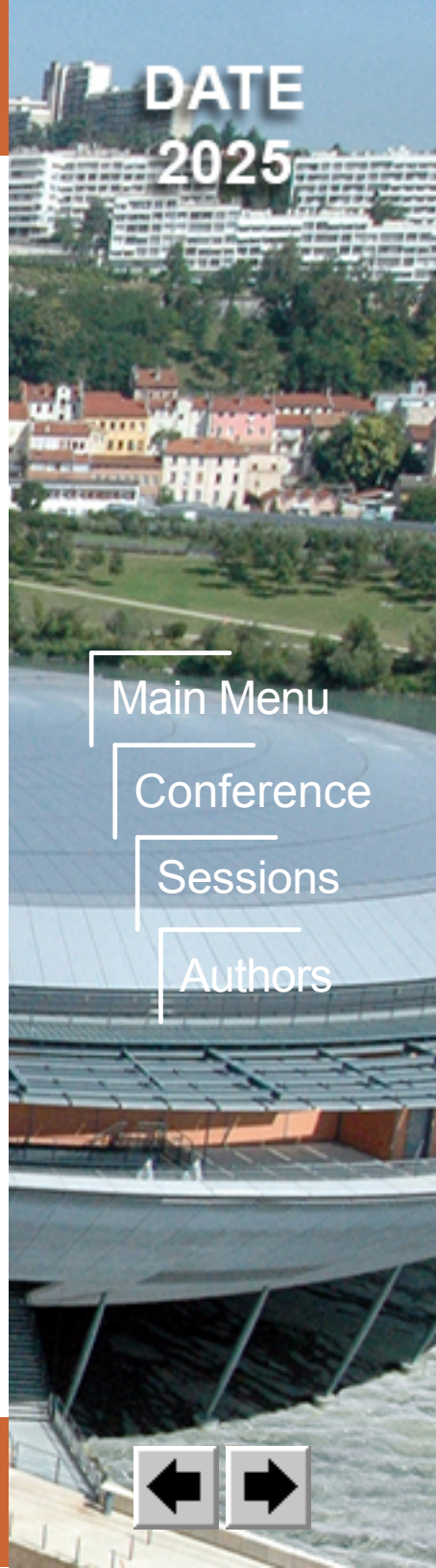
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A5 Applications of Emerging Technologies

Chair: Mariagrazia Graziano, Politecnico di Torino, IT
Co-Chair: Sébastien Le Beux, Concordia University, CA

A6 Applications of Artificial Intelligence

Chair: Christos Kyrkou, KIOS CoE, University of Cyprus, CY
Co-Chair: Stylianos Venieris, Samsung AI, GB



Conference Information

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Zhiqiang Que, Imperial College London, GB
Qing Wang, Delft University of Technology, NL
Lei Xun, University of Southampton, GB
Shuochao Yao, George Mason University, US

T1 Modelling and Mitigation of Defects, Faults, Variability, and Reliability

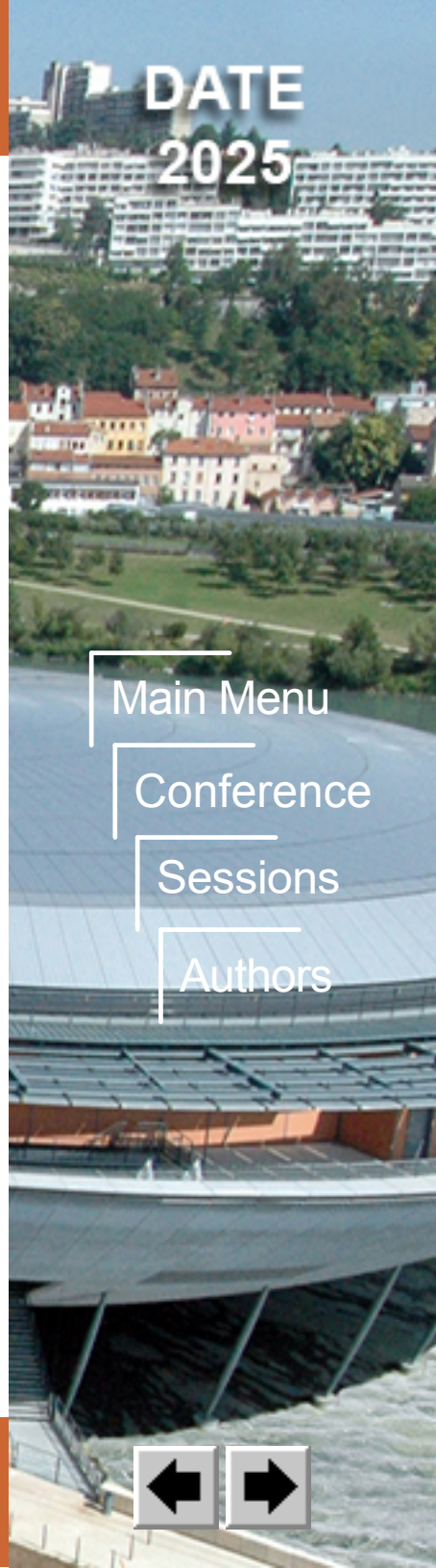
Chair: Leticia Maria Bolzani Poehls, IHP, DE
Co-Chair: Mottaqiallah Taouil, Delft University of Technology, NL

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Daniel Arumi, UPC, ES
Sarah Azimi, Politecnico di Torino, IT
Riccardo Cantoro, Politecnico di Torino, IT
Victor Champac, INAOE, MX
Bram Kruseman, NXP Semiconductors, NL
Huawei Li, Institute of Computing Technology, Chinese Academy of Sciences, CN
Cristina Meinhardt, UFSC, BR
Jaan Raik, Tallinn University of Technology, EE

T2 Test Generation, Test Architectures, Design for Test, and Diagnosis

Chair: Sybille Hellebrand, Paderborn University, DE
Co-Chair: Jerzy Tyszer, Poznan University of Technology, PL

Paolo Bernardi, Politecnico di Torino, IT
Jennifer Dworak, Southern Methodist University, US
Stephan Eggersgluess, Siemens EDA, DE
Stefan Holst, Kyushu Institute of Technology, JP
Yu Huang, HiSilicon, US
Maksim Jenihhin, Tallinn University of Technology, EE
Chrysovalantis Kavousianos, Department of Computer Science and Engineering, University of Ioannina, GR
Artur Pogiel, Siemens Digital Industries Software, PL
Annachiara Ruospo, Politecnico di Torino, IT
Melanie Schillinsky, NXP Germany GmbH, DE

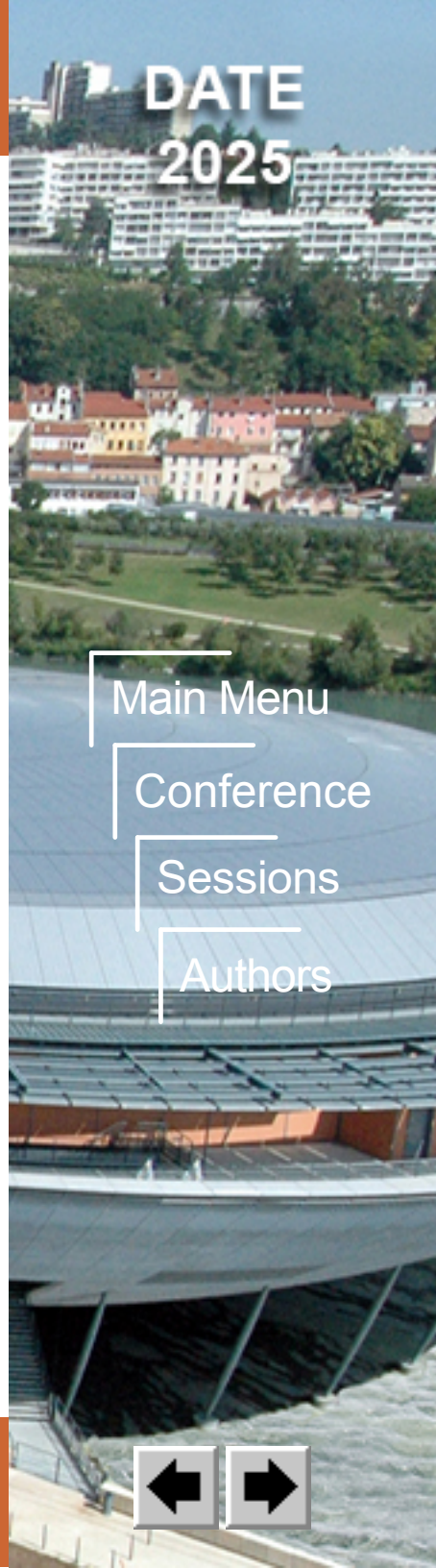


Conference Information

Christian Sauer, Synopsys, DE
Arnaud Virazel, LIRMM, FR
Hank Walker, Texas A&M University, US

T3 Dependability and System-Level Test	DT4 Design and test for analog and mixed-signal circuits and systems, and MEMS
Chair: Dimitris Gizopoulos, University of Athens, GR Co-Chair: Osman Unsal, Barcelona supercomputing center, ES	Chair: Salvador Mir, CNRS/Univ. Grenoble Alpes/TIMA, FR Co-Chair: Ricardo Martins, Instituto de Telecomunicações / Instituto Superior Técnico – Universidade de Lisboa, PT
Cristiana Bolchini, Politecnico di Milano, IT Stefano Di Carlo, Politecnico di Torino, IT Harish Dixit, Meta Platforms Inc., US Sudhanva Gurumurthi, Advanced Micro Devices, Inc (AMD), US Siva Kumar Sastry Hari, NVIDIA, US Jiun-Lang Huang, National Taiwan University, TW David Kaeli, Northeastern University, US Yanjing Li, University of Chicago, US Cameron McNairy, Tenstorrent, US	Engin Afacan, Gebze Technical University, TR Florence AZAIS, Univ. Montpellier, CNRS, LIRMM, FR Tiago Balen, UFRGS, BR Manuel Barragan, TIMA Laboratory, FR Hung-Ming Chen, Institute of Electronics, National Yang Ming Chiao Tung University, TW William Eisenstadt, University of Florida, US Maria Helena Fino, Nova University of Lisbon, PT Estelle Lauga-Larroze, Univ Grenoble Alpes, FR Raghu Maddali, Senior Director of Test, NXP Semiconductors, US Piero Malcovati, University of Pavia, IT Sule Ozev, ASU, US Fabio Passos, University of Lisbon and INESC-ID, PT Elisenda Roca, Instituto de Microelectronica de Sevilla, ES Rosa Rodríguez-Montañés, UPC, ES Renato Silveira Feitoza, PROPHESEE, FR Armin Tajalli, University of Utah, US Dani Tannir, Lebanese American University, LB Jose Tejada, Analog Devices Inc, ES Ender Yilmaz, Rambus, US

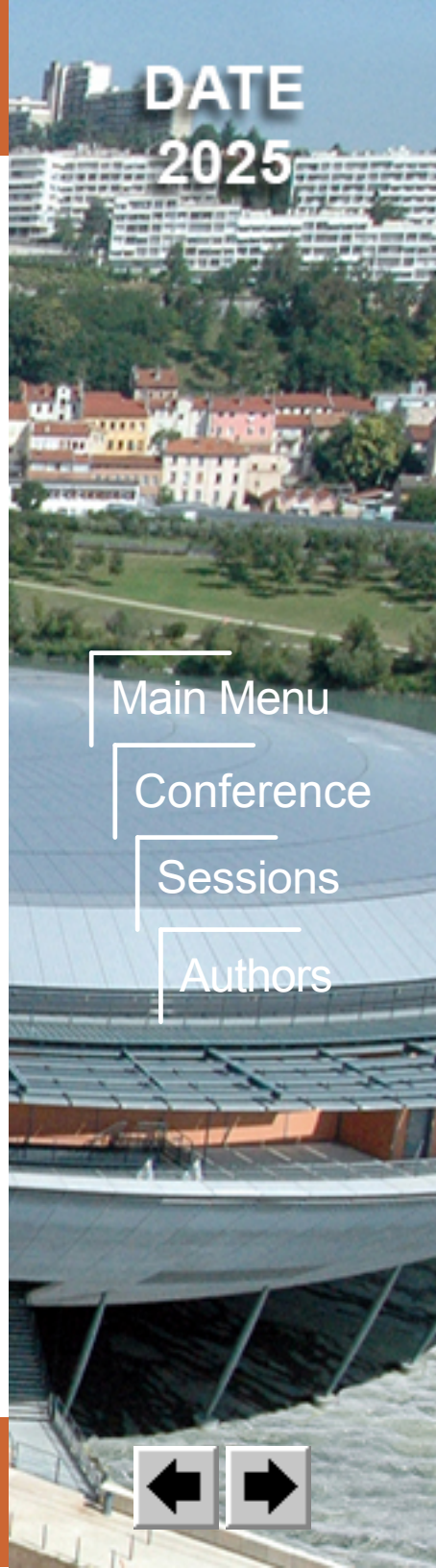
DT5 Design and Test of Hardware Security Primitives	DT6 Design and Test of Secure Systems
Chair: Mike Hutter, PQShield, AT Co-Chair: Fatemeh Ganji, Worcester Polytechnic Institute, US	Chair: Tobias Schneider, NXP Semiconductors, AT Co-Chair: Elif Bilge Kavun, University of Passau, DE
Aydin Aysu, North Carolina State University, US Samuel Chef, Nanyang Technological University, SG Lukasz Chmielewski, Masaryk University (Brno, Czechia), CZ	Anita Aghaie, Siemens AG, DE Victor Arribas, Rambus Inc., NL Josep Balasch, KU Leuven, BE Davide Bellizia, Telsy, IT



Conference Information

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Ahmet Can Mert, i2ware Technology, AT
Thorben Moos, UCLouvain, BE
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Erdinc Ozturk, Intel, GB
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Samah Saeed, City College of New York, US
Erkay Savas, Sabanci University, TR
Nicolas Sklavos, Computer Engineering and Informatics Department, University of Patras, GR
Junko Takahashi, NTT Social Informatics Laboratories, JP
Tolga Yalcin, Qualcomm, US



Conference Information

E1 Embedded Software Architecture, Compilers and Tool Chains

Chair: Ahmed Rezine, Linköping University, SE
Co-Chair: Linh Thi Xuan Phan, University of Pennsylvania, US

Nicola Bombieri, University of Verona, IT
Timothy Bourke, Inria / ENS, FR
David Broman, KTH Royal Institute of Technology, SE
Jeronimo Castrillon, TU Dresden, DE
Hsiang-Yun Cheng, Academia Sinica, TW
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Nan Guan, City University of Hong Kong, HK
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Ramkumar Jayaseelan, Meta, US
Christoph Kessler, Linköping University, SE
Michele Lora, University of Verona, IT
Liqiang Lu, Zhejiang University, CN
Francesca Palumbo, University of Cagliari, IT
Hiren Patel, University of Waterloo, CA
Sara Royuela, Barcelona Supercomputing Center, ES
Konstantinos Sagonas, Uppsala University & Nat. Tech. Univ, of Athens, SE
Soheil Samii, Linköping University, SE
Martin Schoeberl, Technical University of Denmark, DK
Yi Wang, Shenzhen University, CN
Kasim Sinan Yildirim, University of Trento, IT

E2 Real-time, Dependable and Privacy-Enhanced Systems

Chair: Jing Li, New Jersey Institute of Technology, US
Co-Chair: Matthias Becker, KTH Royal Institute of Technology, SE

Yasmina ABDEDDAIM, Univ Gustave Eiffel, CNRS, LIGM, FR
Federico Aromolo, Scuola Superiore Sant'Anna, IT
Jatin Arora, VORTEX CoLab and CISTER Research Centre, PT
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Emmanuel Grolleau, LIAS, ISAE-ENSMA, Universite de Poitiers, FR
Tanja Harbaum, KIT, DE
Sena Hounsinou, Metro State University, US
Tingting Hu, University of Luxembourg, LU
Zhe Jiang, South East University, CN
Behnaz Ranjbar, Ruhr University Bochum, DE
Federico Reghenzani, Politecnico di Milano, IT
Yue Tang, Northeastern University, CN
Corey Tessler, University of Nevada, Las Vegas, US
Peter Ulbrich, Technische Universität Dortmund, DE
An Zou, Shanghai Jiao Tong University, CN
Alexander Zuepke, Technical University of Munich, DE

E3 Machine Learning Solutions for Embedded and Cyber-Physical Systems

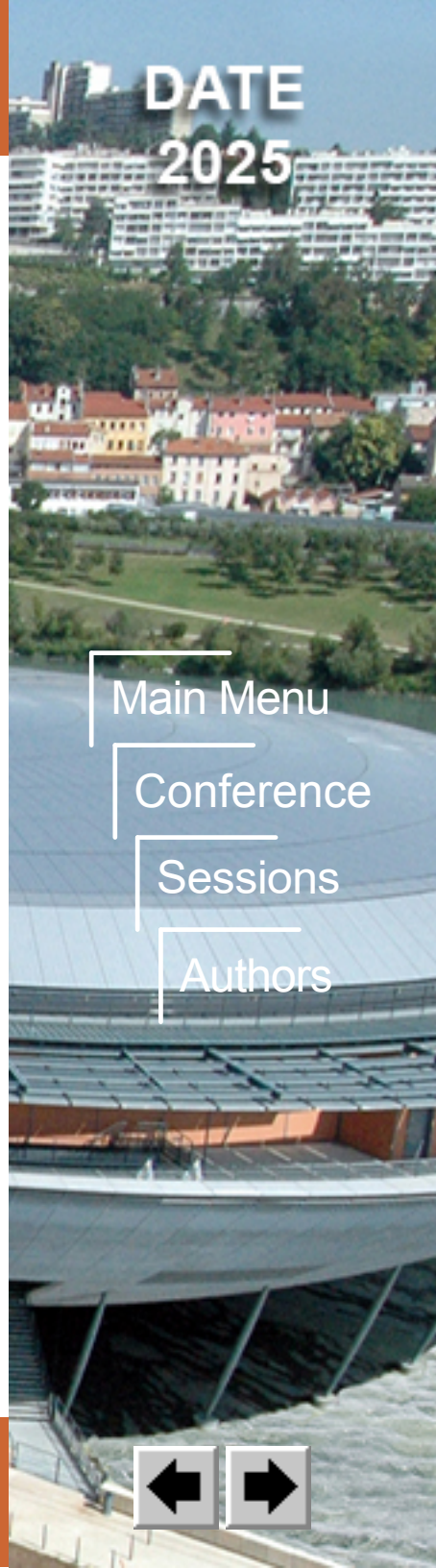
Chair: Francesco Conti, University of Bologna, IT
Co-Chair: Irem Boybat, IBM Research Europe - Zurich, CH

Elnaz Ansari, Meta, US
Mladen Berekovic, Universität zu Lübeck, DE

E4 Design Methodologies for Machine Learning Architectures

Chair: Smail Niar, INSA Hauts-de-France, CNRS, FR
Co-Chair: Priyadarshini Panda, Yale University, US

Hadjer Benmeziane, IBM Research, CH
Ganapati Bhat, Washington State University, US



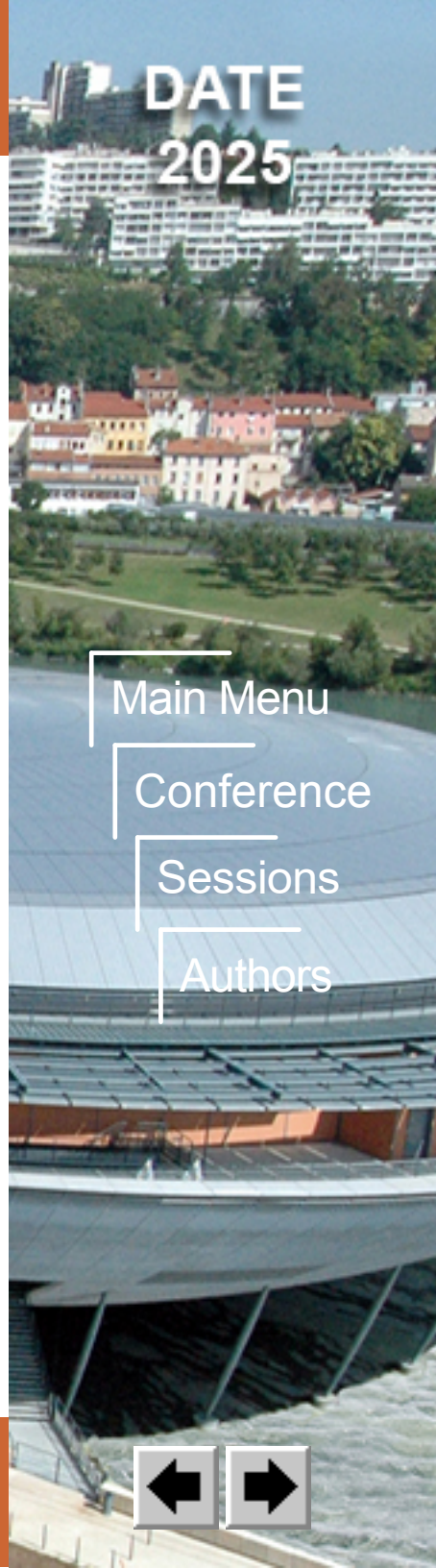
Conference Information

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Carmine Cappetta, STMicroelectronics, IT
Anup Das, Drexel University, US
Kaoutar El Maghraoui, IBM, US
Angelo Garofalo, University of Bologna, ETH Zurich, IT
Maryam Hemmati, University of Auckland, NZ
Daniele Jahier Pagliari, Politecnico di Torino, IT
Axel Jantsch, TU Wien, AT
Eiman Kanjo, Imperial College London, GB
Minkyu Kim, Qualcomm, US
Gokul Krishnan, Apple, US
Hyoukjun Kwon, University of California, Irvine, US
Charles Mackin, IBM Research, US
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Amirreza Yousefzadeh, University of Twente, NL
Marina Zapater, University of Applied Sciences Western Switzerland (HES-SO), CH
Lirong Zheng, Fudan University, CN
Guanwen Zhong, AMD Research and Advanced Development (RAD), SG

E5 Design, Specification, Modelling and Verification for Embedded and Cyber-Physical Systems

Chair: Patricia Derler, PARC, US
Co-Chair: Julio Medina, University of Cantabria, ES

Luis Almeida, University of Porto, PT
Grzegorz Bazydło, University of Zielona Góra, PL
Chadlia Jerad, University of Manouba, TN
Hokeun Kim, Arizona State University, US
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Haoran You, Georgia Institute of Technology, US
Fan Zhang, Google, US



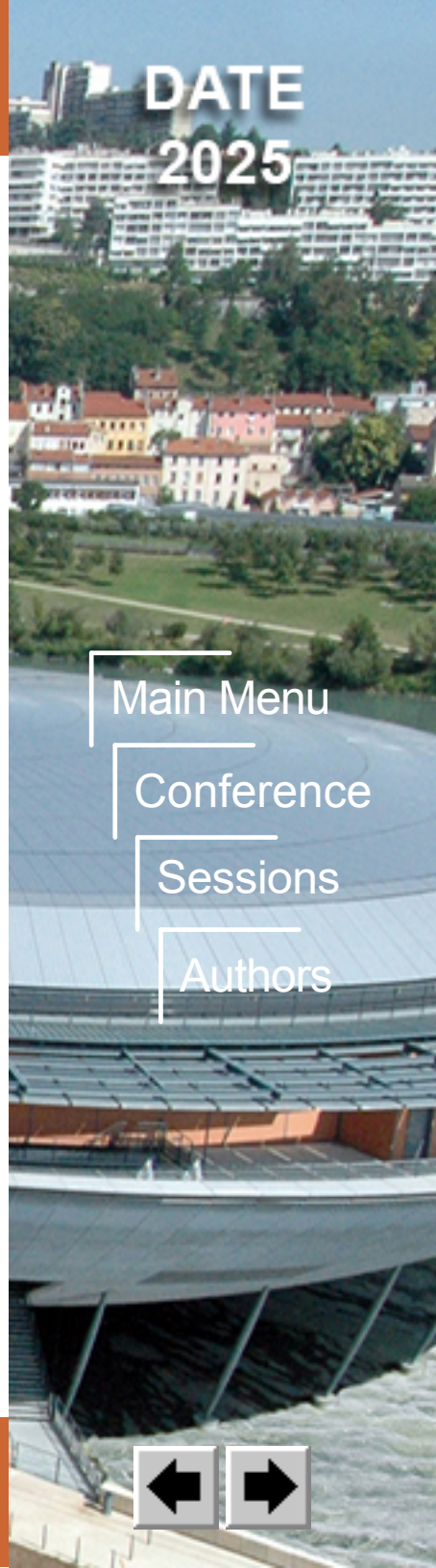
Conference Information

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Vittoriano Muttillo, University of Teramo, IT
Gianluca Palermo, Politecnico di Milano, IT
Georgios L. Stavrinides, KIOS Research and Innovation Center of Excellence, University of Cyprus, CY
Todor Stefanov, Leiden University, NL

Late Breaking Results (LBR)

Co-chair: Annachiara Ruospo, Politecnico di Torino, IT
Co-chair: Pascal Vivet, CEA, France

Leticia Maria Bolzani Poehls, IHP, DE
Mario R. Casu, Politecnico di Torino, Department of Electronics and Telecommunications, IT
Valentina Ciriani, Universita' degli Studi di Milano, IT
William Fornaciari, Politecnico di Milano - DEIB, IT
Dimitris Gizopoulos, University of Athens, GR
Mariagrazia Graziano, Politecnico di Torino, IT
Daniel Grosse, Johannes Kepler University Linz, AT
Mike Hutter, PQShield, AT
Jan Moritz Joseph, RWTH Aachen University, DE
Matthias Jung, Fraunhofer IESE, DE
Maria K. Michael, Electrical and Computer Engineering & KIOS Center of Excellence, University of Cyprus, CY
Leonidas Kosmidis, Barcelona Supercomputing Center (BSC) and Universitat Politecnica de Catalunya (UPC), ES
Chung-Wei Lin, National Taiwan University, TW
Michele Lora, Universita` degli Studi di Verona, IT
Daniel Menard, INSA Rennes, FR
Antonio Miele, Politecnico di Milano, IT
Jean-Philippe Noel, CEA, FR
Bogdan Pasca, Intel, FR
Francesco Regazzoni, University of Amsterdam and ALaRI - USI, CH
Semeen Rehman, TU Wien, AT
Davide Zoni, Politecnico di Milano, IT



Conference Information

DATE 2025 Best Paper Awards

The **DATE 2025** best papers are:

D Track

To be announced

A Track

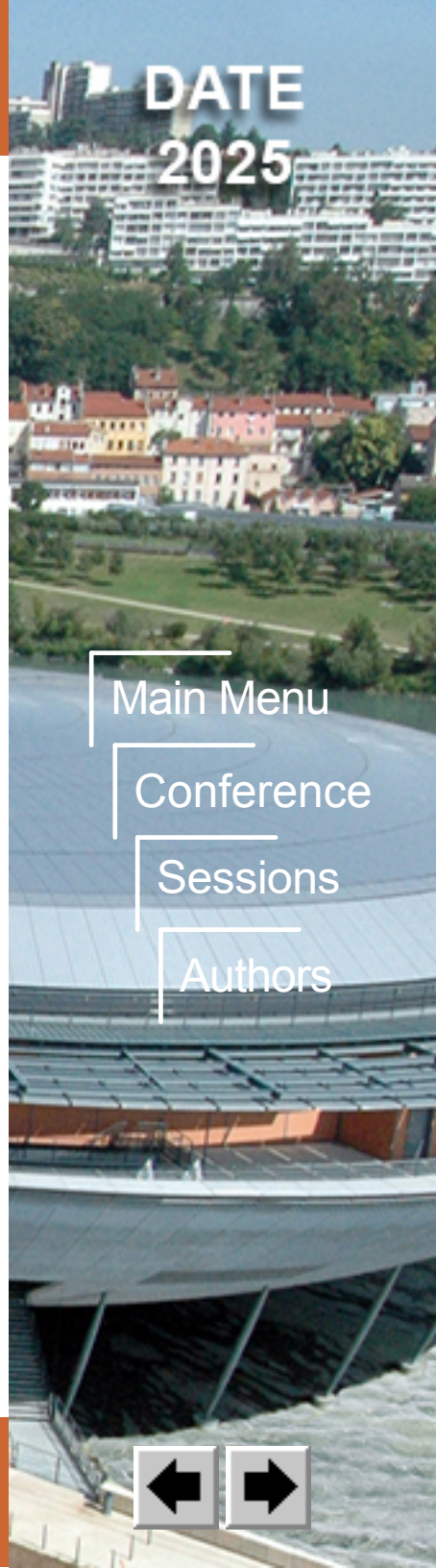
To be announced

T (&DT) Track

To be announced

E Track

To be announced



Conference Information

Best Paper Award Nominations

TYRCA: A RISC-V Tightly-coupled accelerator for Code-based Cryptography Alessandra Dolmeta[1]; Stefano Di Matteo[2,3]; Emanuele Valea[3]; Mikael Carmona[2]; Antoine Loiseau[2]; Maurizio Martina[1]; Guido Masera[1]
[1]DET - Politecnico di Torino; [2] CEA – Leti; [3]CEA-List

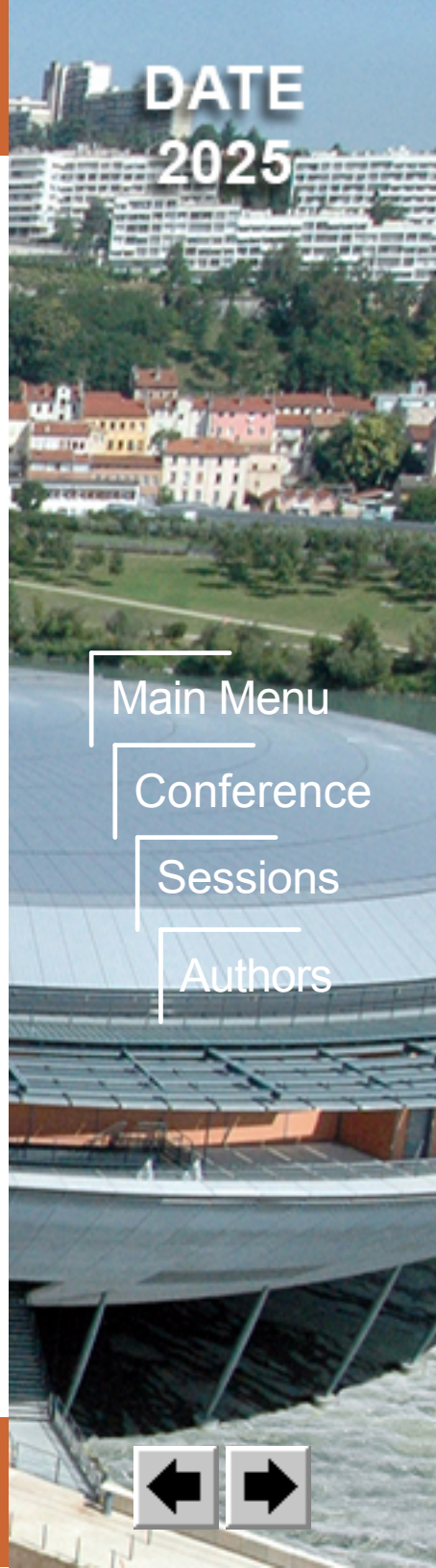
Timing-Driven Global Placement by Efficient Critical Path Extraction
Yunqi Shi[1]; Siyuan Xu[2]; Shixiong Kai[2]; Xi Lin[1]; Ke Xue[1]; Mingxuan Yuan[2]; Chao Qian[1]
[1]Nanjing University; [2] Huawei Noah's Ark Lab

Quantifying Trade-Offs in Power, Performance, Area, and Total Carbon Footprint of Future Three-Dimensional Integrated Computing Systems
Danielle Grey-Stewart; Mariam Elgamal; David Kong; Georgios Kyriazidis; Jalil I. Morris; Gage Hills
Harvard University

qGDP: Quantum Legalization and Detailed Placement for Superconducting Quantum Computers
Junyao Zhang[1]; Guanglei Zhou[1]; Feng Cheng[1]; Jonathan Hao-Cheng Ku[1]; Qi Ding[2]; Jiaqi Gu[3]; Hanrui Wang[4]; Hai (Helen) Li[1]; Yiran Chen[1]
[1]Duke University; [2] Massachusetts Institute of Technology; [3] Arizona State University; [4]UCLA

RVEBS: Event-Based Sampling on RISC-V
Tiago Rocha; Nuno Neves; Nuno Roma; Pedro Tomás; Leonel Sousa
INESC-ID, Instituto Superior Tecnico, Universidade de Lisboa

RankMap: Priority-Aware Multi-DNN Manager for Heterogeneous Embedded Devices
Andreas Karatzas[1]; Dimitrios Stamoulis[2]; Iraklis Anagnostopoulos[1]
[1]Southern Illinois University Carbondale; [2]University of Texas at Austin



Conference Information

A Lightweight CNN for Real-Time Pre-Impact Fall Detection
Cristian Turetta[1]; Muhammed Toqeer Ali[1]; Florenc Demrozi [2]; Graziano Pravadelli[1]
[1]University of Verona; [2]Department of Electrical Engineering and Computer Science, University of Stavanger

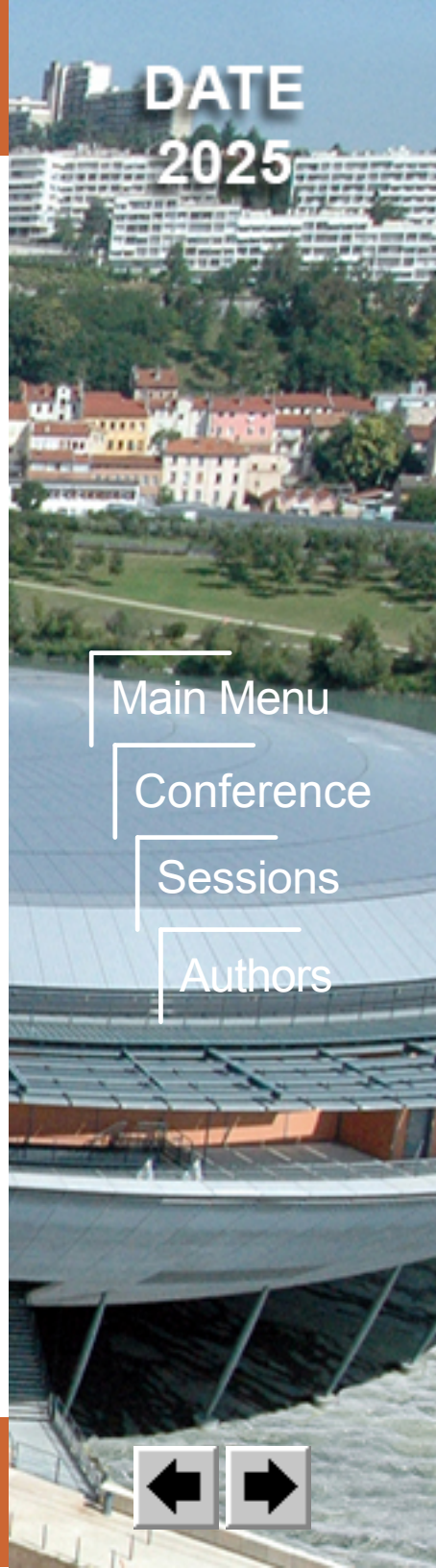
Compute-in-Memory Array Design using Stacked Hybrid IGZO/Si eDRAM cells
Munhyeon Kim[1]; Yulhwa Kim[2]; Jae-Joon Kim[1]
[1]Seoul National University; [2]Sungkyunkwan University

ReBERT: LLM for Gate-Level to Word-Level Reverse Engineering
Lizi Zhang[1]; Azadeh Davoodi[1]; Rasit Topaloglu[2]
[1]University of Wisconsin Madison; [2]Adeia

Xray: Detecting and Exploiting Vulnerabilities in Arm AXI Interconnects
Melisande Zonta; Nora Hinderling; Shweta Shinde
ETH Zürich

A Soft Error Tolerant Dual Storage Mode Flip-Flop for eFPGA Configuration Hardening in 22nm FinFET Process
Prashanth Mohan[1]; Siddharth Das[1]; Oguz Aatli[1]; Josh Joffrion[2]; Ken Mai[1]
[1]Carnegie Mellon University; [2]Sandia National Laboratories

Cocktail: Chunk-Adaptive Mixed-Precision Quantization for Long-Context LLM Inference
Wei Tao[1]; Bin Zhang[1]; Xiaoyang Qu[2]; Jiguang Wan[1]; Jianzong Wang[2]
[1]Huazhong University of Science and Technology; [2]Ping An Technology (shenzhen)Co., Ltd



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Authors

Conference Information

DATE 2025 Special Day on New Trends in AI/ML

This Special Day focuses on exploring the latest trends and innovations in Artificial Intelligence (AI) and Machine Learning (ML) in the context of DATE. As AI (and mainly generative AI) is booming, especially since the release of chat-GPT, we expect AI/ML will change the way to approach Design, Automation, and Test. In this context, field experts will present their thoughts on the challenges and opportunities of AI/ML, and will engage the audience in an open discussion about the trends that the DATE community should pursue.

This Special Day will highlight the following topics:

- Design of hardware architectures and software, including automatic exploration of large design spaces, assistance of the human designer, resource selection and optimization
- Verification of hardware architectures, with topics such as performance prediction, (formal) design validation, accelerating simulations thanks to AI-Augmented Surrogate Models
- AI-Accelerated Physical Design and Validation of layout and floorplans
- New AI accelerators architectures

These topics will be addressed by a lineup of six distinguished speakers, experts in their respective fields. The day will conclude with a panel discussion allowing experts and the audience to engage in an informal exchange of ideas and trigger discussions on the future research directions and/or the interaction between the various domains presented during the day.

This special day is the ideal even for AI/ML researchers, data scientists, hardware designers, software developers, sustainability advocates, and anyone interested in the future directions of AI and ML for Design, Automation and Test.

Tuesday, 1 April 2025

8:30 – 8:45

INTRODUCTION TO THE SPECIAL DAY

Ana Lucia Varbanescu, University of Amsterdam, NL

8:45 – 9:15:

TBD

TBD

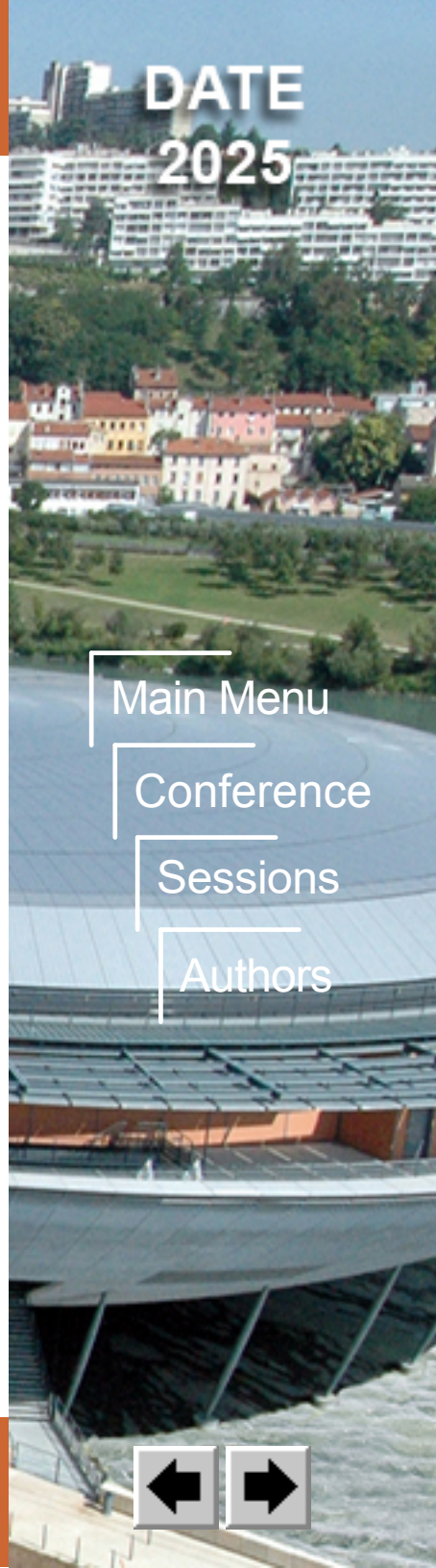
Summary: TBD.

9:15 – 9:45

TBD

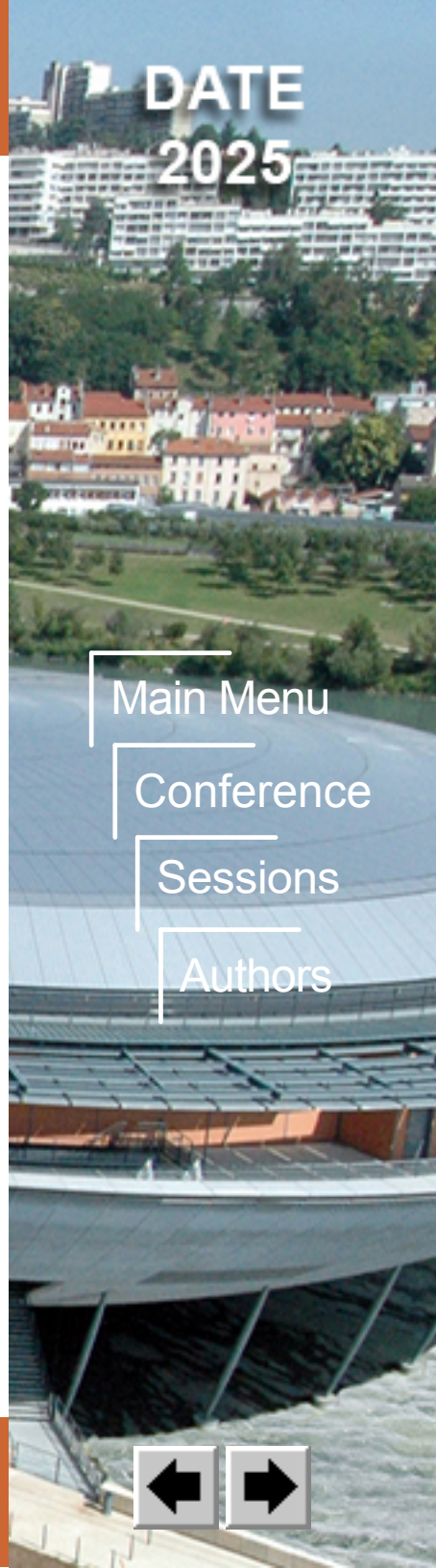
TBD

Summary: TBD.



Conference Information

9:45 – 10:00
TBD
TBD
Summary: TBD.



Conference Information

DATE 2025 Special Day on Emerging Computing Paradigms

Sustaining increasingly challenging compute workloads requires going beyond technology scaling with von Neumann architectures in traditional CMOS. Examples include NP-hard optimisation, massive sensor processing in IoT, as well as deep learning and artificial intelligence where training compute requirements grow by ~750x every two years. Therefore, rethinking computing toward more sustainable and efficient solutions is urgently needed. This can take place by bringing computation closer to its physical substrate, or by seeking new computing paradigms across all layers of the compute stack, thereby spanning architecture, circuit, and device solutions.

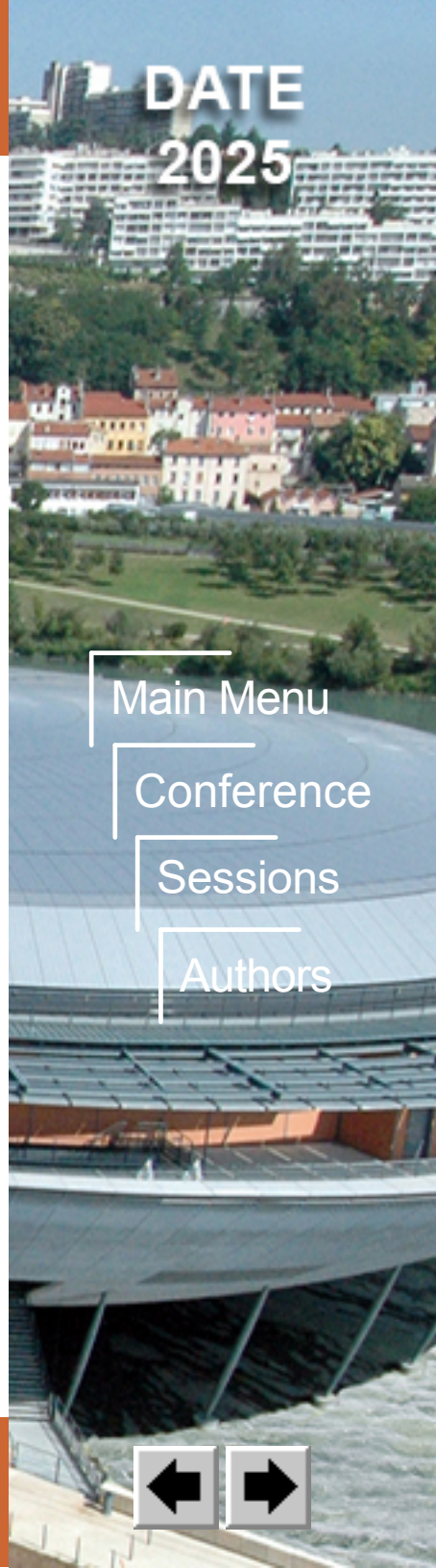
The Special Day on Emerging Computing Paradigms covers key emerging topics in the areas of quantum computing, neuromorphic engineering, physics-based computing, probabilistic computing, reversible and adiabatic computing, and cellular automata. Starting with talks by key experts and closing with a panel discussion, this Special Day aims to outline tradeoffs and synergies in the wide landscape of unconventional computing approaches.

Wednesday, 2 April 2025

8:30
OPENING AND INTRODUCTION TO THE SPECIAL DAY
John Paul Strachan, Forschungszentrum Juelich GmbH, DE

8:30 – 9:00
ERROR PROPAGATION THROUGH SPACE, TIME AND THE BRAIN
Mihai Petrovici, University of Bern, CH
9:00 – 9:30
SPINTRONIC NEURAL NETWORKS
Julie Grollier, CNRS/Thales, FR
9:30 – 10:00
SILICON PHOTONICS FOR AI – THE GOOD, THE BAD AND THE UGLY
Thomas Van Vaerenbergh, Hewlett Packard Labs, BE

11:00 – 11:30
HOW TO BUILD QUANTUM COMPUTERS AND HOW TO USE THEM
Tommasso Calarco, University of Cologne, DE



Conference Information

11:30 – 12:00

CELLULAR COMPUTING/AUTOMATA

Sebastian Risi, IT Copenhagen, DK

12:00 – 12:30

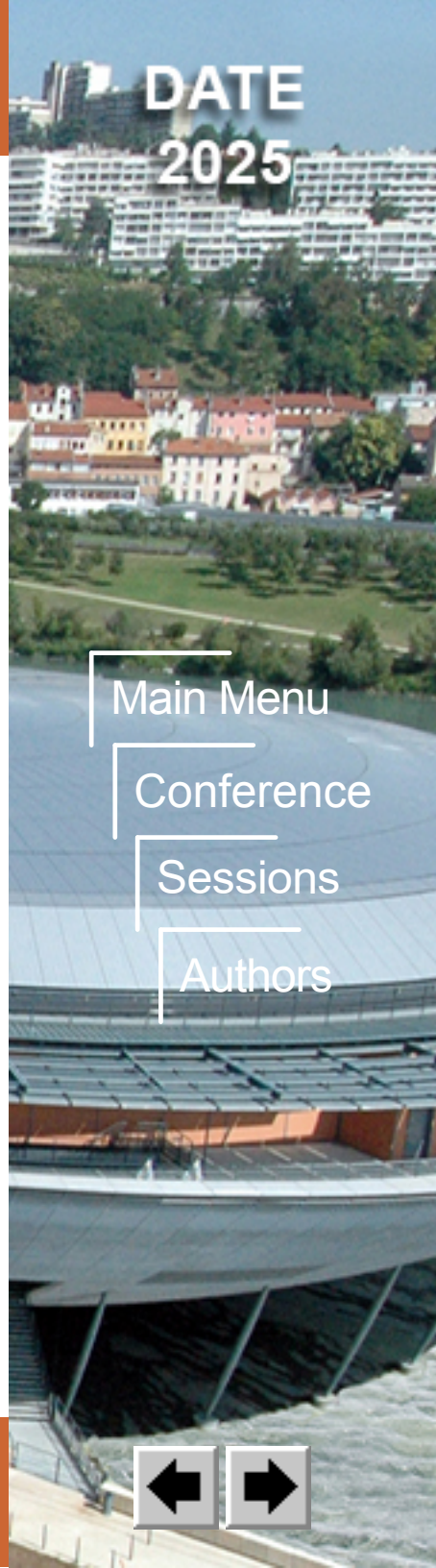
TOWARDS SCALABLE PROBABILISTIC COMPUTERS FOR BINARY OPTIMIZATION AND BEYOND

Corentin Delacour, University of California, Santa Barbara, US

13:15 – 14:00

SPECIAL DAY EMERGING COMPUTING PARADIGM LUNCHTIME KEYNOTE: "NEUROMORPHIC COMPUTING AT CLOUD LEVEL"

Christian Mayr, TU Dresden, DE



DATE 2025 Initiative on Autonomous Systems Design (ASD)

Fueled by the progress of artificial intelligence, autonomous systems become more and more integral parts of many Internet-of-Things (IoT) and Cyber-Physical Systems (CPS) applications, such as automated driving, robotics, avionics, industrial automation and smart systems in general. Autonomous systems are self-governed and self-adaptive systems that are designed to operate in an open and evolving environment which is not completely defined at design time. This poses a unique challenge to the design and verification of dependable autonomous systems. Following the successful editions from previous years, DATE is again hosting the Initiative on Autonomous Systems Design. The initiative will include peer-reviewed papers, invited contributions and interactive sessions.

Date: Monday, 31 March 2025
Time: 11:00 - 12:30 CET

ASD01 Regular Session "Enhancing Dependability and Efficiency in Automotive and Autonomous Systems"

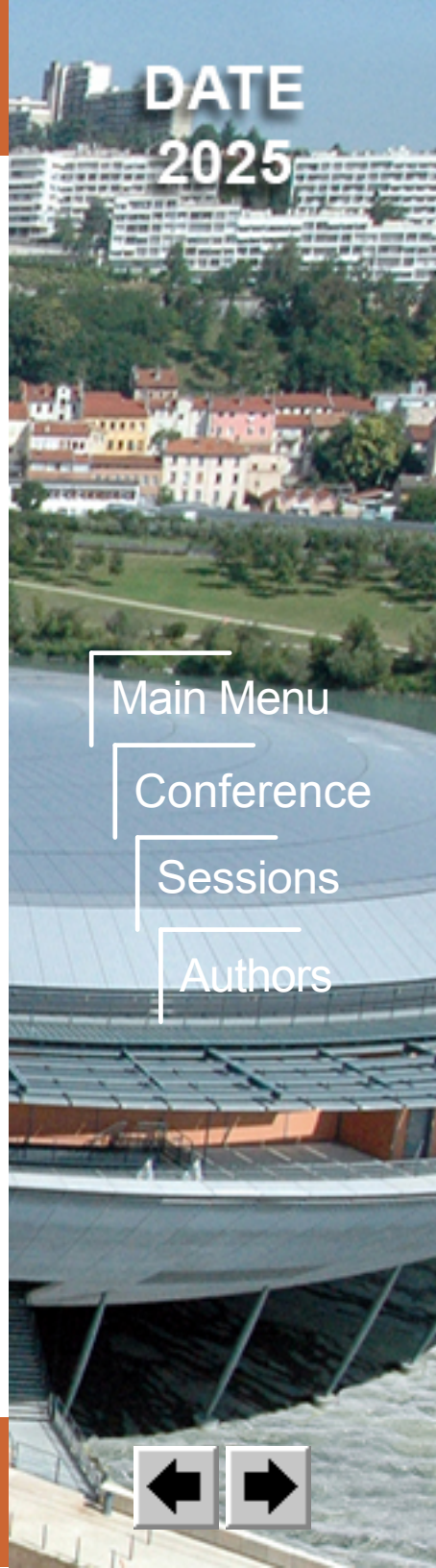
Session chair: Selma Saidi, TU Braunschweig, DE
Session co-chair: Dirk Ziegenbein, Robert Bosch GmbH, DE

This session explores advancements in automotive and autonomous systems, focusing on achieving predictability, reliability, and efficiency. The session begins with a proposal on extending the AUTOSAR Adaptive standard using the System-Level Logical Execution Time (SL-LET) paradigm to ensure determinism, critical for the predictability of modern automotive systems. The second presentation demonstrates noise perturbation attacks on image segmentation, a core perception component of safety-critical autonomous systems, and how they can be predicted and mitigated. Finally, a framework designed to optimize the efficiency of 3D object detection in autonomous vehicles through pattern pruning and quantization is presented, significantly enhancing real-time performance and energy efficiency on resource-limited platforms.

ASD01.1 MODELING THE SL-LET PARADIGM IN AUTOSAR ADAPTIVE

Davide Bellassai[1], Gerlando Sciangula[2], Claudio Scordino[3], Daniel Casini[4] and Alessandro Biondi[4]
[1]Evidence S.r.l., Scuola Superiore Sant'Anna, IT; [2]Huawei and Scuola Superiore Sant'Anna, IT; [3]Huawei Inc, IT; [4]Scuola Superiore Sant'Anna, IT

Abstract: The AUTOSAR consortium has proposed the AUTOSAR Adaptive standard to tackle the challenges introduced by the design of modern automotive functionality. It consists of a service-oriented architecture (SoA) implemented in C++ and built on top of POSIX operating systems. However, unlike the previous AUTOSAR Classic specifications, this novel standard does not address non-functional requirements, including determinism, which is



of key importance to guarantee the system's functional safety. This paper proposes extensions to the AUTOSAR Adaptive standard to achieve determinism by leveraging the System-Level Logical Execution Time (SL-LET) paradigm, which is already used in the context of AUTOSAR Classic but needs to be revisited to be employed in Adaptive. We evaluate the feasibility of the proposed model extension on the AUTOSAR Adaptive Platform Demonstrator (APD), which provides an implementation of AUTOSAR Adaptive specifications using a realistic automotive application.

ASD01.2 GENERATING AND PREDICTING OUTPUT PERTURBATIONS IN IMAGE SEGMENTERS

Matthew Bozoukov[1], Nguyen Anh Vu Doan[2] and Bryan Donyanavard[3]
[1]Miramar college, US; [2]Infineon Technologies AG & TU Munich, DE; [3]San Diego State University, US

Abstract: Image segmentation applications are a core component of safety-critical autonomous software pipelines. Sensor data input noise can lead to segmentation output corruption that threatens safety in both DNN- and transformer-based segmenters. Previous work has proposed methods for generating malicious noise to cause DNN- and transformer-based object detection and classification output corruption. We perform the same task for image segmentation applications using genetic algorithms for optimization. We then propose a novel method to predict whether an input image will yield a corrupted segmentation output due to noise. We evaluate the optimal noise generation and corruption prediction on state-of-the-art image segmenters YOLOv8 and DETR. We observe that we can (a) cause segmentation output corruption with noise that is undetectable to the human eye and unrelated to the corrupted region of the image; and (b) predict output corruption due to image noise with over 96% accuracy.

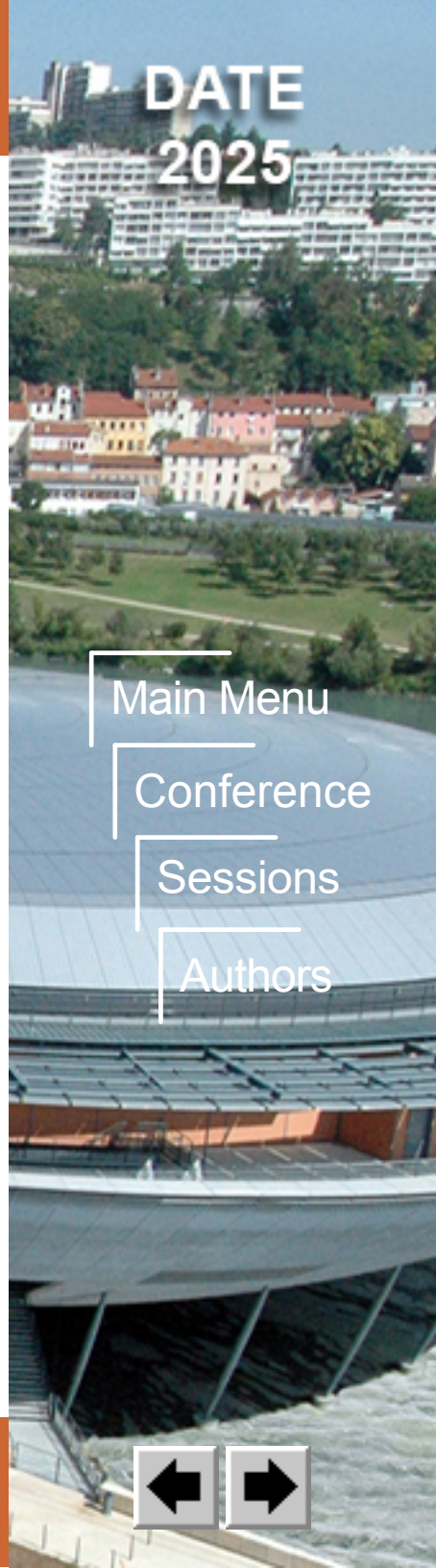
ASD01.3 UPAQ: A FRAMEWORK FOR REAL-TIME AND ENERGY-EFFICIENT 3D OBJECT DETECTION IN AUTONOMOUS VEHICLES

Abhishek Balasubramaniam[1], Febin Sunny[2] and Sudeep Pasricha[3]
[1]Colorado State University, N/; [2]AMD, N/; [3]Colorado State University, US

Abstract: To enhance perception in autonomous vehicles (AVs), recent efforts are concentrating on 3D object detectors, which deliver more comprehensive predictions than traditional 2D object detectors, at the cost of increased memory footprint and computational resource usage. We present a novel framework called UPAQ, which leverages semi-structured pattern pruning and quantization to improve the efficiency of LiDAR point-cloud and camera-based 3D object detectors on resource-constrained embedded AV platforms. Experimental results on the Jetson Orin Nano embedded platform indicate that UPAQ achieves up to 5.62× and 5.13× model compression rates, up to 1.97× and 1.86× boost in inference speed, and up to 2.07× and 1.87× reduction in energy consumption compared to state-of-the-art model compression frameworks, on the Pointpillar and SMOKE models respectively.

Date: Monday, 31 March 2025
Time: 14:00 - 15:30 CET

ASD02 Focus session: Cybersecurity Challenges of Autonomous Systems



Conference Information

Organizer: Sebastian Steinhorst, TU Munich, DE

With the recent dramatic increase in performance of artificial intelligence and related computing systems, together with advanced sensing, connectivity, and technological platforms, autonomous systems are poised to enter many application domains such as transportation and manufacturing. However, as autonomy increases, the risks of cybersecurity threats are equally rising, requiring the development of sophisticated methods on all layers of autonomous systems architectures. In this session, five experts from different areas of cybersecurity research in industry and academia will present challenges ranging from the physical layer to the system of systems layer of autonomous systems. Using the example of autonomous vehicles to highlight current developments, this session will discuss the efforts necessary to achieve secure and safe autonomous systems. The session will comprise individual 10-minute presentations of the five speakers, followed by a panel discussion that will involve the audience and further deepen the exchange.

ASD02.1 PHYSICAL LAYER INTEGRITY CHECKS
Mridula Singh, CISPA Helmholtz Center for Information Security, DE

ASD02.2 ETHERNETIFICATION OF CAN
Alexander Zeh, Infineon Technologies, DE

ASD02.3 SELF-SOVEREIGN IDENTITIES FOR SOFTWARE-DEFINED VEHICLES
Christian Prehofer, fortiss GmbH, DE

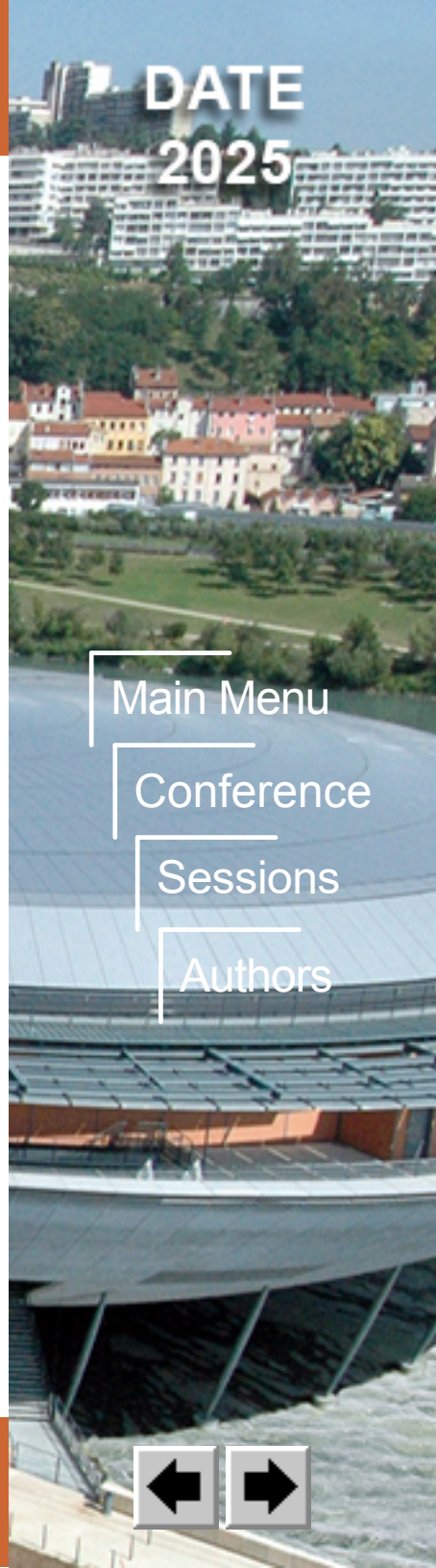
ASD02.4 CAN WE ACHIEVE ACCEPTABLE SECURITY FOR AUTONOMOUS SYSTEMS?
Mikael Asplund, Linköping University, SE

ASD02.5 MANAGING CYBERSECURITY IN THE AUTONOMOUS VEHICLE MOBILITY-AS-A-SERVICE SYSTEM-OF-SYSTEMS
Tobias Löhr, P3 automotive GmbH, DE

ASD02.6 PANEL DISCUSSION

Date: Monday, 31 March 2025
Time: 16:30 - 18:00 CET

ASD03 Focus session: Dynamic, Multi-Agent Sensing-to-Action Loops in Distributed Autonomous Edge Computing Systems: Opportunities and Challenges



Conference Information

Organizers:
Amit Ranjan Trivedi, University of Illinois at Chicago, US
Saibal Mukhopadhyay, Georgia Tech, US

Autonomous edge computing in robotics, smart cities, and autonomous vehicles depends on seamlessly integrating sensing, processing, and actuation for real-time decision-making in dynamic environments. At its core is the sensing-to-action loop, which continuously aligns sensor inputs with computational models to drive adaptive control. These loops enhance responsiveness by adapting to hyper-local conditions but face challenges like resource constraints, synchronization delays in multi-modal data fusion, and the risk of cascading errors. This focus session examines how proactive, context-aware sensing-to-action and action-to-sensing adaptations can improve efficiency by dynamically adjusting sensing and computation based on task demands, such as selectively sensing a small part of the environment and predicting the rest. Action-to-sensing pathways improve task relevance and resource use by guiding sensing through control actions but require robust monitoring to prevent cascading errors. Multi-agent sensing-action loops extend these benefits through coordinated sensing and actions, optimizing resources via collaboration. Additionally, neuromorphic computing, inspired by biological systems, enables spike-based, event-driven processing that conserves energy, reduces latency, and supports hierarchical control—making it well-suited for multi-agent optimization. Finally, the session highlights the importance of co-designing algorithms, hardware, and environmental dynamics to improve throughput, precision, and adaptability, ultimately advancing energy-efficient edge autonomy in complex environments.

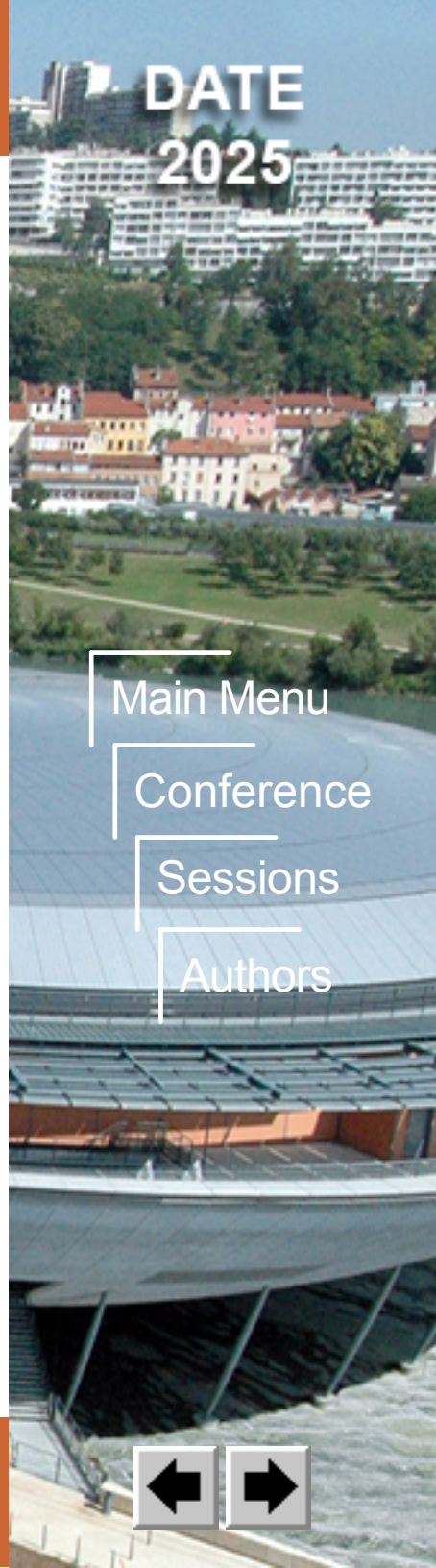
ASD03.1 SPECULATIVE EDGE-CLOUD DECODING FOR FAST AND RELIABLE DECISION-MAKING IN AUTONOMOUS SYSTEMS
Priyadarshini Panda, Yale University, US

ASD03.2 FILLING IN THE SENSING BLANKS WITH GENERATIVE AI: ULTRA-FRUGAL LIDAR PERCEPTION USING MASKED AUTOENCODERS FOR AUTONOMOUS NAVIGATION
Amit Trivedi, University of Illinois at Chicago, US

ASD03.3 ROBOKOOP: EFFICIENT VISUAL CONTROL REPRESENTATIONS FOR ROBOTICS VIA THE KOOPMAN OPERATOR
Saibal Mukhopadhyay, Georgia Tech, US

ASD03.4 NEUROMORPHIC NAVIGATION IN THE REAL WORLD: INTEGRATING REAL-TIME EVENT-BASED VISION WITH PHYSICS-GUIDED PLANNING
Kaushik Roy, Purdue University, US

ASD03.5 PANEL DISCUSSION



Conference Information

Date: Tuesday, 1 April 2025
Time: 8:30 - 10:00 CET

ASD01 Regular Session "Enhancing Dependability and Efficiency in Automotive and Autonomous Systems"

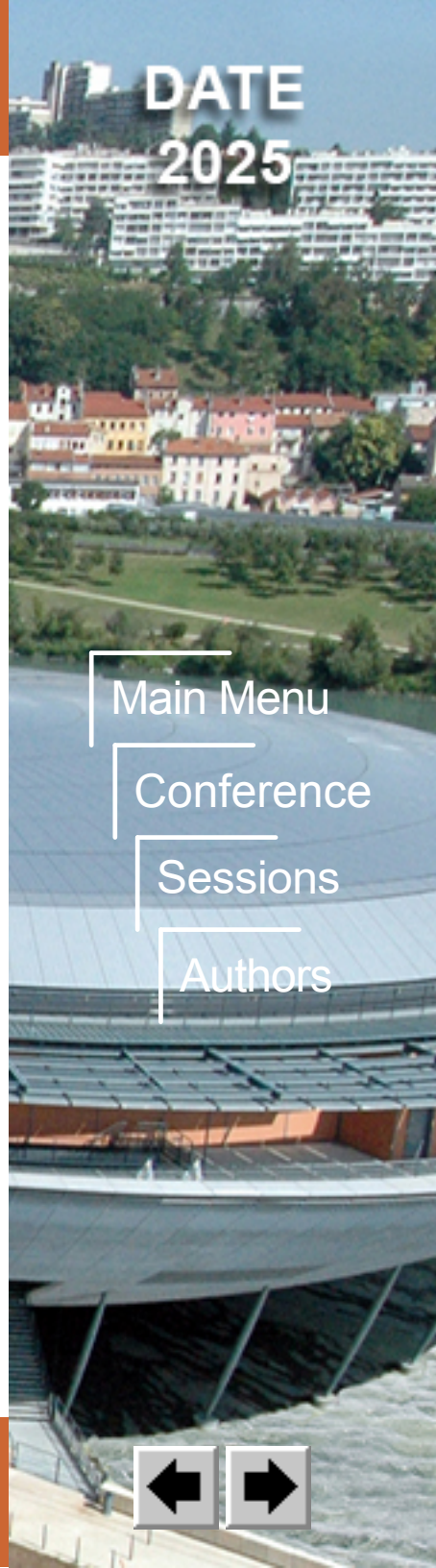
Session chair Dirk Ziegenbein, Robert Bosch GmbH, DE
Session co-chair: Rolf Ernst, TU Braunschweig, DE

This session discusses key design aspects for safety, adaptability, and legality of autonomous systems. First, a framework that utilizes cross-channel safety performance indicators (SPIs) to identify and tackle hazardous driving scenarios for automated vehicles and corresponding evidence from a proof-of-concept implementation is presented. The session continues with the introduction of the Reflex pattern, an innovative approach inspired by biological reflexes that enhances system resilience by dynamically responding to fluctuating resources, demonstrated through a drone image processing scenario. Lastly, the role of legal considerations in the design of automated vehicles is explored, especially those intended to transport intoxicated individuals, underscoring the need for a multidisciplinary collaboration among management, marketing, engineering, and legal teams to ensure the development of functionally robust and legally sound systems.

ASD04.1 IDENTIFICATION OF HAZARDOUS DRIVING SCENARIOS USING CROSS-CHANNEL SAFETY PERFORMANCE INDICATORS

Caspar Hanselaar[1], Murali Manohar Selva Kumar[2], Yuting Fu[2], Andrei Terechko[2], Ranga Rao Venkatesha Prasad[3] and Emilia Silvas[1]
[1]Eindhoven University of Technology, NL; [2]NXP, N/; [3]TU Delft, NL

Abstract: Automated Driving (AD) vehicles are slowly being deployed on public roads. These AD vehicles will encounter hazardous (dangerous) scenarios due to unforeseen test cases at design time and changing environments on the road after deployment. To allow developers of AD systems to mitigate such unforeseen risks, the safety of AD vehicles needs to be continuously monitored after deployment. To this end, the UL4600 standard and AVSC guidelines recommend the use of safety performance indicators (SPIs) by AD vehicle developers. Our paper presents a framework which uses SPIs to identify potentially hazardous scenarios specific to the evaluated AD system, covering both AD vehicles and cloud operations. The framework uses the perception systems and motion plans of heterogeneous redundant multi-channel architectures to detect hazards invisible in single-channel-based systems. We propose three cross-channel SPIs and use them to identify hazardous scenarios in the AD vehicle and validate this approach with a proof-of-concept implementation. In a test of 6 challenging routes in the CARLA simulator our framework automatically identifies 86% of hazardous situations. Next it identifies contributing issues in the AD vehicle, such as missed object detections or dangerous planned trajectories. With this proof of concept, we show that this framework provides evidence on the safety of deployed systems, identifies AD vehicle functions in need of improvement and provides lessons for the development of future AD systems.



ASD04.2 DESIGNING RESILIENT AUTONOMOUS SYSTEMS WITH THE REFLEX PATTERN

Julian Demicoli and Sebastian Steinhorst, TU Munich, DE

Abstract: Autonomous systems face significant challenges due to fluctuating resources and unstable environments, where traditional redundancy strategies for resilience can be inefficient. We present the Reflex pattern, inspired by biological reflexes, promoting system resilience by dynamically adapting to changing resource conditions. By switching between complex and resource-efficient algorithms based on availability, the pattern optimizes efficient resource utilization without extensive redundancy, ensuring essential functionalities remain operational under constraints. To facilitate adoption, we introduce ReflexLang, a domain-specific language (DSL) enabling automated code generation for reflex-pattern-based systems. We validate the pattern's effectiveness in a drone image processing scenario, demonstrating its potential to enhance operational integrity and resilience.

ASD04.3 LAW AS A DESIGN CONSIDERATION FOR AUTOMATED VEHICLES SUITABLE TO TRANSPORT INTOXICATED PERSONS

Marilyn Wolf[1] and William Widen[2]
[1]University of Nebraska, US; [2]University of Miami, US

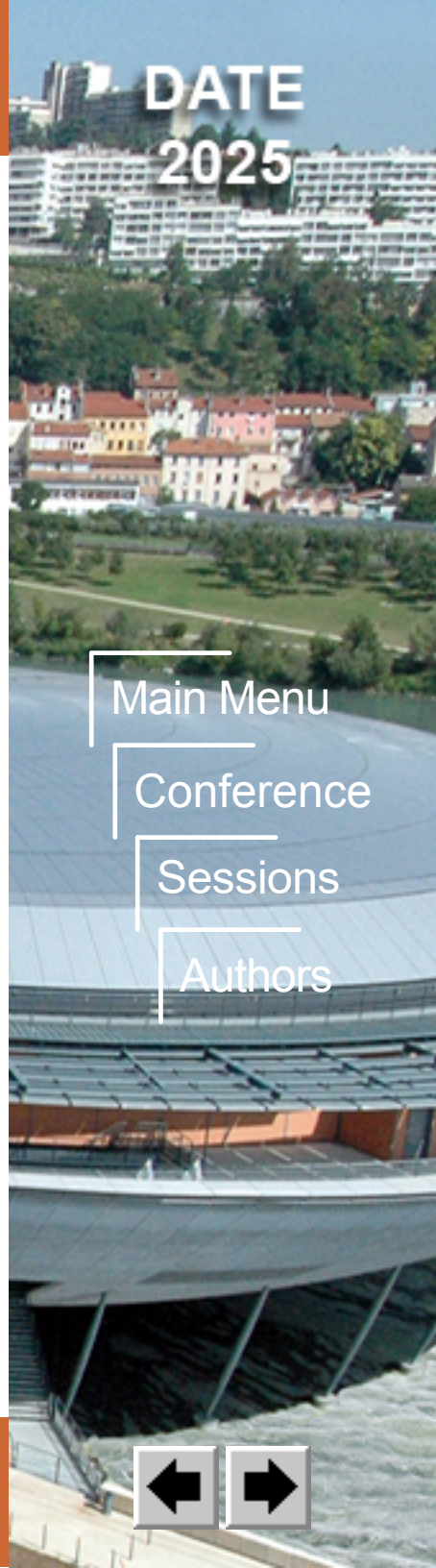
Abstract: *This essay explains why an automated vehicle (AV) manufacturer should consider law during the design process for an AV intended as "fit-for-purpose" to transport intoxicated persons. It suggests that management, marketing, engineering, and legal functions collaborate to develop product requirements and specifications that shield owner/occupants from criminal liability for DUI manslaughter and negligent homicide, as well as guard against civil liability.*

Date: Tuesday, 1 April 2025
Time: 11:00 - 12:30 CET

ASD03 Focus session: Dynamic, Multi-Agent Sensing-to-Action Loops in Distributed Autonomous Edge Computing Systems: Opportunities and Challenges

Organizers:
Frank Diermeyer, TU Munich, DE
Rolf Ernst, TU Braunschweig, DE

In the foreseeable future, highly automated mobile systems, such as vehicles, robots, UAVs, or trains, will be confronted with difficult situations that require external support. The availability of such external support corresponds to level 4 driving automation and is an essential feature in current robotaxis and automated public transportation. While the first generation of level 4 prototypes relied on safety driver support, commercial systems are gradually moving towards support by teleoperation. Designing teleoperation support for level 4 systems is an end-to-end problem involving two main research and practical challenges, the teleoperation function defining the remote human interface with its scene representation and



available control functions, and the real-time communication channel involving wired and wireless segments, which must provide reliable end-to-end data transport.

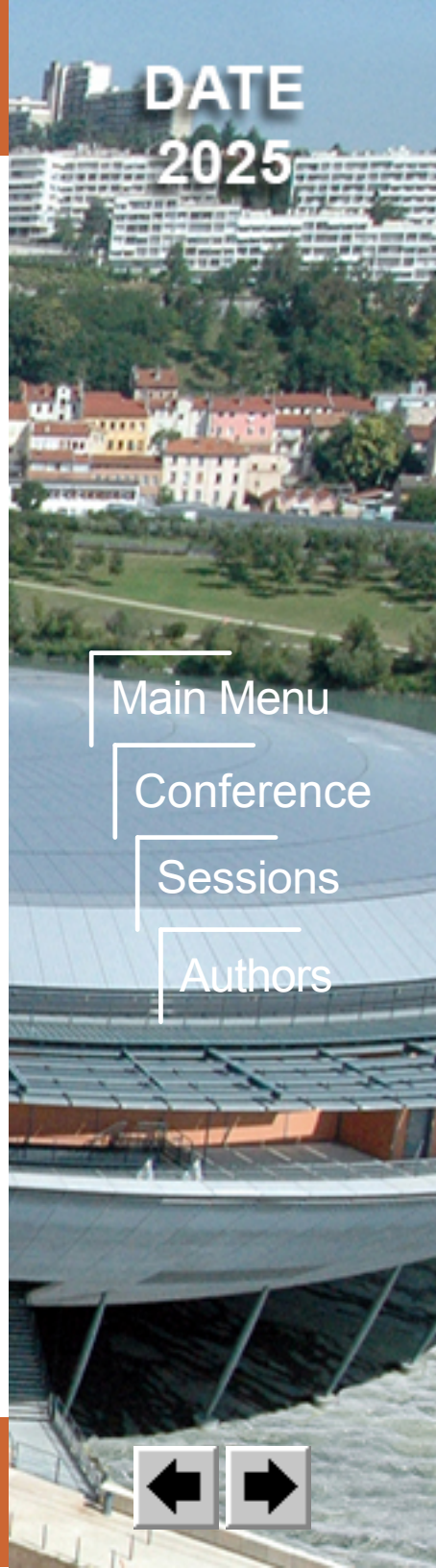
ASD05.1 AUTOMATED VEHICLE TELEOPERATION – VISION AND CHALLENGES

Frank Diermeyer, TU Munich, DE

ASD05.3 RELIABLE REAL-TIME COMMUNICATION FOR TELEOPERATION

Selma Saidi, Technische Universität Braunschweig, DE

ASD05.4 PANEL DISCUSSION



DATE 2025 Focus Sessions

Date: Monday, 31 March 2025
Time: 11:00 - 12:30 CET

FS01 Focus Session: Specifications Mining a World of Generative AI: Extensions, Applications and Pitfalls

Session chair: Graziano Pravadelli, Università di Verona, IT
Session chair: Badri Gopalan, Synopsys, US
Organisers: Graziano Pravadelli, Università di Verona, IT and Samuele Germiniani, Marconi University of Rome, IT

The session consists of three technical contributions (15 mins each) and one panel (45 mins), totaling 90 minutes, focused on R&D challenges, emerging trends, and solutions for the automatic generation of formal specifications in system-level assertion-based verification (ABV). The first part of the session will explore the role of LLMs in assertion generation, delve into the automatic mining of assertions for security verification, and present a framework for the fair qualification and evaluation of current and future assertion miners. Then, in the second part, the panel will highlight unmet needs in specification mining, motivating researchers to develop new approaches and tools that move beyond academic proofs of concept and position automatic assertion generation as a practical, industry-ready solution for ABV.

FS01.1 Are LLMs ready for practical adoption for assertion generation?

Vaishnavi Pulavarthi[1], Deeksha Nandal[2] and Debjit Pal[2]
[1]UIC, US; [2]University of Illinois at Chicago, US

Abstract*:* Assertions have been the de facto collateral for simulation-based and formal verification of hardware designs for over a decade. The quality of hardware verification, i.e., detection and diagnosis of corner-case design bugs, is critically dependent on the quality of the assertions. With the onset of generative AI such as Transformers and Large-Language Models (LLMs), there has been a renewed interest in developing novel, effective, and scalable techniques of generating functional and security assertions from design source code. While there have been recent works that use commercial-of-the-shelf (COTS) LLMs for assertion generation, there is no comprehensive study in quantifying the effectiveness of LLMs in generating syntactically and semantically correct assertions. In this paper, we first discuss AssertionBench from our prior work, a comprehensive set of designs and assertions to quantify the goodness of a broad spectrum of COTS LLMs for the task of assertion generations from hardware design source code. Our key insight was that COTS LLMs are not yet ready for prime-time adoption for assertion generation as they generate a considerable fraction of syntactically and semantically incorrect assertions. Motivated by the insight, we propose AssertionLLM, a first of its kind LLM model, specifically fine-tuned for assertion generation. Our initial experimental results show that AssertionLLM considerably improves the semantic and syntactic correctness of the generated assertions over COTS LLMs.

FS01.2 Security assertions for trusted execution environments

Hasini Witharana, Hansika Weerasena and Prabhat Mishra, University of Florida, US

Abstract: Trusted Execution Environment (TEE) provides a secure and isolated execution environment for sensitive applications. In order to design secure and trustworthy TEE-based systems, it is crucial to verify the trustworthiness of TEE implementations. Property checking is a promising avenue to guarantee that the TEE implementation satisfies the security properties. In the presence of a vulnerability, property checking will fail and provide a counterexample that can be utilized to fix the vulnerability. A major challenge in TEE property checking is that it relies on manual definition of the security properties, which can be cumbersome and error-prone. In this paper, we propose an efficient framework for automated generation and verification of TEE specific properties. Specifically, we leverage Finite State Machine (FSM) analysis to automatically derive and validate security properties utilizing templates. The effectiveness of the proposed method is demonstrated through experimental evaluation of Intel Trust Domain Extension (TDX), highlighting its potential for verifying security and trustworthiness of modern trusted execution environments.

FS01.3 A baseline framework for the qualification of specifications miners

Samuele Germiniani[1,2], Daniele Nicoletti[1] and Graziano Pravadelli[1]
[1]Università di Verona, IT; [2]University of Guglielmo Marconi, IT

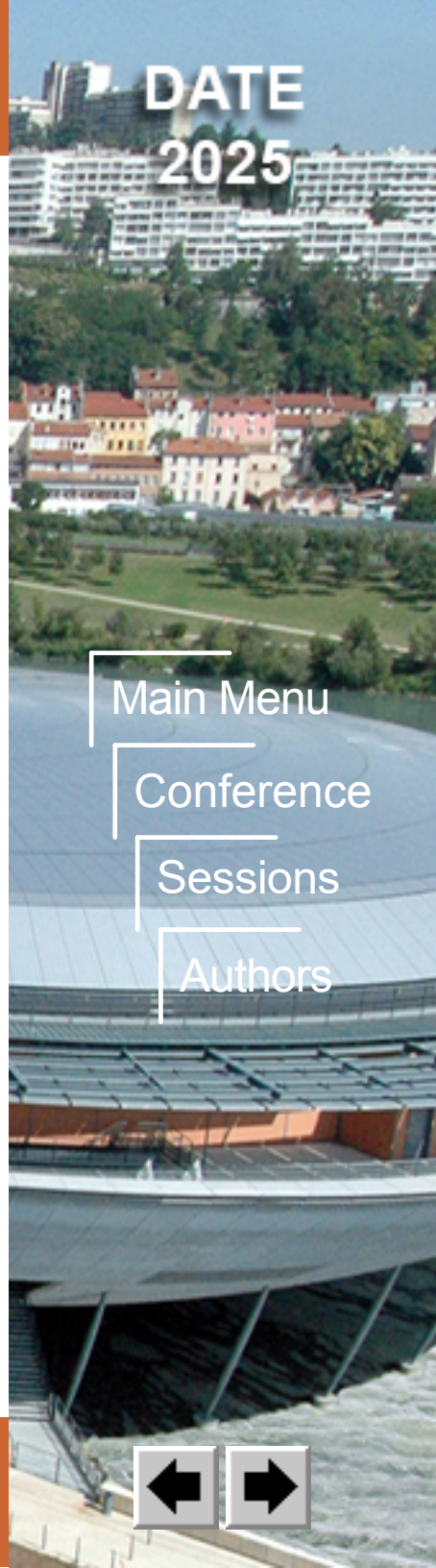
Abstract: Over the past few decades, the verification community has developed several specification miners as an alternative to manual assertion definition. However, assessing their effectiveness remains a challenging task. Most studies evaluate these miners using predefined ranking metrics, which often fail to ensure the quality of the inferred specifications, especially when no fixed ground truth exists and the relevance of the specifications varies depending on the use case. This paper presents a comprehensive framework aimed at facilitating the evaluation and comparison of LTL specification miners. Unlike traditional approaches, which struggle with subjective analyses and complex tool configurations, our framework provides a structured method for assessing and comparing the quality of specifications generated by multiple sources, using both semantic and syntactic techniques. To achieve this, the framework offers users an easy-to-extend environment for installing, configuring, and running third-party miners via Docker containers. Additionally, it supports the inclusion of new evaluation methods through a modular design. Miner comparison can be based either on user-defined designs or on synthetic benchmarks, which are automatically generated to serve as a non-subjective ground truth for the evaluation of the miners. We demonstrate the utility of our framework through comparative analyses with four well-known LTL miners, illustrating its ability to standardize and enhance the specification mining evaluation process.

FS01.4 Specification mining facing generative AI

Goerschwin Fey[1], Harry Foster[2], Jaan Raik[3], Badri Gopalan[4], Joerg Mueller[5] and Manish Pandey[4]
[1]TU Hamburg, DE; [2]Siemens/Mentor Graphics, US; [3]Department of Computer System, Tallinn University of Technology, Estonia, EE; [4]Synopsys, US; [5]Formal Verification Expert, DE

Abstract: Specifications for complex designs and their consistency are always a headache. Automated specification mining – including but not limited to generative AI – offers attractive solutions, but there are also various unmet needs. This panel will highlight unmet needs in specification mining, motivating researchers to develop new approaches and tools that move beyond academic proofs of concept and position automatic assertion generation as a practical, industry-ready solution for ABV.

Date: Monday, 31 March 2025
Time: 14:00 - 15:30 CET



FS08 Focus Session: Panel on The European Chips Act: Ready to Take-Off

Session chair: Anton Klotz, Fraunhofer, DE, Pascal Vivet, CEA, FR
Organisers: Anton Klotz, Fraunhofer, DE, Pascal Vivet, CEA, FR
Panellists: *Jari Kinaret, CHIPS JU, BE, Olivier Thomas, CEA, FR, Inge Asselberghs, IMEC, BE, Amelie Hagelauer, Fraunhofer, DE, Helio Fernandez Tellez, IMEC, BE*

EU Chips Act is the biggest EU initiative to support European microelectronics industry. After it entered into force on 21. September 2023, first calls have been issued in 2024. It is time to take a look at the progress which has been made in the past two years and take an outlook what lies ahead in 2025 and following years. Our panelists are representing various activities of the EU Chips Act, we have the head of Chips JU, the representatives of the pilot lines and Virtual Design Platform initiative. After impulse presentations, there will be a panel discussion, where the panelists will answer the questions from the audience on the EU Chips Act.

Date: Monday, 31 March 2025
Time: 16:30 - 18:00 CET

FS03 Focus Session: Design Automation for Physical Computing Systems

Session chair: Antonino Tumeo, PNNL, US
Organisers: Anup Das, Drexel University, US

FS03.1 Analog system synthesis for FPAAS and custom analog IC design

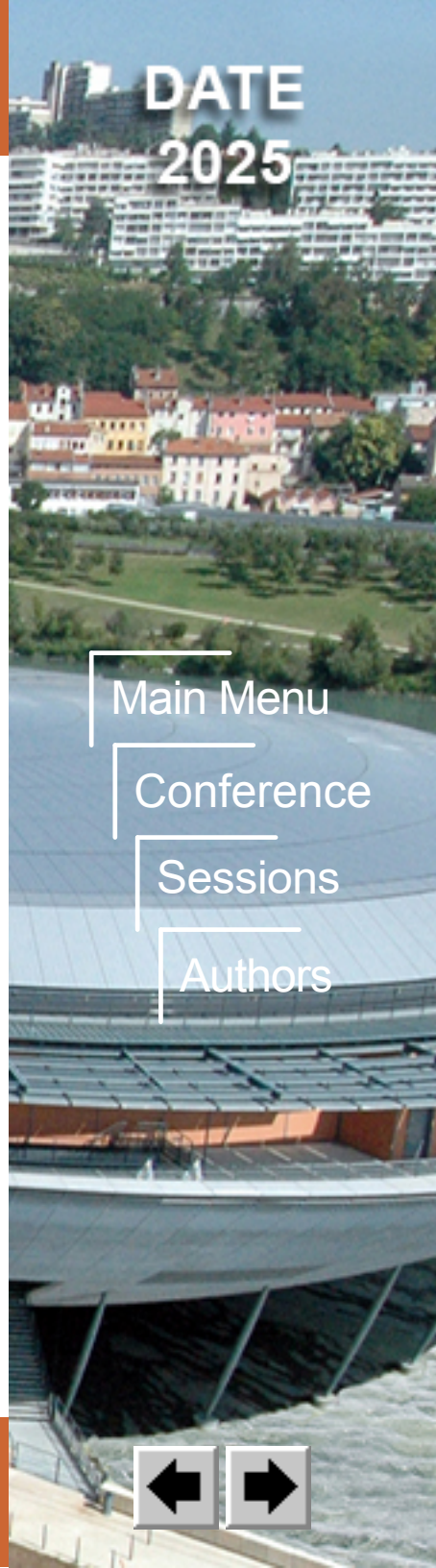
Afolabi Ige and Jennifer Hasler, Georgia Tech, US

Abstract*:* Synthesis tools can unlock the potential of analog architectures to achieve real-time computation, signal processing, inference and learning for low SWaP systems in commercial timescales. We present a methodology and results towards system analog and mixed-signal synthesis both for FPAAs and Custom Analog IC design. Building on previously efforts on large-scale Field Programmable Analog Arrays (FPAA) targeting tools enables tools capable of synthesizing new ICs. The IC synthesis is built upon our recent work on analog & mixed-signal programmable CMOS standard cell library that can be demonstrates across a range of CMOS process nodes (e.g. 180nm, 130nm, 65nm, 28nm, and 16nm CMOS). This synthesis can be extended to synthesizing new configurabile fabrics for a new IC and generate the resulting configuration files to target that fabric. The entire tool-flow is being developed as an open-source tool that can be widely available. These approaches enable moving analog and mixed-signal design towards structured Design Space Exploration}(DSE), and create a significant need towards rapid analog simulation.

FS03.2 Gain-based computing with coupled light and matter

Natalia Berloff, University of Cambridge, GB

Abstract*:* Gain-based computing based on light-matter interactions is a novel approach to physics-based hardware and physics-inspired algorithms. In gain-based computing, the complex optimisation problems are encoded in the gain and loss rates of driven-dissipative systems. The system is driven through a symmetry-breaking transition on the changing loss landscape until a mode that minimises losses is selected, manifesting the optimal solution to the original problem. This process allows for solving important combinatorial optimisation problems via mapping to



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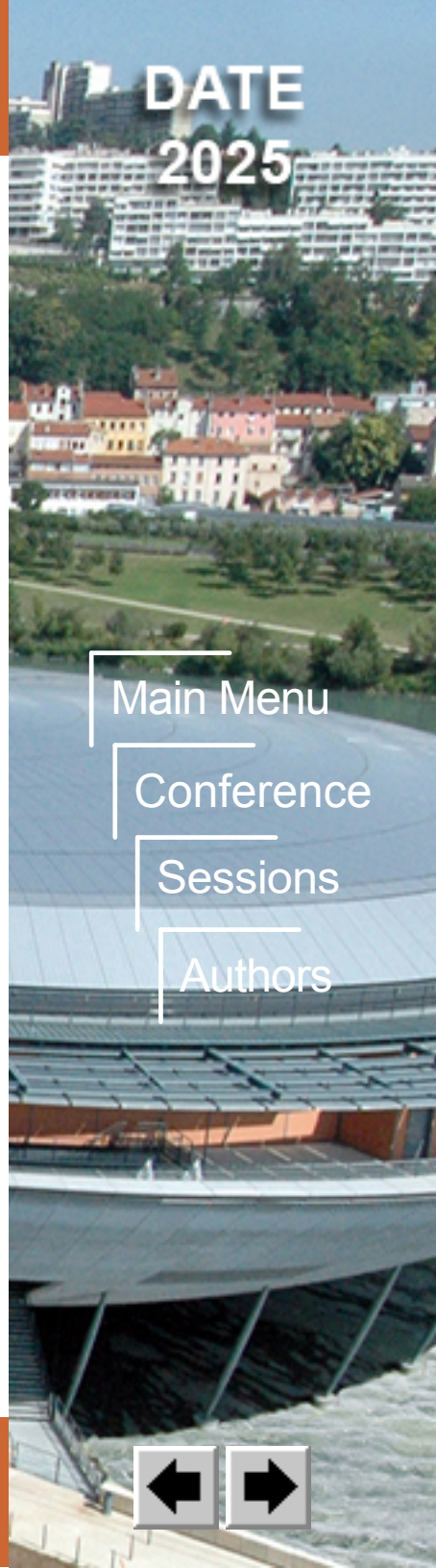
Ising, XY, and k-local Hamiltonians, emphasising the system's applicability across various physical platforms, including photonic, electronic, and atomic systems. Two primary directions have emerged for developing gain-based analogue hardware, each using distinct aspects of physics' role in computational processes. The first approach exploits natural evolution principles of physical systems influenced and driven by external parameters, with the challenge of establishing controllable couplings between 'spins'. Polariton condensates in inorganic and organic-inorganic halide perovskites, atoms in QEDs and degenerate laser systems exemplify this. Conversely, the second approach, represented by technologies like analogue interactive machines (AIM) and spatial photonic machines (SPIM), focuses on establishing couplings through processes like light propagation, optical modulation, and signal detection, thereby managing system dynamics through feedback loops. Both platforms' core is the critical process leading to the optimum solution. Despite advancements in the physical realisation of these concepts, critical questions remain about scalability, the influence of phase space structures on system performance, and identifying problems best suited for these unconventional computing architectures. We need to understand the dynamic behaviour of the systems during symmetry-breaking transitions, trajectory optimisation towards global minima, error probabilities, and the potential for dissipation and nonlinearities to rectify these errors, highlighting the pivotal role of theory in addressing these challenges. By comparing various experimental platforms, including polaritons, lasers, and cold atoms, we should emphasise and exploit the universal nature of these questions. My talk outlines a strategic plan to tackle these outstanding questions while discussing and contrasting different approaches.

FS03.3 CHEMCOMP: Compiling and computing with chemical reaction networks

Nicolas Agostini, Connah Johnson, William Cannon and Antonino Tumeo,
Pacific Northwest National Laboratory, US

Abstract*:* The exponential growth in computing demands driven by scientific computing, data analytics, and artificial intelligence is pushing conventional CMOS-based high-performance computing systems to their physical and energy efficiency limits. As we approach the era of post-exascale computing, disruptive approaches are necessary to overcome these barriers and achieve substantial gains in energy efficiency. Analog and hybrid digital-analog computing systems have emerged as promising alternatives, offering the potential for orders-of-magnitude improvements in efficiency. Among these, biochemical computing stands out as a novel paradigm capable of leveraging the natural efficiency of chemical reactions, which inherently solve optimization problems by converging to steady states. By scaling up reaction networks or reaction vessel sizes, biochemical systems present an opportunity to meet the high-performance demands of modern computing tasks. Despite their promise, significant theoretical and practical challenges remain, particularly in formulating and mapping computational problems to chemical reaction networks (CRNs) and designing viable biochemical computing devices. This paper addresses these challenges by introducing ChemComp, a comprehensive framework for chemical computation. The framework features an abstract chemical reaction dialect implemented as a multi-level intermediate representation (MLIR) compiler extension and provides a systematic approach to translating mathematical problems into CRNs. We demonstrate the potential of our framework through a case study emulating a simplified chemical reservoir computing device. This work establishes the foundational tools and methodologies necessary to harness the computational power of chemistry, paving the way for the development of energy-efficient, high-performance computing systems tailored to contemporary and future computational needs.

FS03.4 Exploring dendritic computation in bio-inspired architectures for dynamic programming



Anup Das, Drexel University, US

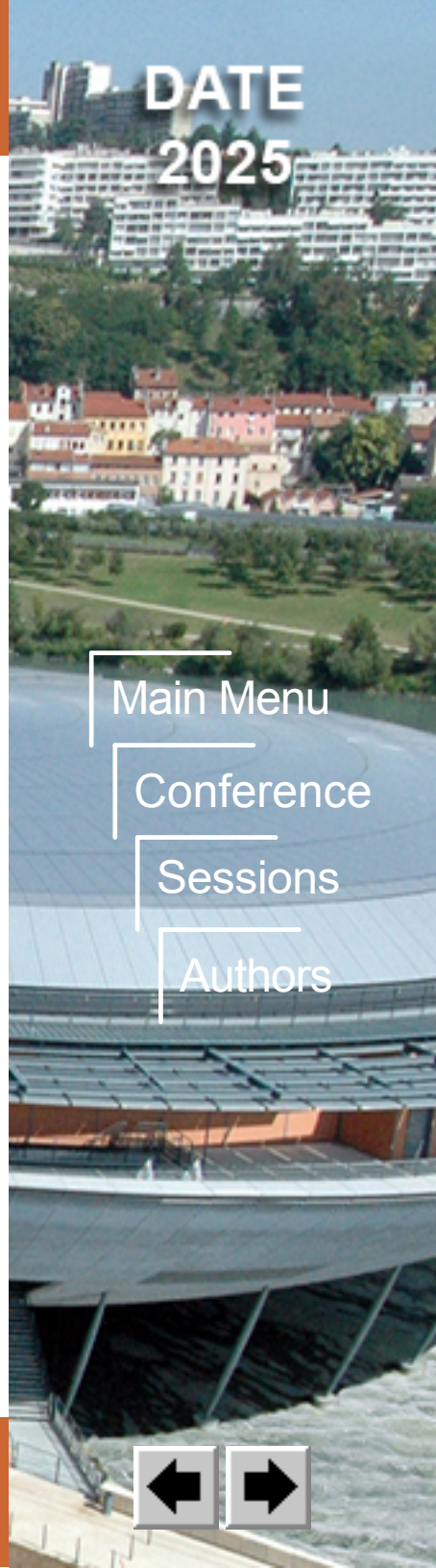
Abstract*:* Dynamic programming is a classical optimization technique that systematically decomposes a complex problem into simpler sub-problems to find an optimal solution. We explore the use of bio-inspired architectures to find the shortest path between two nodes in a graph using dynamic programming. We leverage dendritic computations, which are linear and non- linear mechanisms in neuronal dendrites that allow to implement different computational primitives. We exploit two key mechanisms: 1) a dendrite acts as a delay line to propagate an excitatory post-synaptic potential to the soma, and 2) a feedback mechanism from the soma into the dendrites to control this delay. Our key ideas are the following. First, we model each node on a graph as a leaky integrate-and-fire (LIF) neuron, supporting the two dendritic mechanisms. We use a countdown counter to implement forward propagation of a delayed synaptic potential and eligibility trace-based feedback to update the delay by incorporating the cost of edges in a graph. Next, we formulate dynamic programming in terms of the time to the first spike in neurons. We breakdown the shortest path problem into sub- problems of finding the earliest firing times of neurons and iteratively building the final solution from these smaller sub- problems by tracing backward. We implement this approach for several real-world graphs and show its scalability. We also show an early prototype on a Virtex UltraScale FPGA.

Date: Tuesday, 1 April 2025
Time: 08:30 - 10:00 CET

FS05 Focus Session: 3D Integration, Cryogenic Circuits and Superconducting Logic: Emerging Trends Shaping the Future of High-Performance Computing

Session chair: Ahmedullah Aziz, University of Tennessee Knoxville, US
Session co-chair: Hussam Amrouch, TU Munich, DE
Organiser: Hussam Amrouch, TU Munich, DE

As CMOS scaling approaches its fundamental limits, the explosive rise of artificial intelligence (AI) and large language models (LLMs) is exposing profound challenges in today's computing architectures. The immense demand for memory, speed, and energy efficiency is pushing classical chips to their breaking point. This focus session will explore three transformative trends that are poised to redefine the future of high-performance computing and address the escalating challenges of AI-driven workloads. The first trend is 3D integration, an innovative paradigm that allows memory layers to be fabricated in the back end of line (BEOL), dramatically increasing on-chip memory capacity. Of the emerging memory technologies, ferroelectric memories stand out as particularly promising due to their compatibility with BEOL CMOS and their low-power, high-density operation. The second trend, cryogenic CMOS, leverages the advantages of operating circuits at cryogenic temperatures (77K and below), significantly enhancing transistor performance with steeper subthreshold slopes, higher on-currents, and lower off-currents, delivering remarkable speed and efficiency gains. The last trend is superconducting logic, which is set to revolutionize computing by achieving zero resistance, unlocking unprecedented levels of speed and energy efficiency. Our session brings together leading experts from both industry and academia to present cutting-edge solutions that are already reshaping the semiconductor landscape. Attendees will gain a deep, comprehensive understanding of the emerging trends that will drive the next generation of high-performance computing, providing a critical window into the chips that will fuel future advances in AI.



FS05.1 Pushing the boundaries of AI chips: from monolithic 3D CMOS to cryogenic computing

Mahdi Benkhelifa[1], Shivendra Parihar[2], Anirban Kar[1], Girish Pahwa[3], Yogesh Chauhan[4] and Hussam Amrouch[5]
[1]TU Munich, DE; [2]University of California, Berkeley, US; [3]National Yang Ming Chiao Tung University, TW; [4]IIT Kanpur, IN; [5]TU Munich (TUM), DE

Abstract: As CMOS scaling approaches its fundamental limits, the explosiverise of AI and LLMs has unveiled profound bottlenecks in computing architectures. This talk presents two groundbreaking paradigms poised to reshape the landscape of high-performance computing and meet the surging demands of AI-driven workloads. The first paradigm is 3D monolithic integration, a revolutionary approach that achieves unprecedented logic density through Complementary FETs (CFETs), where pMOS and nMOS transistors are vertically stacked, and a dramatic expansion of on-chip memory capacity by integrating memory layers atop logic transistors. The second paradigm leverages the transformative potential of operating chips at cryogenic temperatures—specifically around 77K—where transistors exhibit significantly enhanced performance, and parasitic resistances are substantially minimized. These advancements hold the promise of redefining computing efficiency and performance for the AI era.

FS05.2 Transistor aging and circuit reliability at cryogenic temperatures

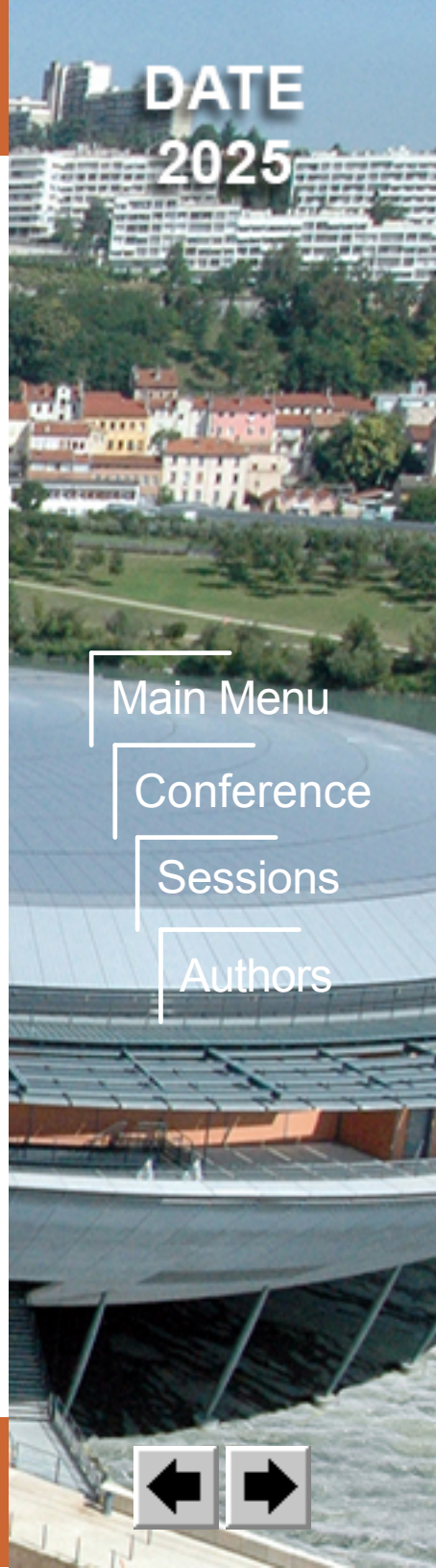
Javier Fortuny and Vishal Nayar, IMEC, BE

Abstract: The increasing interest in cryogenic circuits is driven by their transformative potential across high-performance computing, medical devices, space exploration, and quantum technologies. Operating transistors at cryogenic temperatures, such as 77 K and below, yields substantial improvements, including increased ON current, reduced OFF current, and enhanced sub-threshold slope. While recent studies have explored device-level reliability at cryogenic temperatures, circuit-level reliability—particularly under bias temperature instability (BTI)—remains underexamined, leaving critical aging mechanisms at these temperatures not well understood. To bridge this gap, we designed and fabricated a customized chip in a commercial HKMG 28 nm technology. The chip integrates several ring oscillator (RO) circuits for precise characterization of accelerated aging effects, enabling evaluation of their impact on performance at cryogenic temperatures. Finally, we project technology degradation in a 10-year future comparing, the achieved wear out between room temperature (298 K) and at 77 K when operating circuits at the nominal voltage, revealing the significant mitigation of BTI aging when operating at affordable cryogenic temperatures.

FS05.3 Ferroelectric-superconducting synergy for future computing

Shamiul Alam[1] and Ahmedullah Aziz[2]
[1]University of Tennessee Knoxville, US; [2]University of Tennessee, Knoxville, US

Abstract: Ferroelectric Superconducting Quantum Interference Devices (Fe-SQUIDs) have recently gained attention as a transformative technology for superconducting computing, offering voltage-controlled switching that is essential for large-scale digital circuits. This unique technology has the potential to drive advancements in cryogenic computing by enabling scalable memory systems and voltage-controlled logic circuits. These innovations are critical for the realization of large-scale quantum computers and hold significant promise for high-performance computing and space exploration. In this article, we explore how Fe-SQUIDs, integrated with heater cryotrons (hTrons), can be harnessed to develop key components of computing systems. These include non-volatile memory, voltage-controlled logic circuits, in-memory matrix-vector multiplication systems, and ternary content-addressable memory. We also examine how changes in the key characteristics of Fe-SQUIDs and hTrons influence the



performance of these applications, providing insights into the design and optimization of next-generation superconducting hardware.

FS05.4 Material-to-system co-optimization for advanced semiconductor manufacturing

Gaurav Thareja, Applied Materials, US

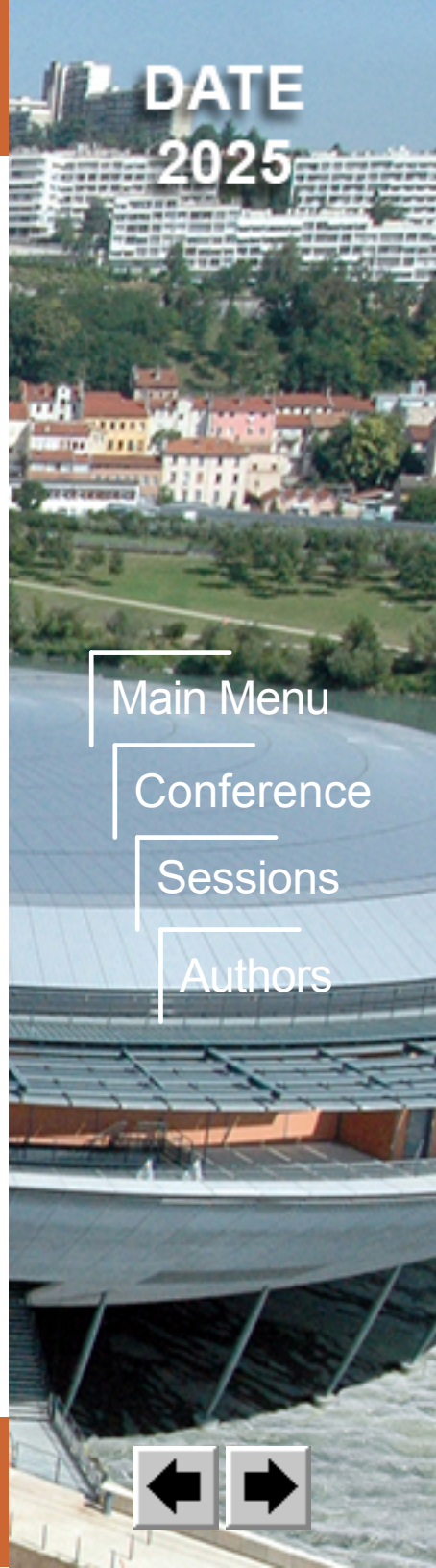
Abstract: The exponential growth of AI is tied to groundbreaking advancements in semiconductor technology, driven by the PPACt metrics: low Power, high Performance, reduced Area, low Cost, and faster Time to market. Traditionally, achieving these metrics has required years—often decades—of meticulous semiconductor innovation, progressing from concept to high-volume manufacturing. This process unfolds through four critical phases: materials discovery, process optimization, device engineering, and chip design. In this talk, we will explore how ML-driven methods are revolutionizing the semiconductor industry, significantly accelerating progress across all stages of development. We will highlight the key discoveries necessary for enabling novel materials that power cryogenic circuits, ferroelectric memories, and 3D integration.

Date: Tuesday, 1 April 2025
Time: 11:00 - 12:30 CET

FS06 Focus Session: Panel on Improving Chip Design Enablement for Universities in Europe

Session chair: Ulf Schlichtmann, TU Munich, DE
Session co-chair: Holger Blume, Leibniz University Hannover, DE
Organisers: Norbert When and Lukas Krupp, University of Kaiserslautern-Landau, DE
Panellists: *X. Sharon Hu[1], Joachim Rodrigues[2], Luca Benini[3], Ian O'Connor[4], Andreas Brüning[5] and Patrick Haspel[6]*
[1]University of Notre Dame, US; [2]Lund University, SE; [3]ETH Zurich, CH | Università di Bologna, IT; [4]Lyon Institute of Nanotechnology, FR; [5]FMD, DE; [6]Synopsys, DE

The semiconductor industry is central to the European economy, particularly in the industrial and automotive sectors. Semiconductor fabrication and chip design are the two largest segments of the microelectronics value chain. While Europe is strengthening semiconductor fabrication and technology with considerable investments, e.g., in new fabs, chip design capabilities fall far short of the required capacities. The EU MicroElectronics Training, Industry and Skills (METIS) Report 2023 has shown that chip designers are the job profiles identified as the most difficult to find in the European microelectronics industry. European universities face many challenges hindering their ability to produce skilled graduates and contribute to the semiconductor ecosystem. While student interest in, e.g., AI is booming, we observe a decreasing interest in microelectronics. The main reasons for this are the high entry barriers for students, reinforced by the lack of chip design enablement in academia. Hence, there are ongoing initiatives in different European countries, on the EU level, and worldwide to strengthen chip design education and research. This focus session will bring together stakeholders of these initiatives from Europe and the USA to explore the critical challenges, opportunities, and potential strategies facing chip design enablement in European academic institutions. The session will be held in the panel format with active audience participation to guarantee inclusiveness and foster a broad view of the topic.



Conference Information

Date: Tuesday, 1 April 2025
Time: 14:00 - 15:30 CET

FS10 Focus Session: GenAI-Native EDA : Redefining Verification with Large Language Models

Session chair: Pierre-Emmanuel Gaillardon, University of Utah, US
Organisers: Pierre-Emmanuel Gaillardon, University of Utah, US

As hardware design processes grow in complexity and scale, verification methodologies reliant on human expertise and manual effort are increasingly insufficient to handle intricate interdependencies and challenging constraints across design stages. Generative AI (GenAI), particularly Large Language Models (LLMs), offers a breakthrough approach, enabling sophisticated pattern recognition, multimodal data integration, and adaptive learning to tackle these verification challenges. From early-stage Power, Performance, and Area (PPA) estimations to advanced anomaly detection and layout optimization, AI-driven tools are set to transform verification workflows. By synthesizing circuit representations across specifications, netlists, and physical layouts, these AI models promise not only enhanced verification precision but also significant reductions in time-to-market, making verification processes more scalable for next-generation design technologies. In this special session, attendees will explore cutting-edge GenAI applications for EDA with a focus on hardware verification, gaining insights into how advanced techniques like multimodal learning, LLM-based optimization, and multi-agent systems can boost verification accuracy. Discussions will highlight foundational shifts toward AI-native EDA tools and examine the potential of LLMs to automate and scale verification to meet the demands of increasingly complex hardware systems. Presentations will also cover AI- driven approaches to optimizing verification workflows and automating the detection of potential design flaws.

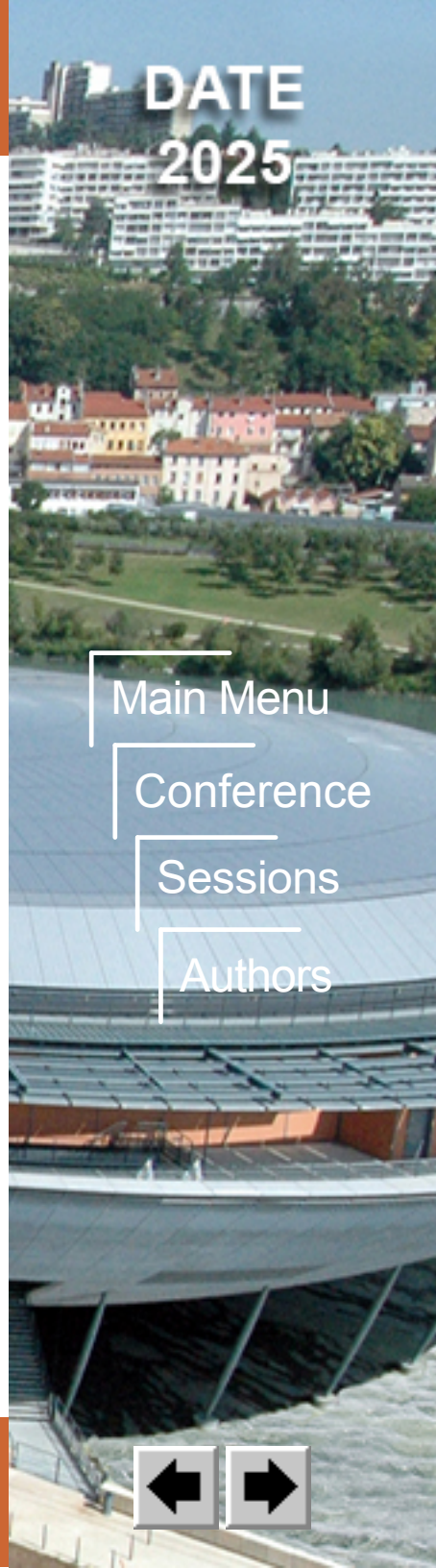
FS10.1 Revolutionizing Verification With GenAI-Powered Automation: A Paradigm Shift Towards Agentic Workflows

Andy Penrose, Cadence, UK

Abstract: The verification of complex System-on-Chip (SoC) designs is undergoing a significant transformation with the advent of Artificial Intelligence (AI) powered automation. Traditional single-run, single-engine algorithms are giving way to data-driven approaches that leverage insights from multiple runs of diverse engines across the entire verification campaign. The Verisium platform exemplifies this shift, optimizing verification workloads, enhancing coverage, and accelerating bug diagnosis. Recent advances in Large Language Models (LLMs) and Large Reasoning Models (LRMs) are further propelling this trend, profoundly impacting the capabilities of automation tools. While individual applications of LLMs can yield substantial productivity gains, the most profound benefits will emerge from integrating multiple GenAI powered tasks into multi-step automated workflows. This vision of an agentic workflow for design and verification represents the future trajectory of the field.

FS10.2 Generative AI in Semiconductor Development: Automating Design and Verification for the Next Era of Innovation

Jin Zhang, Synopsys, Inc., US



Abstract: Generative AI (GenAI) is reshaping the semiconductor industry by streamlining both design and verification, traditionally seen as distinct yet interdependent disciplines. With the increasing complexity of modern chips, conventional methodologies face growing challenges in scalability, efficiency, and verification coverage. GenAI introduces new opportunities by automating RTL generation, optimizing design space exploration, and enhancing verification processes through AI-driven test generation and formal reasoning. This talk explores how GenAI can accelerate chip development while reducing the manual effort required for design validation. We discuss the potential benefits, including improved design efficiency, faster iteration cycles, and enhanced verification robustness, as well as key considerations such as AI trustworthiness, integration with existing workflows, and the evolving role of engineers in an AI-augmented development environment. As the industry moves toward more autonomous design and verification flows, understanding the opportunities and challenges of GenAI-driven automation will be critical in shaping the future of semiconductor innovation.

FS10.3 EDA-aware RTL generation with Large Language Models

Mubashir Islam[1], Humza Sami[1], Pierre-Emmanuel Gaillardon[2] and Valerio Tenace[1]
[1]PrimisAI, US; [2]University of Utah -- PrimisAI, US

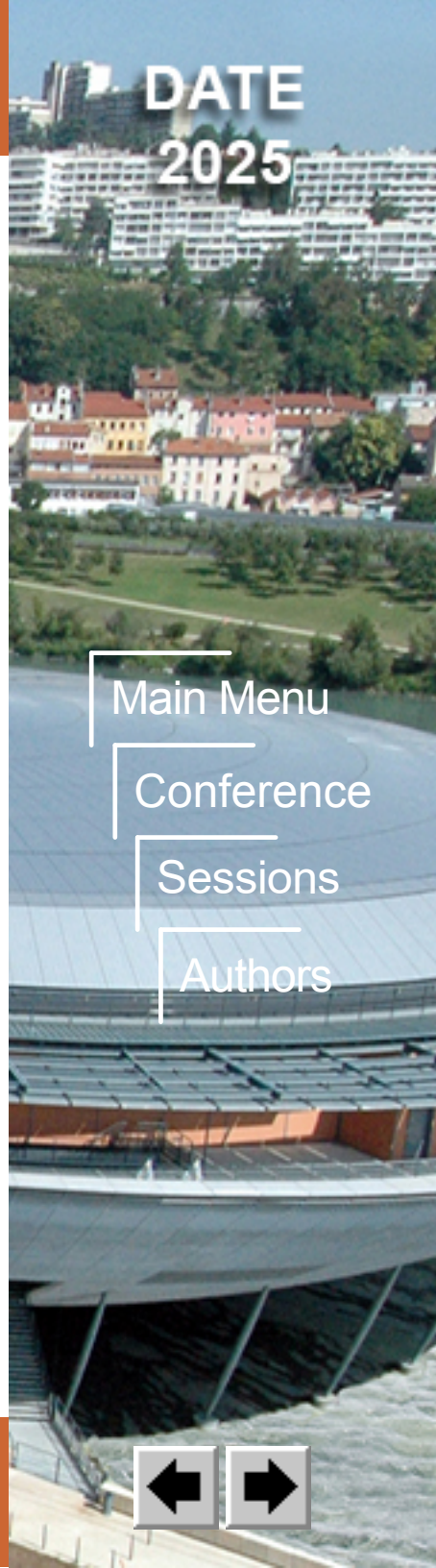
Abstract: Large Language Models (LLMs) have become increasingly popular for generating RTL code. How- ever, producing error-free RTL code in a zero-shot setting remains highly challenging even for state-of-the-art LLMs, often leading to issues that require manual, iterative refinement. This additional debugging process can dramatically increase the verification workload, underscoring the need for robust, automated correction mechanisms to ensure code correctness from the start. We will AIVRIL2, a self-verifying, LLM-agnostic agentic framework aimed at enhancing RTL code generation through iterative corrections of both syntax and functional errors. Our approach leverages a collaborative multi-agent system that incorporates feedback from error logs generated by EDA tools to automatically identify and resolve design flaws. Experimental results, conducted on the VerilogEval-Human benchmark suite, demonstrate that our framework significantly improves code quality, achieving nearly a 3.4× enhancement over prior methods. In the best-case scenario, functional pass rates of 77% for Verilog and 66% for VHDL were obtained, thus substantially improving the reliability of LLM-driven RTL code generation.

Date: Tuesday, 1 April 2025
Time: 16:30 - 18:00 CET

FS02 Focus Session: AI-Driven Design Evolution: Benchmarking and Infrastructure for the Next Era of Semiconductors and Photonics

Session chair: Anthony Agnesina, NVIDIA Corp., US
Session chair: Hao Geng, Shanghai Tech University, CN
Organisers: Haoyu Yang, NVIDIA Corp., US. Yuzhe Ma, Hong Kong University of Science and Technology (GZ), CN

As AI and machine learning models become increasingly integrated into semiconductor and photonic design workflows, the need for rigorous benchmarking, robust datasets, and scalable infrastructures is paramount. This special session presents pioneering research on evaluating AI capabilities across digital hardware, formal verification, and photonic device design, with a strong focus on the importance of benchmark frameworks and dataset development. The session will feature four key talks: 1) ChipVQA is a benchmark designed to evaluate visual language models (VLMs) in chip design, requiring a visual



understanding of diagrams and schematics across five disciplines. Current models, including GPT-4o, struggle with domain-specific tasks, while a novel agent-based approach shows potential for improved performance. 2) FVEval is a comprehensive benchmark designed to evaluate large language models (LLMs) in formal verification tasks for digital chip design. It assesses LLMs' abilities to generate SystemVerilog assertions and reason about design RTL. The benchmark includes both expert-written and synthetic examples, offering insights into current LLM capabilities and potential for improving formal verification productivity. 3) MAPS introduces an open-source infrastructure to standardize AI-based solvers for photonic device simulation and inverse design. It provides a rich dataset, a neural operator model zoo for training, and a scalable framework for benchmarking AI-based photonic simulators. MAPS aims to accelerate innovation in photonic hardware by bridging the gap between AI-driven physics simulations and photonic design optimization. 4) PICEval introduces a benchmark to evaluate large language models (LLMs) for automating the design of photonic integrated circuits (PICs). The benchmark spans device- to circuit-level designs and assesses the functionality and fidelity of LLM-generated netlists by comparing them to expert-written solutions. It highlights the challenges and potential of LLMs in automating PIC design and identifies areas for further research to optimize their application. Together, these talks underscore the crucial role of benchmarks, datasets, and scalable infrastructure in advancing AI for chip and photonic design, shaping the future of automated and intelligent design workflows

FS02.1 CHIPVQA: Benchmarking visual language models for chip design

Haoyu Yang, Qijing Huang, Nathaniel Pinckney, Walker Turner, Wenfei Zhou, Yanqing Zhang, Chia-Tung Ho, Chen-Chia Chang and Haoxing Ren, NVIDIA Corp., US

Abstract: Large-language models (LLMs) have shown great potential in assisting chip design and analysis, with recent research focusing primarily on text-based tasks such as general QA, debugging, and design tool scripting. However, the chip design and implementation workflow often requires a visual understanding of diagrams, flowcharts, graphs, schematics, waveforms, and more, necessitating the development of multi-modality foundation models. To address this gap, we propose ChipVQA, a benchmark designed to evaluate the capability of visual language models (VLMs) for chip design. ChipVQA comprises 142 carefully crafted and collected VQA questions spanning five chip design disciplines: Digital Design, Analog Design, Architecture, Physical Design, and Semiconductor Manufacturing. Unlike existing VQA benchmarks, ChipVQA questions are meticulously created by chip design experts and require in-depth domain knowledge and reasoning to solve. Our comprehensive evaluations on both open-source and proprietary multi-modal models reveal significant challenges posed by the benchmark suite, with existing VLMs struggling to meet the demands of chip design knowledge and reasoning. Notably, GPT-4o achieves only a 44% correctness rate. Additionally, we conducted a preliminary study on an alternative VLM inference methodology using an agent, which showed improved performance in certain categories without additional training, highlighting the potential of leveraging LLM agents as an alternative approach for VLM deployment in chip design.

FS02.2 FVEVAL: Understanding language model capabilities in formal verification of digital hardware

Minwoo Kang[1], Mingjie Liu[2], Ghaith Bany Hamad[2], Syed Suhaib[2] and Haoxing Ren[2]
[1]University of California, Berkeley, US; [2]NVIDIA Corp., US

Abstract: The remarkable reasoning and code generation capabilities of large language models (LLMs) have spurred significant interest in applying LLMs to enable task automation in digital chip design. In particular, recent

work has investigated early ideas of applying these models to formal verification (FV), an approach to verifying hardware implementations that can provide strong guarantees of confidence but demands significant amounts of human effort. While the value of LLM-driven automation is evident, our understanding of model performance, however, has been hindered by the lack of holistic evaluation. In response, we present FVEval, the first comprehensive benchmark and evaluation framework for characterizing LLM performance in tasks pertaining to FV. The benchmark consists of three sub-tasks that measure LLM capabilities at different levels---from the generation of SystemVerilog assertions (SVAs) given natural language descriptions to reasoning about the design RTL and suggesting assertions directly without ad

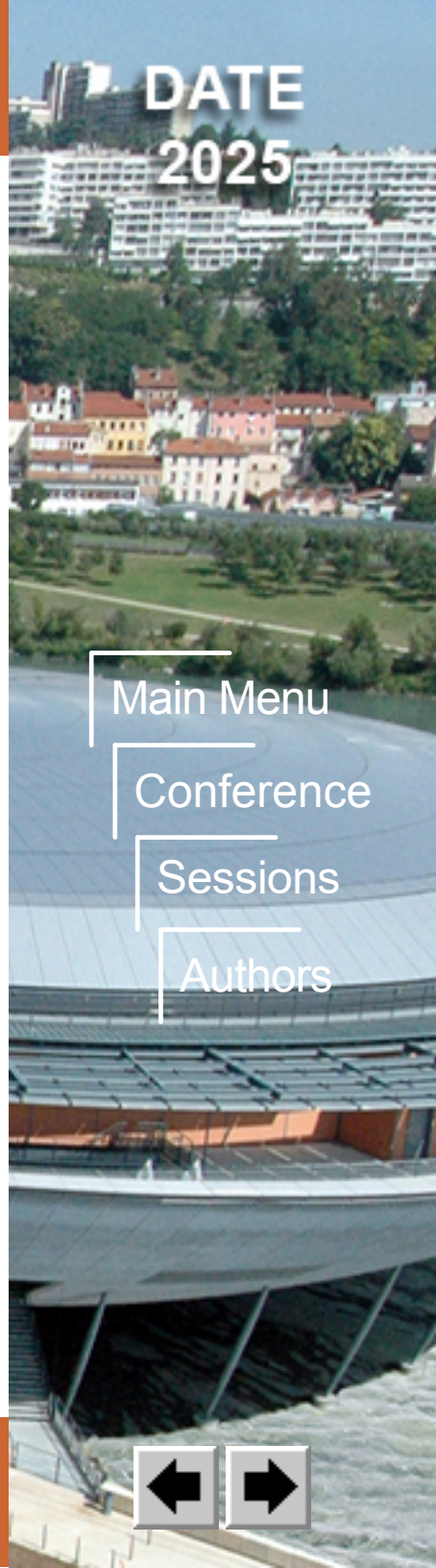
FS02.3 MAPS: Multi-fidelity AI-augmented photonic simulation and inverse design infrastructure

Pingchuan Ma[1], Zhengqi Gao[2], Meng Zhang[3], Haoyu Yang[4], Haoxing Ren[4], Rena Huang[3], Duane Boning[2] and Jiaqi Gul.

[1]Arizona State University, US; [2]Massachusetts Institute of Technology, US; [3]Rensselaer Polytechnic Institute, US; [4]NVIDIA Corp., US

Abstract: Inverse design has become a powerful approach in photonic device optimization, enabling access to high-dimensional, non-intuitive design spaces that lead to ultra-compact devices with superior performance, ultimately advancing the development of high-density photonic integrated circuits (PICs). The adjoint method plays a key role in this process by efficiently computing both the figure of merit (FoM) and its analytical gradient with only two simulations, enabling gradient-based device topology optimization. However, a significant computational bottleneck remains, i.e., the reliance on solving partial differential equations (PDEs) or eigenvalue problems within simulation-in-the-loop optimization frameworks, which hinders scalability. Recent advancements in AI-based solvers offer a promising solution by accelerating the solving of these PDEs and eigenvalue problems, enabling faster and more scalable inverse design processes. Despite these advancements, a major challenge persists—the absence of an open-source, standardized, widely available infrastructure and dataset for training and benchmarking AI-based PDE solvers tailored to photonic hardware. In this work, we introduce MAPS (Multi-Fidelity AI-Augmented Photonic Simulation and Inverse Design Benchmarking Infrastructure) to fill this gap. MAPS features: 1. MAP-Data: A photonic device dataset that covers a broad design space of representative device types, capturing both high- and low-performance designs. The dataset integrates multi-modal inputs (structure, light source, etc.) and physically significant evaluation metrics (FoMs and light fields, etc.), offering a rich data source for AI-based photonic simulation research. 2. MAPS-Train: A standardized AI-for-photonics neural operator model zoo and training framework, featuring extensible configurations and seamless integration with MAPS-Data pipelines, facilitating fair comparisons and standardized benchmarking of AI-based, physics-inspired photonic simulators. 3. MAPS-InvDes: An advanced adjoint method-based inverse design infrastructure that abstracts complex physical details, making it accessible to both computer-aided design (CAD) and machine learning (ML) communities. It integrates seamlessly with pre-trained AI-based PDE solvers and incorporates customized fabrication variation models (e.g., differentiable lithography and etching) to validate practical applicability in real-world inverse design tasks. This infrastructure MAPS bridges the gap between AI-for-physics and photonic device design by providing a standardized, open-source platform for developing and benchmarking AI-based solvers, ultimately accelerating innovation in both photonic hardware optimization and scientific ML

FS02.4 PICBENCH: Benchmarking LLMs for photonic integrated circuit design



Yuchao Wu[1], Xiaofei Yu[1], Hao Chen[1], Yang Luo[1], Yeyu Tong[2] and Yuzhe Ma[1]
[1]The Hong Kong University of Science and Technology (Guangzhou), CN; [2]The Hong Kong University of Science and Technology (Guangzhou)), CN

Abstract: While large language models (LLMs) have shown remarkable potential in automating various tasks in digital chip design, the field of Photonic Integrated Circuits (PICs)—a promising solution to advanced chip designs—remains relatively unexplored in this context. The design of PICs is time-consuming and prone to errors due to the extensive and repetitive nature of code involved in photonic chip design. In this paper, we introduce PICBench, the first benchmarking and evaluation framework specifically designed to automate PIC design generation using LLMs, where the generated output takes the form of a netlist. Our benchmark consists of dozens of meticulously crafted PIC design problems, spanning from fundamental device designs to more complex circuit-level designs. It automatically evaluates both the syntax and functionality of generated PIC designs by comparing simulation outputs with expert-written solutions, leveraging an open-source simulator. We evaluate a range of existing LLMs, while also conducting comparative tests on various prompt engineering techniques to enhance LLM performance in automated PIC design. The results reveal the challenges and potential of LLMs in the PIC design domain, offering insights into the key areas that require further research and development to optimize automation in this field.

Date: Wednesday, 2 April 2025
Time: 8:30 - 10:00 CET

FS07 Focus Session: Panel on European Startups on AI – Path to success

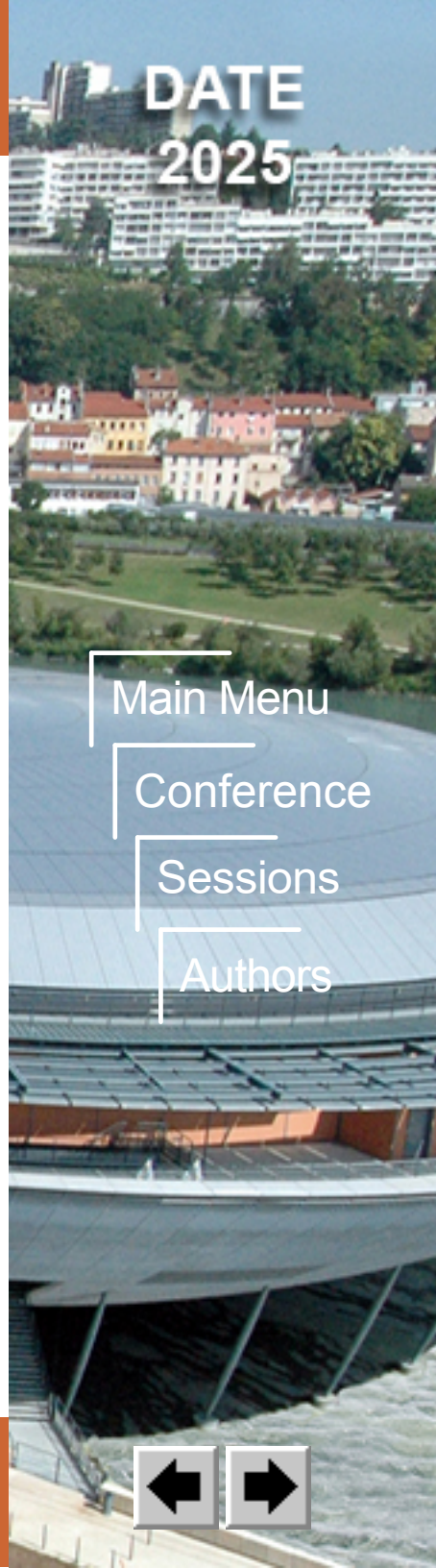
Session chair: *Anton Klotz, Fraunhofer, DE*
Organiser: *Marco Inglardi, Synopsys, IT*
Panellists: *Manu Nair, Synthara, CH, Patrick Couvert, NEUrXCORE, FR, Sean Redmond, Silicon Catalyst, UK, David Atienza, EPFL, CH, Edith Euan Diaz, Axelera, NL*

AI is one of the hottest and influential topics of this decade. Specialized hardware is required to run AI algorithms and several companies are working on designing such hardware, among these companies there are several European startups. There are multiple challenges that these startups have to overcome like lack of financing, lack of skilled workforce, challenge to find interested customer, who take the risk and work with a startup and not with an established market leader. In this session several startups come to word and tell how they have managed to overcome the challenges. We also have perspectives from a commercial startup incubator, which has specialized on microelectronics startups and from academic, who has spin-off several startups. After impulse presentations, there will be a panel discussion, where the panelists will answer the questions from the audience on the landscape of microelectronic startups in Europe.

Date: Wednesday, 2 April 2025
Time: 11:00 - 12:30 CET

FS09 Focus Session: Empowering European Innovation by Making Leading-Edge Technologies Accessible to Academia

Session chair: *Catherine Le Lan, Synopsys, FR*
Organisers: *Catherine Le Lan, Synopsys, FR. Olivier Sentieys, Inria, FR*



Conference Information

Academia and fundamental research are the driving forces behind groundbreaking advancements. Innovation is the cornerstone of the semiconductor industry's success. By providing access to leading-edge technologies, we support and accelerate semiconductor research, paving the way for a brighter, technologically advanced future. During this session, we will discuss how pilot lines can play a major role in enabling technology access to academia. Additionally, we will explore the perspective of academia on how this access can drive fundamental research and its contributions.

FS09.1 How can academia ride the wave of new semiconductor investment and technological change?

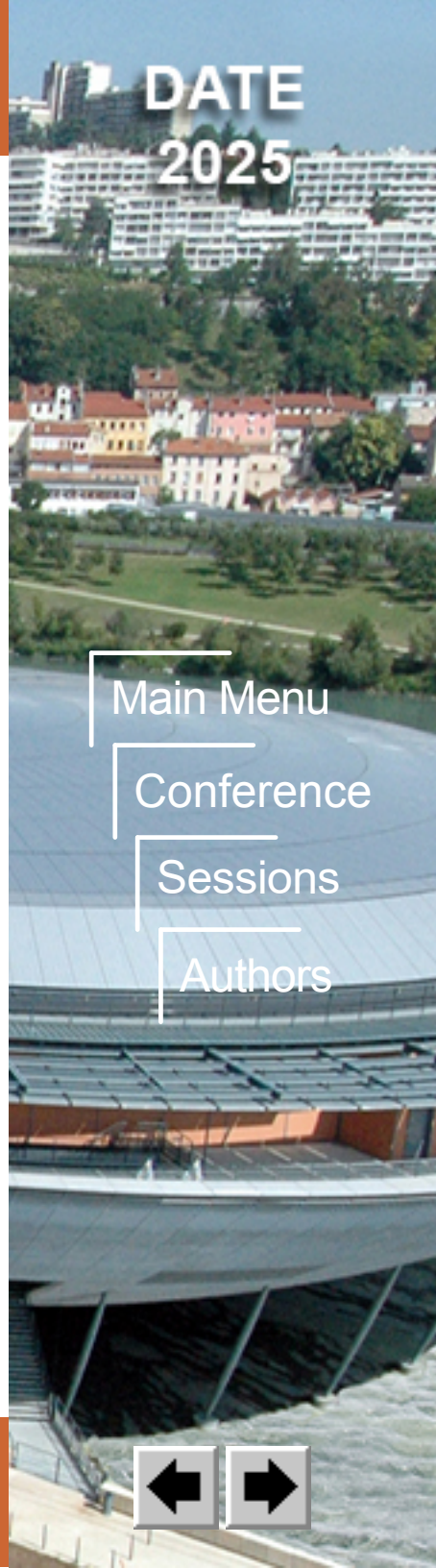
John Darlington, University of Southampton, GB

Abstract: Quoting from Aristotle, first mover in scientific method and formal logic, “The more you know, the more you realize you don’t know”. After a relatively long period of incremental change in electronic design and computing architectures we are now in a period of significant change. New forms of transistors, new memories, new methods of connection and packaging, new compute demands and fabrics, new design considerations, making the scope of our design discipline ever broader. What are some of the opportunities and also the challenges for Academia in this period of change and how can investments in semiconductor innovation in Europe benefit. Academia will have similar capacity to educate students, mentor PhDs and undertake fundamental research. Adoption of community-based design, broader collaboration networks, and simplified access to capabilities and skills, can help make best use of that capacity, leading to greater adoption of technological advances. Similarly they can help provide a pathway from fundamental research to demonstrable impact for society. Examples of more collaborative research will help inform the debate on how to benefit from change and investment in semiconductors.

FS09.2 NANOIC Platform

Giuseppe Fiorentino, Imec, BE

Abstract: In the context of the Chips JU Act, a European consortium of Research Centers including IMEC, CEA-LETI, Tyndall Institute, CSNNT, Fraunhofer Institute and VTT, is developing an ambitious five year program focused on the development of of beyond-2nm systems-on-chip (SoC). The NanoIC pilot line aims in the first place lowers the threshold to innovation by offering early-stage process design kits (PDKs) to companies that want to explore novel solutions. Start-ups, SMEs, universities, and design and system companies can use: - design pathfinding PDKs for early design exploration in future IC technologies, - system exploration PDKs for prototyping of advanced technology components on top of or embedded in the stack of commercially available foundry wafers. The result is a leading technology platform where European and international companies can explore beyond-2nm SoC technologies before they’re introduced into large-scale production. This will enable the European supplier ecosystem to enhance it competitiveness while boosting the global chip value chain and offer companies the opportunity to explore the most advanced chip technology solutions for their future applications. The NanoIC pilot line will be based on an extension of the pilot line facilities that imec built up over the previous decades. Through improvements in terms of repeatability, variability and defectivity of the process modules, the baseline flows aim for a technology readiness level of 4-6 – bringing breakthrough technologies closer to the market. As the landscape of RTOs, SMEs and Universities is widely diffused over the European territory, the EU commission gave recently the green light to the formation of the Competence Centers (CCs), which have as key mission to connect and direct interested users to the most appropriate semiconductor technology offer. In this context, the NanoIC Team is already



working to establish a stable collaboration with all the newly formed CCs. To further enhance the possibility to access and exploit the pilot line possibilities, the NanoIC project is developing a host of initiatives aimed at education and workforce development: courses on beyond-2nm technologies, access to affordable design tools and prototyping services for universities, internships, and training programs, etc.

FS09.3 PREVAIL: Multi HUB Platform to facilitate circuit design

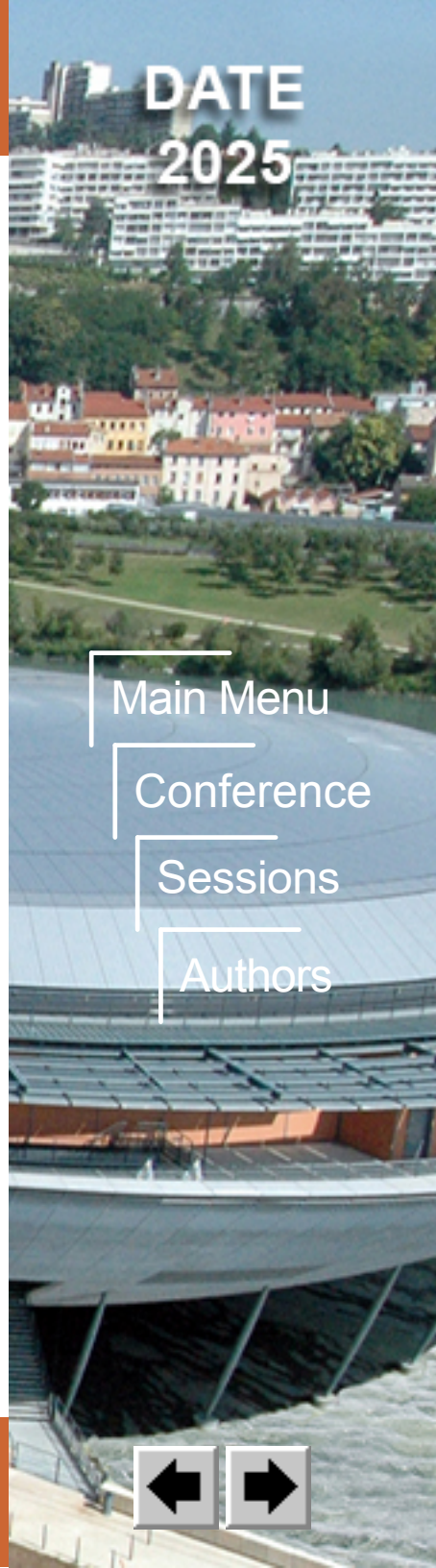
Sergio Nicoletti, CEA, FR

Abstract: The TEF-PREVAIL project brings together CEA-Leti, imec, Fraunhofer-Gesellschaft and VTT with the goal of accelerating the development of next-generation edge-AI technologies. At the heart of the PREVAIL project is a networked, multi-hub platform designed to provide stakeholders across the EU with the capability to fabricate prototype chips for advanced artificial intelligence technologies. Leveraging the power of clean-room tools, on advanced fabrication processes and on expertise and resources of its founding members, the consortium aims to facilitate the design, evaluation, testing, and rapid fabrication of state-of-the-art circuits.

FS09.4 The FAMES Pilot Line: advanced FD-SOI semiconductor technologies with embedded non-volatile Memories, RF components, 3D heterogeneous integration options, and Power Management IC components

Bruno Paing, CEA, FR

Abstract: The EU Chips Act aims to strengthen Europe's semiconductor industry and support its technological sovereignty. The Chips Joint Undertaking, or Chips JU, is boosting the development and adoption of advanced systems and nano-electronic chip technologies manufactured in Europe by supporting, together with participating States, a series of Pilot Line developments in Europe. FAMES, one of the initial 4 Pilot Lines launched via the first Pilot Line call, gathers a technical infrastructure and a leading-edge R&D program that offers European semiconductor stakeholders from industry, research, and academia access to a unique palette of advanced FD-SOI semiconductor technologies with embedded non-volatile Memories, RF components, 3D integration and PMIC components. The FAMES Pilot Line is distributed among a consortium of 11 public research partners from 8 European countries: CEA-Leti (coordinating partner), CEZAMAT-WUT, Fraunhofer, Grenoble INP, Imec, SAL, SiNANO Institute, Tyndall, UC Louvain, Universidad de Granada and VTT. Each partner brings a key and complementary skill to maximize the impact of the FAMES Pilot Line. The FAMES Pilot Line will strengthen the current ecosystem and support key European semiconductor players, leveraging highly differentiating technologies to address the rapid growth of low power, high connectivity and robustly secure integrated circuits driven by the automotive, IoT and smart mobile device markets, to name a few. The project has received 44 letters of support from industrial companies covering all the electronic systems value chain, including Nokia, Ericsson, Nordic, Soitec, ASML, ASM, AMAT, TEL, GlobalFoundries, IBM, Intel, STMicroelectronics, Siemens, Orange, Meta, Stellantis, Valeo. The R&D Services offered by the FAMES Pilot Line include pathfinding PDKs and chip design, PDKs to access silicon via multi-project wafers, advanced manufacturing processes, characterization and testing capabilities and regular training courses and workshops to build the skills and competencies required to ensure the future of semiconductors. The FAMES Pilot Line Partners reach out to Potential Users by way of dedicated workshops, talks and booths at the major electronics conferences and forums and through Design Platforms and Competence Centres. In this talk we will present the different technologies offered by the FAMES Pilot Line and the manner in which Potential Users from companies, research centers and academia can gain access to the FAMES Pilot Line R&D Services.



FS09.5 Heterogeneous Integration and Advanced Packaging Technologies at the APECS Pilot Line

Andreas Brüning, Fraunhofer, DE

Date: Wednesday, 2 April 2025
Time: 14:00 - 15:30 CET

FS04 Focus Session: Designing Secure Space Systems

Session chair: *Sebastian Steinhorst, TU Munich, DE*
Session co-chair: *Daniel Lüdtke, German Aerospace Center (DLR), DE*
Organisers: *Sebastian Steinhorst, TU Munich, DE, Michael Felderer, German Aerospace Center (DLR), DE*

As the scope of space exploration expands, the need for robust cybersecurity measures has become more urgent than ever. Nowadays, private companies are entering the space sector, leading to a big increase in satellite launches and space activities. While this expansion reduces launch costs, it also elevates the risk of cyber threats. Historically, cybersecurity in space has been overlooked, leaving critical vulnerabilities exposed. This hot-topic session will bring together four experts from industry, government, and research to tackle the critical challenges and explore innovative solutions in building a secure space ecosystem.

FS04.1 Offensive security testing for space systems

Milenko Starcik, VisionSpace Technologies GmbH, DE

Abstract: Space missions, especially commercial space systems, are targeted by state-backed Advanced Persistent Threat (APT) actors since they increasingly share capacity between government and private users. The attacks often exploit legacy hardware, software, and outdated protocols. Legacy system vulnerabilities and the effects of the COVID-19 pandemic have further exposed space systems to potential exploitation. Recently, there have been incidents, such as attacks on satellite terminals with the widespread impact of the 2022 ViaSat incident, showing how legacy systems have led to a security breach. While the space systems community has a strong safety and test engineering history, security validation is often neglected. Our security research on currently used space protocols, mission control software, and spacecraft onboard software frameworks shows that security measures are still not applied throughout the space mission life cycle.

FS04.2 Locking your door does not make you secure at home, similarly your satellite!

Zain Hammadeh, German Aerospace Center (DLR), DE

Abstract: Securing the link between the ground segment and the satellite is essential to protect the satellite from cyber-attacks. Solutions including end-to-end encryption can help avoid attacks like spoofing and reply attacks. However, developers of on-board software should not assume that a satellite environment is secure, especially in an era where a satellite will serve as an execution service for 3rd party software, which can be malicious. Efficient intrusion detection systems (IDS) are essential for monitoring network traffic and system behavior to identify malicious activities in real-time. Additionally, an effective intrusion response mechanism must be in place to ensure

that the satellite can continue functioning even under attack. This requires a fail-operational mode that guarantees essential systems remain operational while isolating and neutralizing compromised components. Given the constraints on computational resources in space systems, these security solutions must be optimized for low-latency response and minimal resource consumption, all while ensuring high reliability and resilience against evolving cyber threats.

FS04.3 Security engineering (not just) for space

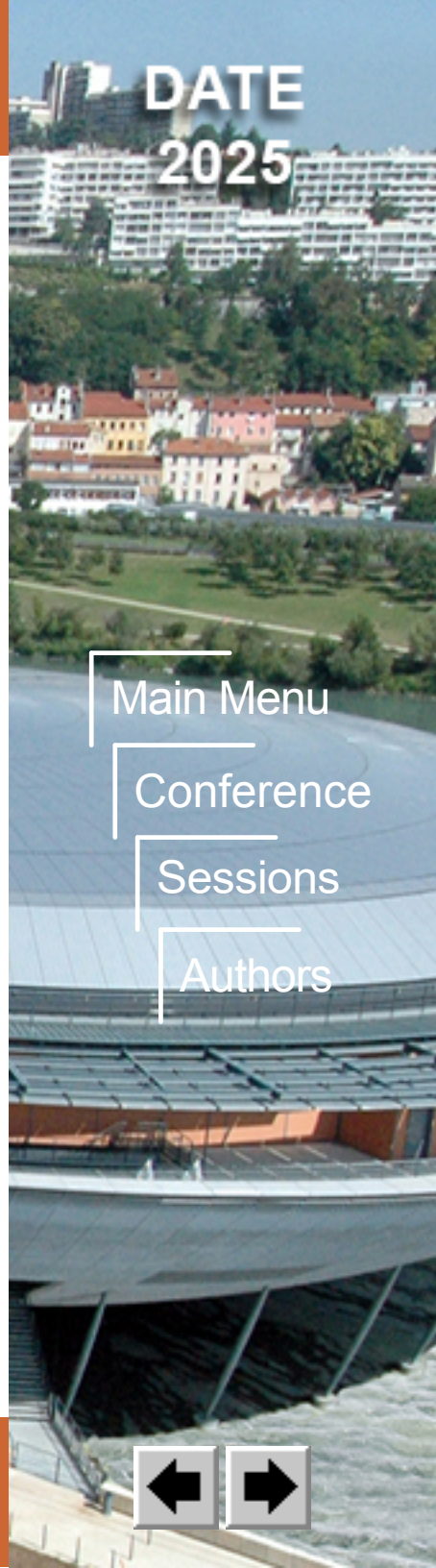
Stefan Langhamme, OHB Digital Connect GmbH, DE

Abstract: As space exploration advances and the commercialization of space technologies grows, the security of space assets has become a critical concern. In a related trend the use of "off the shelf" hard- and software facilitates the commercial use of space, but also creates new attack surfaces. This creates a need for off the shelf solutions for security risks. And while a lot of very good solutions exist, experience shows that adding "security" to a system does not automatically lead to an increase in security. This was just recently demonstrated by the global IT outage caused by the CrowdStrike security software. What is needed is the integration of cybersecurity into the engineering lifecycle. In this talk we will investigate ways in which the diverse field of cybersecurity - ranging from organisational and management questions to deeply technical topics – can be integrated into the engineering lifecycle of space systems. The underlying aim is improving the security stance of the system without adding new problems or unnecessary complexity. Key areas covered include threat modelling, risk assessment, secure software and hardware design, encryption, and response strategies. Our aim is to deepen the listeners understanding of what security is, how to achieve it and how to learn from mistakes made in "non-space" IT systems.

FS04.4 A joint effort: standardization of cybersecurity in space

Florian Göhler, Germany's Federal Office for Information Security (BSI), DE

Abstract: Cybersecurity should be an integrated part of every space mission, and security aspects need to be considered throughout all phases of a project. However, there is a lack of universally applicable security standards that address cyberthreats in space, as existing security standards often miss security measures against space-specific threats. Especially small institutions, start-ups, and research facilities suffer from this lack of guidance, but the issue is also pressing for established industry stakeholders. To overcome this situation, the German Federal Office for Information Security founded an expert group for cybersecurity in space that invites experts from governmental institutions, industry, and academics to work together on standardization and regulation. In a joint effort and based on existing standards, the expert group developed multiple documents that aim to mitigate cyberthreats on space and ground segments. These guidelines focus on every life cycle phase of a space mission, and they are adaptable to the scope and complexity of any given project. Furthermore, the expert group aims to identify emerging new technologies and regulations that may impact cybersecurity in space. These efforts also take international developments into account.



DATE 2025 PhD Forum

Date: Monday, 31 March 2025
Time: 18:30 - 20:00 CET

The PhD Forum is a poster session hosted by EDAA, ACM SIGDA, and IEEE CEDA for PhD students who have completed their Ph.D. thesis within the last 12 months or are close to completing their thesis work. It represents an excellent opportunity for them to get feedback on their research and for the industry to get a glance at the state-of-the-art in system design and design automation.

Admitted Presentations

ADAPTIVE HARDWARE FOR ENERGY-EFFICIENT FPGA-BASED DATA CENTERS
Mattia Tibaldi, Politecnico di Milano, IT

SAFETY CONCEPT OF HIGHLY AUTOMATED DRIVING FOR A TRANSVERSE GUIDANCE SYSTEM
Marzana Khatun, University of Ulm, DE

DETECTION AND REPAIR OF DEFECTS IN RTL CODE USING STATIC ANALYSIS AND GENERATIVE AI
Baleegh Ahmad, New York University, US

LOW-POWER TIME-DOMAIN HARDWARE ACCELERATOR FOR EDGE COMPUTING
Jie Lou and Tobias Gemmeke, RWTH Aachen University, DE

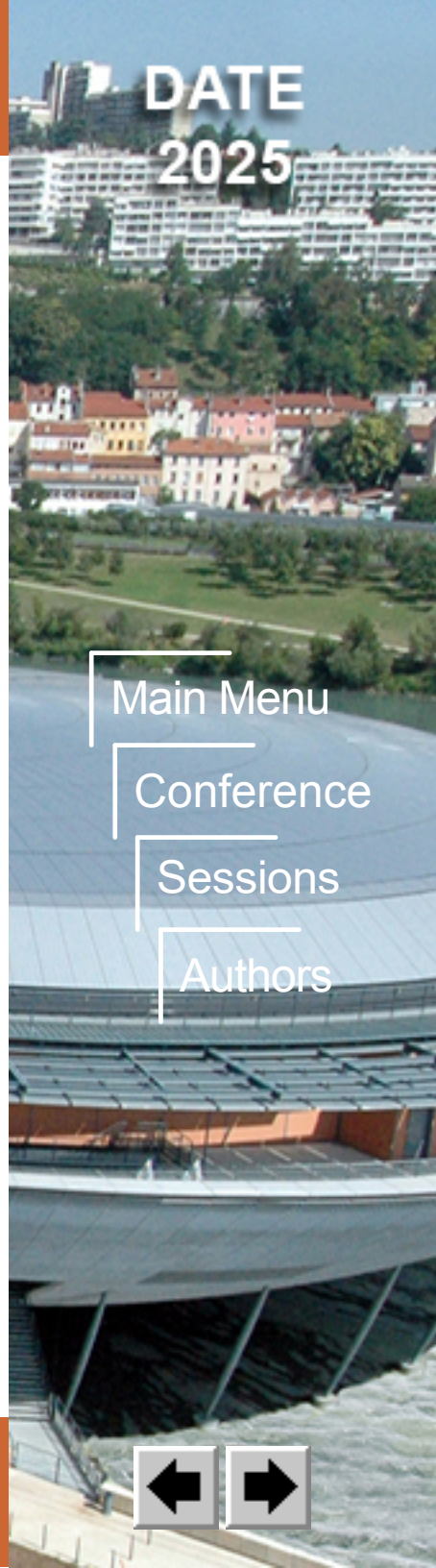
SIMULATION TECHNIQUES FOR RAPID SOFTWARE DEVELOPMENT AND VALIDATION
Mohammadreza Amel Solouki and Massimo Violante, Politecnico di Torino, IT

SOFTWARE AND HARDWARE CO-OPTIMIZATION FOR GRAPH NEURAL NETWORKS ON FPGA
Ruiqi Chen[1], Kun Wang[2] and Bruno da Silva[1], [1]Vrije Universiteit Brussel, BE; [2]Fudan University, CN

SEMI-TENSOR PRODUCT OF MATRICES AND ITS APPLICATION IN LOGIC SYNTHESIS
Hongyang Pan[1], Zhufei Chu[2] and Fan Yang[1], [1]Fudan University, CN; [2]Ningbo University, CN

EXPLORING LAYER-FUSED MAPPING OF DNNS ON HETEROGENEOUS DATAFLOW ACCELERATORS
Arne Symons[1] and Marian Verhelst[2], [1]MICAS, KU Leuven, BE; [2]KU Leuven, BE

INVESTIGATING SECURITY ISSUES IN PROGRAMMABLE LOGIC CONTROLLERS AND RELATED PROTOCOLS
Wael Alsabbagh, IHP – Leibniz Institute for High Performance Microelectronics, DE



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LEARNING-BASED METHODS FOR ENABLING ON-EDGE, ACCURATE, SUSTAINABLE, AND HUMAN-CENTERED INTELLIGENT MANUFACTURING
Luigi Capogrosso, Marco Cristani and Franco Fummi, Università di Verona, IT

HIGH-DENSITY AND RELIABLE COMPUTE-IN-MEMORY CIRCUITS AND ARCHITECTURES FOR BIG DATA PROCESSING
Hongtao Zhong and Xueqing Li, Tsinghua University, CN

HARDWARE RELIABILITY ASSESSMENT AND ENHANCEMENT FOR DEEP NEURAL NETWORKS
Mohammad Hasan Ahmadilivani, Tallinn University of Tehnology, EE

TOWARD RELIABLE AI ACCELERATORS
Eleonora Vacca and Luca Sterpone, Politecnico di Torino, IT

DESIGN AND SIMULATION OF ATOMIC-SCALE COMPUTING: BRIDGING COMPUTER SCIENCE, ELECTRICAL ENGINEERING, AND PHYSICS
Jan Drewniok and Robert Wille, TU Munich, DE

LEARNING-BASED ANALOG ICS LAYOUT AUTOMATION
Davide Basso, University of Trieste, IT

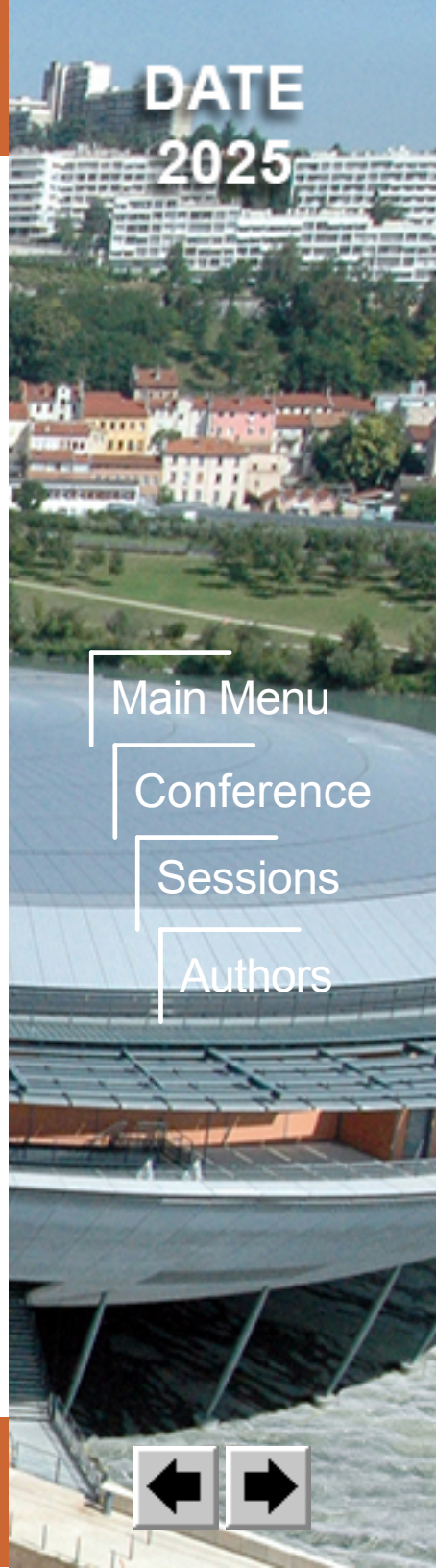
PHYSICAL DESIGN FOR FIELD-COUPLED NANOCOMPUTING
Simon Hofmann and Robert Wille, TU Munich, DE

TOWARDS SOUND AND COMPLETE ANALYSIS OF INTEGRATED CIRCUITS AT TRANSISTOR-LEVEL
Oussama Oulkaid[1,2], Matthieu Moy[2], Pascal Raymond[2], Bruno Ferres[2] and Mehdi Khosravian[3], [1]University Lyon, EnsL, UCBL, CNRS, Inria; [2]FR - University Grenoble Alpes, CNRS, Grenoble INP, VERIMAG, FR; [3]Aniah, FR

FULL-STACK SYSTEM DESIGN AND PROTOTYPING FOR PRACTICAL PHOTONIC-ELECTRONIC NEUROCOMPUTING
Yinyi Liu, The Hong Kong University of Science and Technology, HK

DYNAMIC MEMORY MANAGEMENT OPTIMIZATIONS OVER HETEROGENEOUS MEMORY SYSTEMS
Manolis Katsaragakis[1], Francky Catthoor[2] and Dimitrios Soudris[1], [1]National TU Athens, GR; [2]IMEC, BE

SYSTEM-LEVEL DESIGN IN THE ERA OF BRAIN-COMPUTER INTERFACES
Guy Eichler and Luca Carloni, Columbia University, US



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POWER, PERFORMANCE, AND THERMAL TRADE-OFFS IN MANYCORE ARCHITECTURES
Gaurav Narang, Washington State University, US

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Wenshuo Yue and Bonan Yan, Peking University, CN

ACTIVE ROOT-OF-TRUST ARCHITECTURES FOR LOW-END EMBEDDED SYSTEMS
Youngil Kim, University of California, Irvine, US

SYSTEMATIC DESIGN AND EFFICIENT AUTOMATED IMPLEMENTATION OF LOGIC LOCKING
Akashdeep Saha[1], Debdeep Mukhopadhyay[2] and Rajat Subhra Chakraborty[2], [1]New York University Abu Dhabi, AE; [2]IIT Kharagpur, IN

AGING PHENOMENA IN DIGITAL CIRCUITS: CHARACTERIZATION, MITIGATION AND EXPLOITATION
Andres Santana Andreo, Rafael Castro Lopez, Elisenda Roca and Francisco Fernandez, Instituto de Microelectrónica de Sevilla, IMSE, CNM (CSIC, Universidad de Sevilla), ES

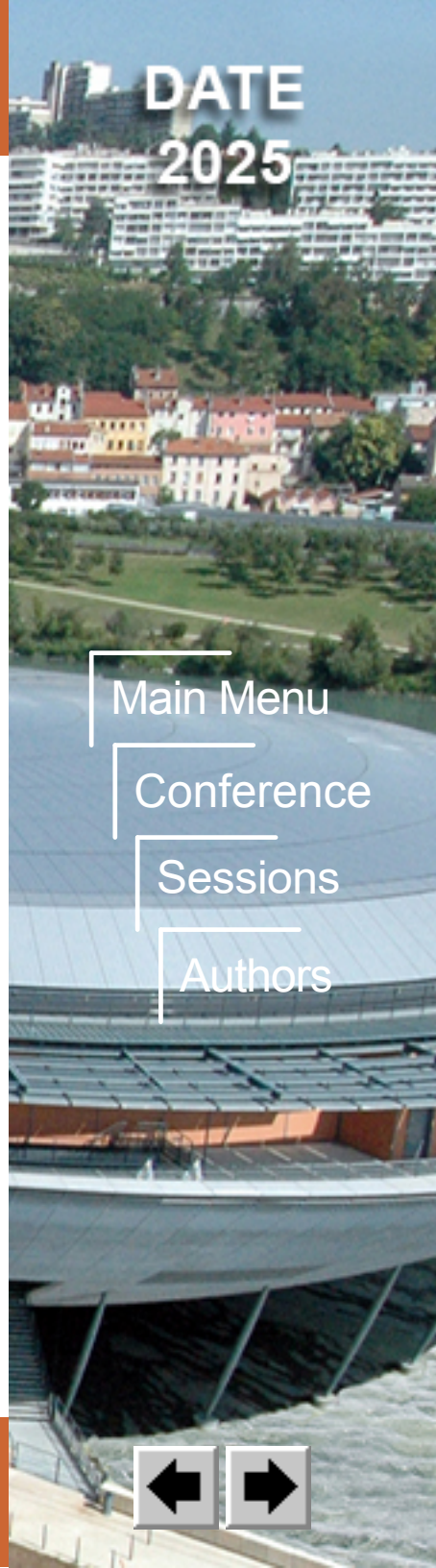
DIGITAL TWINS IN AIRCRAFT: MERGING CYBER-PHYSICAL SYSTEM AND HUMAN DECISION-MAKING
Francesco Biondani and Franco Fummi, Università di Verona, IT

FAULTY BEHAVIORS SIMULATION IN INDUSTRIAL CYBER-PHYSICAL SYSTEMS FOR SAFETY ANALYSIS
Francesco Tosoni, Università di Verona, IT

HIGH-PERFORMANCE AND FLEXIBLE HARDWARE ARCHITECTURES FOR FPGA-BASED SMARTNICS
Klajd Zyla and Andreas Herkersdorf, TU Munich, DE

THE ACCELERATION OF GAUSSIAN BELIEF PROPAGATION USING RECONFIGURABLE HARDWARE
Omar Sharif, Imperial College London, GB

DOMAIN-SPECIFIC BENCHMARKS AND ARCHITECTURES FOR APPLICATIONS USING GRAPH-BASED DATA
Andrew McCrabb and Valeria Bertacco, University of Michigan, US



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TOWARDS PERSONALIZED AI HEALTHCARE BACKED BY EMERGING TECHNOLOGIES
Ruiyang Qin and Yiyu Shi, University of Notre Dame, US
ENERGY-EFFICIENT MIXED-SIGNAL IN-SENSOR AND IN-MEMORY COMPUTING
Md Abdullah-Al Kaiser and Akhilesh Jaiswal, University of Wisconsin-Madison, US

PRINTED NEUROMORPHIC COMPUTING FOR ULTRA-RESOURCE-CONSTRAINED EDGE INTELLIGENCE
Priyanjana Pal and Mehdi Tahoori, Karlsruhe Institute of Technology, DE

ENERGY-EFFICIENT ACCELERATORS FOR ML APPLICATIONS WITH IMPROVED RRAM DEVICE LIFETIME
Neethu K[1], Rekha James[1] and Sumit Mandal[2], [1]School of Engineering, Cochin University of Science and Technology, IN; [2]Indian Institute of Science, IN

IMPLEMENTATION AND EVALUATION OF DIFFERENT STRATEGIES OF COUNTERMEASURES TO PROTECT A RISC-V CORE AGAINST BOTH SOFTWARE AND PHYSICAL ATTACKS
William Pensec[1], Vianney Lapotre[1] and Guy Gogniat[2], [1]Université Bretagne Sud, Lab-STICC, FR; [2]Université Bretagne Sud, FR

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Nils Quetschlich and Robert Wille, TU Munich, DE

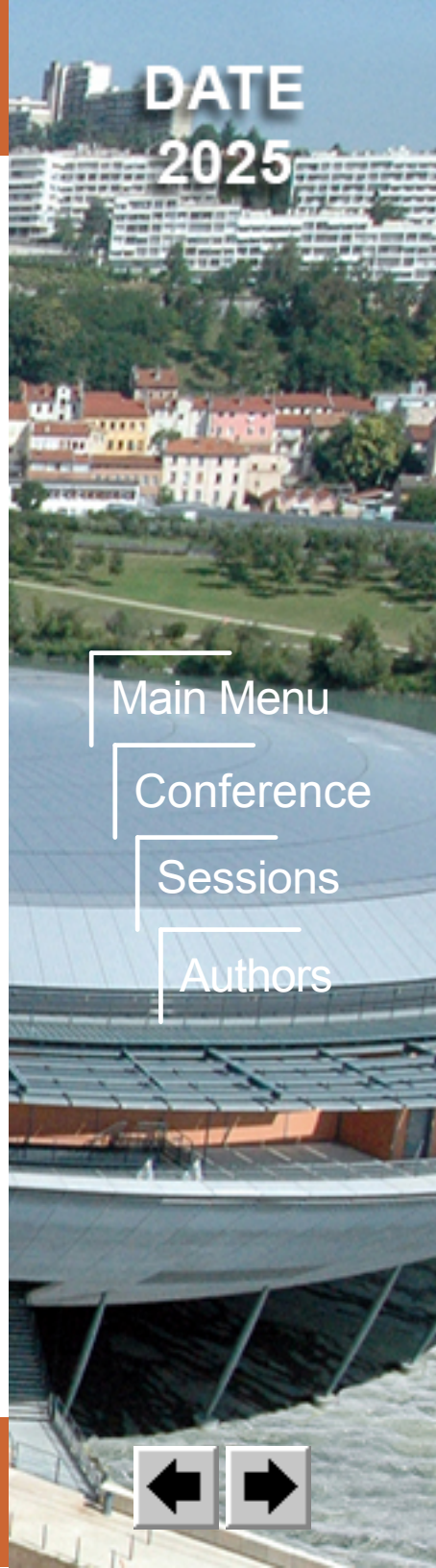
FAULT-TOLERANT CNN ACCELERATOR WITH RECONFIGURABLE CAPABILITIES
Rizwan Tariq Syed and Milos Krstic, Leibniz-Institut für innovative Mikroelektronik, DE

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Carmine Rizzi and Lana Josipovic, ETH Zurich, CH

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Michele Boldo and Nicola Bombieri, Università di Verona, IT

COLLECTIVE METHODOLOGIES FOR EFFICIENT HIGH-LEVEL SYNTHESIS
Aggelos Ferikoglou[1], Sotirios Xydis[1] and Dimitrios Soudris[2], [1]National TU Athens, GR; [2]National Technical University of Athens, GR

OPTIMIZATION OF A REMOTE MONITORING PLATFORM FOR EDGE DEVICES
Mirco De Marchi and Nicola Bombieri, Università di Verona, IT



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Milad Kokhazadeh[1], Georgios Keramidas[1,2] and Vasilios Kelefouras[3]
[1]Aristotle University of Thessaloniki, GR; [2]Think Silicon S.A., GR; [3]University of Plymouth, GB

POWER-EFFICIENT APPROXIMATE 4:2 COMPRESSORS FOR IMAGE MULTIPLICATION AND NEURAL NETWORKS
Vinicius Zanandrea and Cristina Meinhardt, Federal University of Santa Catarina, BR

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Bindu G Gowda and Madhav Rao, International Institute of Information Technology, Bangalore, IN

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Anjum Riaz and Satyadev Ahlawat, IIT Jammu, IN

OPEN-SOURCE DESIGN OF A LOW-POWER SNN HARDWARE ACCELERATOR FOR EDGE AI
Luca Martis and Paolo Meloni, Università degli Studi di Cagliari, IT

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Peer Adelt[1] and Achim Rettberg[2], [1]Hamm-Lippstadt University of Applied Sciences, DE; [2]Carl von Ossietzky University Oldenburg, DE

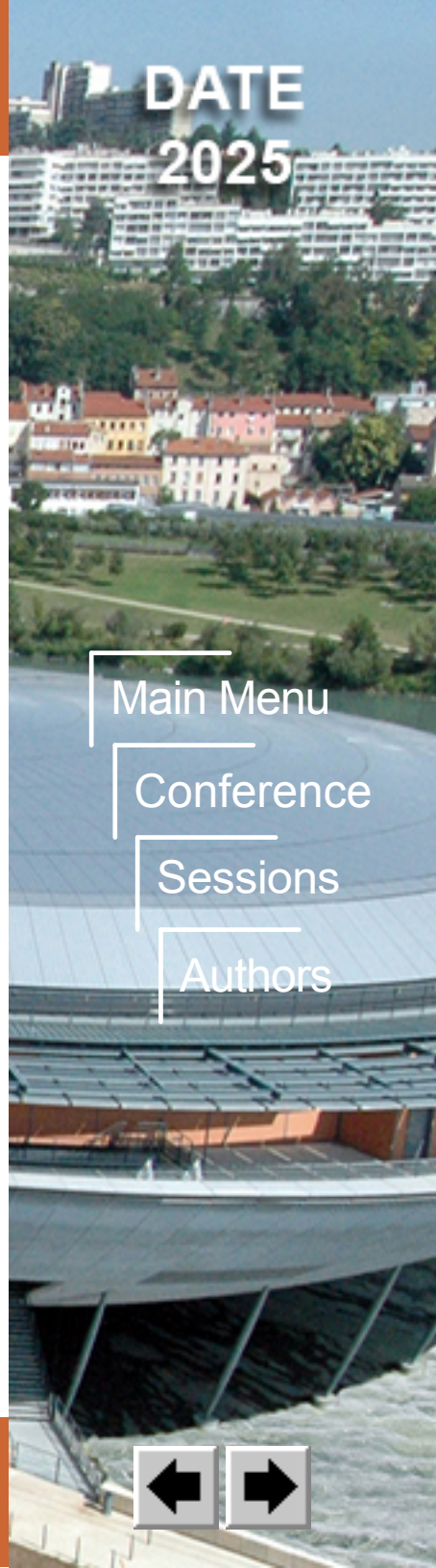
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Sumit Diware and Rajendra Bishnoi, TU Delft, NL

OPTIMIZING LEARNING THROUGH CO-DESIGN IN NEUROMORPHIC COMPUTING
Lakshmi Varshika M and Anup Das, Drexel University, US

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Surendra Hemaram, Karlsruhe Institute of Technology, DE

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Lars Folkerts, University of Delaware, US



Conference Information

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Johnny Rhe and Jong Hwan Ko, Sungkyunkwan University, KR

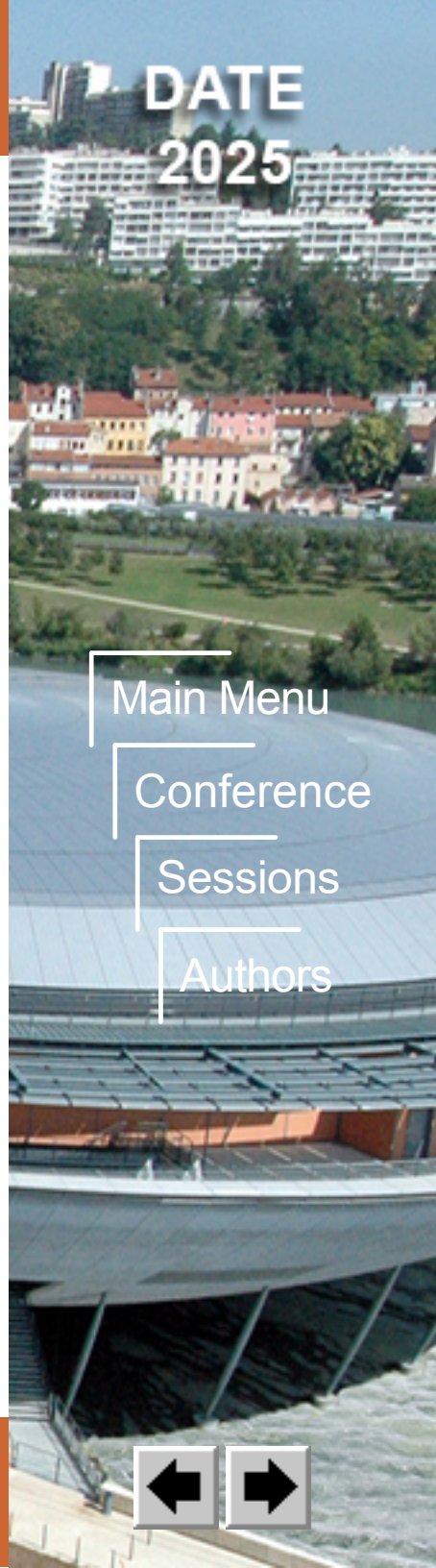
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Veera Venkata Ram Murali Krishna Rao Muvva, University of Nebraska Lincoln, US

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Conference Information

DATE 2025 MEDIA PARTNERS

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62 THE CHIPS TO SYSTEMS CONFERENCE

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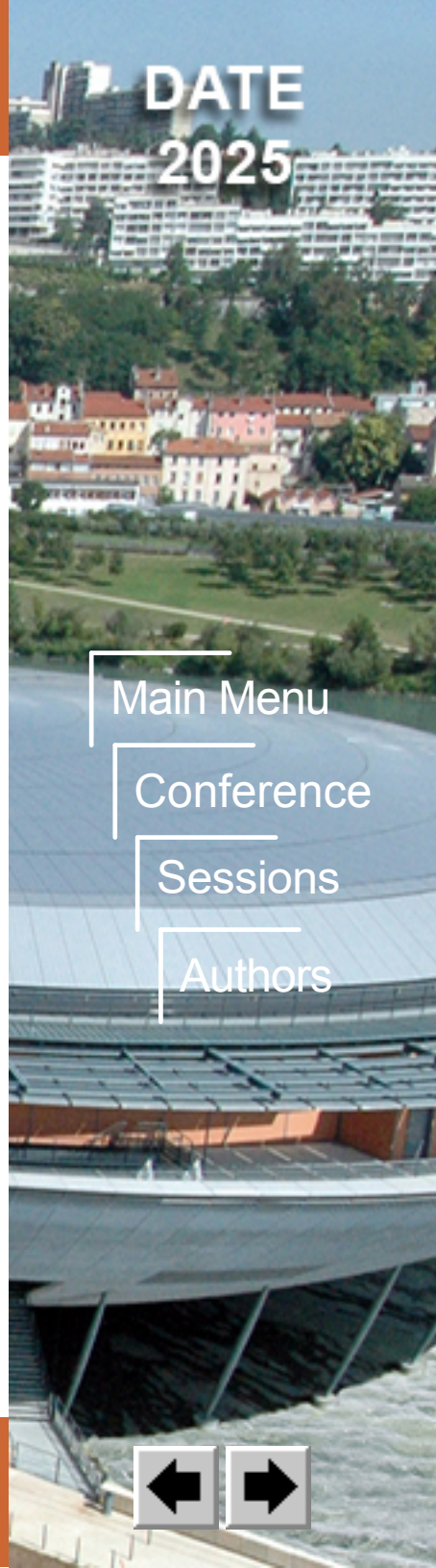
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Keynotes

DATE 2025 Opening Keynotes

Date: Monday, 31 March 2025
Time: 09:00 - 09:45 CET

Opening Keynote 1: Towards greener electronics and a 1000x gain in energy efficiency: co-optimizing innovative IC architectures, disruptive CMOS technologies and new EDA tools.

Jean-René Lèquepeys (CEA-Leti, FR)

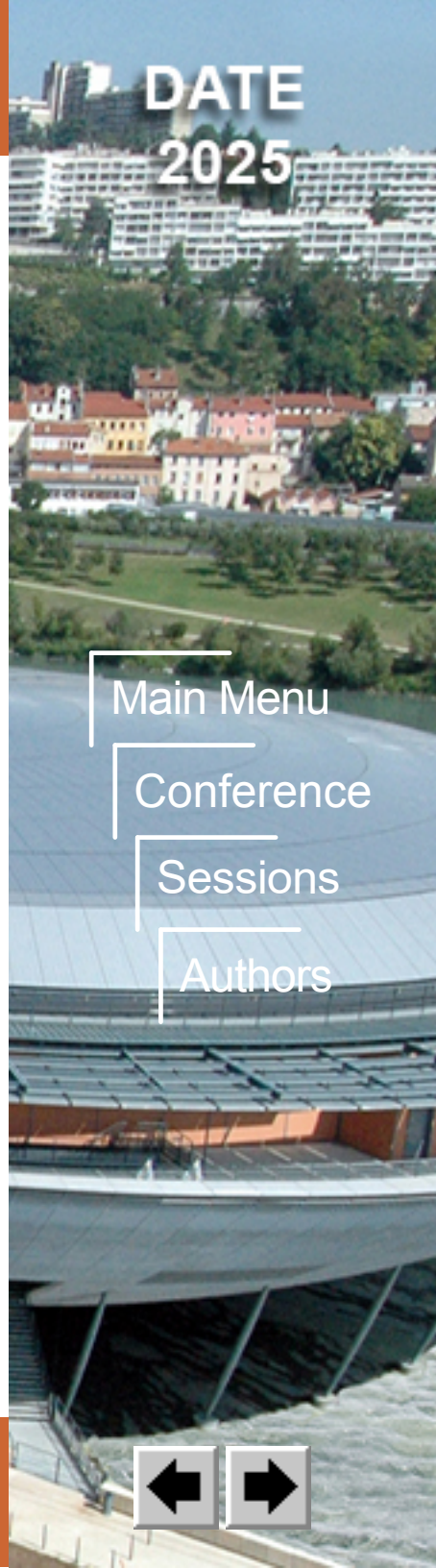
Abstract : *Semiconductors and chips are ever-present in our current digital world. From smart sensors and the industrial Internet of Things to Digital Cities, personalized Medecine, Precision Agriculture, Vehicle Automation, and Cloud & High Performance Computing, semiconductor applications cover a very wide spectrum of society's needs. However, global warming is highlighting the social and environmental impact of the digital transition, and the complex trade-offs and choices that lie ahead if we are to build a sustainable world. How do we pursue digitalization taking into account a limited power budget and the planetary limits? How do we make greener choices in the face of ever-increasing/aggressive competition? How do we choose the right digital performance for each application instead of a one-size-fits-all scenario, with a best performance for all approach? The semiconductor ecosystem is indeed facing a difficult dilemma with complex key tradeoffs.*

With these stakes clearly in mind, the semiconductor community is performing disruptive research to provide greener electronics, able to attain very large gains in energy efficiency and just the right performance for each application. With the help of AI-boosted design methodologies and CAD tools, we have set out to co-optimize innovative CMOS technologies, disruptive chip architectures, computing models with new algorithms for embedded software.

This paper will provide an overview of the global semiconductor landscape and the challenge of mastering the data deluge for the entire semiconductor ecosystem. In order to face this challenge, we must all work together to reduce the collection, transport and storage of fruitless data.

This keynote will spend some time describing recent results from CEA-Leti and CEA-List's research on sustainable and greener technologies.

To conclude, I will present an overview of the European Chips Act initiative, with the launch of the pilot lines, the Design Platforms and Competence Centers, a pan-European program that will be driving key milestones in the next five years to accelerate the accomplishment of our common goal of a sustainable and sovereign digital Europe.



Conference Information

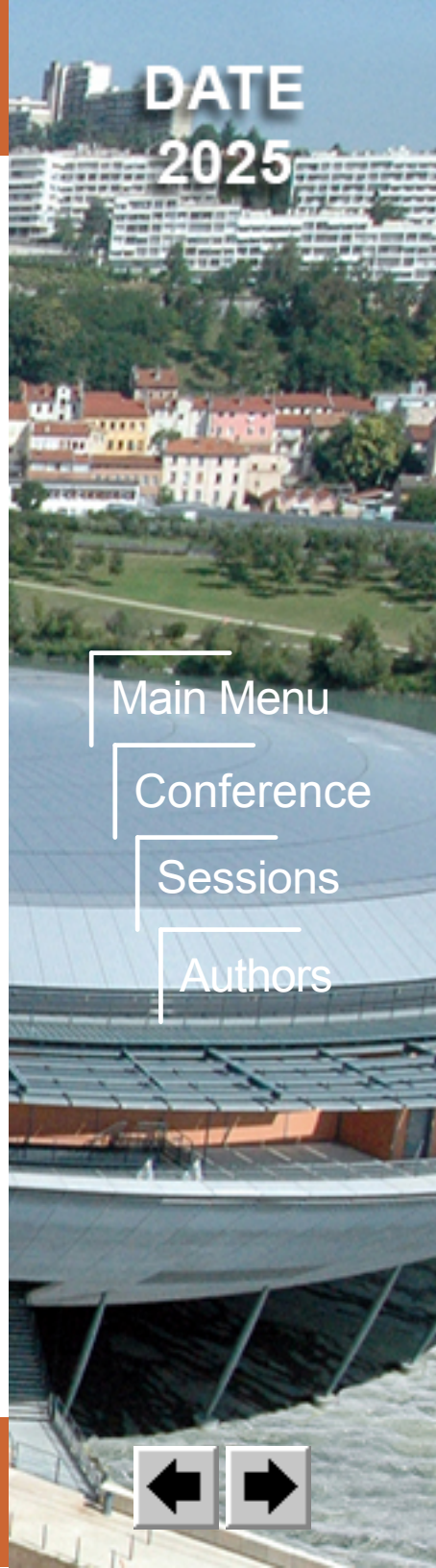
Date: Monday, 31 March 2025
Time: 09:45 - 10:30 CET

Opening Keynote 2: A Vision of Systems and Technology in a Connected Europe

Giovanni de Micheli, EPFL, Switzerland

Abstract: The unprecedented growth of electronic system applications, from AI to smart products, creates both a huge market opportunity and a deep need for talented engineers. Europe will play a dominant role in the thirties if we (i.e., our community) can set up the premises for such a technology expansion now. Whereas the European Chip Act is an important enabler, finance represents only one of the necessary conditions for success. The key aspect is the ability to leverage diverse competences and connect the partially-untapped energies of the various European players, ranging from Industry to Academia.

Europe's strength stems from diversity and the ability to design complex systems from parts, possibly coming from various sources. The 'value added' comes from the engineers who can create functionality and services, and who can adapt it to a diverse market of consumers. Yet I argue that this precious resource, the human capital represented by engineers and technologists, is too scarce and its limitation in size is a main handicap for creating a strong market of intelligent products and services. Education of engineers has to evolve and concentrate on the broader issue of system problem solving based on a deep understanding of technology. Industry has to join forces with academia by sharing knowledge and objectives and by creating a strong enthusiasm for engineering.



Conference Information

DATE 2025 Lunchtime Keynotes

Date: Monday, 31 March 2025
Time: 13:15 - 14:00 CET

IEEE CEDA Lunchtime Panel: on the occasion of CEDA 20th anniversary: Electronic Design Automation: the past and the future

Georges Gielen (moderator), David Atienza, Luca Benini, Valeria Bertacco

Abstract: *In celebration of IEEE CEDA's 20th anniversary, this panel discusses the role of electronic design automation (EDA) in designing today's multi-billion-transistor chips. With CMOS technology scaling approaching the range of a few nanometer and chips going 3D, what design techniques and tools will be needed to design these future integrated systems? Or will other technologies pop up and dominate? Where are the challenges? Who will provide the solutions? Will it be open source?*

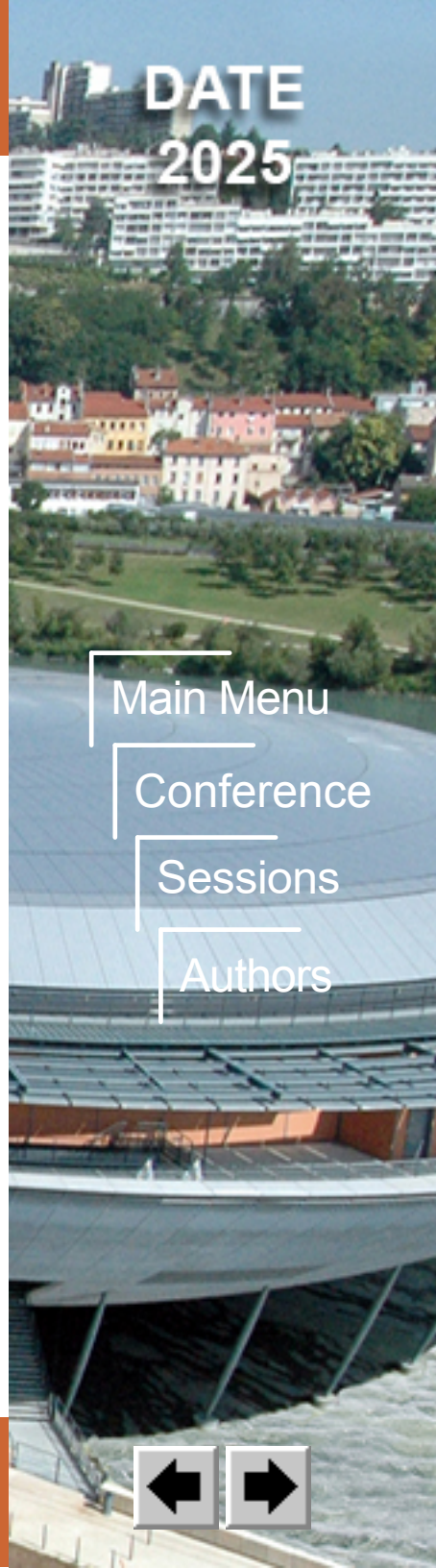
Join us for this special IEEE CEDA anniversary panel to discuss these questions and share your insights.

Date: Tuesday, 1 April 2025
Time: 13:15 - 14:00 CET

ASD Lunchtime Keynote: AI/ML at the Forefront of Semiconductor Evolution: Enhancing Design, Efficiency, and Performance

Yankin Tanurhan, Synopsis, United States

Abstract: *As artificial intelligence (AI) and machine learning (ML) drive innovation, their impact on the semiconductor market is transformative. This keynote will explore the latest AI/ML trends and their implications for SoC designs targeting high-performance compute, edge AI, and IoT applications. The presentation will cover AI/ML's role in developing next-generation semiconductor designs, including how AI/ML algorithms are incorporated into EDA tools to optimize chip design and enable efficient verification and manufacturing. Emerging AI/ML trends driving requirements for advanced neural processing units (NPU) will be explored, including generative AI applications like large language models and text-to-image generators. Finally, the role of transformer-based neural networks in implementing energy-efficient SoCs will be discussed.*



Conference Information

Date: Wednesday, 2 April 2025
Time: 13:15 - 14:00 CET

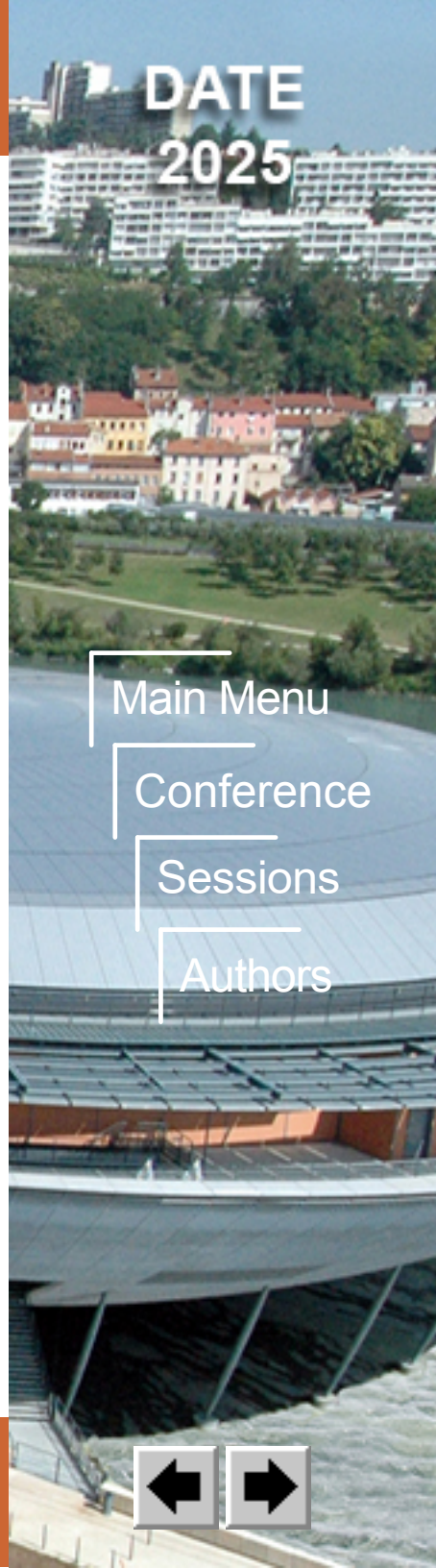
Special Day Emerging Computing Paradigms Lunchtime Keynote: Neuromorphic Computing at Cloud Level

Christian Mayr, TU Dresden, Germany

Abstract: AI is having an increasingly large impact on our daily lives. However, current AI hardware and algorithms are still only partially inspired by the major blueprint for AI, i.e. the human brain. In particular, even the best AI hardware is still far away from the 20W power consumption, the low latency and the unprecedented large scale, high-throughput processing offered by the human brain.

In this talk, I will describe our bio-inspired AI hardware, in particular our award-winning SpiNNaker2 system, which achieves a unique fusion of GPU, CPU, neuromorphic and probabilistic components. It takes inspiration from biology not just at the single-neuron level like current neuromorphic chips, but throughout all architectural levels.

On the algorithm front, I will give examples on how to use general neurobiological computing principles (hierarchy, asynchronity, dynamic sparsity and distance-dependent topologies/hierarchical computing) to reframe conventional AI algorithms, usually achieving an order of magnitude improvement in energy-delay product.



Conference Information

About DATE

DATE is a leading international event providing unique networking opportunities, bringing together designers and design automation users, researchers and vendors, as well as specialists in hardware and software design, test and manufacturing of electronic circuits and systems.

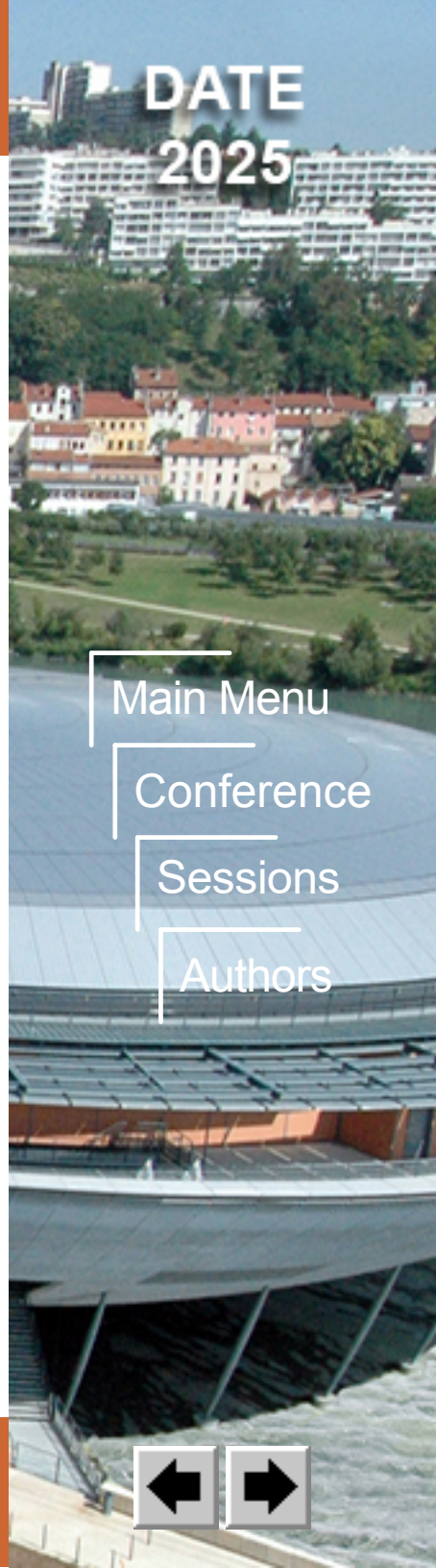
The DATE 2025 conference, which is in its 28th edition, will be held at the at the Centre de Congres de Lyon, France, from 31 March to 2 April 2025, and will be chaired by Aida Todri-Sanial, Eindhoven University of Technology, NL.

DATE 2025 offers an intensive three-day format, focussing on interaction and further strengthening of our already tight-knit community. The vast majority of regular papers will be presented in technical sessions using short flash-presentations, where the emphasis is on embedded poster-supported live interactions (in addition to common full-length presentation videos available before, during and after the conference). By using this format, we make sure that the attendees can actually spend their time doing what conferences are truly about: meeting, discussing and exchanging ideas.

Besides a record number of technical paper presentations, this year‘s DATE programme includes a large variety of other interesting events: Focus sessions on hot topics, Late Breaking Results sessions on breakthrough approaches and new research directions, Unplugged sessions with discussions around the “unconventional computing” theme, embedded workshops as well as embedded tutorials, multi-partner project sessions, and the Young People Programme to support PhD students with their career development including HackTheSilicon DATE and SoC Lab half-day events. Moreover, the programme also features the by now traditional Special Initiative on Autonomous Systems Design as well as two Special Days with, respectively, “Emerging Computing Paradigms“ and “AI and ML Trends“ as themes.

Lyon, France's third-largest city, is a captivating blend of history and modernity nestled at the confluence of the Rhône and Saône rivers. With a rich heritage dating back to Roman times, Lyon boasts an impressive array of architectural styles, from ancient Roman ruins to Renaissance-era traboules, the iconic Basilique Notre-Dame de Fourvière and contemporary designs in the Confluence district. The city is renowned for its gastronomic excellence, earning the title of the capital of French cuisine. With over 4000 restaurants ranging from traditional bouchons to Michelin-starred establishments, Lyon continues to innovate and redefine culinary tastes. Lyon's cultural scene is vibrant and diverse, featuring numerous museums, including the Lumière Museum, which celebrates the city's role in the birth of cinema. The city hosts various events throughout the year, such as the Biennial Contemporary Art and Dance festivals.

At the heart of Lyon's business and event hosting capabilities lies the Lyon Convention Centre, located in the Cité Internationale district. This prestigious venue, designed by renowned architect Renzo Piano, offers 24000m² of modular space, including three auditoriums with capacities of 300, 900, and 3000 seats. The centre also features



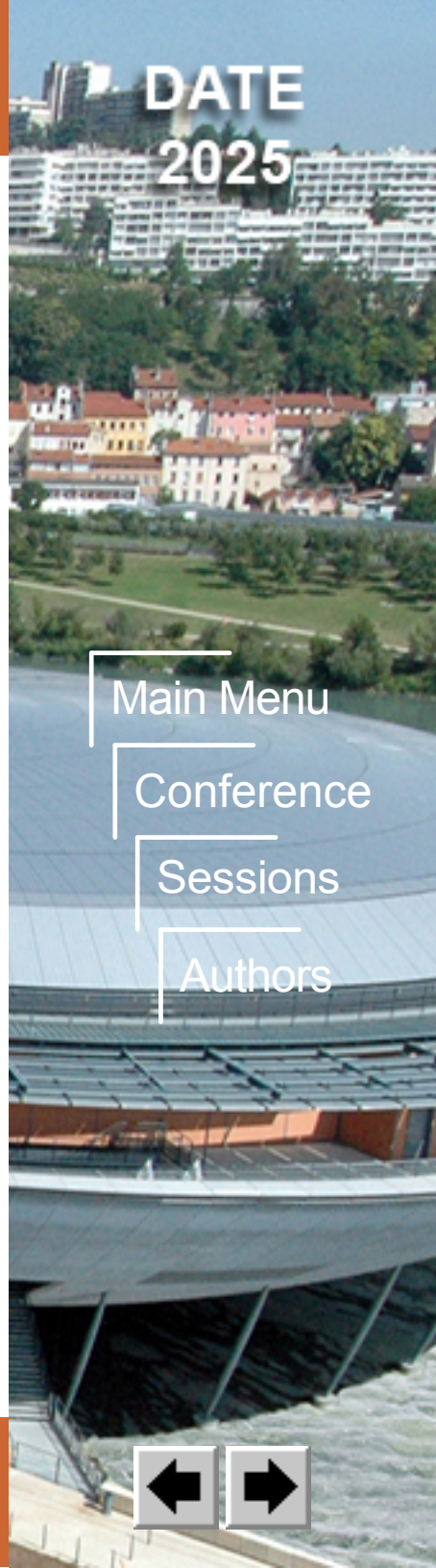
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35 meeting rooms accommodating between 50 and 450 people, and a versatile 8400m² space perfect for various events. The Lyon Convention Centre's standout feature is its unique L'Amphithéâtre 3000, inspired by ancient Gallo-Roman constructions, featuring a 180° semi-circular hall opening onto the stage area. This world-class facility hosts over 200 events annually, including major international conferences such as DATE.

Lyon's prowess in business tourism is evident in its rankings. In 2024, it was ranked as the second French destination and 30th worldwide for congress organization by the International Congress & Convention Association. The city's commitment to responsible tourism also earned it the 15th position globally in the Global Destination Sustainability Index. As Lyon prepares to celebrate the 130th anniversary of the world's first film shot in the city in 2025, it continues to attract global attention. Condé Nast Traveler has selected Lyon as one of the must-visit European cities for 2025, further cementing its status as a leading destination for both leisure and business travellers.

Join us in celebrating another exciting edition of the DATE conference – the top scientific event in Design, Automation, and Test of microelectronics and embedded systems for the academic and industrial research communities worldwide!

Updated information about the conference is always available online at:
https://www.date-conference.com/



Conference Information

Call for Papers

Design, Automation and Test in Europe Conference

The European Event for Electronic System Design & Test

Scope of the Event

The 29th DATE conference is the main European event bringing together designers and design automation users, researchers and vendors as well as specialists in hardware and software design, test and manufacturing of electronic circuits and systems. DATE puts strong emphasis on both technology and systems, covering ICs/SoCs, emerging technologies, embedded systems and embedded software.

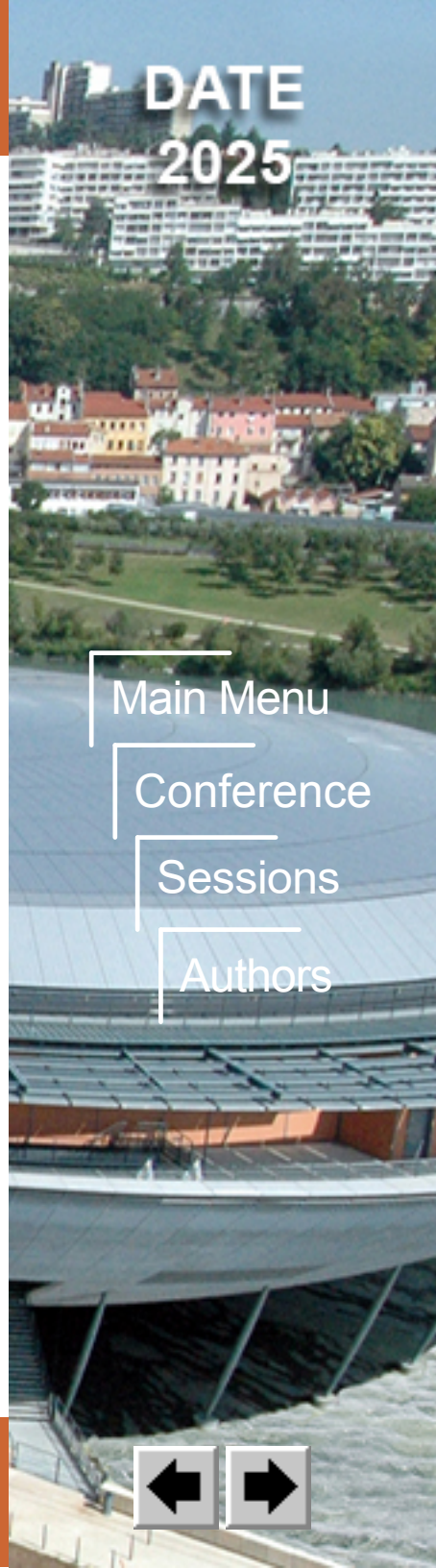
Structure of the Event

The multi-day event consists of a conference with keynote talks, regular papers, panels, hot-topic sessions, tutorials, workshops, special focus days and a track for executives. The organisation of user group meetings, fringe meetings, a Young People Programme, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design automation, design and test communities. Special space will also be allocated for multi-partner innovative research projects to show their results. More details will be available on the DATE website: http://www.date-conference.com.

Areas of Interest

Within the scope of the conference, the main areas of interest are: design automation, design tools and hardware architectures for electronic and embedded systems; test and dependability at system, chip, circuit and device level for analogue and digital electronics; modelling, analysis, design and deployment of embedded software and cyber-physical systems; application design and industrial design experiences. Topics of interest include, but are not restricted to:

- Quantum Computing Solutions
- System-level design methodologies and high-level synthesis
- System simulation and validation
- Design and test for analogue and mixed-signal circuits and systems, and MEMS
- Design and test of hardware security primitives
- Design and test of secure systems
- Formal methods and verification
- Network on chip and on-chip communication
- Architectural and microarchitectural design
- Low-power, energy-efficient and thermal-aware design
- Approximate computing
- Reconfigurable systems
- Smart Society and Digital Wellness
- Secure Systems, Circuits and Architectures
- Autonomous Systems and Smart Industry
- Applications of Emerging Technologies
- Applications of Artificial Intelligence Systems
- Applications of Emerging Technologies
- Modelling and mitigation of defects, faults, variability, and reliability
- Test generation, test architectures, design for test, and diagnosis
- Dependability and system-level test
- Embedded software architecture, compilers and tool chains
- Real-time, dependable and privacy-enhanced systems



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- Logical analysis and design
- Physical analysis and design
- Emerging design technologies for future computing
- Emerging design technologies for future memories
- Power-efficiency and Smart Energy Systems for Sustainable Computing
- Machine learning solutions for embedded and cyber-physical systems
- Design methodologies for machine learning architectures
- Design modelling and verification for embedded and cyber-physical systems

Submission of Papers

All papers must be registered by mid-September 2025

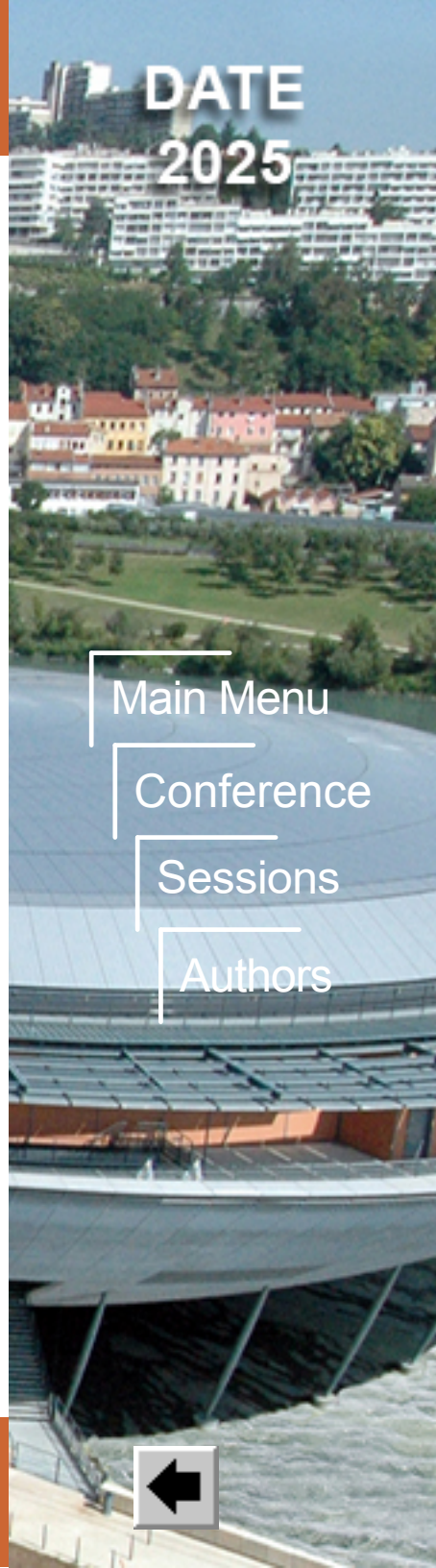
Chairs

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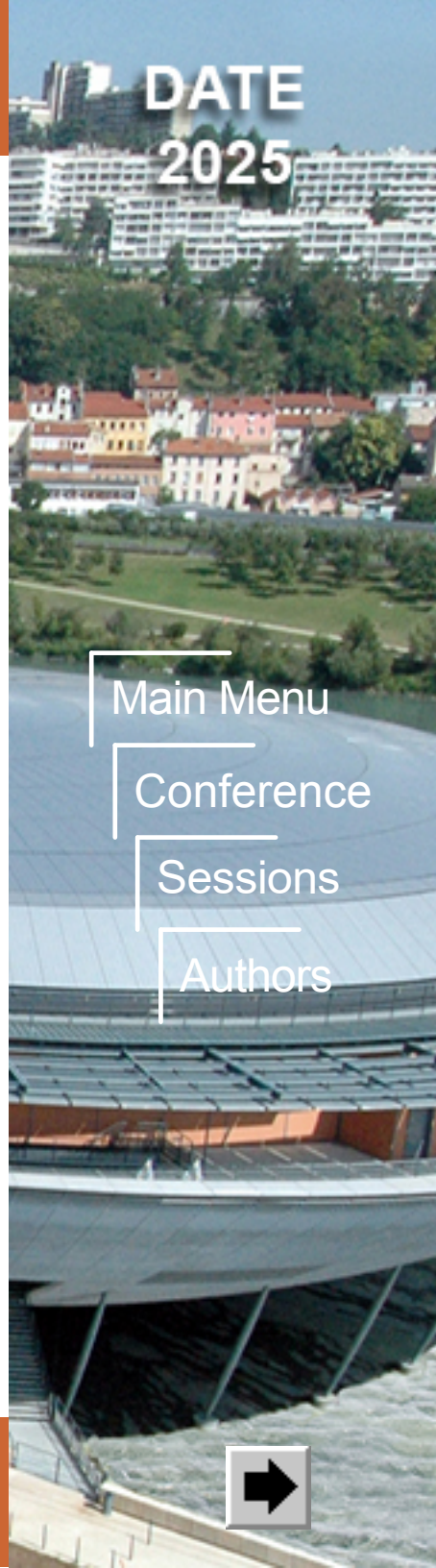


Conference

Sessions

- Focus Session - Specifications Mining in a World of Generative AI: Extensions, Applications, and Pitfalls
- BPA Session 1
- Emerging Design Technologies for Future Computing
- Secure Systems, Circuits, and Architectures
- ASD Technical Session: Enhancing Dependability and Efficiency in Automotive and Autonomous Systems
- BPA Session 2
- Embedded Software Architecture, Compilers and Tool Chains
- ASD Focus Session: Cybersecurity Challenges of Autonomous Systems
- Focus Session - Design Automation for Physical Computing Systems
- BPA Session 3
- Emerging Design Technologies for Future Memories

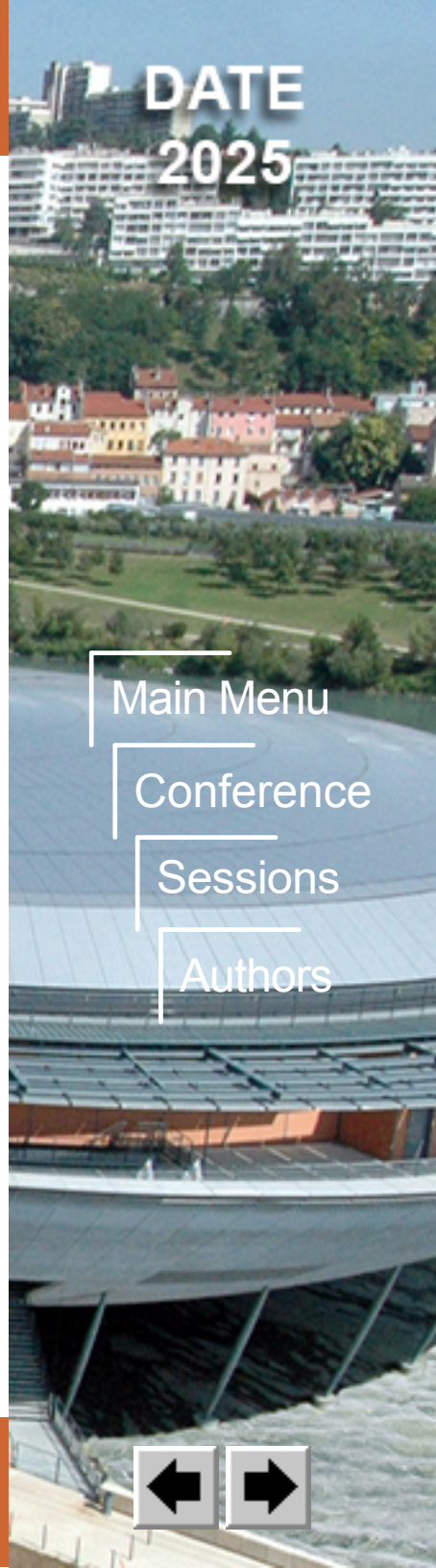
Click on a session for a list of papers



Conference

- System-Level Design Methodologies and High-Level Synthesis
- ASD Focus Session: Dynamic, Multi-Agent Sensing-to-Action Loops in Distributed Autonomous Edge Computing Systems: Opportunities and Challenges
- Focus Session - 3D Integration, Cryogenic Circuits and Superconducting Logic: Emerging Trends Shaping the Future of High-Performance Computing
- BPA Session 4
- Design Automation for Quantum Computing
- Applications of Emerging Technologies
- ASD Regular Session: Novel Safety Metrics, Adaptive Patterns for Resilience, and Legal Frameworks in Autonomous Systems Design
- Focus Session: Improving Chip Design Enablement for Universities in Europe
- Design Methodologies and Applications for Machine Learning
- Low-Power, Energy-Efficient and Thermal-Aware Design
- Applications of Artificial Intelligence Systems

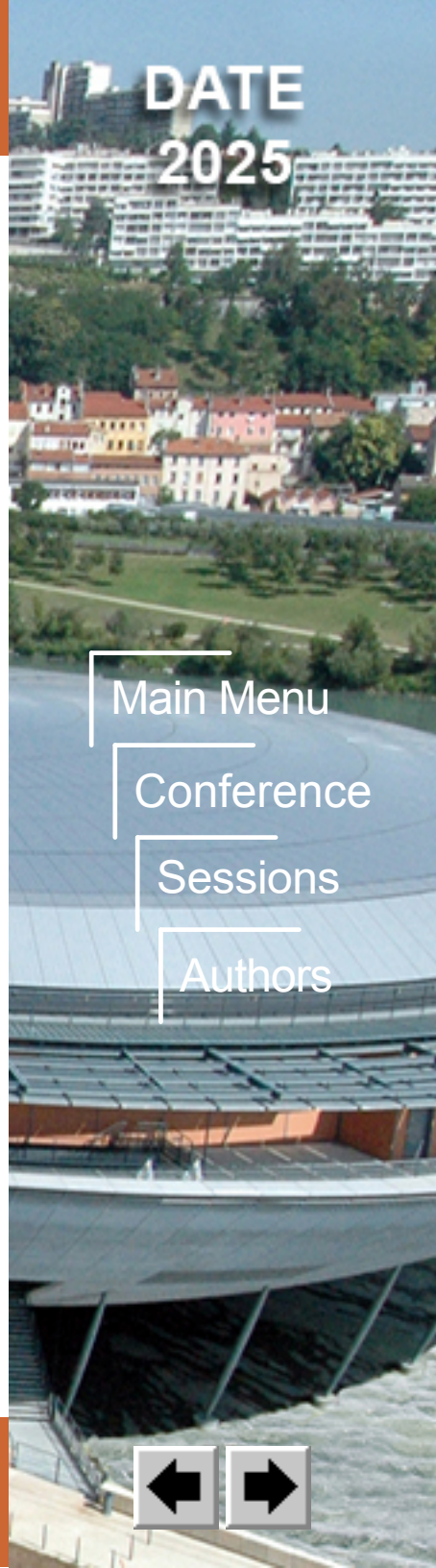
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Conference

- Driving KDT JU Initiative towards the Chips Act Multi-Partner Projects
- ASD Focus Session: Teleoperation as a Step Towards Fully Autonomous Systems
- Focus Session - GenAI-Native EDA: Redifining Verification with Large Language Models
- Architectural and Microarchitectural Design - 1
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- Embedded, Real-Time and Dependable Systems
- Architectural and Microarchitectural Design - 2
- Power and Energy Efficient Systems
- Design, Test, Modeling and Mitigation of Defects and Faults
- System Simulation and Validation

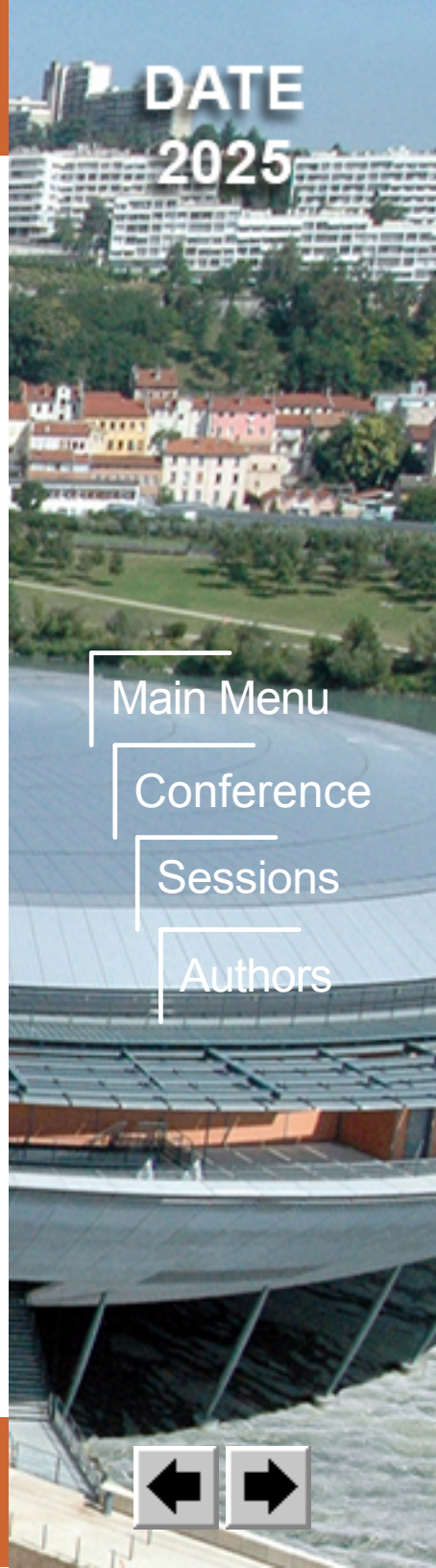
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Conference

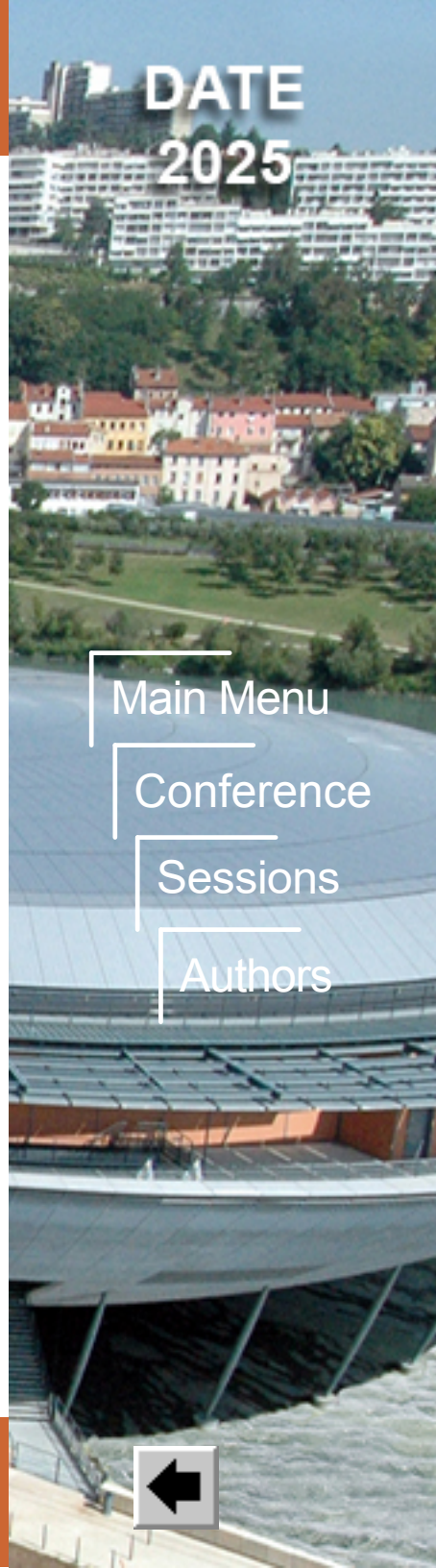
- Machine Learning Solutions for Embedded and Cyber-Physical Systems
- Design and Test of Secure Systems
- Late Breaking Results on AI Algorithms And Architectures
- Physical Analysis and Design
- Design Methodologies for Machine Learning Architectures
- Design and Test of Hardware Security Primitives
- Reconfigurable Systems
- Multi-Partner Projects
- Focus Session - Designing Secure Space Systems
- Logical Analysis and Design
- Design and Test for Machine Learning and Machine Learning for Design and Test
- Design and Test for Analog and Mixed-Signal Circuits / Systems / MEMS
- Design for On-Chip Interconnects
- Test and Verification for Dependability

Click on a session for a list of papers



Conference

- Approximate Computing Solutions
- System Level Design and Test, Modeling and Verification
- Emerging Design Technologies
- Late Breaking Results



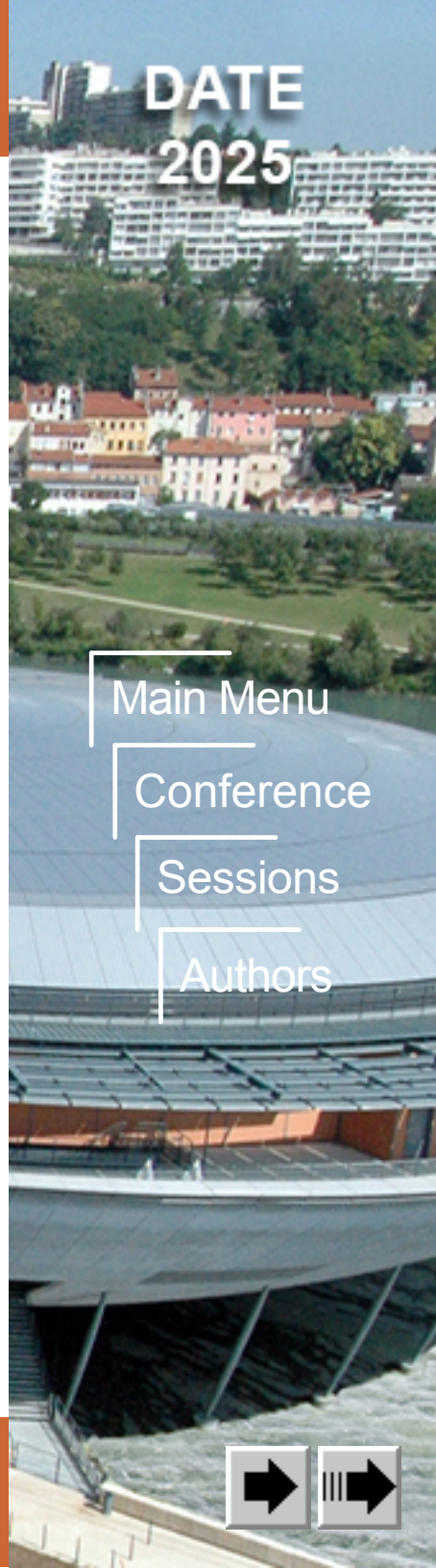
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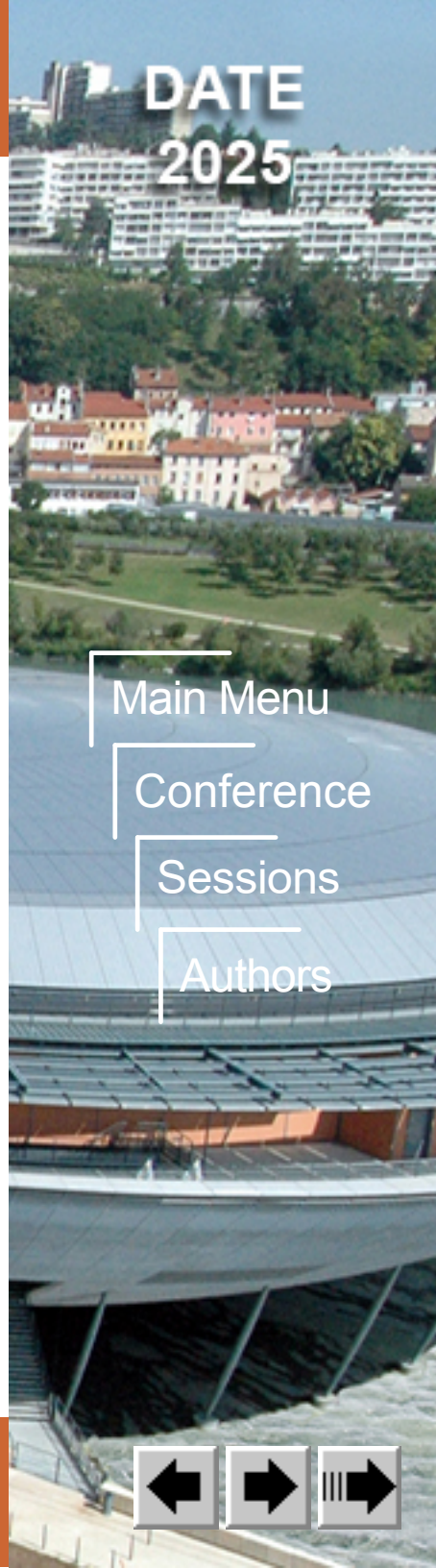
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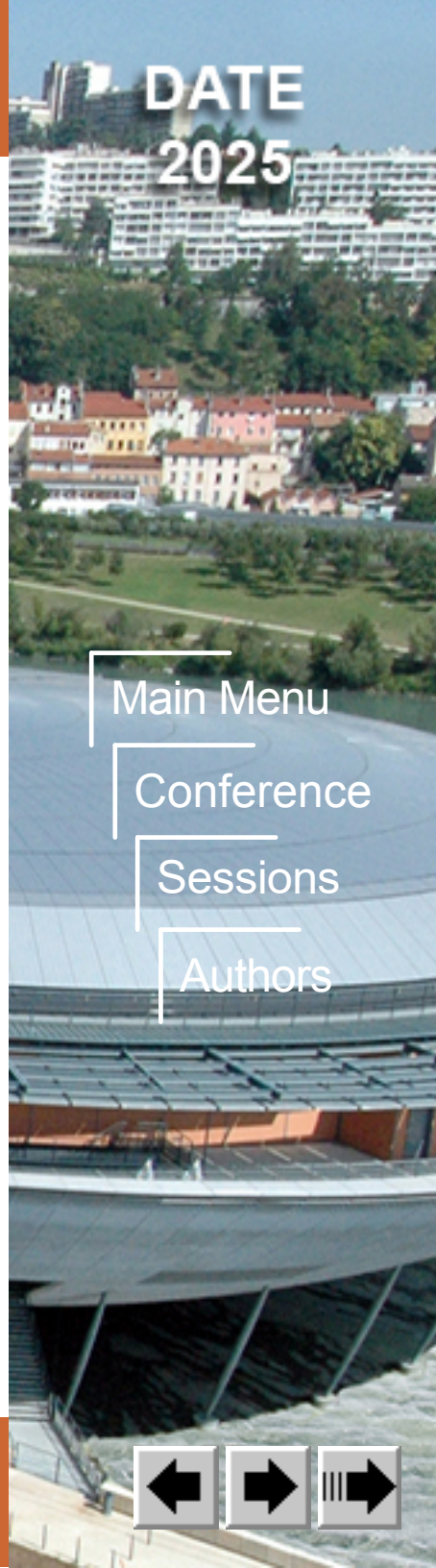


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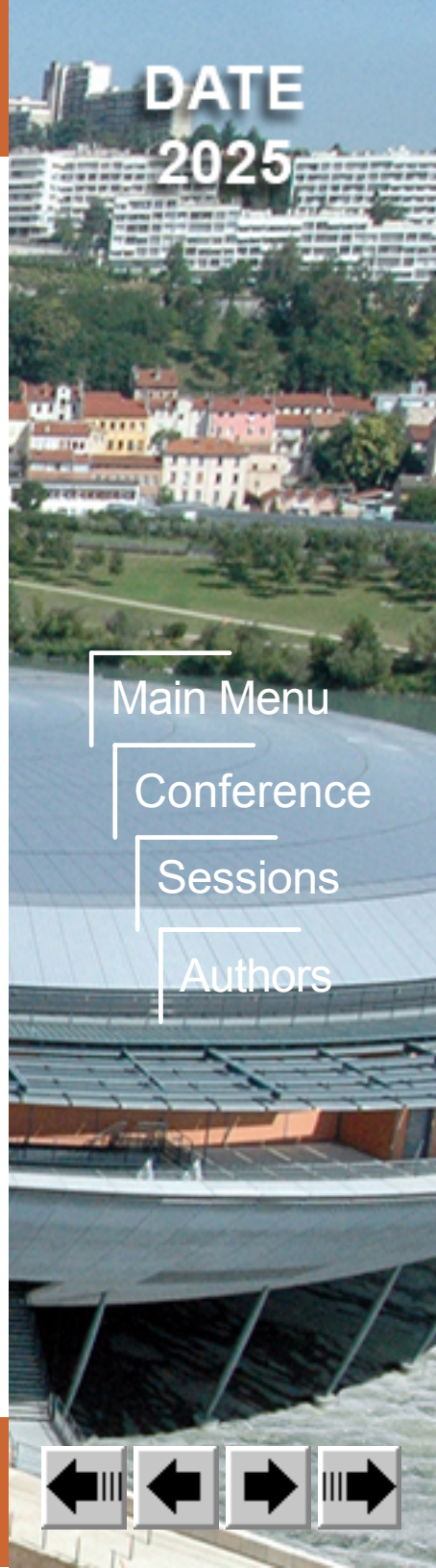
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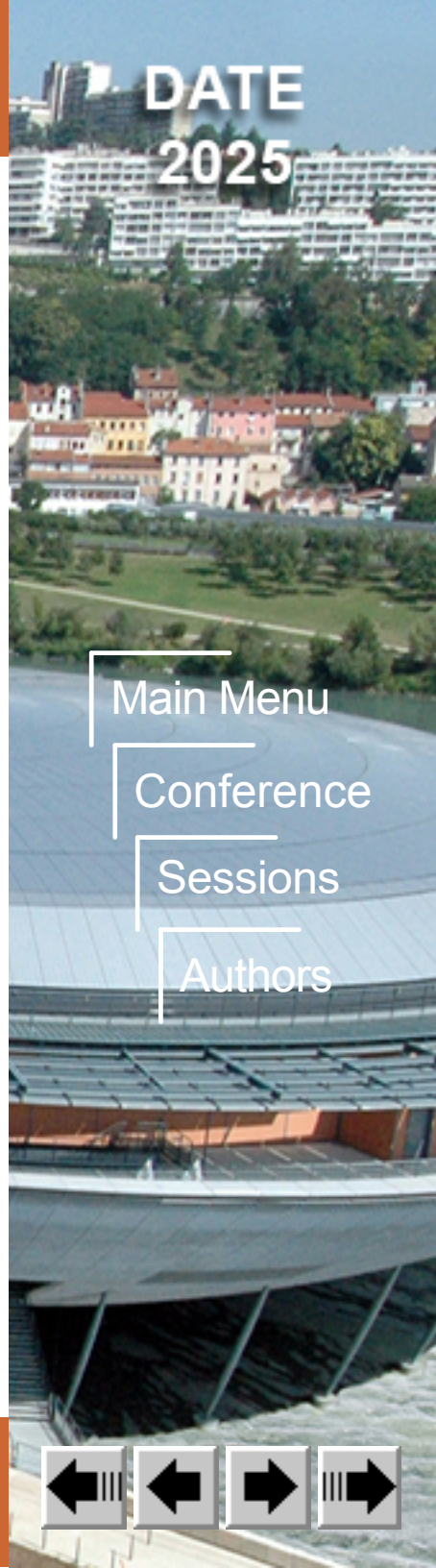
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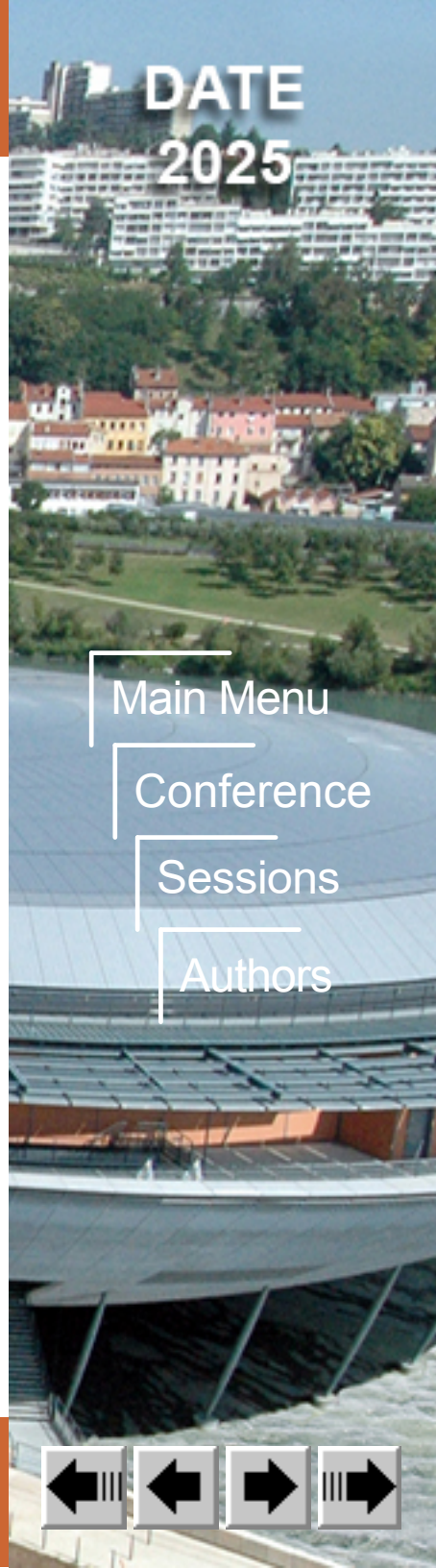


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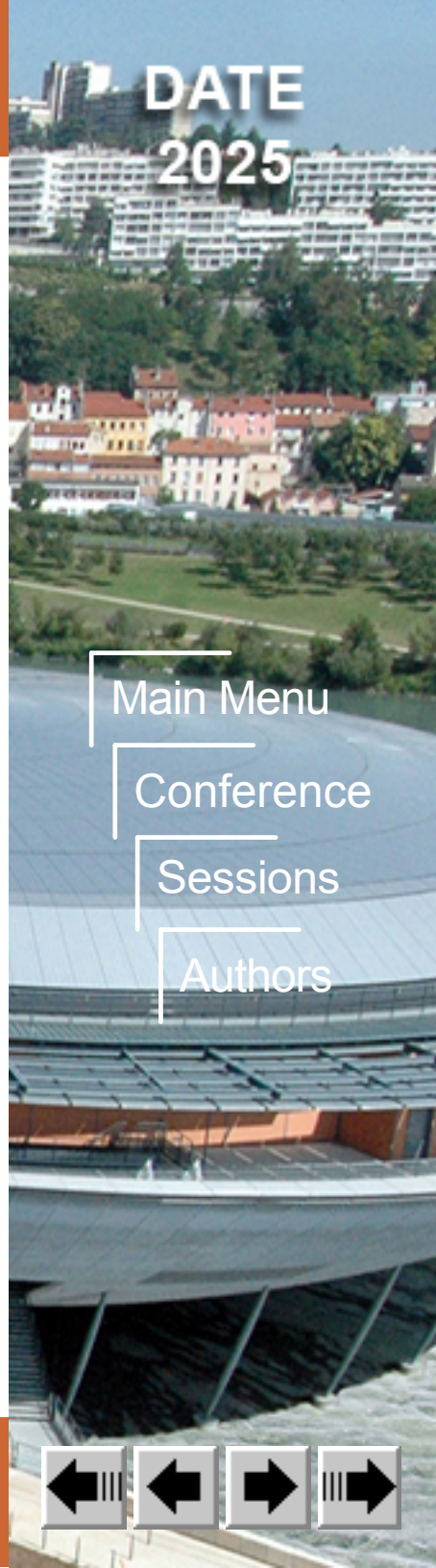
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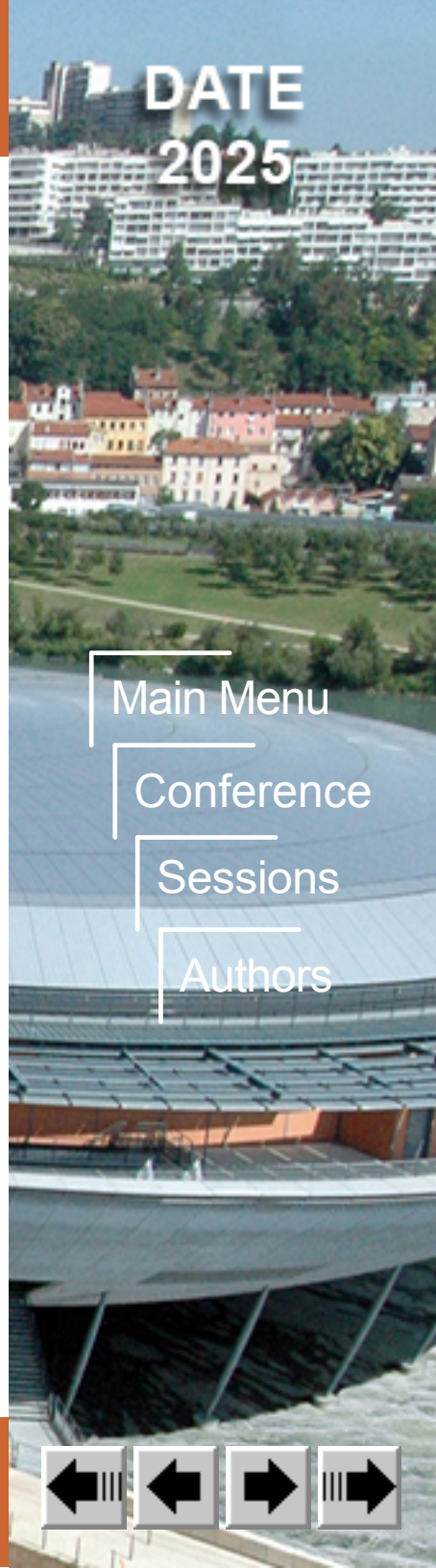


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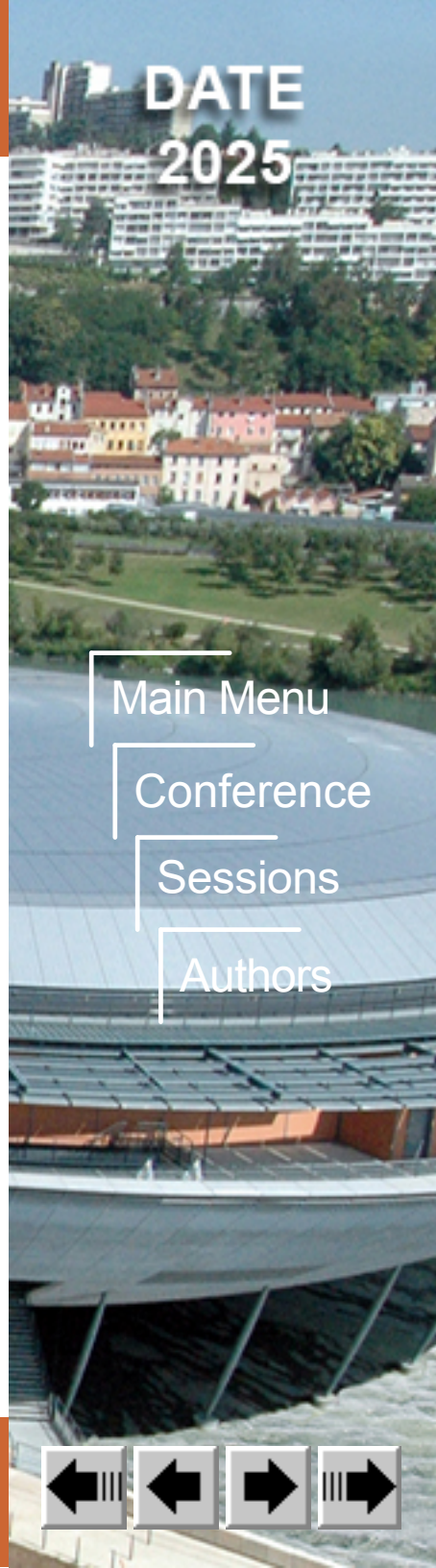


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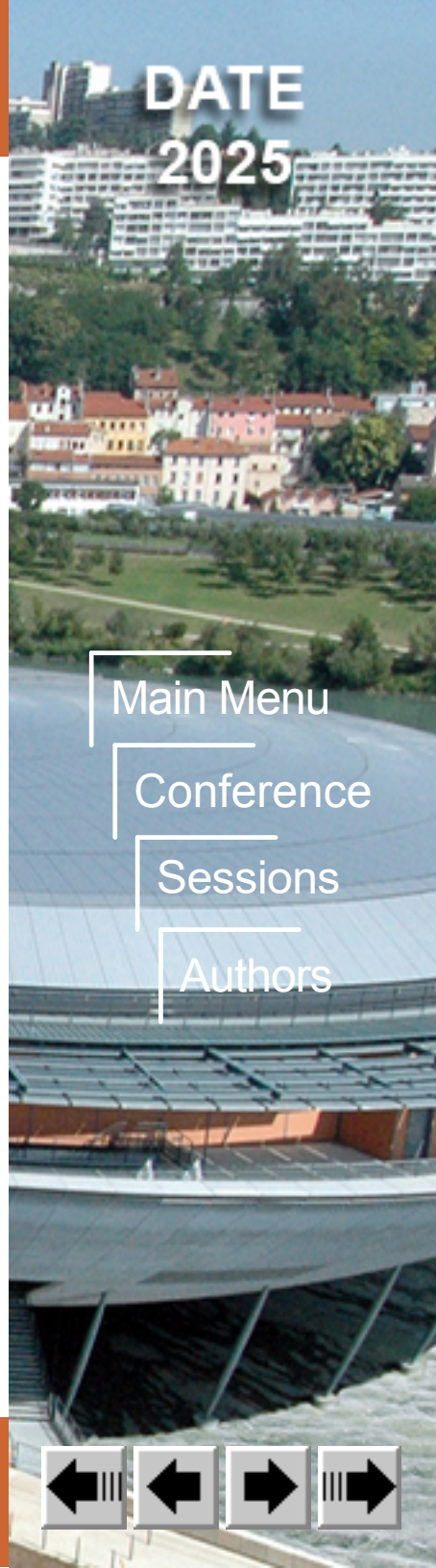


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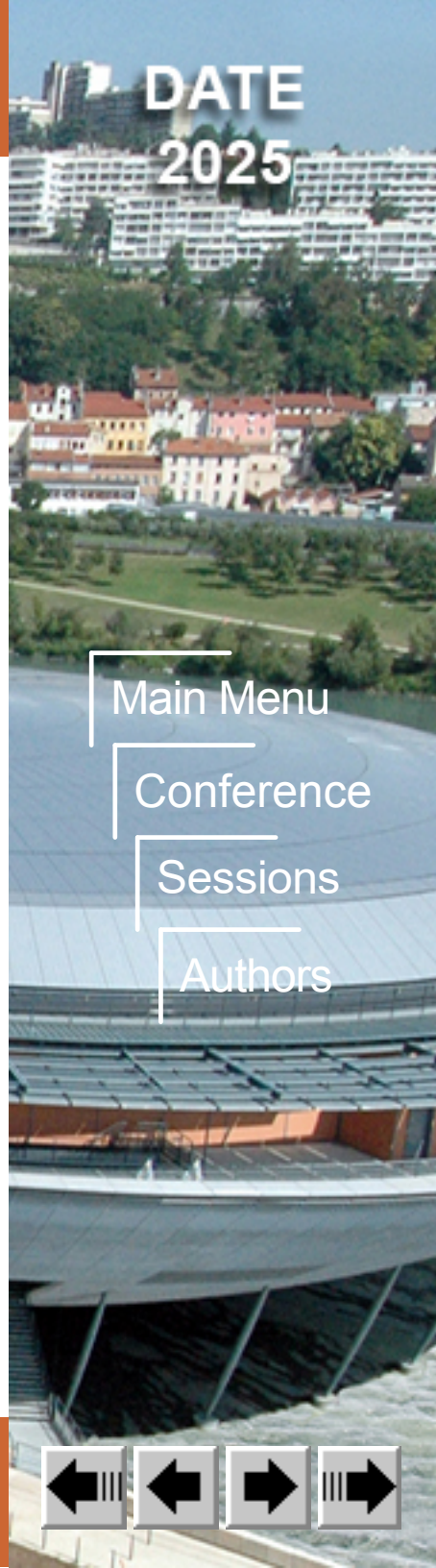
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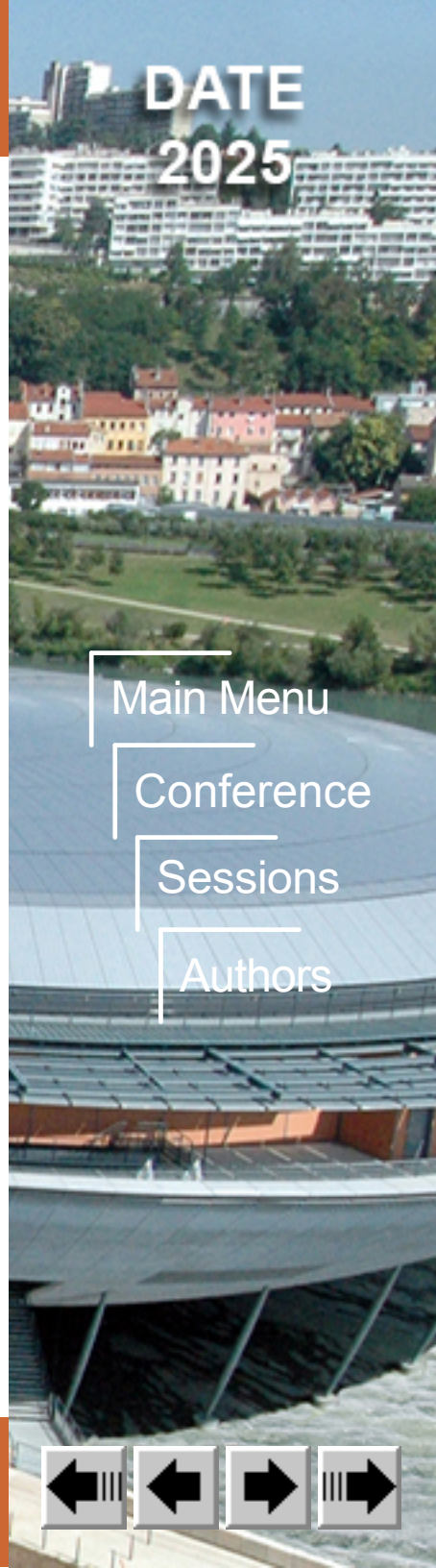


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- Cybersecurity Challenges of Autonomous Systems

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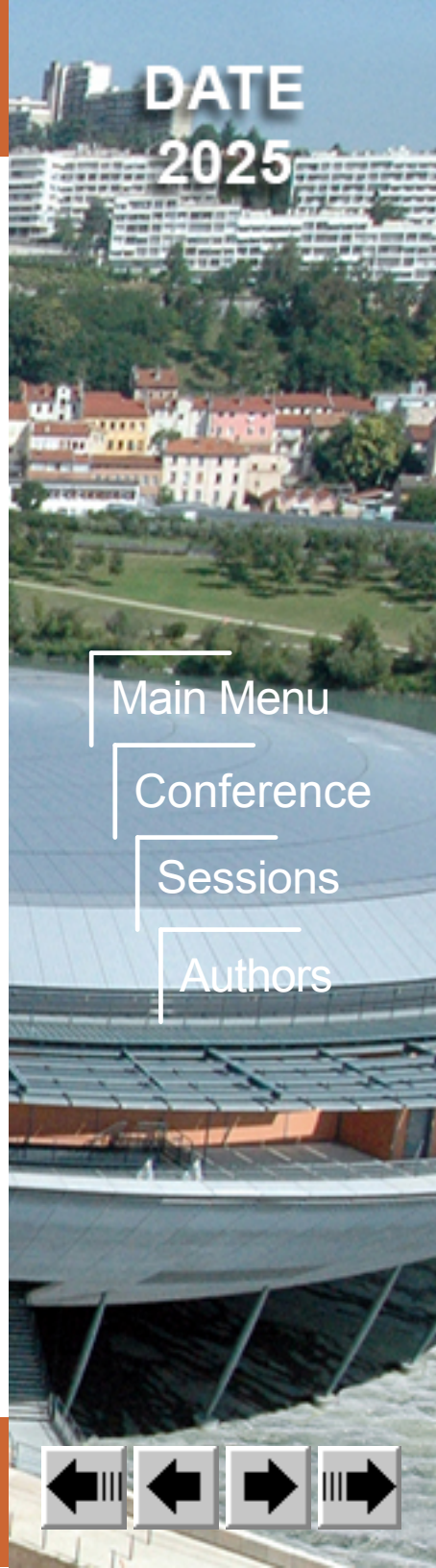


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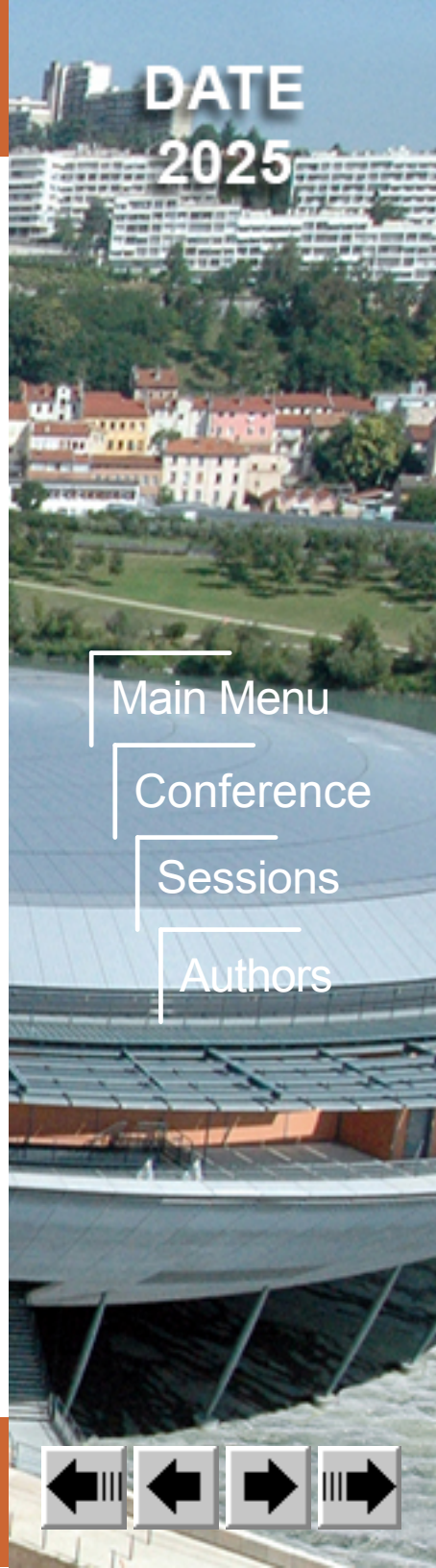


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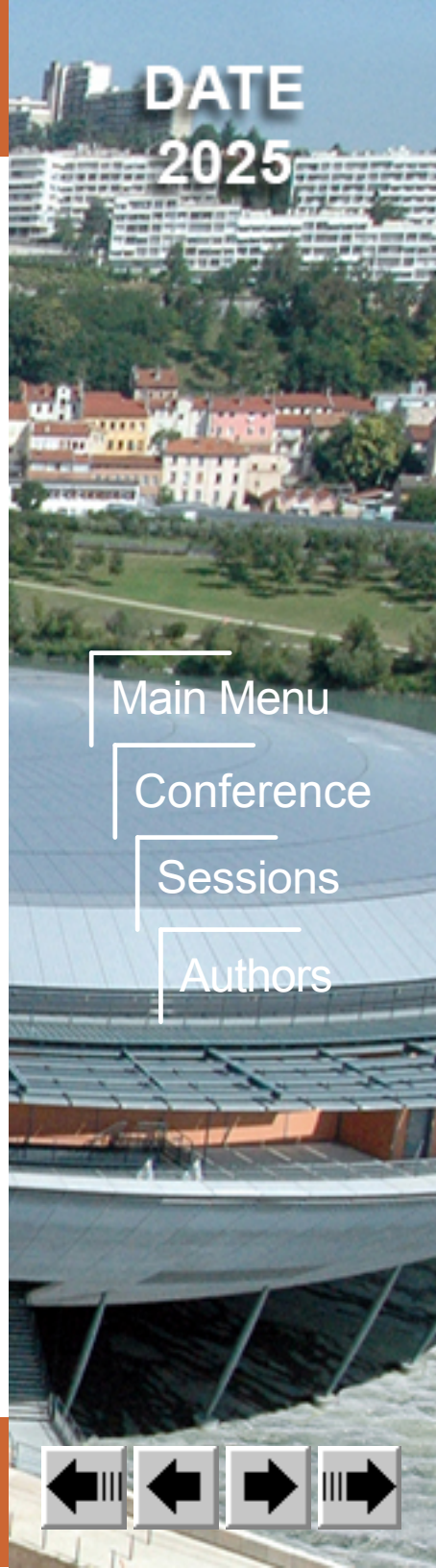


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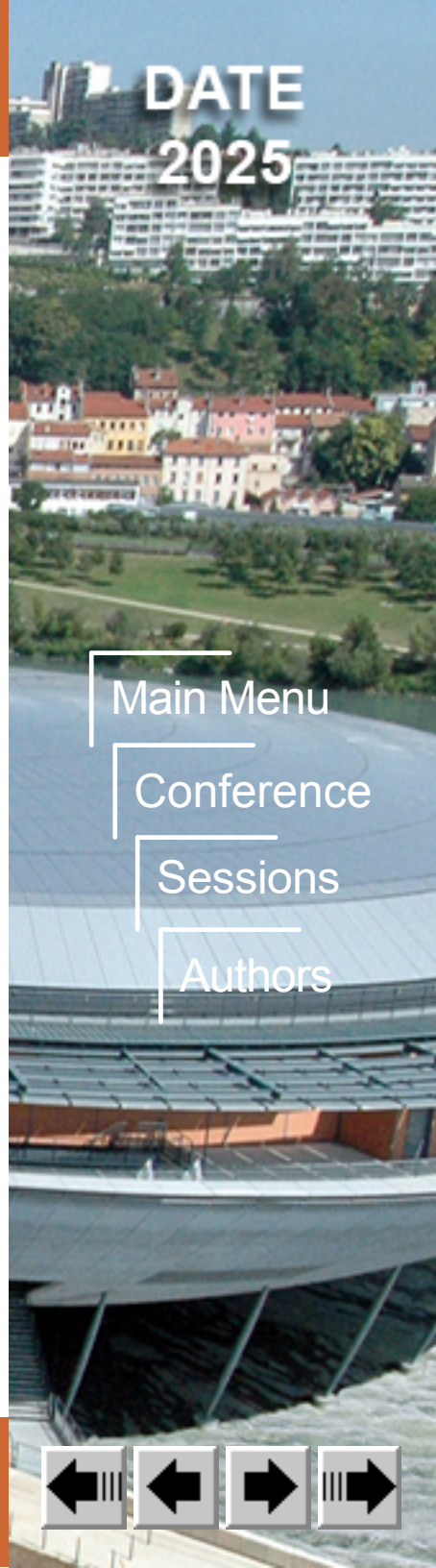
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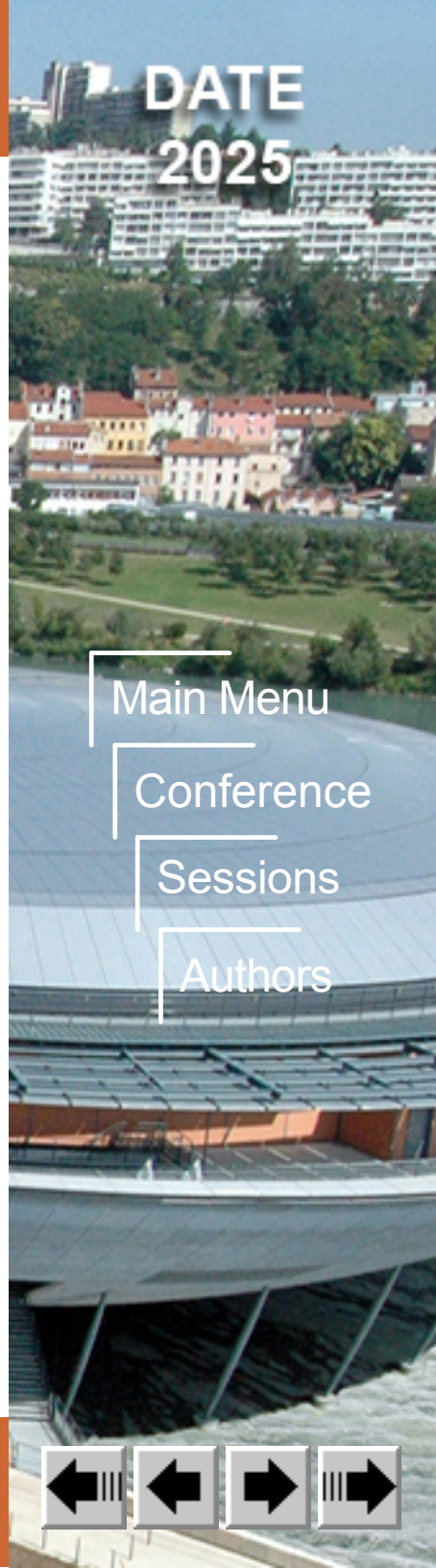


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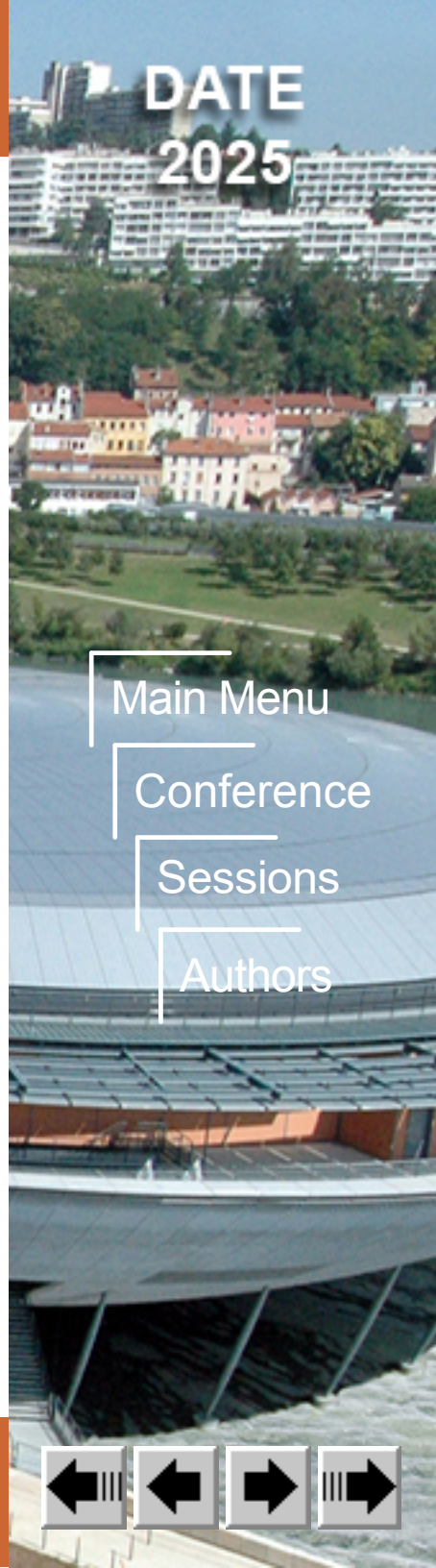
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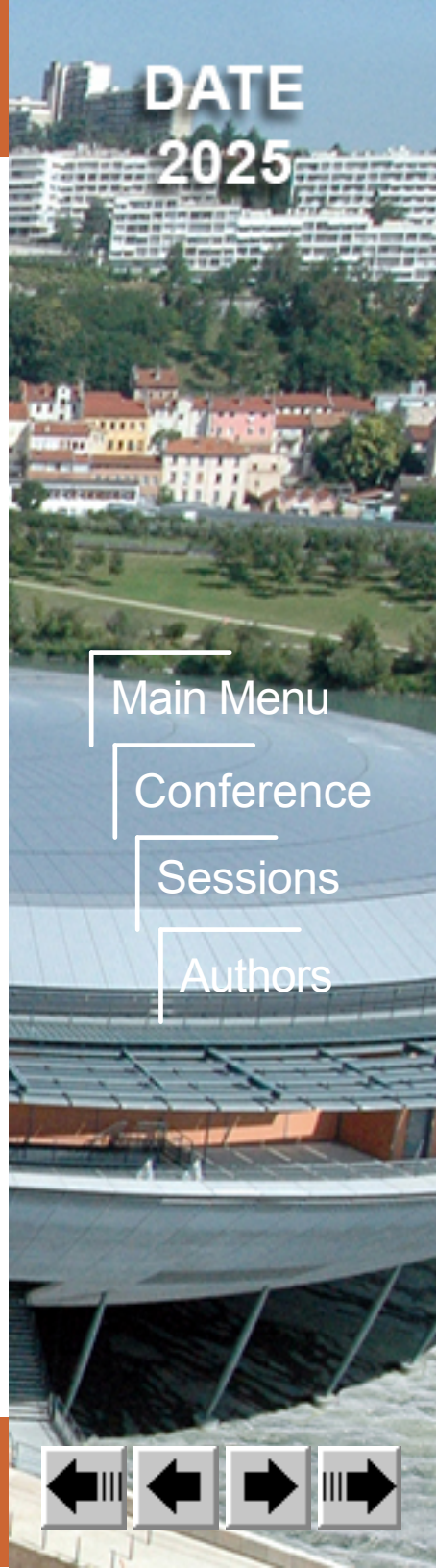
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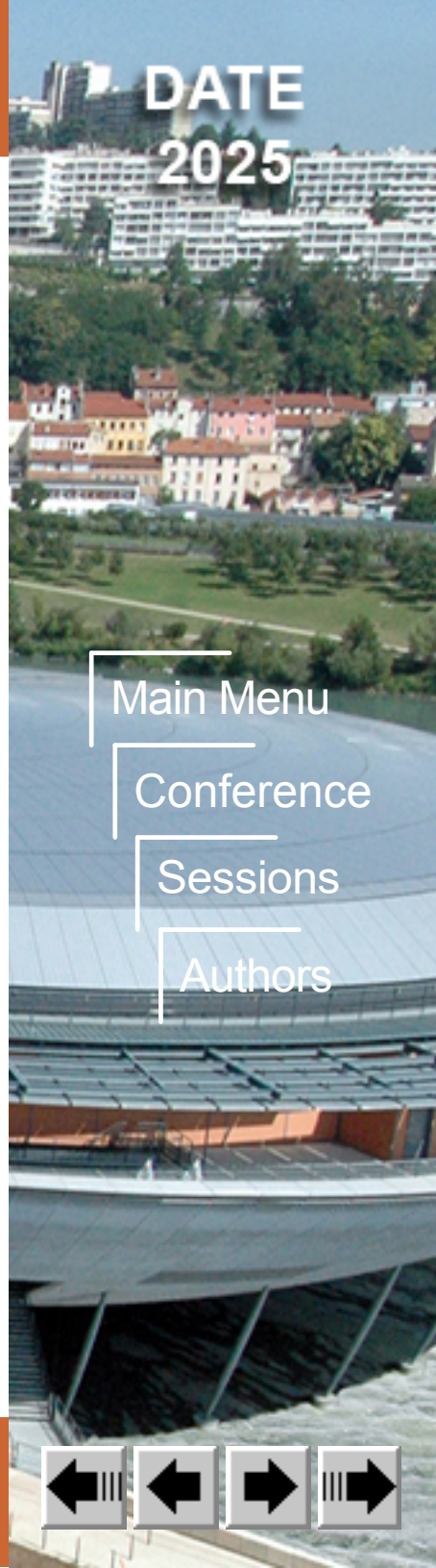


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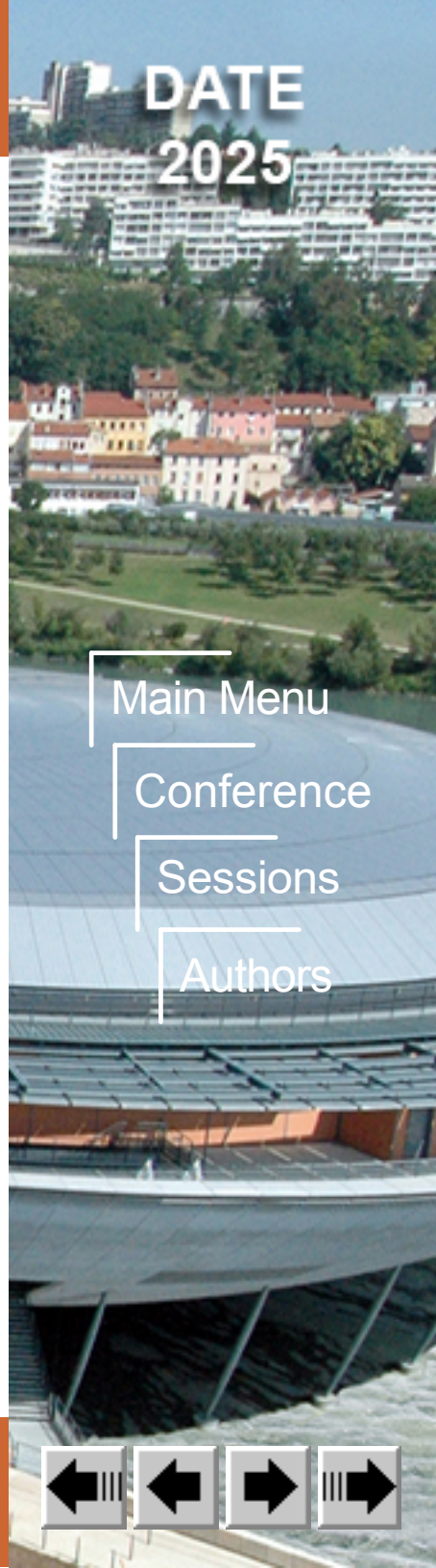


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- Deterministic Fault-Tolerant State Preparation for Near-Term Quantum Error Correction: Automatic Synthesis using Boolean Satisfiability
  Ludwig Schmid, Tom Peham, Lucas Berent, Markus Müller, and Robert Wille

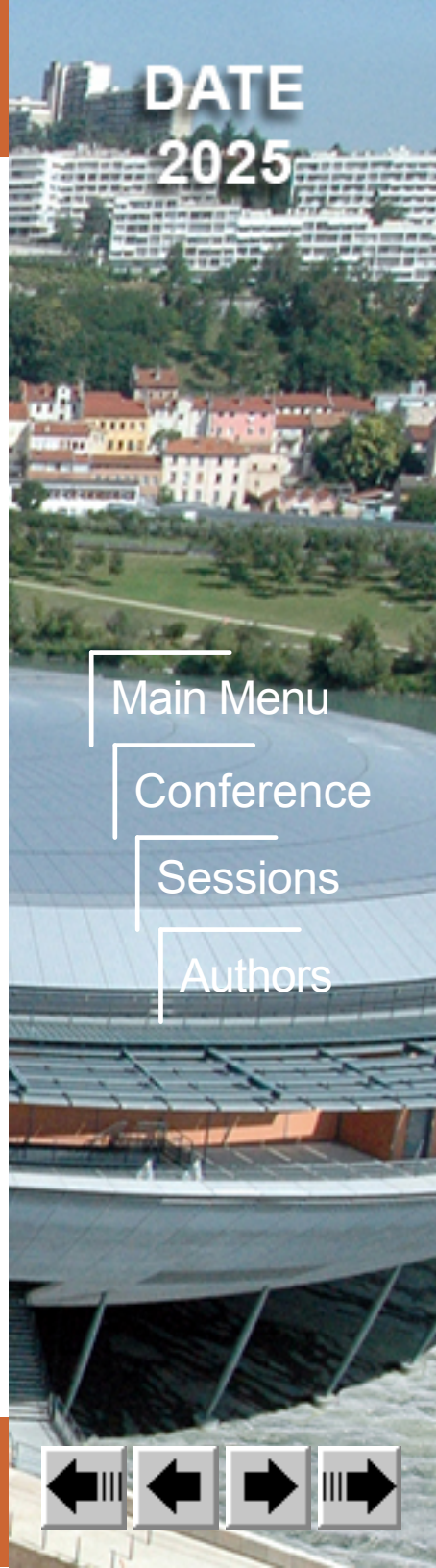
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Papers by Session

- Optimizing Qubit Assignment in Modular Quantum Systems via Attention-Based Deep Reinforcement Learning
  Enrico Russo, Maurizio Palesi, Davide Patti, Giuseppe Ascia, and Vincenzo Catania
- Neural Circuit Parameter Prediction for Efficient Quantum Data Loading
  Dohun Kim, Sunghye Park, and Seokhyeong Kang
- CIM-Based Parallel Fully FFNN Surface Code High-Level Decoder for Quantum Error Correction
  Hao Wang, Erjia Xiao, Songhuan He, Zhongyi Ni, Lingfeng Zhang, Xiaokun Zhan, Yifei Cui, Jinguo Liu, Cheng Wang, Zhongrui Wang, and Renjing Xu

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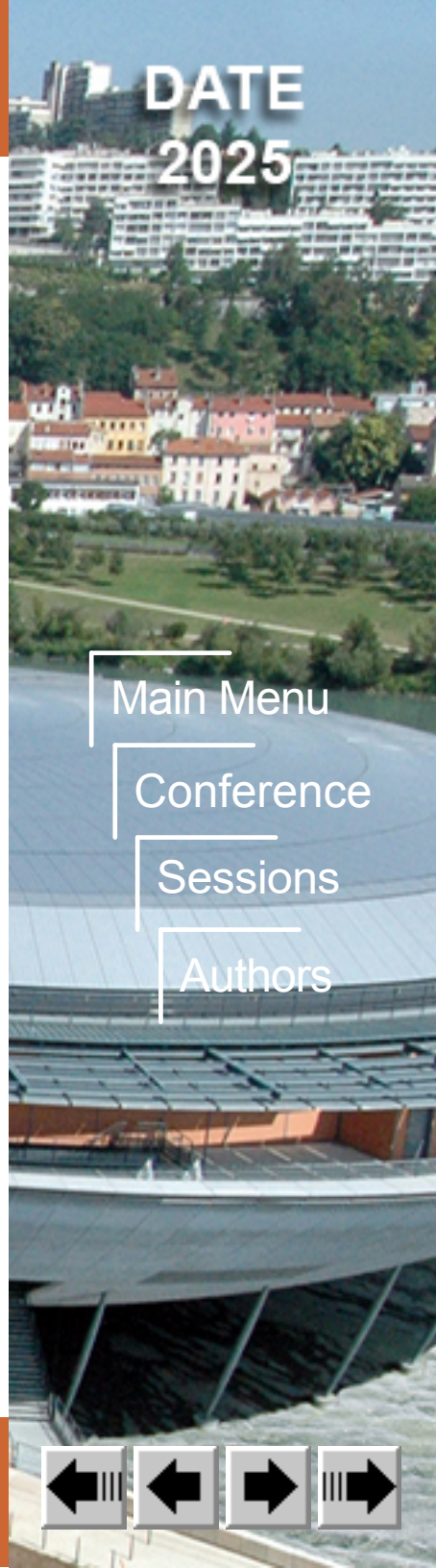


Papers by Session

Applications of Emerging Technologies

- HyperDyn: Dynamic Dimensional Masking for Efficient Hyper-Dimensional Computing
  Fangxin Liu, Haomin Li, Zongwu Wang, Dongxu Lyu, and Li Jiang
- C3CIM: Constant Column Current Memristor-Based Computation-in-Memory Micro-Architecture
  Yashvardhan Biyani, Rajendra Bishnoi, Theofilos Spyrou, and Said Hamdioui
- ASNPC: An Automated Generation Framework for SNN and Neuromorphic Processor Co-Design
  Xiangyu Wang, Yuan Li, Zhijie Yang, Chao Xiao, Xun Xiao, Renzhi Chen, Weixia Xu, and Lei Wang
- Simultaneous Denoising and Compression for DVS with Partitioned Cache-Like Spatiotemporal Filter
  Qinghang Zhao, Yixi Ji, Jiaqi Wang, Jinjian Wu, and Guangming Shi
- Practical MU-MIMO Detection and LDPC Decoding through Digital Annealing
  Po-Shao Chen, Wei Tang, and Zhengya Zhang
- LLM-SRAF: Sub-Resolution Assist Feature Generation using Large Language Model
  Tianyi Li, Zhexin Tang, Tao Wu, Bei Yu, Jingyi Yu, and Hao Geng

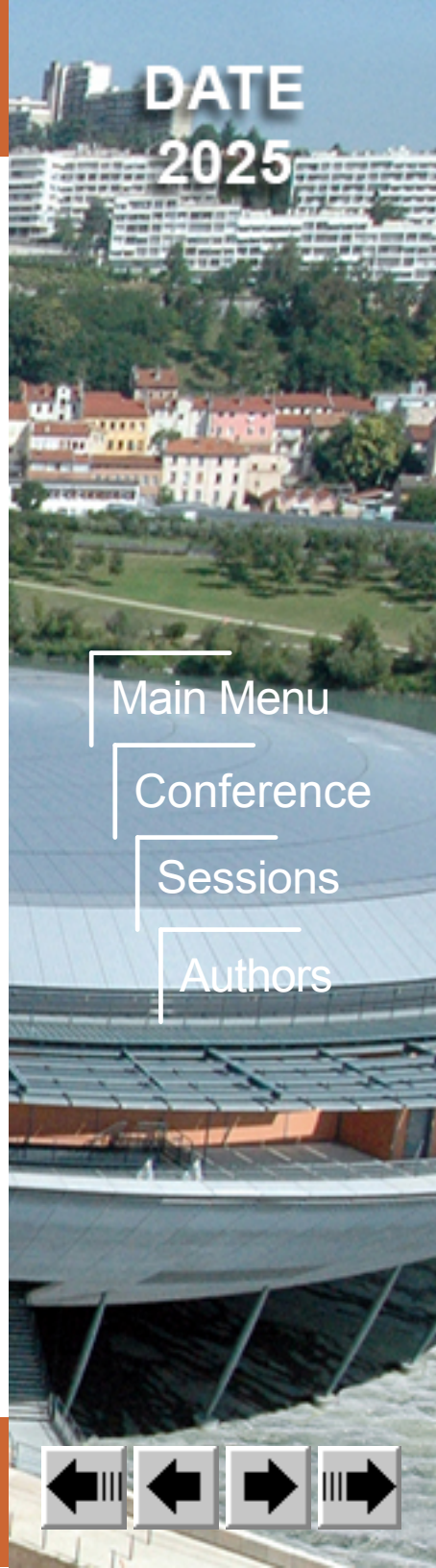
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Papers by Session

- A Multi-Stage Potts Machine Based on Coupled CMOS Ring Oscillators
  Yilmaz Ege Gonul and Baris Taskin
- ADAPT-pNC: Mitigating Device Variability and Sensor Noise in Printed Neuromorphic Circuits with SO Adaptive Learnable Filters
  Tara Gheshlaghi, Priyanjana Pal, Haibin Zhao, Michael Hefenbrock, Michael Beigl, and Mehdi B. Tahoori
- Self-Adaptive Ising Machines for Constrained Optimization
  Corentin Delacour
- Enabling SNN-Based Near-MEA Neural Decoding with Channel Selection: An Open-HW Approach
  Gianluca Leone, Luca Martis, Luigi Raffo, and Paolo Meloni
- Towards Fast Automatic Design of Silicon Dangling Bond Logic
  Jan Drewniok, Marcel Walter, Samuel Sze Hang Ng, Konrad Walus, and Robert Wille
- Loading-Aware Mixing-Efficient Sample Preparation on Programmable Microfluidic Device
  Debraj Kundu, Tsun-Ming Tseng, Shigeru Yamashita, and Ulf Schlichtmann

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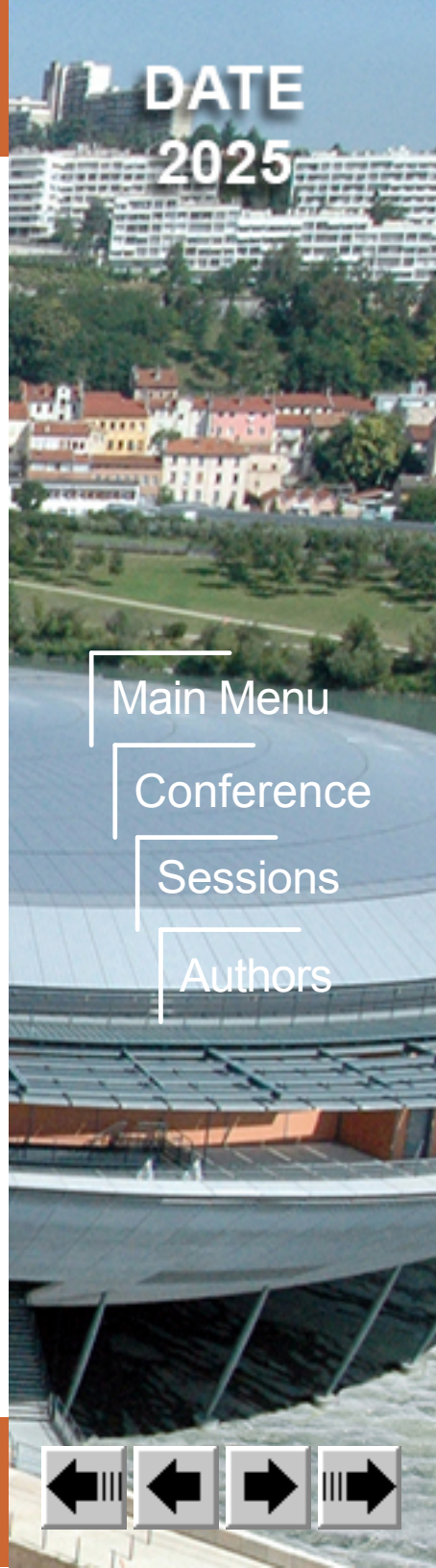


Papers by Session

ASD Regular Session: Novel Safety Metrics, Adaptive Patterns for Resilience, and Legal Frameworks in Autonomous Systems Design

- Identification of Hazardous Driving Scenarios using Cross-Channel Safety Performance Indicators
  C. A. J. Hanselaar, M. M. Selva Kumar, Y. Fu, A. Terechko, R. R. Venkatesha Prasad, and E. Silvas
- Designing Resilient Autonomous Systems with the Reflex Pattern
  Julian Demicoli and Sebastian Steinhorst
- Law as a Design Consideration for Automated Vehicles Suitable to Transport Intoxicated Persons
  William H. Widen and Marilyn C. Wolf

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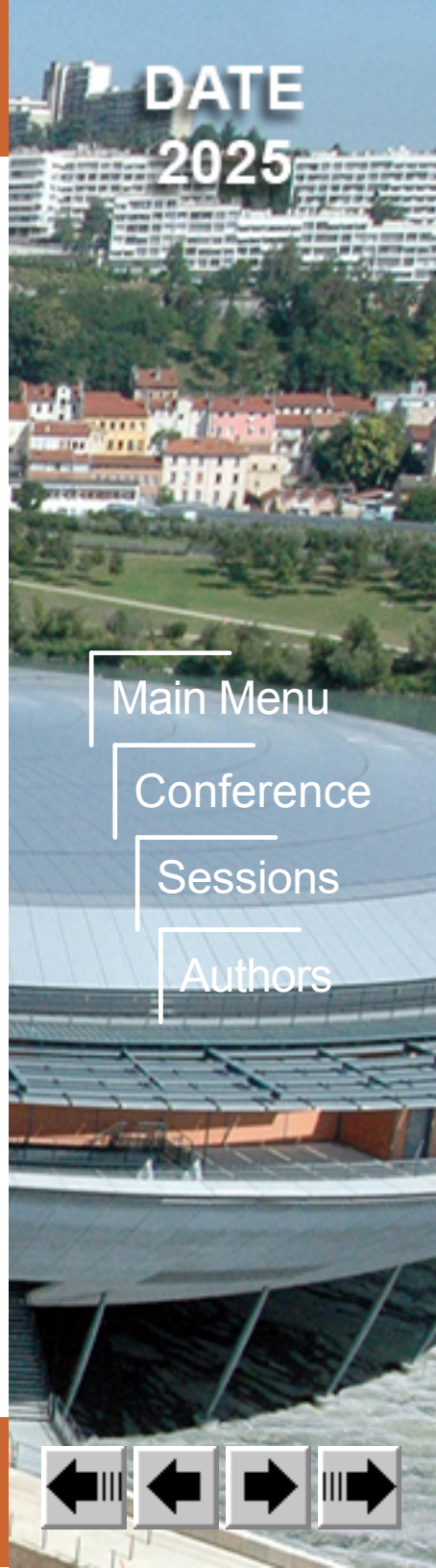


Papers by Session

Focus Session: Improving Chip Design Enablement for Universities in Europe

- Improving Chip Design Enablement for Universities in Europe – A Position Paper

  Lukas Krupp, Ian O'Connor, Luca Benini, Christoph Studer, Joachim Rodrigues, and Norbert Wehn

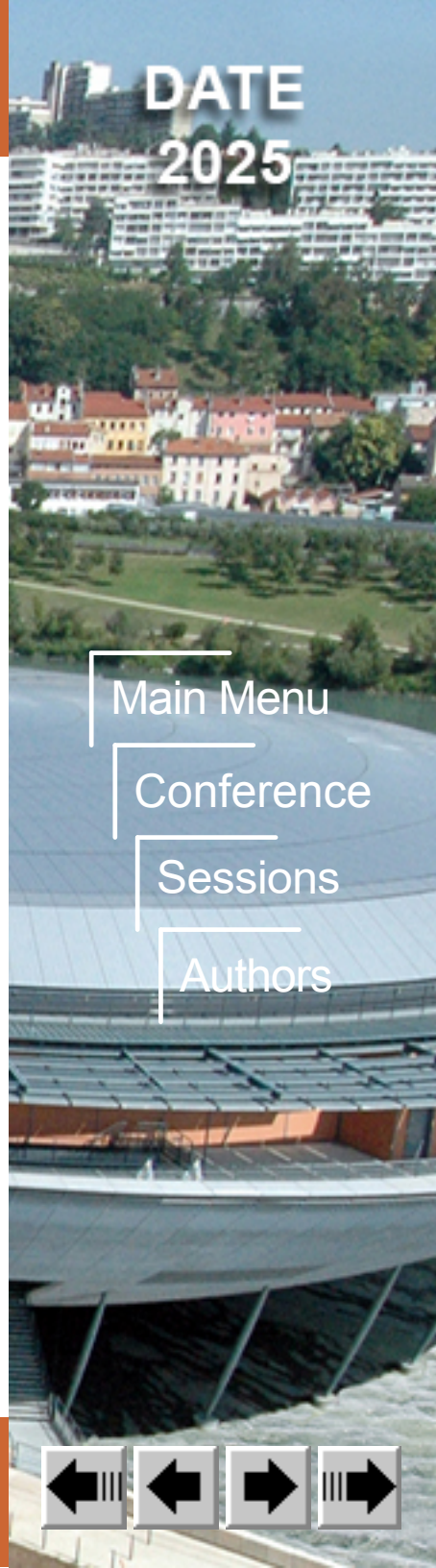


Papers by Session

Design Methodologies and Applications for Machine Learning

- Filter-Based Adaptive Model Pruning for Efficient Incremental Learning on Edge Devices
  Jing-Jia Hung, Yi-Jung Chen, Hsiang-Yun Cheng, Hsu Kao, and Chia-Lin Yang
- DyLGNN: Efficient LM-GNN Fine-Tuning with Dynamic Node Partitioning, Low-Degree Sparsity, and Asynchronous Sub-Batch
  Zhen Yu, Jinhao Li, Jiaming Xu, Shan Huang, Jiancai Ye, Ningyi Xu, and Guohao Dai
- IterL2Norm: Fast Iterative L2-Normalization
  ChangMin Ye, Yonguk Sim, Youngchae Kim, SeongMin Jin, and Doo Seok Jeong
- MPTorch-FPGA: A Custom Mixed-Precision Framework for FPGA-Based DNN Training
  Sami Ben Ali, Silviu-Ioan Filip, Olivier Sentieys, and Guy Lemieux
- MEMHD: Memory-Efficient Multi-Centroid Hyperdimensional Computing for Fully-Utilized In-Memory Computing Architectures
  Do Yeong Kang, Yeong Hwan Oh, Chanwook Hwang, Jinhee Kim, Kang Eun Jeon, and Jong Hwan Ko
- Odin: Learning to Optimize Operation Unit Configuration for Energy-Efficient DNN Inferencing
  Gaurav Narang, Janardhan Rao Doppa, and Partha Pratim Pande

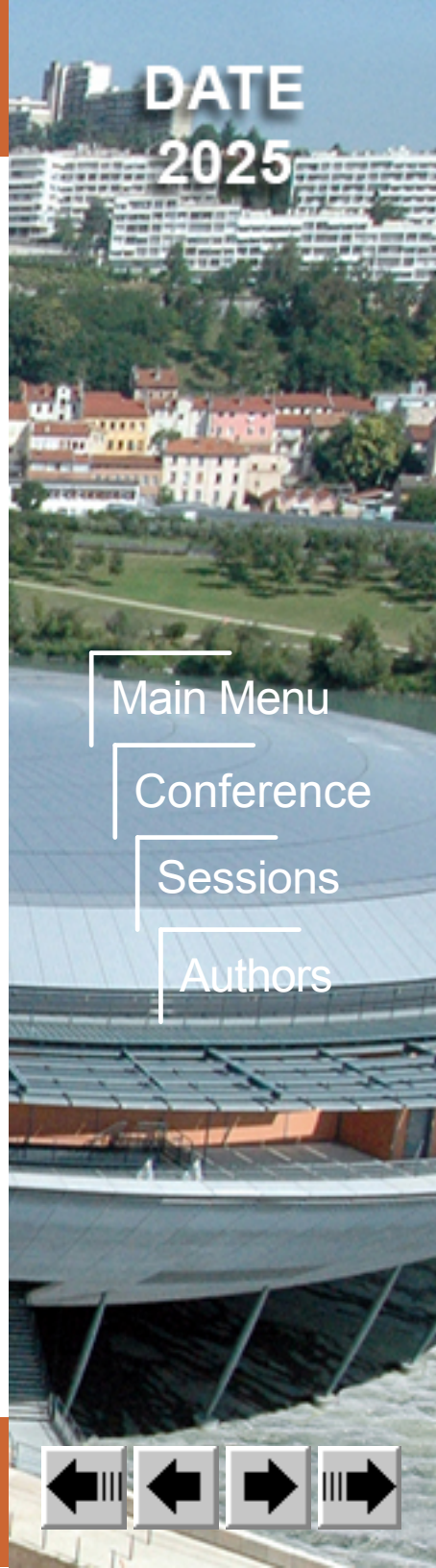
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Papers by Session

- Slipstream: Semantic-Based Training Acceleration for Recommendation Models
  Yassaman Ebrahimzadeh Maboud, Muhammad Adnan, Divya Mahajan, and Prashant J. Nair
- COMPASS: A Compiler Framework for Resource-Constrained Crossbar-Array Based In-Memory Deep Learning Accelerators
  Jihoon Park, Jeongin Choe, Dohyun Kim, and Jae-Joon Kim
- OPS: Outlier-Aware Precision-Slice Framework for LLM Acceleration
  Fangxin Liu, Ning Yang, Zongwu Wang, Xuanpeng Zhu, Haidong Yao, Xiankui Xiong, Qi Sun, and Li Jiang
- OpenC^2: An Open-Source End-to-End Hardware Compiler Development Framework for Digital Compute-in-Memory Macro
  Tianchu Dong, Shaoxuan Li, Yihang Zuo, Hongwu Jiang, Yuzhe Ma, and Shanshi Huang
- Speeding-up Successive Read Operations of STT-MRAM via Read Path Alternation for Delay Symmetry
  Taehwan Kim and Jongsun Park

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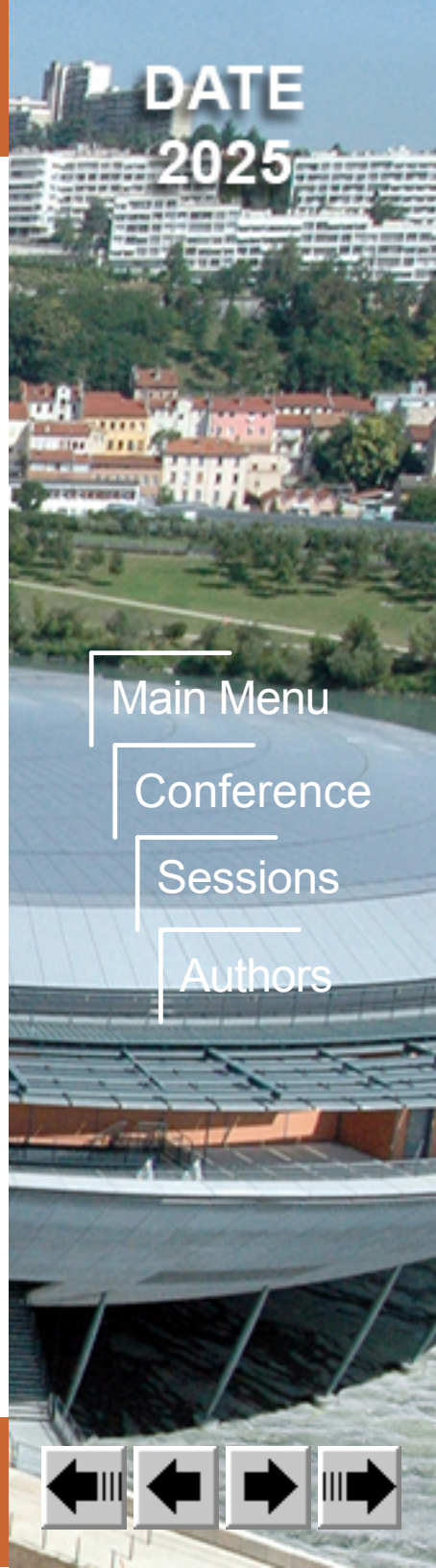


Papers by Session

Low-Power, Energy-Efficient and Thermal-Aware Design

- Co-UP: Comprehensive Core and Uncore Power Management for Latency-Critical Workloads
  Ki-Dong Kang, Gyeongseo Park, and Daehoon Kim
- Flexible Thermal Conductance Model (TCM) for Efficient Thermal Simulation of 3-D ICs and Packages
  Shunxiang Lan, Min Tang, and Jun Ma
- Thanos: Energy-Efficient Keyword Spotting Processor with Hybrid Time-Feature-Frequency-Domain Zero-Skipping
  Sangyeon Kim, Hyunmin Kim, and Sungju Ryu
- Algorithm-Hardware Co-Design of a Unified Accelerator for Non-Linear Functions in Transformers
  Haonan Du, Chenyi Wen, Zhengrui Chen, Li Zhang, Qi Sun, Zheyu Yan, and Cheng Zhuo
- Efficient Hold Buffer Optimization by Supply Noise-Aware Dynamic Timing Analysis
  Lishuo Deng, Changwei Yan, Cai Li, Zhuo Chen, and Weiwei Shan
- LaRED: Efficient IR Drop Predictor with Layout-Preserving Rebuilder-Encoder-Decoder Architecture
  Chengxuan Yu, Yanshuang Teng, Wenhao Dai, Yongjiang Li, Wei W. Xing, Xiao Wu, Dan Niu, and Zhou Jin

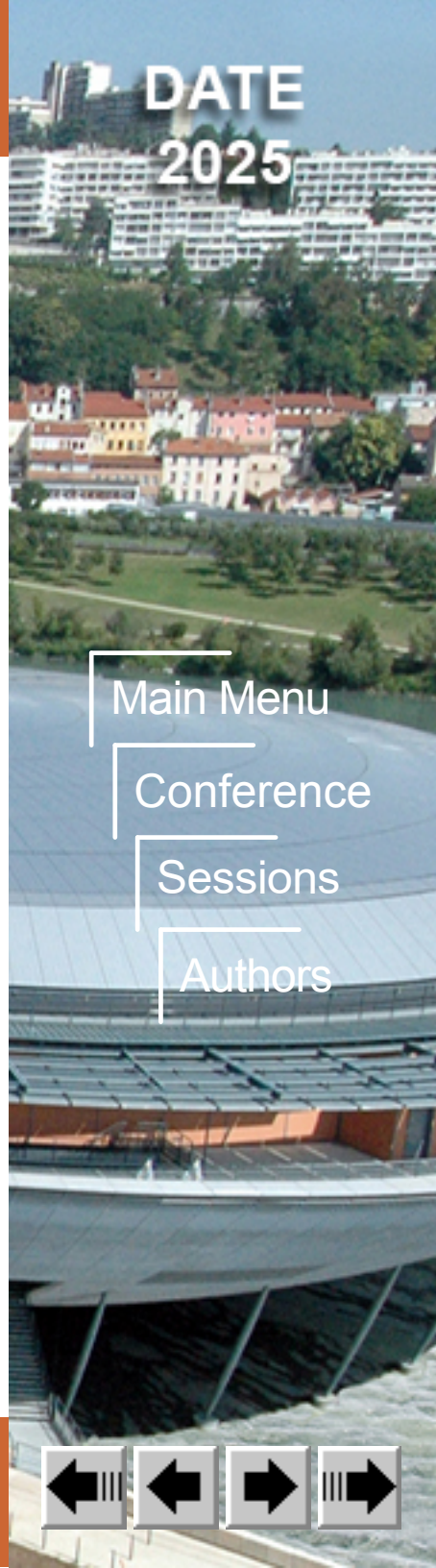
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Papers by Session

- Cool3D: Cost-Optimized and Efficient Liquid Cooling for 3D Integrated Circuits
  Jing Li, Bingrui Zhang, Yuquan Sun, Wei Xing, and Yuanqing Cheng
- Joint DNN Partition and Thread Allocation Optimization for Energy-Harvesting MEC Systems
  Yizhou Shi, Liying Li, Yue Zeng, Peijin Cong, and Junlong Zhou
- Fast Dynamic IR-Drop Prediction with Dual-Path Spatial-Temporal Attention
  Bangqi Fu, Lixin Liu, Qijing Wang, Yutao Wang, Martin D. F. Wong, and Evangeline F. Y. Young
- A Novel Frequency-Spatial Domain Aware Network for Fast Thermal Prediction in 2.5D ICs
  Dekang Zhang, Dan Niu, Zhou Jin, Yichao Dong, Jingweijia Tan, and Changyin Sun

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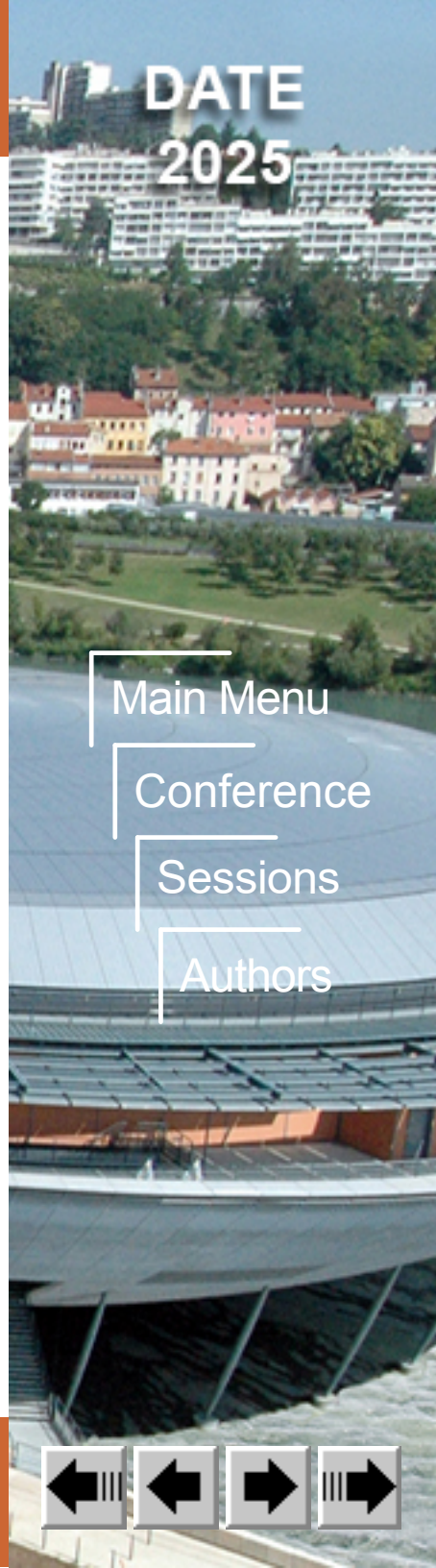


Papers by Session

Applications of Artificial Intelligence Systems

- TAIL: Exploiting Temporal Asynchronous Execution for Efficient Spiking Neural Networks with Inter-Layer Parallelism
  Haomin Li, Fangxin Liu, Zongwu Wang, Dongxu Lyu, Shiyuan Huang, Ning Yang, Qi Sun, Zhuoran Song, and Li Jiang
- Exploiting Boosting in Hyperdimensional Computing for Enhanced Reliability in Healthcare
  SungHeon Jeong, Hamza Errahmouni Barkam, Sanggeon Yun, Yeseong Kim, Shaahin Angizi, and Mohsen Imani
- LCache: Log-Structured SSD Caching for Training Deep Learning Models
  Shucheng Wang, Zhiguo Xu, Zhandong Guo, Jian Sheng, Kaiye Zhou, and Qiang Cao
- OLORAS: Online Long Range Action Segmentation for Edge Devices
  Filippo Ziche and Nicola Bombieri
- Online Learning for Dynamic Structural Characterization in Electron Energy Loss Spectroscopy
  M. L. Varshika, Jonathan Hollenbach, Nicolas Agostini, Ankur Limaye, Antonino Tumeo, and Anup Das
- SCALES: Boost Binary Neural Network for Image Super-Resolution with Efficient Scalings
  Renjie Wei, Zechun Liu, Yuchen Fan, Runsheng Wang, Ru Huang, and Meng Li

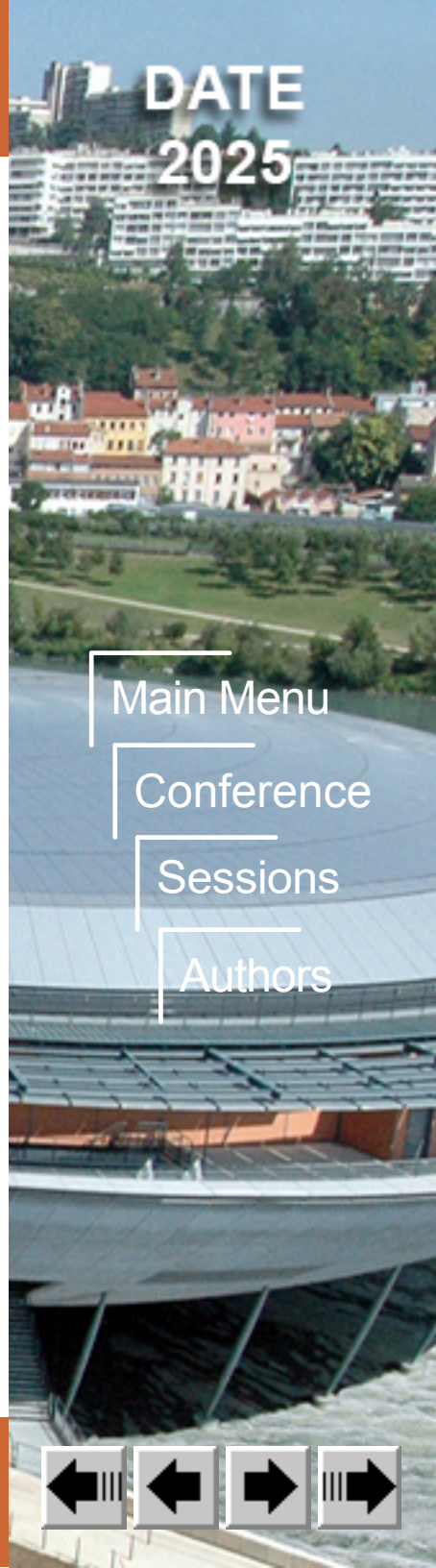
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- Poros: One-Level Architecture-Mapping Co-Exploration for Tensor Algorithms
  Fuyu Wang and Minghua Shen
- A CNN Compression Methodology for Layer-Wise Rank Selection Considering Inter-Layer Interactions
  Milad Kokhazadeh, Georgios Keramidas, Vasilios Kelefouras, and Iakovos Stamoulis
- FineQ: Software-Hardware Co-Design for Low-Bit Fine-Grained Mixed-Precision Quantization of LLMs
  Xilong Xie, Liang Wang, Limin Xiao, Meng Han, Lin Sun, Shuai Zheng, and Xiangrong Xu
- Solving the Cold-Start Problem for the Edge: Clustering and Adaptive Deep Learning for Emotion Detection
  Junjiao Sun, Laura Gutiérrez Martín, Celia López Ongil, Jose Miranda, Jorge Portilla, and Andrés Otero
- KalmMind: A Configurable Kalman Filter Design Framework for Embedded Brain-Computer Interfaces
  Guy Eichler, Joseph Zuckerman, and Luca P. Carloni
- SegTransformer: Enhancing Softmax Performance through Segmentation with a ReRAM-Based PIM Accelerator
  Yu Chen Wang, Ing-Chao Lin, and Yuan-Hao Chang

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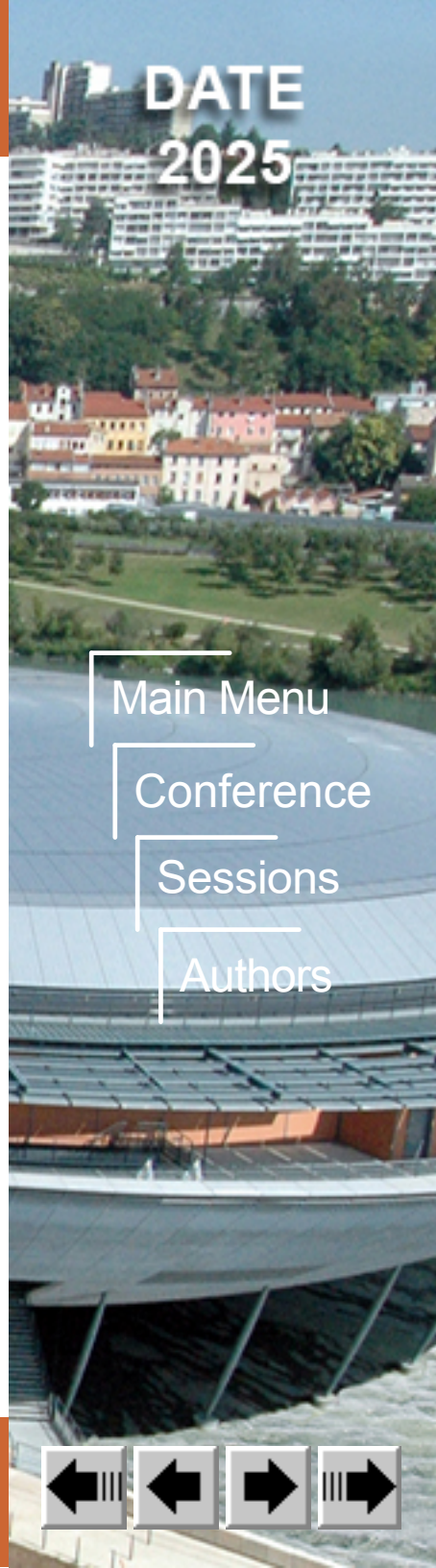


Papers by Session

Driving KDT JU Initiative towards the Chips Act Multi-Partner Projects

- Multi-Partner Project: A Model-Driven Engineering Framework for Federated Digital Twins of Industrial Systems (MATISSE)
  Alessio Bucaioni, Romina Eramo, Luca Berardinelli, Hugo Bruneliere, Benoit Combemale, Djamel Eddine Khelladi, Vittoriano Muttillo, Andrey Sadovykh, and Manuel Wimmer
- Multi-Partner Project: Electric Vehicle Data Acquisition and Valorisation: A Perspective From the OPEVA Project
  Alper Kanak, Salih Ergün, İbrahim Arif, Ali Serdar Atalay, Serhat Ege İnanç, Oguzhan Herkiloğlu, Ahmet Yazıcı, Yunus Sabri Kirca, Muhammed Ozberk, Alim Kerem Erdogmus, Ali Kafalı, Dilara Bayar, Muhammed Oğuz Taş, Luca Davoli, Laura Belli, Gianluigi Ferrari, Badar Muneer, Valentina Palazzi, Luca Roselli, and Fabio Gelati
- Multi-Partner Project: A Deep Learning Platform Targeting Embedded Hardware for Edge-AI Applications (NEUROKIT2E)
  Rajendra Bishnoi, Mohammad Amin Yaldagard, Said Hamdioui, Kanishkan Vadivel, Manolis Sifalakis, Nicolas Daniel Rodriguez, Pedro Julian, Lothar Ratschbacher, Maen Mallah, Yogesh Ramesh Patil, Rashid Ali, and Fabian Chersi
- Multi-Partner Project: Sports Performance and Health Assessment in the DistriMuse Project
  Luca Davoli, Laura Belli, Veronica Mattioli, Riccardo Raheli, Gianluigi Ferrari, Lorenzo Priano, Jaromir Hubalek, Lukas Smital, Andrea Nemcova, Daniela Chlibkova, Vlastimil Benes, and Johan Plomp

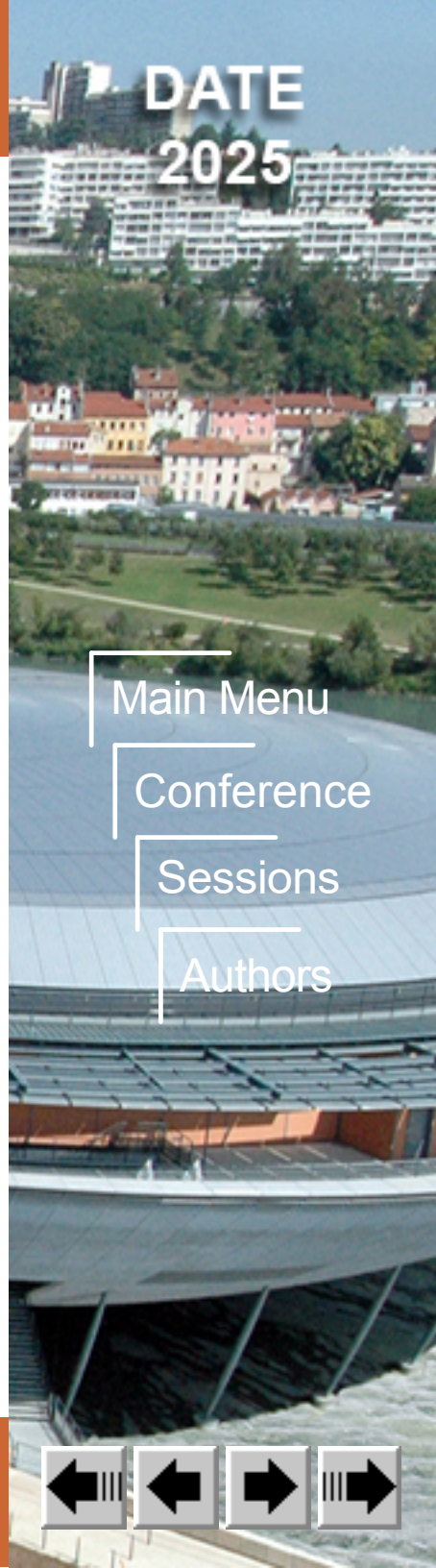
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Papers by Session

- Multi-Partner Project: Advancing the EDA Tools Landscape for the European RISC-V Ecosystem in TRISTAN
  Fatma Jebali, Caaliph Andriamisaina, Mathieu Jan, Wolfgang Ecker, Florian Egert, Bernhard Fischer, Alessio Burrello, Daniele Jahier Pagliari, Sara Vinco, Giuseppe Tagliavini, Ingo Feldner, Andreas Mauderer, Axel Sauer, Arnór Kristmundsson, Alexander Schober, Téo Bernier, Matti Käyrä, Ulf Schlichtmann, and Rocco Jonack
- Multi-Partner Project: Enabling Digital Technologies for Holistic Health-Lifestyle Motivational and Assisted Supervision Supported by Artificial Intelligence Network (H2TRAIN)
  Juan A. Montiel-Nelson, Marco Ottella, and Paolo Azzoni
- Multi-Partner Project: Shaping the Vehicle of the Future - How FEDERATE and HAL4SDV are Steering Europe's Software-Defined Vehicle Ecosystem
  Michael Paulweber, Andreas Eckel, and Paolo Azzoni
- Multi-Partner Project: Artificial Intelligence in Manufacturing Leading to Sustainability and the Consideration of Human Aspects (AIMS5.0)
  Anouar Nechi, Yasin Ghafourian, Belal Abu Naim, Thomas Gutt, George Dimitrakopoulos, Amira Moualhi, Mladen Berekovic, Pal Varga, and Markus Tauber

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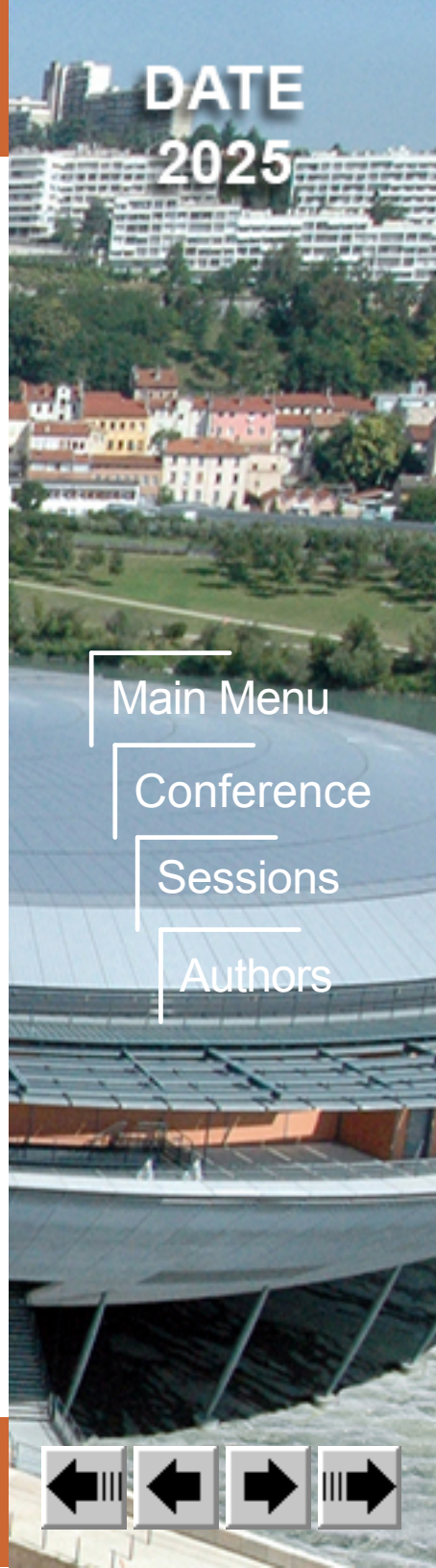


Papers by Session

ASD Focus Session: Teleoperation as a Step Towards Fully Autonomous Systems

- Teleoperation as a Step towards Fully Autonomous Systems

  Alex Bendrick, Daniel Tappe, Nora Sperling, Rolf Ernst, Andrea Nota, Selma Saidi, and Frank Diermeyer



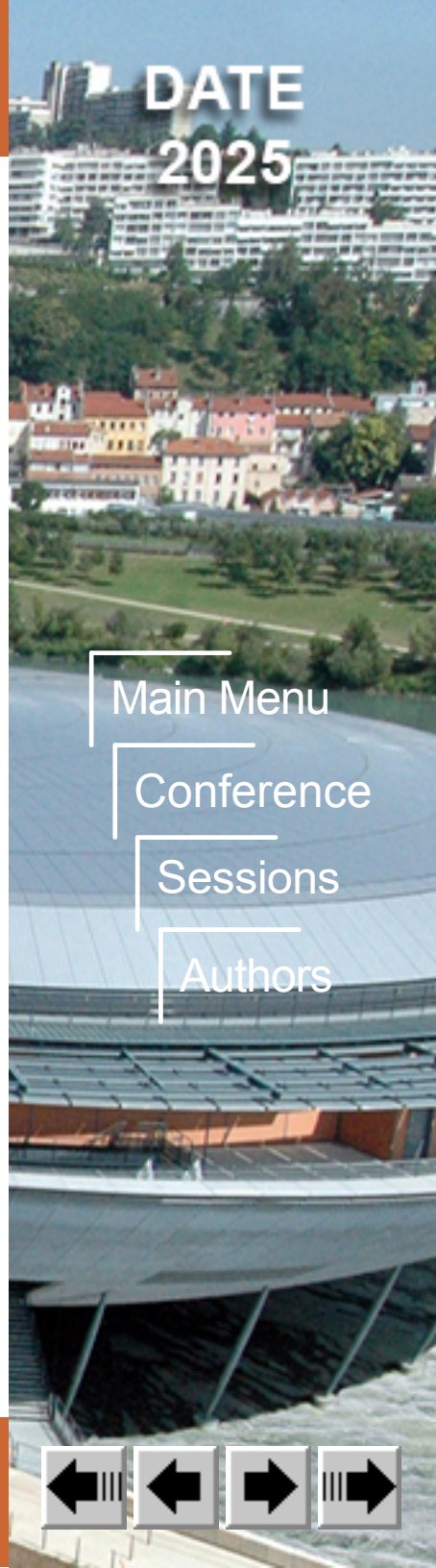
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Papers by Session

Focus Session - GenAI-Native EDA: Redifining Verification with Large Language Models

- EDA-Aware RTL Generation with Large Language Models
  Mubashir ul Islam, Humza Sami, Pierre-Emmanuel Gaillardon, and Valerio Tenace

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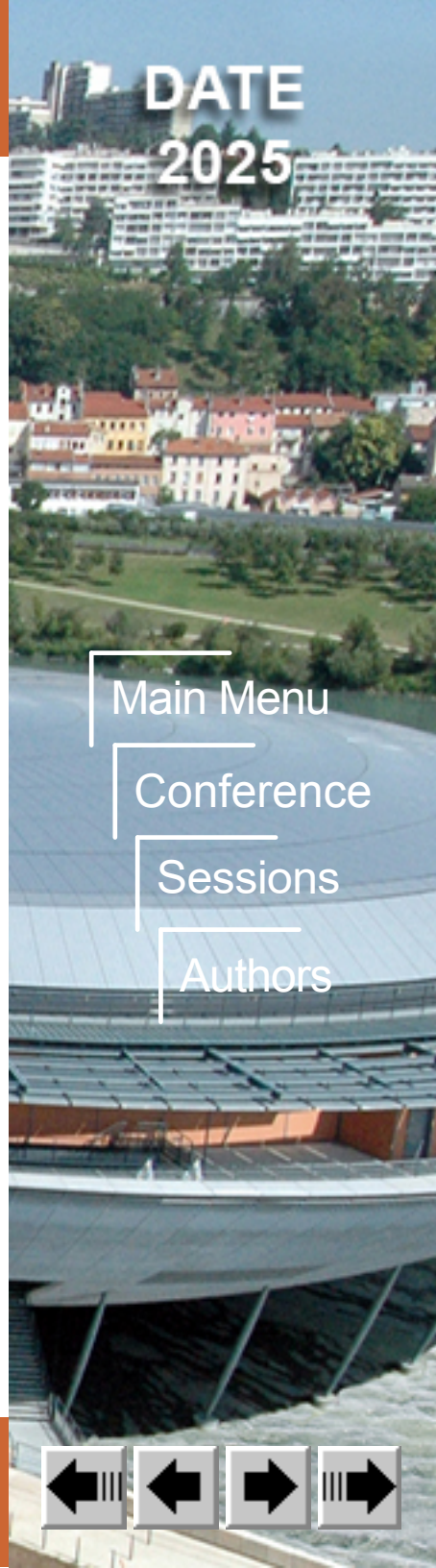


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- Accelerating Authenticated Block Ciphers via RISC-V Custom Cryptography Instructions
  Yuhang Qiu, Wenming Li, Tianyu Liu, Zhen Wang, Zhiyuan Zhang, Zhihua Fan, Xiaochun Ye, Dongrui Fan, and Zhimin Tang
- NDPage: Efficient Address Translation for Near-Data Processing Architectures via Tailored Page Table
  Qingcai Jiang, Buxin Tu, and Hong An
- SPIRE: Inferring Hardware Bottlenecks from Performance Counter Data
  Nicholas Wendt, Mahesh Ketkar, and Valeria Bertacco
- Improving Address Translation in Tagless DRAM Cache by Caching PTE Pages
  Osang Kwon, Yongho Lee, and Seokin Hong
- Exploring the Sparsity-Quantization Interplay on a Novel Hybrid SNN Event-Driven Architecture
  Ilkin Aliyev, Jesus Lopez, and Tosiron Adegbija
- Swift-Sim: A Modular and Hybrid GPU Architecture Simulation Framework
  Xiangrong Xu, Yuanqiu Lv, Liang Wang, Limin Xiao, Meng Han, Runnan Shen, and Jinquan Wang

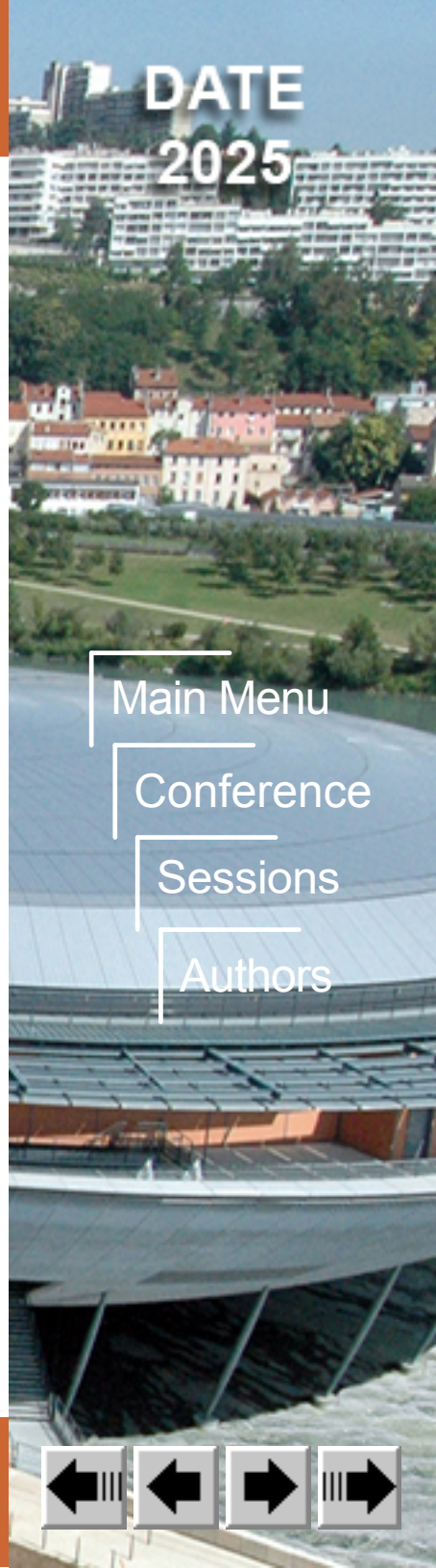
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Papers by Session

- HyMM: A Hybrid Sparse-Dense Matrix Multiplication Accelerator for GCNs
  Hunjong Lee, Jihun Lee, Jaewon Seo, Yunho Oh, Myung Kuk Yoon, and Gunjae Koo
- Buddy ECC: Making Cache Mostly Clean in CXL-Based Memory Systems for Enhanced Error Correction at Low Cost
  Yongho Lee, Junbum Park, Osang Kwon, Sungbin Jang, and Seokin Hong
- A Performance Analysis of Chiplet-Based Systems
  Neethu Bal Mallya, Panagiotis Strikos, Bhavishya Goel, Ahsen Ejaz, and Ioannis Sourdis
- A High-Performance and Flexible Accelerator for Dynamic Graph Convolutional Networks
  Yingnan Zhao, Ke Wang, and Ahmed Louri
- Amphi: Practical and Intelligent Data Prefetching for the First-Level Cache
  Xuan Tang, Zicong Wang, Shuiyi He, Dezun Dong, and Xiangke Liao

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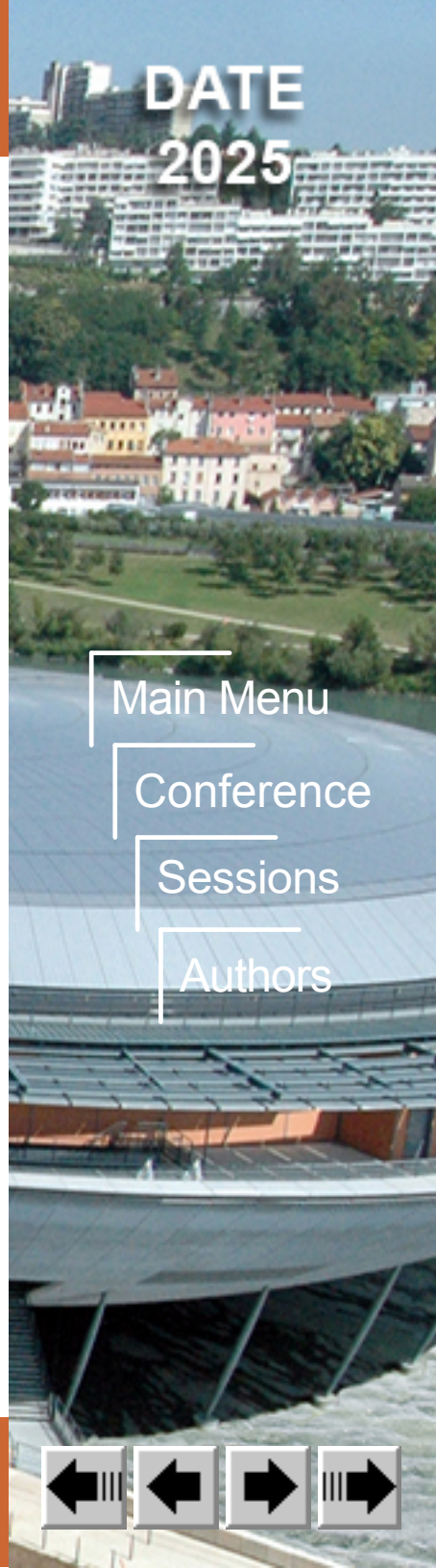


Papers by Session

Smart and Autonomous Systems for a Smart World

- SACK: Enabling Environmental Situation-Aware Access Control for Vehicles in Linux Kernel
  Boyan Chen, Qingni Shen, Lei Xue, Jiarui She, Xiaolei Zhang, Xiapu Luo, Xin Zhang, Wei Chen, and Zhonghai Wu
- Exploiting SysML v2 Modeling for Automatic Smart Factories Configuration
  Mario Libro, Sebastiano Gaiardelli, Marco Panato, Stefano Spellini, Michele Lora, and Franco Fummi
- HiDP:Hierarchical DNN Partitioning for Distributed Inference on Heterogeneous Edge Platforms
  Zain Taufique, Aman Vyas, Antonio Miele, Pasi Liljeberg, and Anil Kanduri
- Coupling Neural Networks and Physics Equations for Li-Ion Battery State-of-Charge Prediction
  Giovanni Pollo, Alessio Burrello, Enrico Macii, Massimo Poncino, Sara Vinco, and Daniele Jahier Pagliari
- Autonomous UAV-Assisted IoT Systems with Deep Reinforcement Learning Based Data Ferry
  Mason Conkel, Wen Zhang, Mimi Xie, Yufang Jin, and Chen Pan

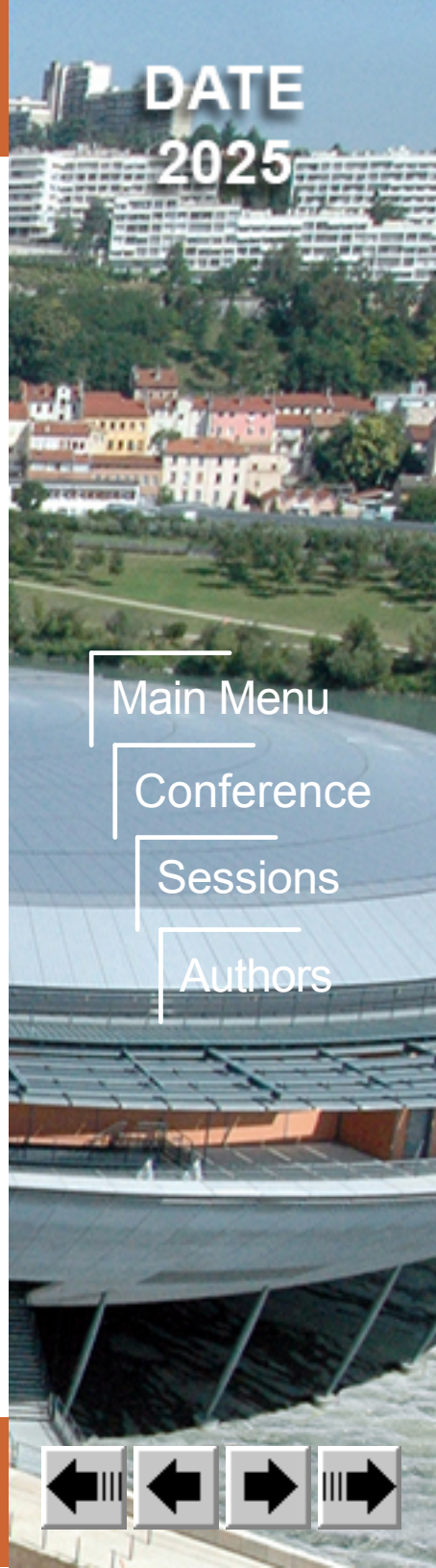
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- AeroDiffusion: Complex Aerial Image Synthesis with Keypoint-Aware Text Descriptions and Feature-Augmented Diffusion Models
  Douglas J. Townsell, Mimi Xie, Bin Wang, Fathi Amsaad, Varshitha Reddy Thanam, and Wen Zhang
- Power- and Deadline-Aware Dynamic Inference on Intermittent Computing Systems
  Hengrui Zhao, Lei Xun, Jagmohan Chauhan, and Geoff Merrett
- Dcha: Distributed-Centralized Heterogeneous Architecture Enables Efficient Multi-Task Processing for Smart Sensing
  Erxiang Ren, Cheng Qu, Li Luo, Yonghua Li, Zheyu Liu, Xinghua Yang, Qi Wei, and Fei Qiao
- FairXbar: Improving the Fairness of Deep Neural Networks with Non-Ideal In-Memory Computing Hardware
  Sohan Salahuddin Mugdho, Yuanbo Guo, Ethan G. Rogers, Weiwei Zhao, Yiyu Shi, and Cheng Wang
- Human-Centered Digital Twin for Industry 5.0
  Francesco Biondani, Luigi Capogrosso, Nicola Dall'Ora, Enrico Fraccaroli, Marco Cristani, and Franco Fummi
- Energy-Aware Error Correction Method for Indoor Positioning and Tracking
  Donguk Kim, Donkyu Baek, Yukai Chen, Enrico Macii, and Massimo Poncino

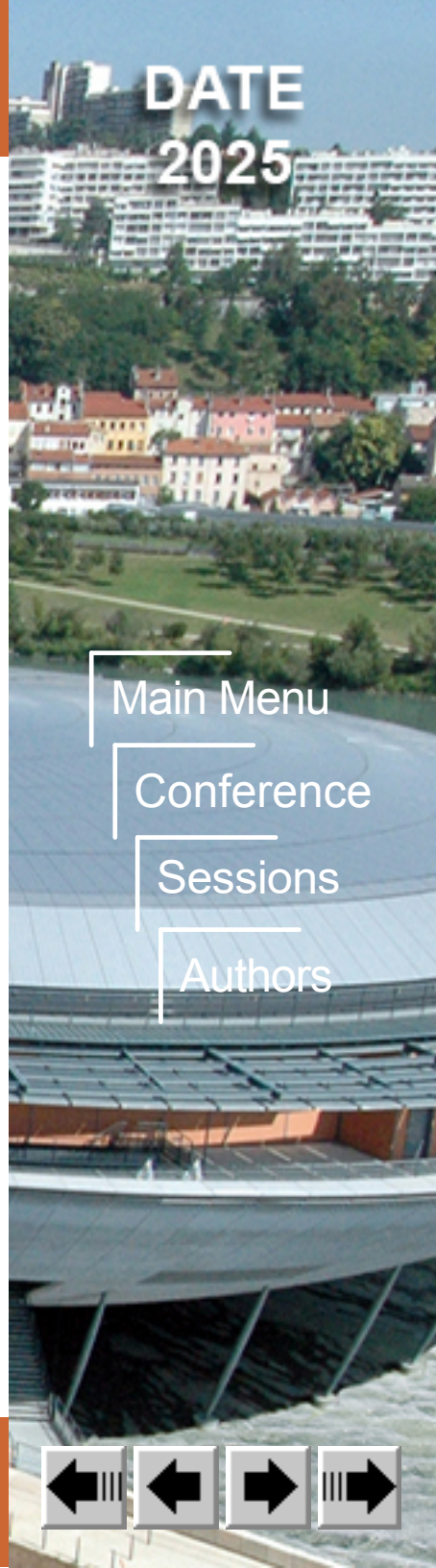
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Papers by Session

- Decentralizing IoT Data Processing: The Rise of Blockchain-Based Solutions
  Giuseppe Spadavecchia, Marco Fiore, Marina Mongiello, and Daniela De Venuto
- Enabling a Portable Brain Computer Interface for Rehabilitation of Spinal Cord Injuries
  Adrian Evans, Victor Roux-Sibillon, Joe Saad, Ivan Miro-Panades, Tetiana Aksenova, and Lorena Anghel

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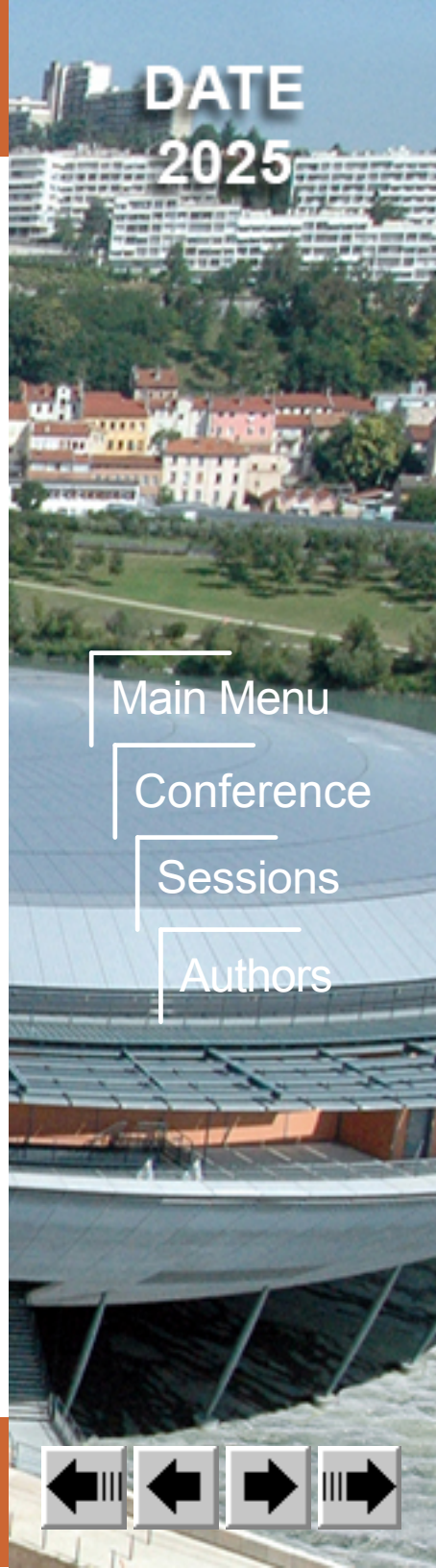


Papers by Session

Focus Session - AI-Driven Design Evolution: Benchmarking and Infrastructure for the Next Era of Semiconductors and Photonics

- ChipVQA: Benchmarking Visual Language Models for Chip Design
  Haoyu Yang, Qijing Huang, Nathaniel Pinckney, Walker Turner, Wenfei Zhou, Yanqing Zhang, Chia-Tung Ho, Chen-Chia Chang, and Haoxing Ren
- FVEval: Understanding Language Model Capabilities in Formal Verification of Digital Hardware
  Minwoo Kang, Mingjie Liu, Ghaith Bany Hamad, Syed M. Suhaib, and Haoxing Ren
- MAPS: Multi-Fidelity AI-Augmented Photonic Simulation and Inverse Design Infrastructure
  Pingchuan Ma, Zhengqi Gao, Meng Zhang, Haoyu Yang, Mark Ren, Rena Huang, Duane S. Boning, and Jiaqi Gu
- PICBench: Benchmarking LLMs for Photonic Integrated Circuits Design
  Yuchao Wu, Xiaofei Yu, Hao Chen, Yang Luo, Yeyu Tong, and Yuzhe Ma

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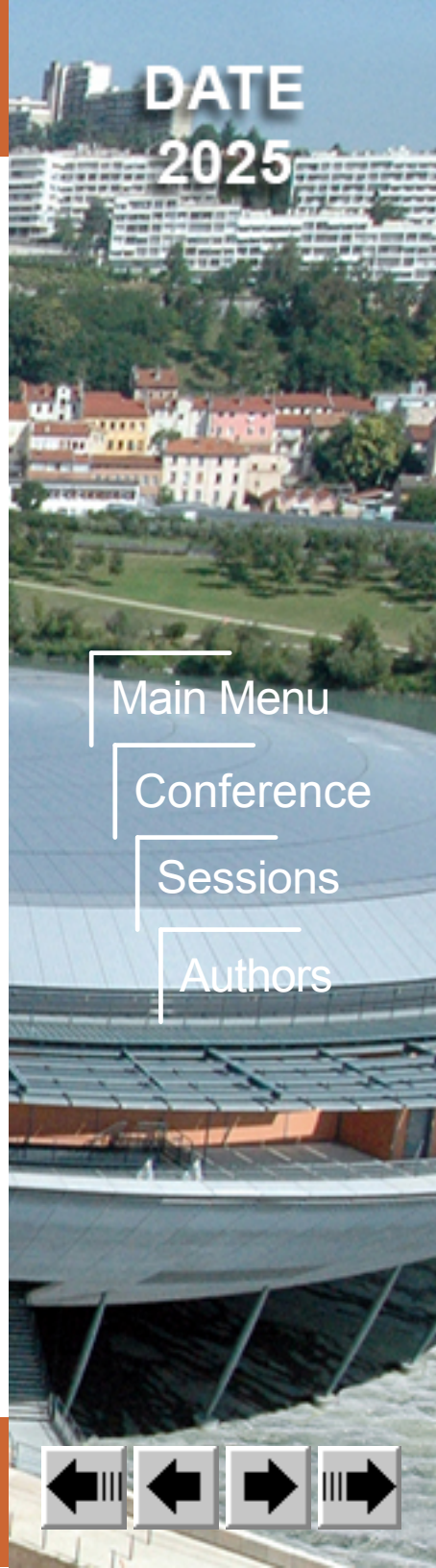


Papers by Session

Embedded, Real-Time and Dependable Systems

- Hardware-Assisted Ransomware Detection using Automated Machine Learning
  Zhixin Pan and Ziyu Shu
- RICH: Heterogeneous Computing for Real-Time Intelligent Control
  Jintao Chen, Yuankai Xu, Yinchen Ni, An Zou, and Yehan Ma
- RT-VirtIO: Towards the Real-Time Performance of VirtIO in a Two-Tier Computing Architecture
  Siwei Ye, Minqing Sun, Huifeng Zhu, Yier Jin, and An Zou
- Enabling Security on the Edge: A CHERI Compartmentalized Network Stack
  Donato Ferraro, Andrea Bastoni, Alexander Zuepke, and Andrea Marongiu
- Towards Reliable Systems: A Scalable Approach to AXI4 Transaction Monitoring
  Chaoqun Liang, Thomas Benz, Alessandro Ottaviano, Angelo Garofalo, Luca Benini, and Davide Rossi
- Exact Schedulability Analysis for Limited-Preemptive Parallel Applications using Timed Automata in UPPAAL
  Jonas Hansen, Srinidhi Srinivasan, Geoffrey Nelissen, and Kim G. Larsen

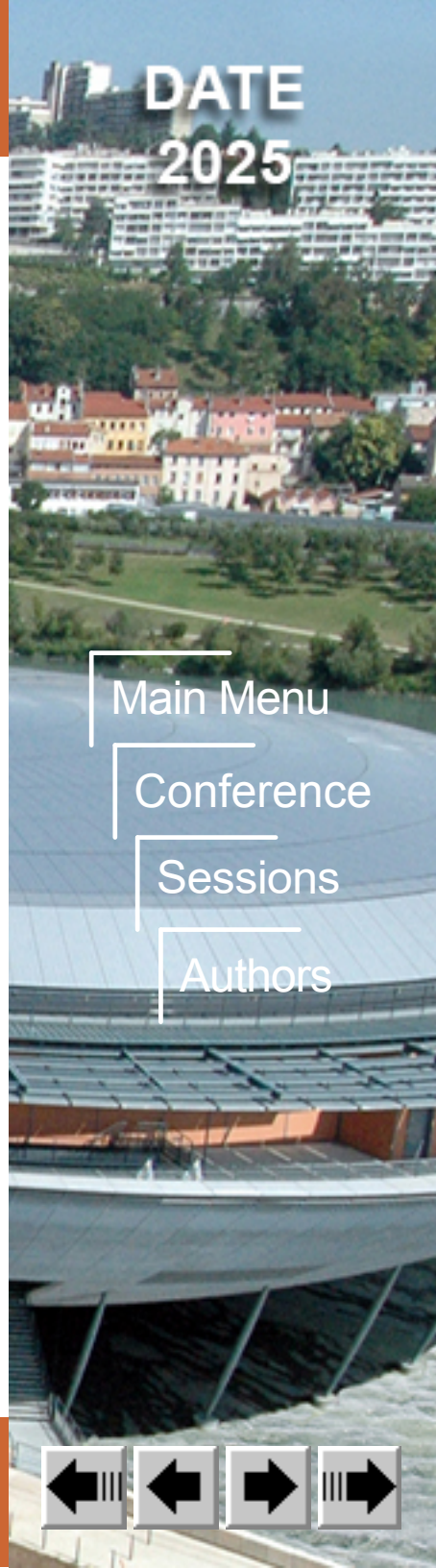
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- Monomorphism-Based CGRA Mapping via Space and Time Decoupling
  Cristian Tirelli, Rodrigo Otoni, and Laura Pozzi
- AttentionLib: A Scalable Optimization Framework for Automated Attention Acceleration on FPGA
  Zhenyu Liu, Xilang Zhou, Faxian Sun, Jianli Chen, Jun Yu, and Kun Wang
- Ensuring Data Freshness for In-Storage Computing with Cooperative Buffer Manager
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- Evaluating Compiler-Based Reliability with Radiation Fault Injection
  Davide Baroffio, Tomás Antonio López, Federico Reghenzani, and William Fornaciari
- Umbra: An Efficient Framework for Trusted Execution on Modern TrustZone-Enabled Microcontrollers
  Stefano Mercogliano and Alessandro Cilardo
- Hardware/Software Co-Analysis for Worst Case Execution Time Bounds
  Can Joshua Lehmann, Lars Bauer, Hassan Nassar, Heba Khdr, and Jörg Henkel

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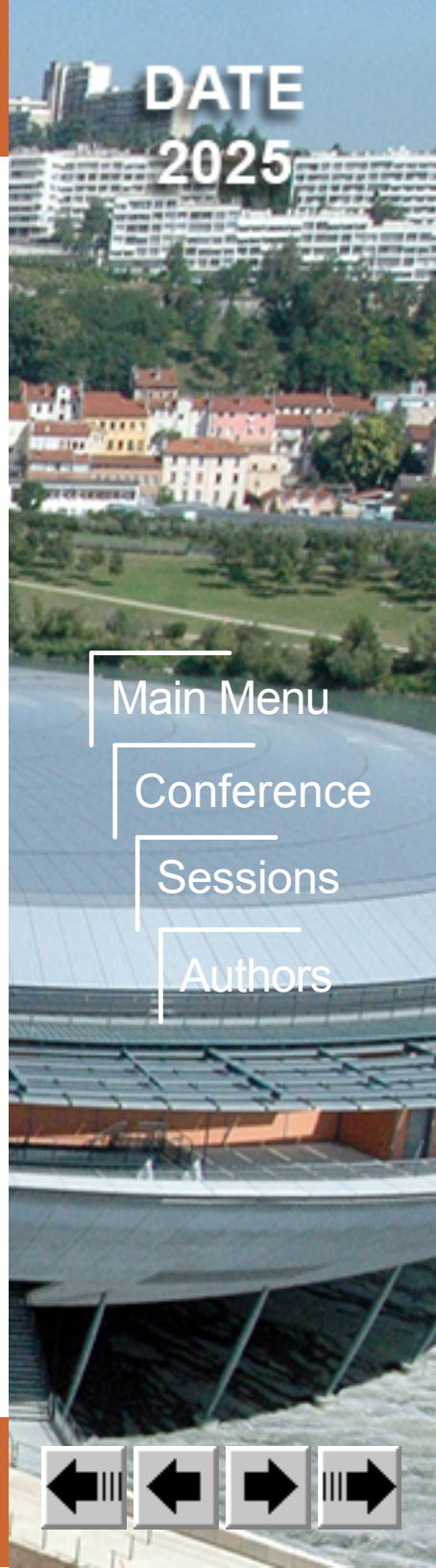


Papers by Session

Architectural and Microarchitectural Design - 2

- SparSynergy: Unlocking Flexible and Efficient DNN Acceleration through Multi-Level Sparsity
  Jingkui Yang, Mei Wen, Junzhong Shen, Jianchao Yang, Yasong Cao, Jun He, Minjin Tang, Zhaoyun Chen, and Yang Shi
- PS-GS: Group-Wise Parallel Rendering with Stage-Wise Complexity Reductions for Real-Time 3D Gaussian Splatting
  Joongho Jo and Jongsun Park
- TxISC: Transactional File Processing in Computational SSDs
  Penghao Sun, Shengan Zheng, Kaijiang Deng, Guifeng Wang, Jin Pu, Jie Yang, Maojun Yuan, Feng Zhu, Shu Li, and Linpeng Huang
- AraXL: A Physically Scalable, Ultra-Wide RISC-V Vector Processor Design for Fast and Efficient Computation on Long Vectors
  Navaneeth Kunhi Purayil, Matteo Perotti, Tim Fischer, and Luca Benini
- Performance Implications of Multi-Chiplet Neural Processing Units on Autonomous Driving Perception
  Mohanad Odema, Luke Chen, Hyoukjun Kwon, and Mohammad Abdullah Al Faruque

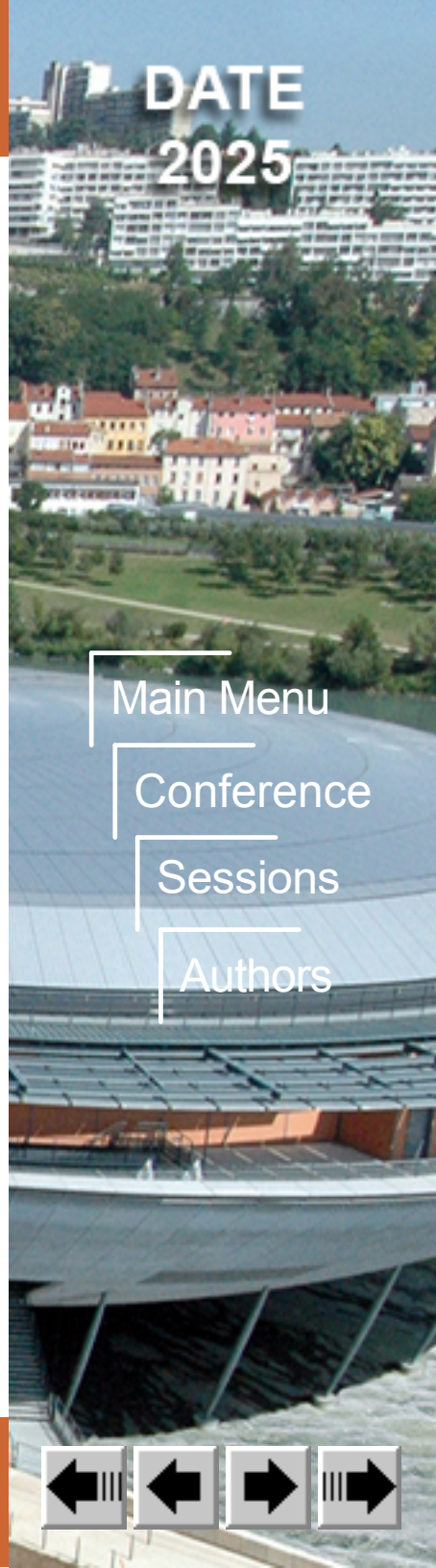
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Papers by Session

- LT-OAQ: Learnable Threshold Based Outlier-Aware Quantization and its Energy-Efficient Accelerator for Low-Precision On-Chip Training
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- LiGNN: Accelerating GNN Training through Locality-Aware Dropout
  Gongjian Sun, Mingyu Yan, Dengke Han, Runzhen Xue, Xiaochun Ye, and Dongrui Fan
- CoupledCB: Eliminating Wasted Pages in Copyback-Based Garbage Collection for SSDs
  Jun Li, Xiaofei Xu, Zhibing Sha, Xiaobai Chen, Jieming Yin, and Jianwei Liao
- LightMamba: Efficient Mamba Acceleration on FPGA with Quantization and Hardware Co-Design
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- Evaluating IOMMU-Based Shared Virtual Addressing for RISC-V Embedded Heterogeneous SoCs
  Cyril Koenig, Enrico Zelioli, and Luca Benini

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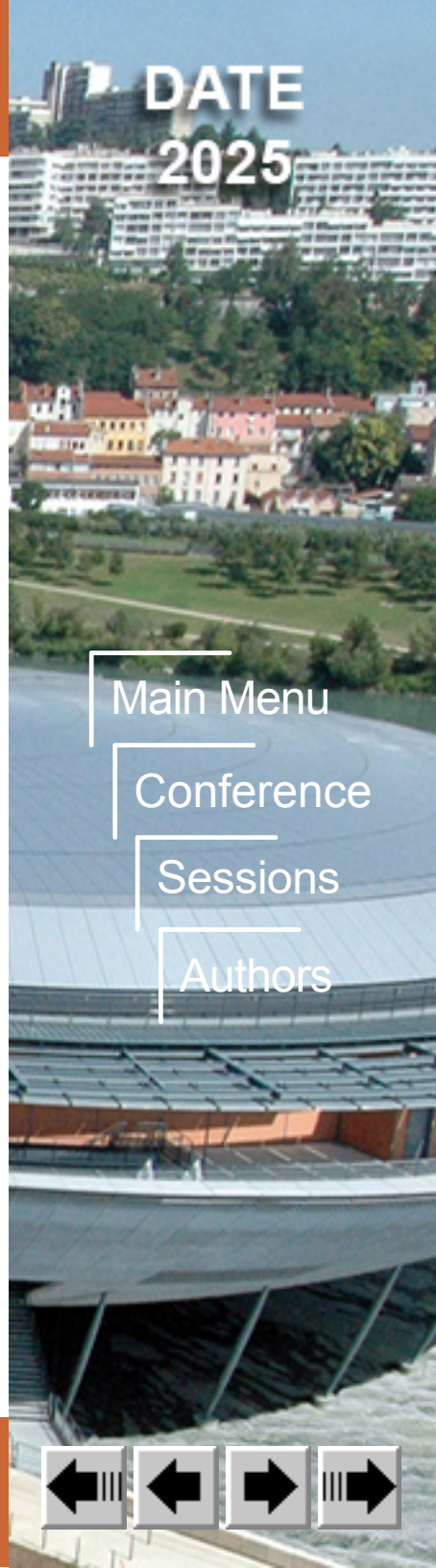


Papers by Session

Power and Energy Efficient Systems

- Less is More: Optimizing Function Calling for LLM Execution on Edge Devices
  Varatheepan Paramanayakam, Andreas Karatzas, Iraklis Anagnostopoulos, and Dimitrios Stamoulis
- SSMDVFS: Microsecond-Scale DVFS on GPGPUs with Supervised and Self-Calibrated ML
  Minqing Sun, Ruiqi Sun, Yingtao Shen, Wei Yan, Qinfen Hao, and An Zou
- A 3D Design Methodology for Integrated Wearable SoCs: Enabling Energy Efficiency and Enhanced Performance at Iso-Area Footprint
  H. Ekin Sumbul, Arne Symons, Lita Yang, Huichu Liu, Tony F. Wu, Matheus Trevisan Moreira, Debabrata Mohapatra, Abhinav Agarwal, Kaushik Ravindran, Chris Thompson, Yuecheng Li, and Edith Beigne
- A Low-Power Mixed-Precision Integrated Multiply-Accumulate Architecture for Quantized Deep Neural Networks
  Xiaolu Hu, Xinkuang Geng, Zhigang Mao, Jie Han, and Honglan Jiang
- Federated Reinforcement Learning for Optimizing the Power Efficiency of Edge Devices
  Benedikt Dietrich, Rasmus Müller-Both, Heba Khdr, and Jörg Henkel

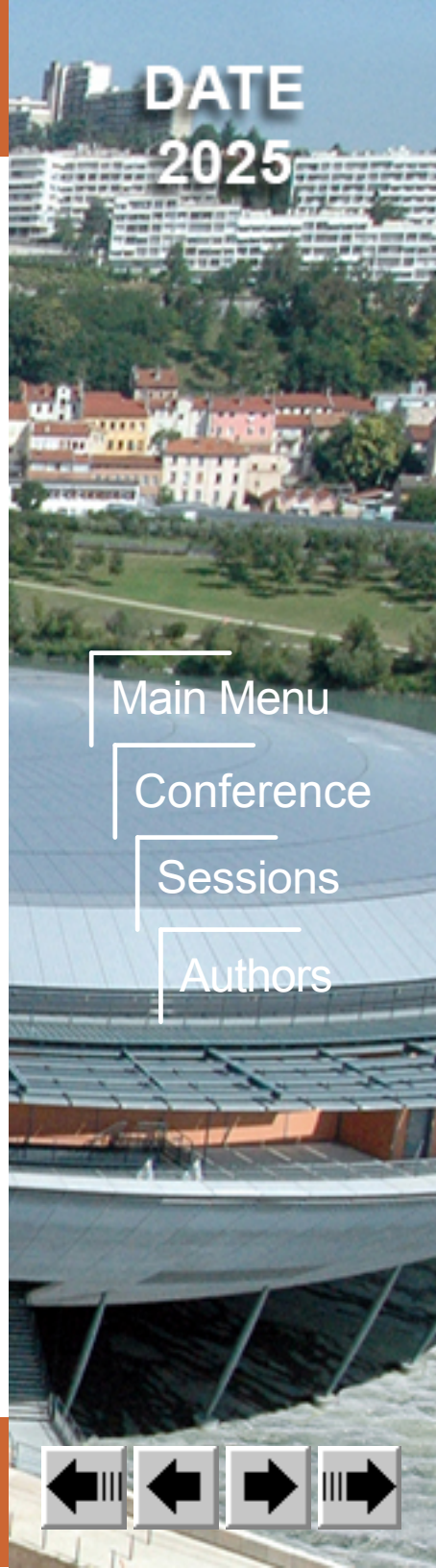
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- Axon: A Novel Systolic Array Architecture for Improved Run Time and Energy Efficient GeMM and Conv Operation with on-Chip im2col
  Md Mizanur Rahaman Nayan, Ritik Raj, Gouse Basha Shaik, Tushar Krishna, and Azad J. Naeemi
- Tempus Core: Area-Power Efficient Temporal-Unary Convolution Core for Low-Precision Edge DLAs
  Prabhu Vellaisamy, Harideep Nair, Thomas Kang, Yichen Ni, Haoyang Fan, Bin Qi, Jeff Chen, Shawn Blanton, and John Paul Shen
- Adaptive Multi-Threshold Encoding for Energy-Efficient ECG Classification Architecture using Spiking Neural Network
  Sumit Diware, Yingzhou Dong, Mohammad Amin Yaldagard, Said Hamdioui, and Rajendra Bishnoi
- LowGradQ: Adaptive Gradient Quantization for Low-Bit CNN Training via Kernel Density Estimation-Guided Thresholding and Hardware-Efficient Stochastic Rounding Unit
  Sangbeom Jeong, Seungil Lee, and Hyun Kim
- PFASware: Quantifying the Environmental Impact of Per- and Polyfluoroalkyl Substances (PFAS) in Computing Systems
  Mariam Elgamal, Abdulrahman Mahmoud, Gu-Yeon Wei, David Brooks, and Gage Hills

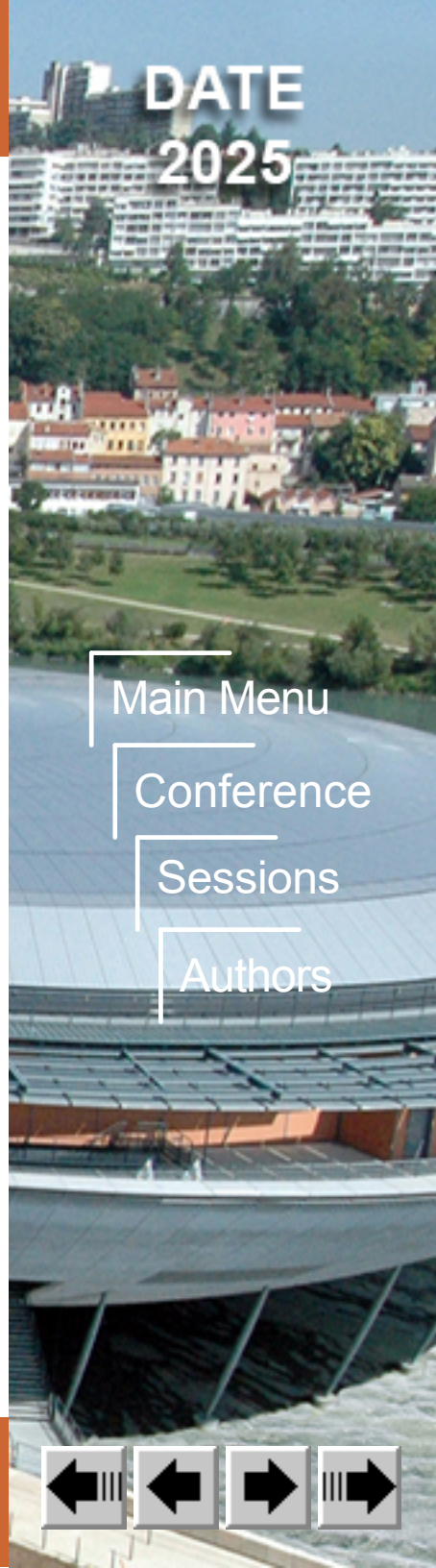
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- Fast Machine Learning Based Prediction for Temperature Simulation using Compact Models
  Mohammadamin Hajikhodaverdian, Sherief Reda, and Ayse K. Coskun
- CPP-SGS: Cycle-Accurate Power Prediction Framework via SNN and Genetic Signal Selection
  Tong Liu, Zijun Jiang, and Yangdi Lyu

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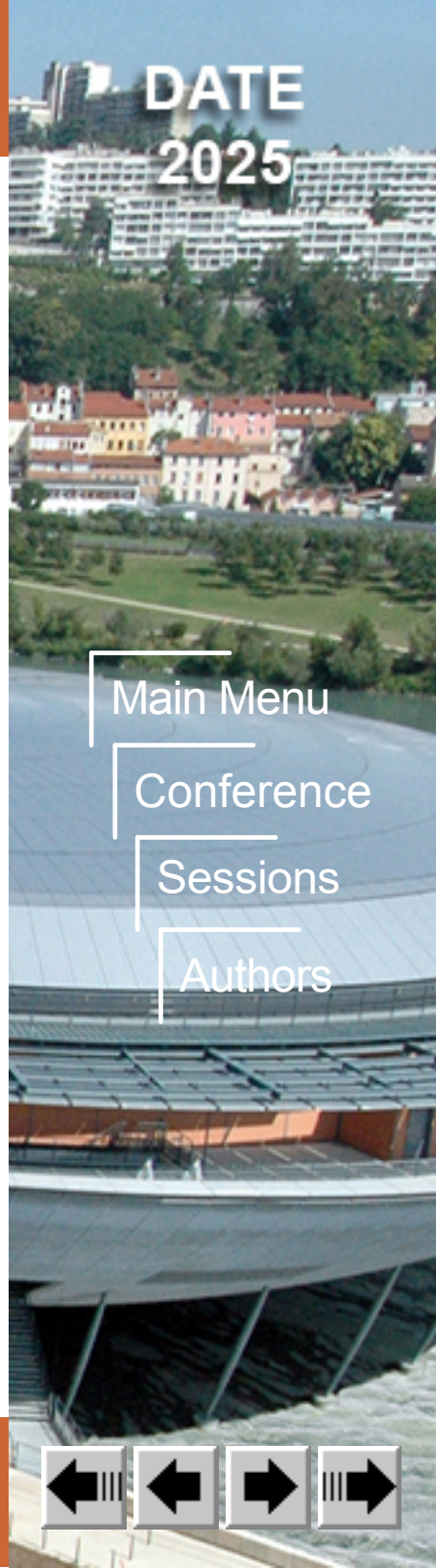


Papers by Session

Design, Test, Modeling and Mitigation of Defects and Faults

- FUSIS: Fusing Surrogate Models and Importance Sampling for Efficient Yield Estimation
  Yanfang Liu and Wei W. Xing
- RoTA: Rotational Torus Accelerator for Wear Leveling of Neural Processing Elements
  Taesoo Lim, Hyeonjin Kim, Jingu Park, Bogil Kim, and William J. Song
- Location is All You Need: Efficient Lithographic Hotspot Detection using Only Polygon Locations
  Yujia Wang, Jiaxing Wang, Dan Feng, Yuzhe Ma, and Kang Liu
- Efficient Modulated State Space Model for Mixed-Type Wafer Defect Pattern Recognition
  Mu Nie, Shidong Zhu, Aibin Yan, Cheng Zhuo, Xiaoqing Wen, and Tianming Ni
- MORE–Stress: Model Order Reduction Based Efficient Numerical Algorithm for Thermal Stress Simulation of TSV Arrays in 2.5D/3D IC
  Tianxiang Zhu, Qipan Wang, Yibo Lin, Runsheng Wang, and Ru Huang

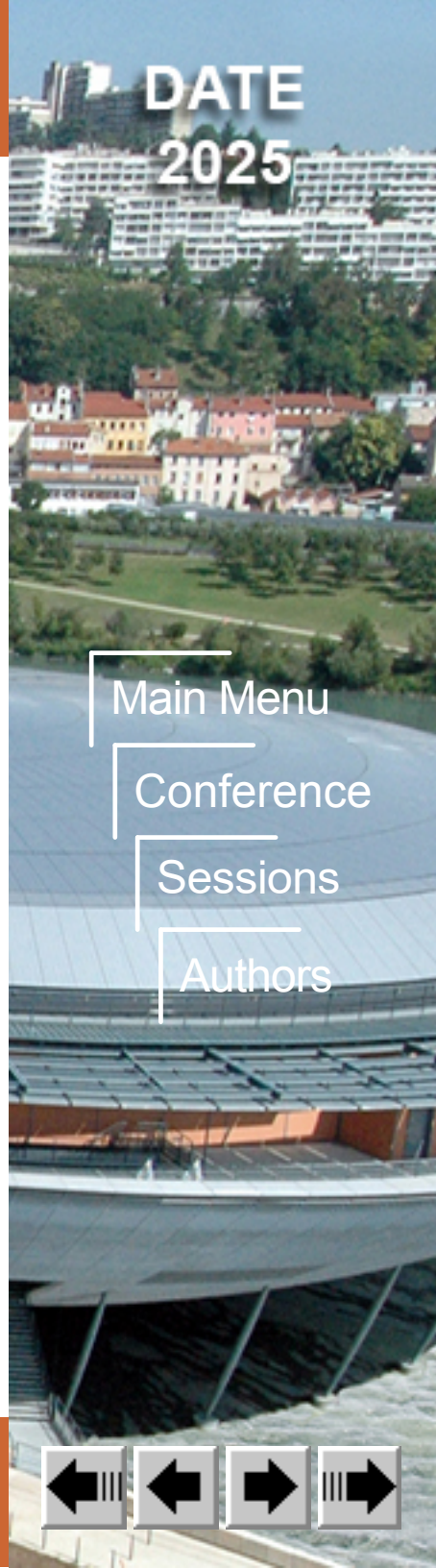
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- Dynamic IR-Drop Prediction through a Multi-Task U-Net with Package Effect Consideration
  Yu-Hsuan Chen, Yu-Chen Cheng, Yong-Fong Chang, Yu-Che Lee, Jia-Wei Lin, Hsun-Wei Pao, Peng-Wen Chen, Po-Yu Chen, Hao-Yun Chen, Yung-Chih Chen, Chun-Yao Wang, and Shih-Chieh Chang
- Minimum Time Maximum Fault Coverage Testing of Spiking Neural Networks
  Spyridon Raptis and Haralampos-G. Stratigopoulos
- EGIS: Entropy Guided Image Synthesis for Dataset-Agnostic Testing of RRAM-Based DNNs
  Anurup Saha, Chandramouli Amarnath, Kwondo Ma, and Abhijit Chatterjee
- NVSRLO: A FeFET-Based Non-Volatile and SEU-Recoverable Latch Design with Optimized Overhead
  Aibin Yan, Wangjin Jiang, Han Bao, Zhengfeng Huang, Tianming Ni, Xiaoqing Wen, and Patrick Girard
- InterA-ECC: Interconnect-Aware Error Correction in STT-MRAM
  Surendra Hemaram, Mahta Mayahinia, Mehdi B. Tahoori, Francky Catthoor, Siddharth Rao, Sebastien Couet, Tommaso Marinelli, Anita Farokhnejad, and Gouri Sankar Kar
- Assessing Soft Error Reliability in Vectorized Kernels: Vulnerability and Performance Trade-offs on Arm and RISC-V ISAs
  Geancarlo Abich

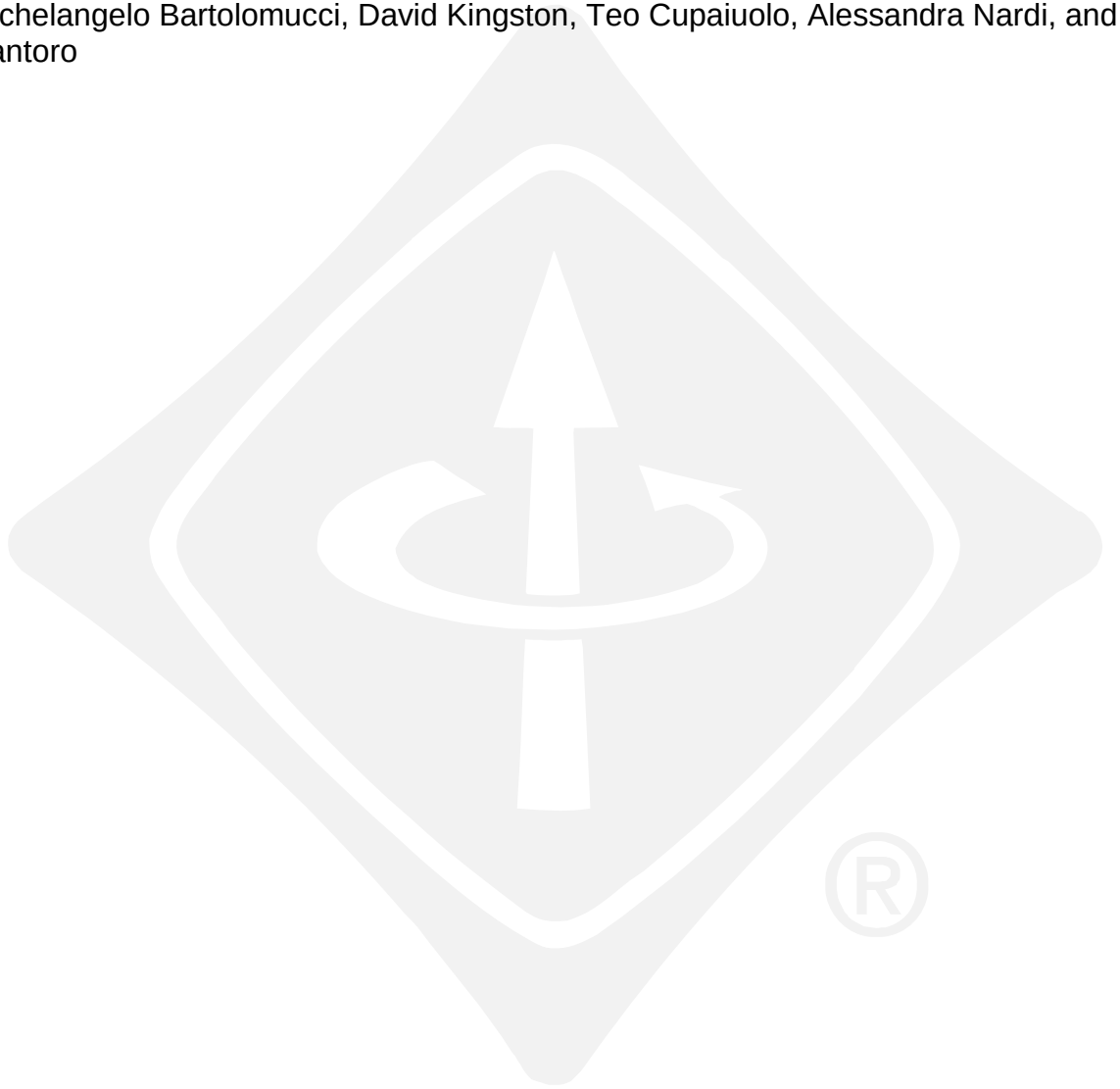
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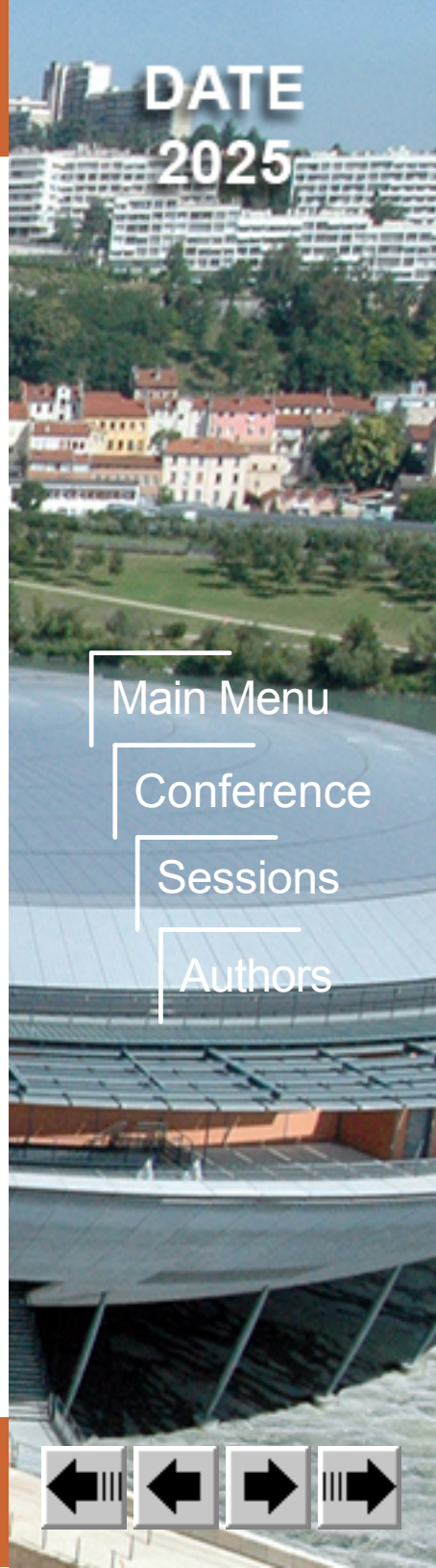
Papers by Session

- Early Functional Safety and PPA Evaluation of Digital Designs

  Michelangelo Bartolomucci, David Kingston, Teo Cupaiuolo, Alessandra Nardi, and Riccardo Cantoro



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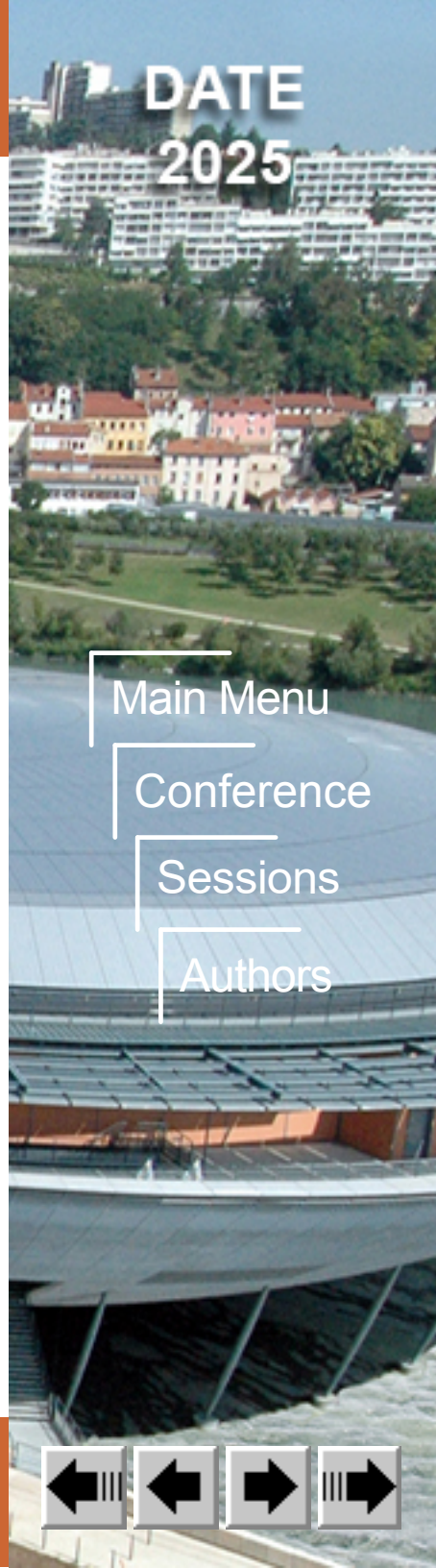


Papers by Session

System Simulation and Validation

- FloppyFloat: An Open Source Floating Point Library for Instruction Set Simulators
  Niko Zurstraßen, Nils Bosbach, and Rainer Leupers
- Handling Latch Loops in Timing Analysis with Improved Complexity and Divergent Loop Detection
  Xizhe Shi, Zizheng Guo, Yibo Lin, Runsheng Wang, and Ru Huang
- Static Global Register Allocation for Dynamic Binary Translators
  Niko Zurstraßen, Nils Bosbach, Lennart M. Reimann, and Rainer Leupers
- CorrectBench: Automatic Testbench Generation with Functional Self-Correction using LLMs for HDL Design
  Ruidi Qiu, Grace Li Zhang, Rolf Drechsler, Ulf Schlichtmann, and Bing Li
- CISGraph: A Contribution-Driven Accelerator for Pairwise Streaming Graph Analytics
  Songyu Feng, Mo Zou, Tian Zhi, and Zidong Du
- High-Performance ARM-on-ARM Virtualization for Multicore SystemC-TLM-Based Virtual Platforms
  Nils Bosbach, Rebecca Pelke, Niko Zurstraßen, Jan Henrik Weinstock, Lukas Jünger, and Rainer Leupers

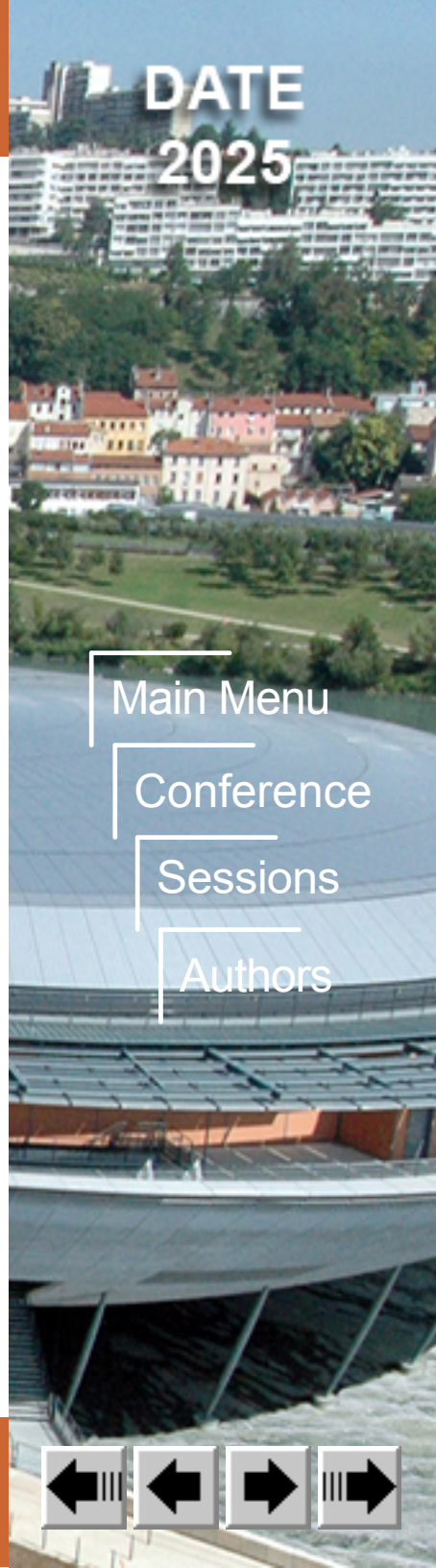
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Papers by Session

- RTHeter: Simulating Real-Time Scheduling of Multiple Tasks on Heterogeneous Architectures
  Yinchen Ni, Jiace Zhu, Yier Jin, and An Zou
- Fast Interpreter-Based Instruction Set Simulation for Virtual Prototypes
  Manfred Schlägl and Daniel Große
- c2c-gem5: Full System Simulation of Cache-Coherent Chip-to-Chip Interconnects
  Luis Bertran Alvarez, Ghassan Chehaibar, Stephen Busch, Pascal Benoit, and David Novo
- A 101 TOPS/W and 1.73 TOPS/mm^2 6T SRAM-Based Digital Compute-in-Memory Macro Featuring a Novel 2T Multiplier
  Priyanshu Tyagi and Sparsh Mittal

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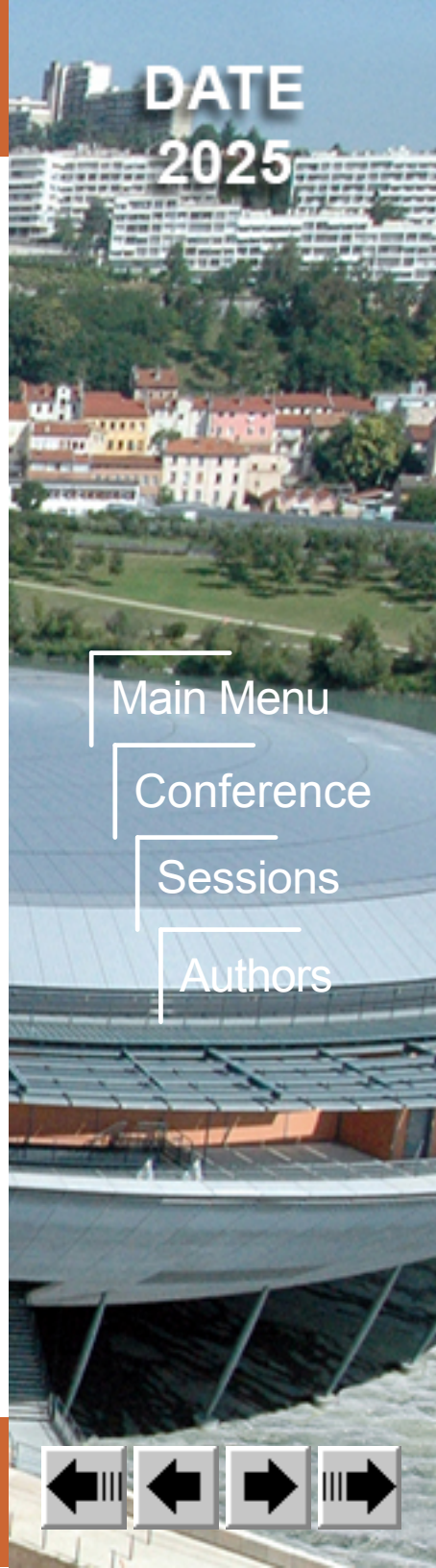


Papers by Session

Machine Learning Solutions for Embedded and Cyber-Physical Systems

- DE^{2}R: Unifying DVFS and Early-Exit for Embedded AI Inference via Reinforcement Learning
  Yuting He, Jingjin Li, Chengtai Li, Qingyu Yang, Zheng Wang, Heshan Du, Jianfeng Ren, and Heng Yu
- Continuous GNN-Based Anomaly Detection on Edge using Efficient Adaptive Knowledge Graph Learning
  Sanggeon Yun, Ryozo Masukawa, William Youngwoo Chung, Minhyoung Na, Nathaniel D. Bastian, and Mohsen Imani
- BMP-SD: Marrying Binary and Mixed-Precision Quantization for Efficient Stable Diffusion Inference
  Cheng Gu, Gang Li, Xiaolong Lin, Jiayao Ling, Jian Cheng, and Xiaoyao Liang
- Distributed Inference with Minimal Off-Chip Traffic for Transformers on Low-Power MCUs
  Severin Bochem, Victor J. B. Jung, Arpan Suravi Prasad, Francesco Conti, and Luca Benini
- HiFi-SAGE: High Fidelity GraphSAGE-Based Latency Estimators for DNN Optimization
  Shambhavi Balamuthu Sampath, Leon Hecht, Moritz Thoma, Lukas Frickenstein, Pierpaolo Mori, Nael Fasfous, Manoj Rohit Vemparala, Alexander Frickenstein, Walter Stechele, Daniel Mueller-Gritschneder, and Claudio Passerone

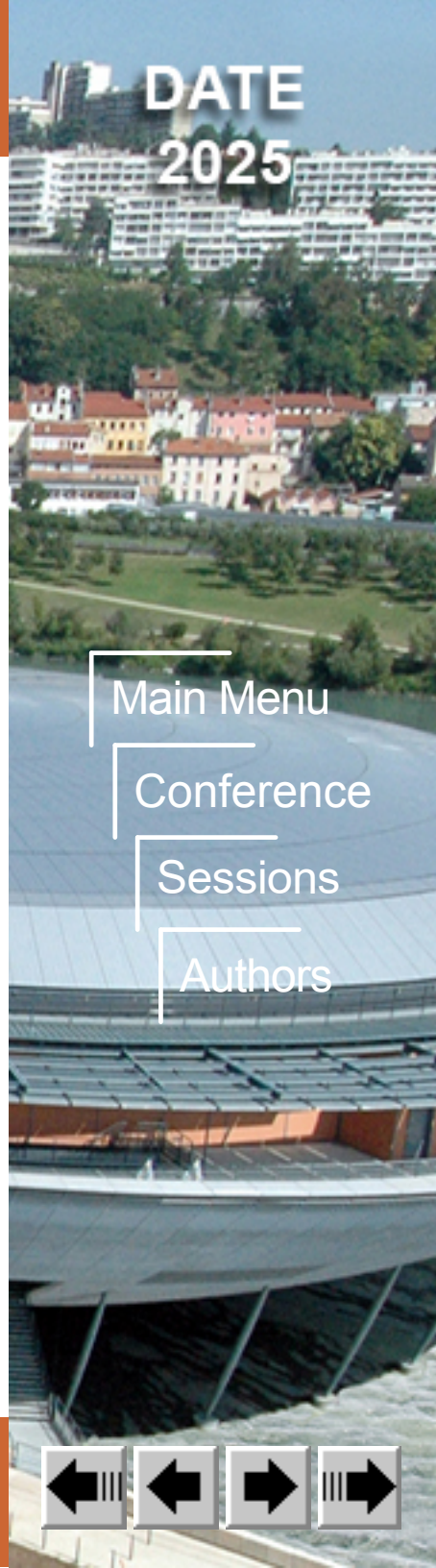
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Papers by Session

- SolarML: Optimizing Sensing and Inference for Solar-Powered TinyML Platforms
  Hao Liu, Qing Wang, and Marco Zuniga
- SAFELOC: Overcoming Data Poisoning Attacks in Heterogeneous Federated Machine Learning for Indoor Localization
  Akhil Singampalli, Danish Gufran, and Sudeep Pasricha
- Hybrid Token Selector Based Accelerator for ViTs
  Akshansh Yadav, Anadi Goyal, and Palash Das
- DAOP: Data-Aware Offloading and Predictive Pre-Calculation for Efficient MoE Inference
  Yujie Zhang, Shivam Aggarwal, and Tulika Mitra
- SpikeStream: Accelerating Spiking Neural Network Inference on RISC-V Clusters with Sparse Computation Extensions
  Simone Manoni, Paul Scheffler, Luca Zanatta, Andrea Acquaviva, Luca Benini, and Andrea Bartolini
- *REACT*: Randomized Encryption with AI-Controlled Targeting for Next-Gen Secure Communication
  Zhangying He and Hossein Sayadi
- DuSGAI: A Dual-Side Sparse GEMM Accelerator with Flexible Interconnects
  Wujie Zhong and Yangdi Lyu

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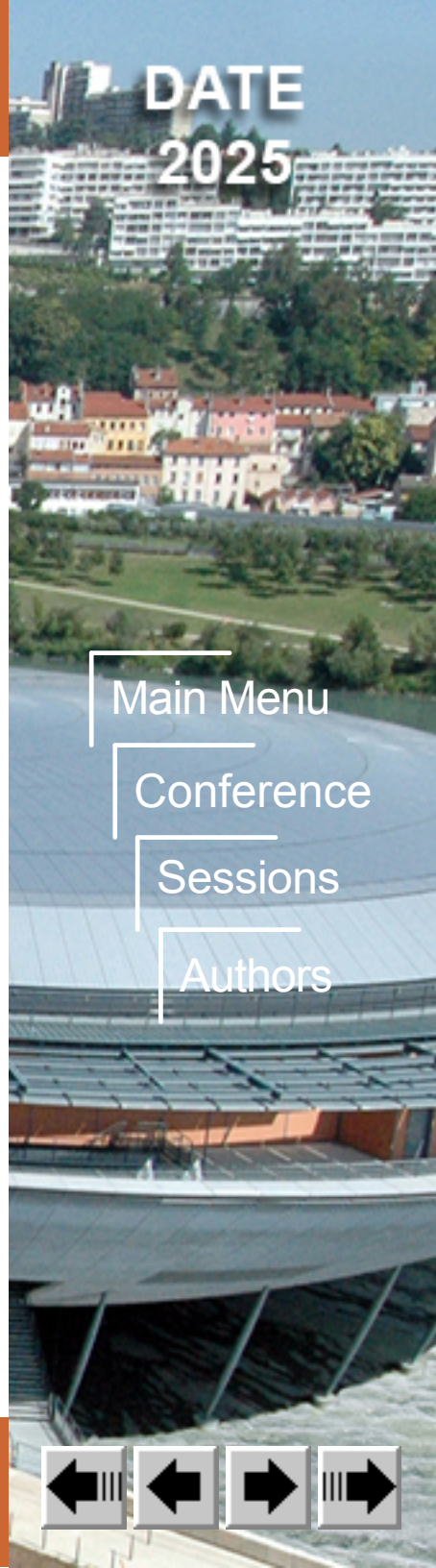


Papers by Session

Design and Test of Secure Systems

- DE2: SAT-Based Sequential Logic Decryption with a Functional Description
  You Li, Guannan Zhao, Yunqi He, and Hai Zhou
- Hardware/Software Runtime for GPSA Protection in RISC-V Embedded Cores
  Louis Savary, Simon Rokicki, and Steven Derrien
- Analog Circuit Anti-Piracy Security by Exploiting Device Ratings
  Hazem H. Hammam, Hassan Aboushady, and Haralampos-G. Stratigopoulos
- Side-Channel Collision Attacks against ASCON
  Hao Zhang, Yiwen Gao, Yongbin Zhou, and Jingdian Ming
- Cute-Lock: Behavioral and Structural Multi-Key Logic Locking using Time Base Keys
  Kevin Lopez and Amin Rezaei
- SafeLight: Enhancing Security in Optical Convolutional Neural Network Accelerators
  Salma Afifi, Ishan Thakkar, and Sudeep Pasricha
- One More Motivation to Use Evaluation Tools this Time for Hardware Multiplicative Masking of AES
  Hemin Rahimi and Amir Moradi

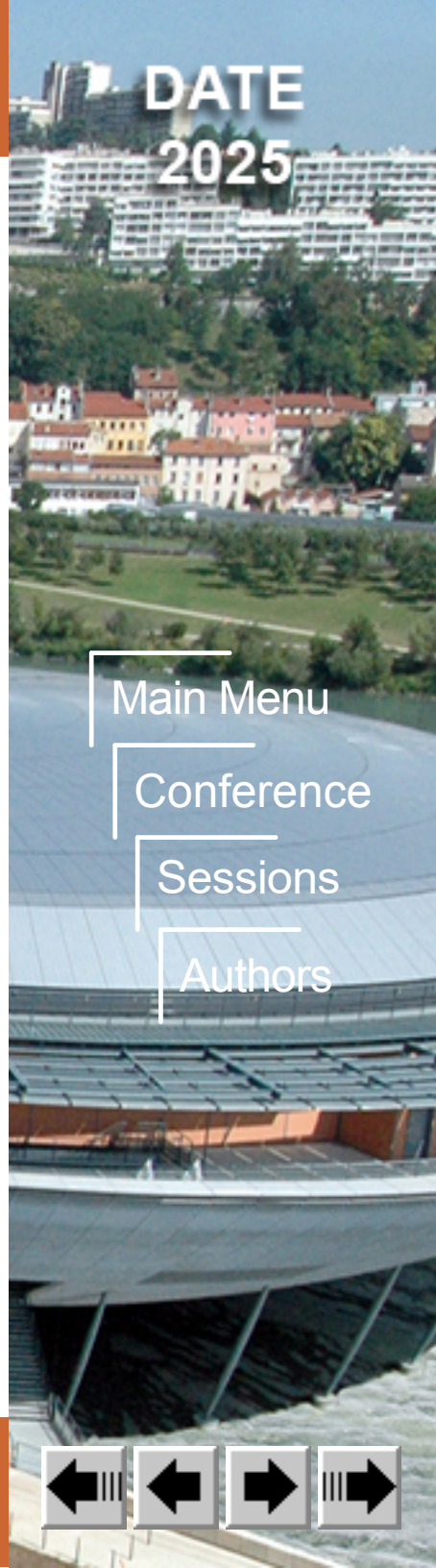
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Papers by Session

- Three Eyed Raven: An On-Chip Side Channel Analysis Framework for Run-Time Evaluation
  M Dhilipkumar, Priyanka Bagade, and Debapriya Basu Roy
- RTL-Breaker: Assessing the Security of LLMs against Backdoor Attacks on HDL Code Generation
  Lakshmi Likhitha Mankali, Jitendra Bhandari, Manaar Alam, Ramesh Karri, Michail Maniatakos, Ozgur Sinanoglu, and Johann Knechtel
- MC^3: Memory Contention-Based Covert Channel Communication on Shared DRAM System-on-Chips
  Ismet Dagli, James Crea, Soner Seckiner, Yuanchao Xu, Selçuk Köse, and Mehmet E. Belviranli
- Comb Frequency Division Multiplexing: A Non-Binary Modulation for AirGap Covert Channel Transmission
  Mohamed Alla Eddine Bahi, Maria Mendez Real, and Maxime Pelcat
- Multi-Sensor Data Fusion for Enhanced Detection of Laser Fault Injection Attacks in Cryptographic Hardware: Practical Results
  Mohammad Ebrahimabadi, Raphael Viera, Sylvain Guilley, Jean-Luc Danger, Jean-Max Dutertre, and Naghmeh Karimi

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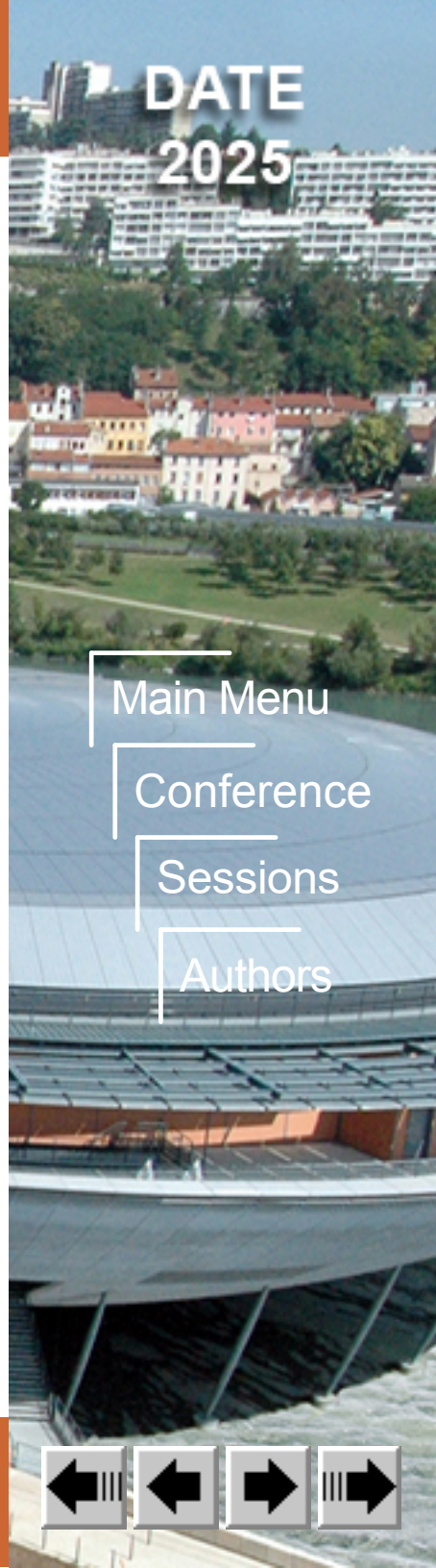


Papers by Session

Late Breaking Results on AI Algorithms and Architectures

- Late Breaking Results: Dynamically Scalable Pruning for Transformer-Based Large Language Models
  Junyoung Lee, Shinhyoung Jang, Seohyun Kim, Jongho Park, Il Hong Suh, Hoon Sung Chwa, and Yeseong Kim
- Late Breaking Results: AFS: Improving Accuracy of Quantized Mamba via Aggressive Forgetting Strategy
  Zhouquan Liu, Libo Huang, Ling Yang, Gang Chen, Wei Liu, Mingche Lai, and Yongwen Wang
- Late Breaking Results: Improving Deep SNNs with Gradient Clipping and Noise Exploitation in Neuromorphic Devices
  Seongsik Park, Jongkil Park, Hyun Jae Jang, Jaewook Kim, YeonJoo Jeong, Gyu Weon Hwang, Inho Kim, Jong-Keuk Park, Kyeong Seok Lee, and Suyoun Lee
- Late Breaking Results: Hyperdimensional Regression with Fine-Grained and Scalable Confidence-Based Learning
  Jiseung Kim, Hyunsei Lee, Tajana Rosing, Mohsen Imani, and Yeseong Kim
- Late Breaking Results: Approximated LUT-Based Neural Networks for FPGA Accelerated Inference
  Xuqi Zhu, Jiacheng Zhu, Huaizhi Zhang, Tamim M. Al-Hasan, Klaus D. McDonald-Maier, and Xiaojun Zhai

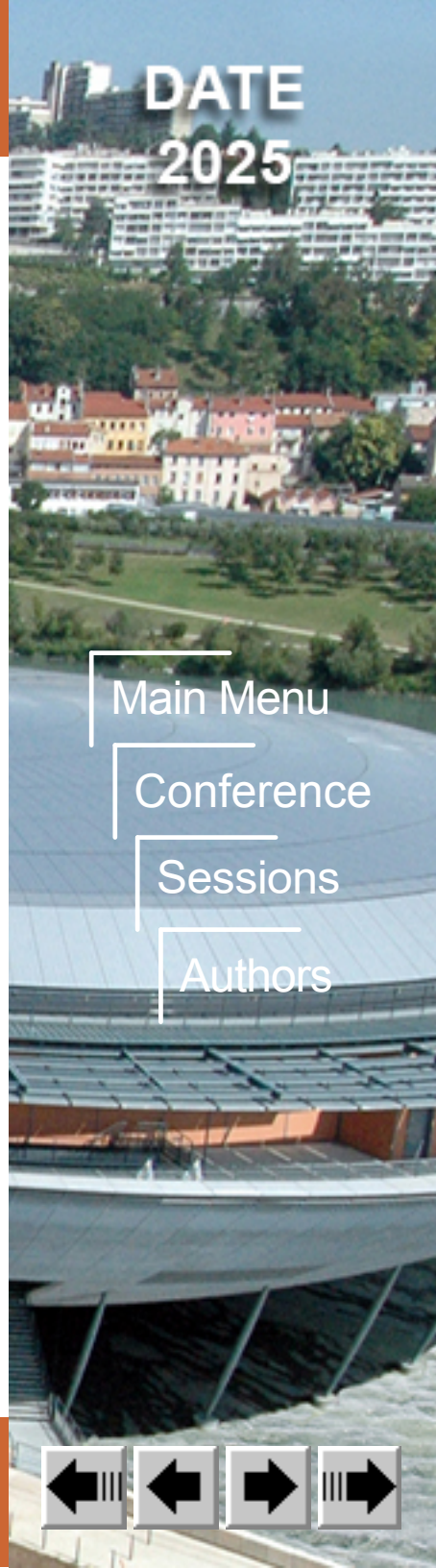
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Papers by Session

- Late Breaking Results: Leveraging Approximate Computing for Carbon-Aware DNN Accelerators
  Aikaterini Maria Panteleaki, Konstantinos Balaskas, Georgios Zervakis, Hussam Amrouch, and Iraklis Anagnostopoulos
- Late Breaking Results: Energy-Efficient Printed Machine Learning Classifiers with Sequential SVMs
  Spyridon Besias, Ilias Sertaridis, Florentia Afentaki, Konstantinos Balaskas, and Georgios Zervakis
- Late Breaking Results: Towards Efficient Formal Verification of Dot Product Architectures
  Lennart Weingarten, Kamalika Datta, and Rolf Drechsler

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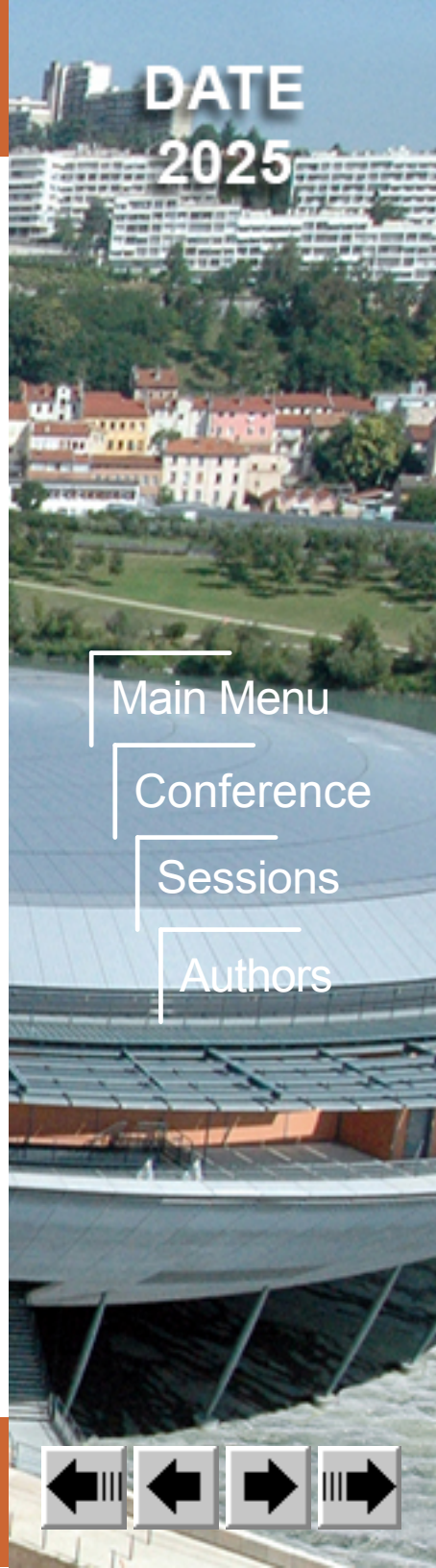


Papers by Session

Physical Analysis and Design

- MegaRoute: Universal Automated Large-Scale PCB Routing Method with Adaptive Step-Size Search
  Haiyun Li and Jixin Zhang
- Timing-Driven Global Placement with Hybrid Heuristics and Nadam-Based Net Weighting
  Linhao Lu, Wenxin Yu, Hongwei Tian, Chenjin Li, Xinmiao Li, Zhaoqi Fu, Zhengjie Zhao, and Jingwei Lu
- IR-Fusion: A Fusion Framework for Static IR Drop Analysis Combining Numerical Solution and Machine Learning
  Feng Guo, Jianwang Zhai, Jingyu Jia, Jiawei Liu, Kang Zhao, Bei Yu, and Chuan Shi
- Timing-Driven Detailed Placement with Unsupervised Graph Learning
  Dhoui Lim and Heechun Park
- Effective Macro Placement for Very Large Scale Designs using MCTS Guided by Pre-Trained RL
  Jai-Ming Lin, Zong-Ze Lee, and Nan-Chu Lin
- DAMIL-DCIM: A Digital CIM Layout Synthesis Framework with Dataflow-Aware Floorplan and MILP-Based Detailed Placement
  Chuyu Wang, Ke Hu, Fan Yang, Keren Zhu, and Xuan Zeng

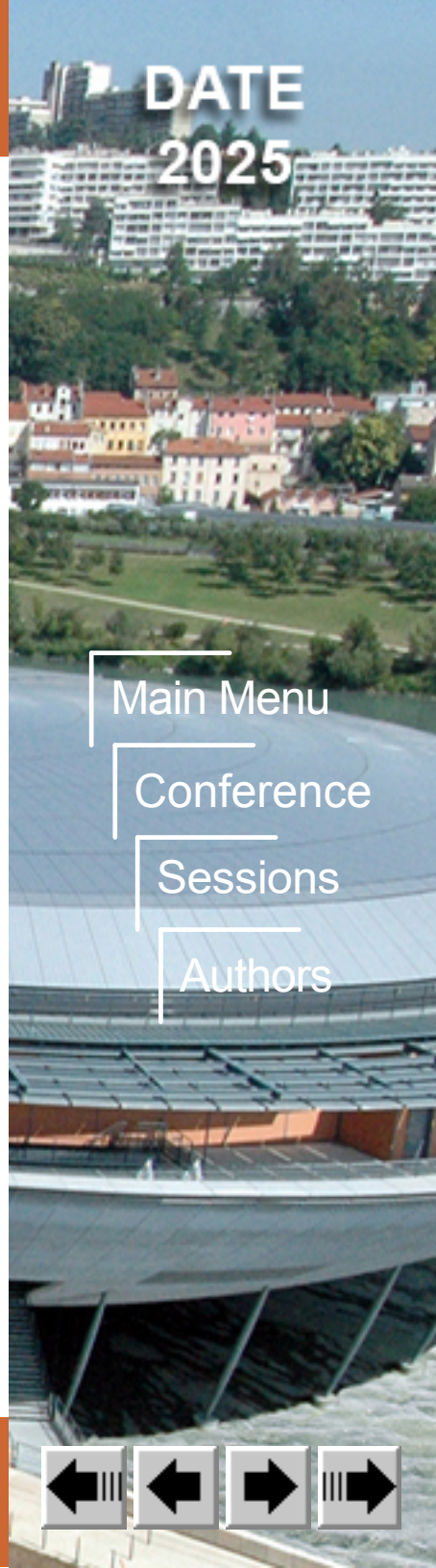
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Papers by Session

- Bi-Level Optimization Accelerated DRC-Aware Physical Design Automation for Photonic Devices
  Hao Chen, Yuzhe Ma, and Yeyu Tong
- GTN-Cell: Efficient Standard Cell Characterization using Graph Transformer Network
  Lihao Liu, Yunhui Li, Beisi Lu, Li Shang, and Fan Yang
- Wire-Bonding Finger Placement for FBGA Substrate Layout Design with Finger Orientation Consideration
  Yu-En Lin and Yi-Yu Liu
- A Parallel Floating Random Walk Solver for Reproducible and Reliable Capacitance Extraction
  Jiechen Huang, Shuailong Liu, and Wenjian Yu
- A Comprehensive Inductance-Aware Modeling Approach to Power Distribution Network in Heterogeneous 3D Integrated Circuits
  Quansen Wang, Vasilis F. Pavlidis, and Yuanqing Cheng

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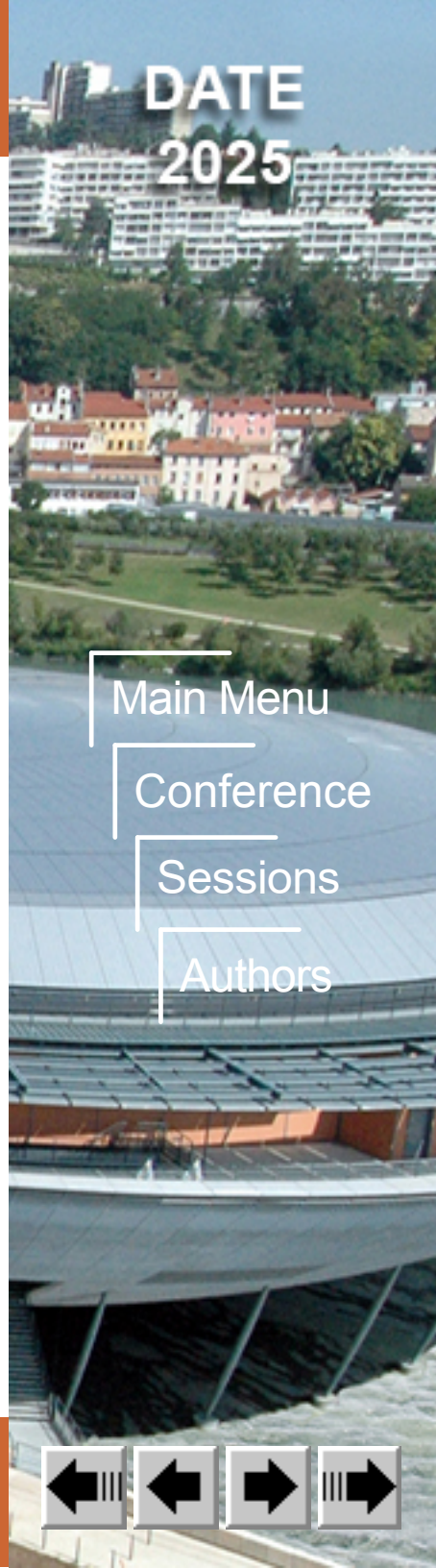


Papers by Session

Design Methodologies for Machine Learning Architectures

- SpNeRF: Memory Efficient Sparse Volumetric Neural Rendering Accelerator for Edge Devices
  Yipu Zhang, Jiawei Liang, Jian Peng, Jiang Xu, and Wei Zhang
- SBQ: Exploiting Significant Bits for Efficient and Accurate Post-Training DNN Quantization
  Jiayao Ling, Gang Li, Qinghao Hu, Xiaolong Lin, Cheng Gu, Jian Cheng, and Xiaoyao Liang
- AIrchitect v2: Learning the Hardware Accelerator Design Space through Unified Representations
  Jamin Seo, Akshat Ramachandran, Yu-Chuan Chuang, Anirudh Itagi, and Tushar Krishna
- Zebra: Leveraging Diagonal Attention Pattern for Vision Transformer Accelerator
  Sukhyun Han, Seongwook Kim, Gwangeun Byeon, Jihun Yoon, and Seokin Hong
- Pushing up to the Limit of Memory Bandwidth and Capacity Utilization for Efficient LLM Decoding on Embedded FPGA
  Jindong Li, Tenglong Li, Guobin Shen, Dongcheng Zhao, Qian Zhang, and Yi Zeng
- Leveraging Compute-in-Memory for Efficient Generative Model Inference in TPUs
  Zhantong Zhu, Hongou Li, Wenjie Ren, Meng Wu, Le Ye, Ru Huang, and Tianyu Jia

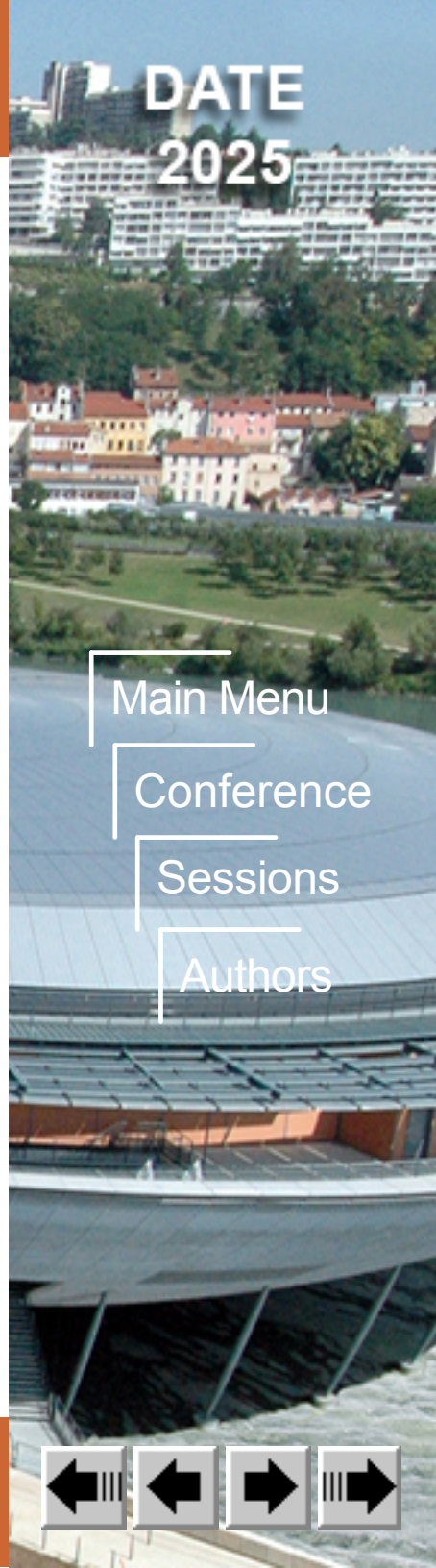
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Papers by Session

- *SparseInfer*: Training-Free Prediction of Activation Sparsity for Fast LLM Inference
  Jiho Shin, Hoeseok Yang, and Youngmin Yi
- Low-Rank Compression for IMC Arrays
  Kang Eun Jeon, Johnny Rhe, and Jong Hwan Ko
- Integer Unit-Based Outlier-Aware LLM Accelerator Preserving Numerical Accuracy of FP-FP GEMM
  Jehun Lee and Jae-Joon Kim
- Leveraging Hot Data in a Multi-Tenant Accelerator for Effective Shared Memory Management
  Chunmyung Park, Jicheon Kim, Eunjae Hyun, Xuan Truong Nguyen, and Hyuk-Jae Lee
- DOTS: DRAM-PIM Optimization for Tall and Skinny GEMM Operations in LLM Inference
  Gyeonghwan Park, Sanghyeok Han, Byungkuk Yoon, and Jae-Joon Kim
- LLM4GV: An LLM-Based Flexible Performance-Aware Framework for GEMM Verilog Generation
  Dingyang Zou, Gaoche Zhang, Kairui Sun, Zhe Wen, Meiqi Wang, and Zhongfeng Wang

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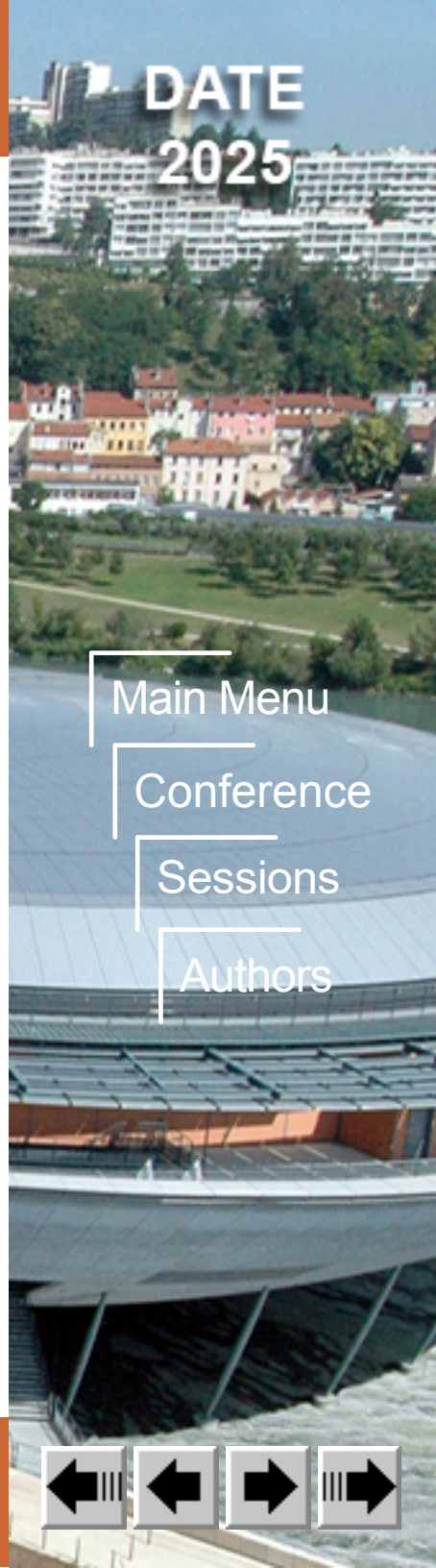


Papers by Session

Design and Test of Hardware Security Primitives

- Using OFF-Set Only for Corrupting Circuit to Resist Structural Attack in CAC Locking
  Hsiang-Chun Cheng, RuiJie Wang, and TingTing Hwang
- Runtime Security Analysis of Monolithic 3D Embedded DRAM with Oxide-Channel Transistor
  Eduardo Ortega, Jungyoun Kwak, Shimeng Yu, and Krishnendu Chakrabarty
- Exploring Large Integer Multiplication for Cryptography Targeting In-Memory Computing
  Florian Krieger, Florian Hirner, and Sujoy Sinha Roy
- A Low-Complexity True Random Number Generation Scheme using 3D-NAND Flash Memory
  Ruibin Zhou, Jian Huang, Xianping Liu, Yuhan Wang, Xinrui Zhang, Yungen Peng, and Zhiyi Yu
- A Synthesizable Thyristor-Like Leakage-Based True Random Number Generator
  Seohyun Kim, Jang Hyun Kim, and Jongmin Lee
- Grafted Trees Bear Better Fruit: An Improved Multiple-Valued Plaintext-Checking Side-Channel Attack against Kyber
  Jinnuo Li, Chi Cheng, Muyan Shen, Peng Chen, Qian Guo, Dongsheng Liu, Liji Wu, and Jian Weng

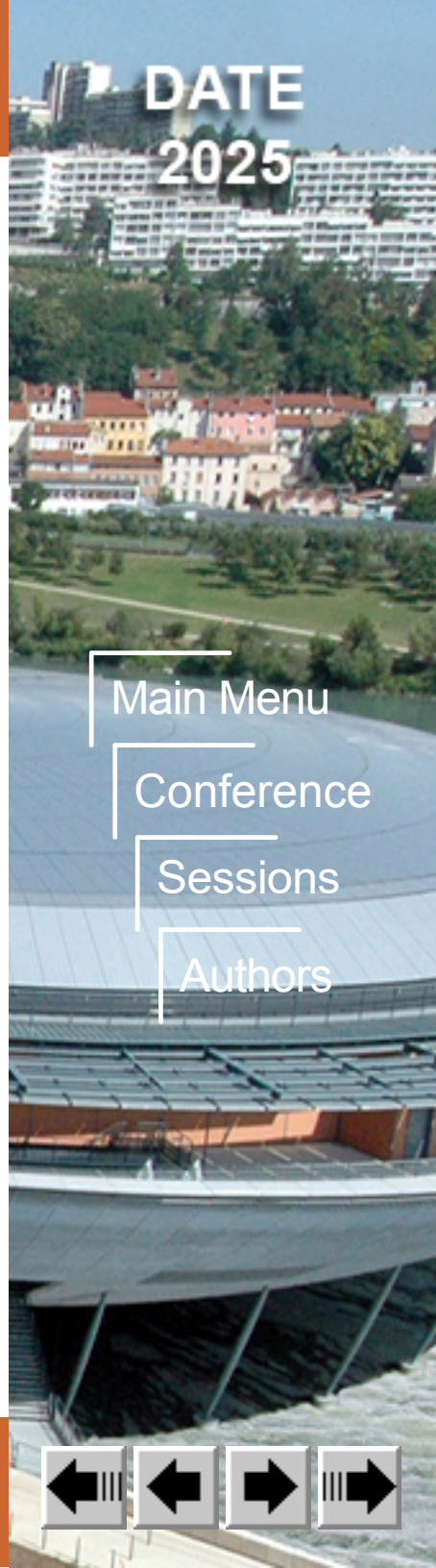
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Papers by Session

- CAS-PUF: Current-Mode Array-Type Strong PUF for Secure Computing in Area Constrained SoCs
  Dimosthenis Georgoulas, Yiorgos Tsiatouhas, and Vasileios Tenentes
- FLASH: An Efficient Hardware Accelerator Leveraging Approximate and Sparse FFT for Homomorphic Encryption
  Tengyu Zhang, Yufei Xue, Ling Liang, Zhen Gu, Yuan Wang, Runsheng Wang, Ru Huang, and Meng Li
- HFL: Hardware Fuzzing Loop with Reinforcement Learning
  Lichao Wu, Mohamadreza Rostami, Huimin Li, and Ahmad-Reza Sadeghi
- REAP-NVM: Resilient Endurance-Aware NVM-Based PUF against Learning-Based Attacks
  Hassan Nassar, Ming-Liang Wei, Chia-Lin Yang, Jörg Henkel, and Kuan-Hsun Chen
- Accelerating Oblivious Transfer with a Pipelined Architecture
  Xiaolin Li, Wei Yan, Hongwei Liu, Yong Zhang, Qinfen Hao, Yong Liu, and Ninghui Sun

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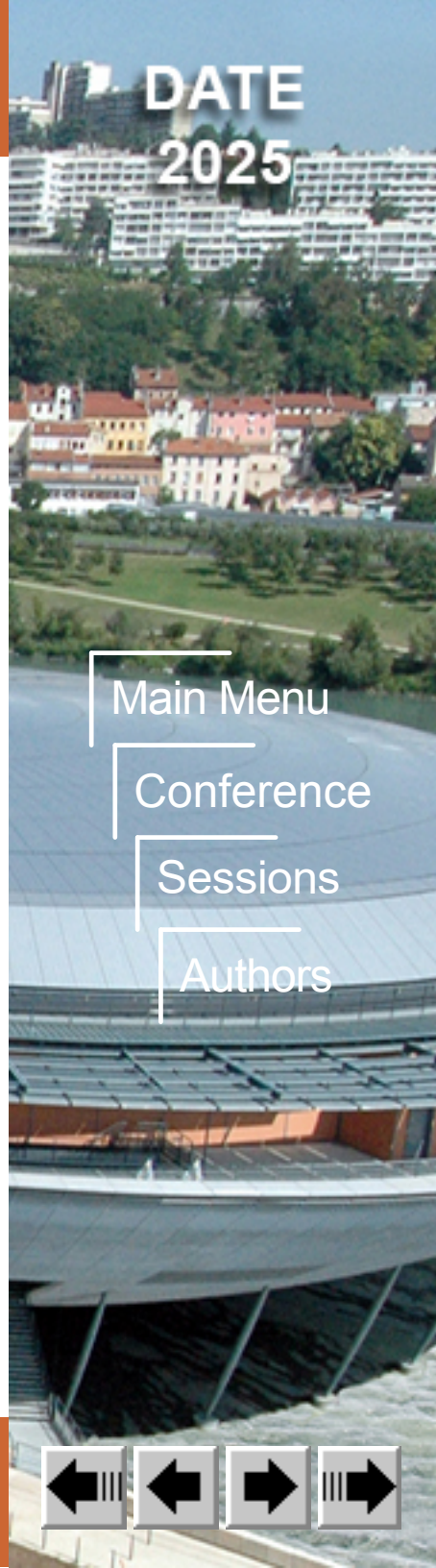


Papers by Session

Reconfigurable Systems

- FPGA-Based Acceleration of MCMC Algorithm through Self-Shrinking for Big Data
  Shuanglong Liu, Shiyu Peng, and Wan Shen
- ATE-GCN: An FPGA-Based Graph Convolutional Network Accelerator with Asymmetrical Ternary Quantization
  Ruiqi Chen, Jiayu Liu, Shidi Tang, Yang Liu, Yanxiang Zhu, Ming Ling, and Bruno da Silva
- PreVV: Eliminating Store Queue via Premature Value Validation for Dataflow Circuit on FPGA
  Kuangjie Zou, Yifan Zhang, Zicheng Zhang, Guoyu Li, Jianli Chen, Kun Wang, and Jun Yu
- PEARL: FPGA-Based Reinforcement Learning Acceleration with Pipelined Parallel Environments
  Jiayi Li, Hongxiao Zhao, Wenshuo Yue, Yihan Fu, Daijing Shi, Anjunyi Fan, Yuchao Yang, and Bonan Yan
- AiSpGEMM: Accelerating Imbalanced SpGEMM on FPGAs with Flexible Interconnect and Intra-Row Parallel Merging
  Enhao Tang, Shun Li, Hao Zhou, Guohao Dai, Jun Lin, and Kun Wang
- FAMERS: An FPGA Accelerator for Memory-Efficient Edge-Rendered 3D Gaussian Splatting
  Yuanfang Wang, Yu Li, Jianli Chen, Jun Yu, and Kun Wang

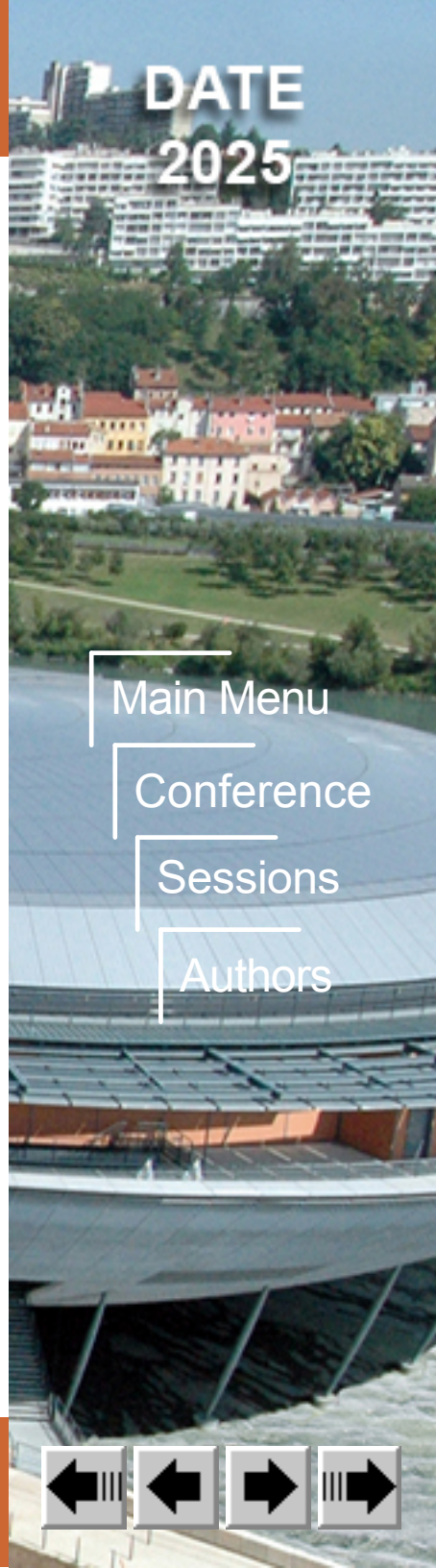
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Papers by Session

- SmartMap: Architecture-Agnostic CGRA Mapping using Graph Traversal and Reinforcement Learning
  Fábio T. Ramos, Pedro E. F. Realino, A. Wagner, Alex B. Vieira, Ricardo S. Ferreira, and José Augusto M. Nacif
- Dataflow Optimized Reconfigurable Acceleration for FEM-Based CFD Simulations
  Anastassis Kapetanakis, Aggelos Ferikoglou, George Anagnostopoulos, and Sotirios Xydis
- A Resource-Aware Residual-Based Gaussian Belief Propagation Accelerator Toolflow
  Omar Sharif and Christos-Savvas Bouganis
- UNIT: A Highly Unified and Memory-Efficient FPGA-Based Accelerator for Torus FHE
  Yuying Zhang, Sharad Sinha, Jiang Xu, and Wei Zhang
- RGHT-Q: Reconfigurable GEMM Unit for Heterogeneous-Homogeneous Tensor Quantization
  Seungho Lee, Donghyun Nam, and Jeongwoo Park

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Papers by Session

Multi-Partner Projects

- Multi-Partner Project: Securing Future Edge-AI Processors in Practice (CONVOLVE)

  Sven Argo, Henk Corporaal, Alejandro Garza, Marc Geilen, Manil Dev Gomony, Tim Güneysu, Adrian Marotzke, Fouwad Mir, Jan Richter-Brockmann, Jeffrey Smith, Mottaqiallah Taouil, and Said Hamdioui

- Multi-Partner Project: Open-Source Design Tools for Co-Development of AI Algorithms and AI Chips (Initial Stage)

  Mehdi Tahoori, Jürgen Becker, Jörg Henkel, Wolfgang Kunz, Ulf Schlichtmann, Georg Sigl, Jürgen Teich, and Norbert Wehn

- Multi-Partner Project: Sustainable Textile Electronics (STELEC)

  Bo Zhou, Mengxi Liu, Sizhen Bian, Daniel Geißler, Paul Lukowicz, Jose Miranda, Jonathan Dan, David Atienza, Mohamed Amine Riahi, Nobert Wehn, Russel Torah, Sheng Yong, Jidong Liu, Stephen Beeby, Magdalena Kohler, Berit Greinke, Junchun Yu, Vincent Nierstrasz, Leila Sheldrick, Rebecca Stewart, Tommaso Nieri, Matteo Maccanti, and Daniele Spinelli

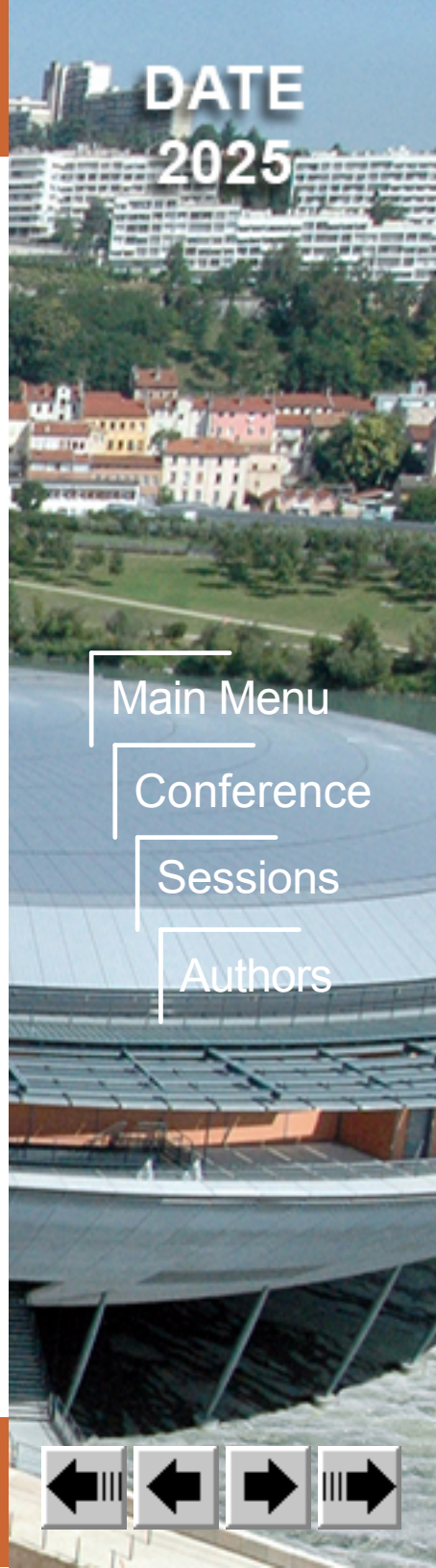
- Multi-Partner Project: Twinning for Excellence in Reliable Electronics (TWIN-RELECT)

  Marko Andjelkovic, Fabian Vargas, Milos Krstic, Luigi Dilillo, Alain Michez, Frederic Wrobel, Davide Bertozzi, Mikel Lujan, Christos Georgakidis, Nikolaos Chatzivangelis, Katerina Tsilingiri, Nikolaos Zazatis, Georgios Ioanis Paliaroutis, Pelopidas Tsoumanis, and Christos Sotiriou

- Multi-Partner Project: LoLiPoP-IoT – Design and Simulation of Energy-Efficient Devices for the Internet of Things

  Jakub Lojda, Josef Strnadel, Pavel Smrz, and Vaclav Simek

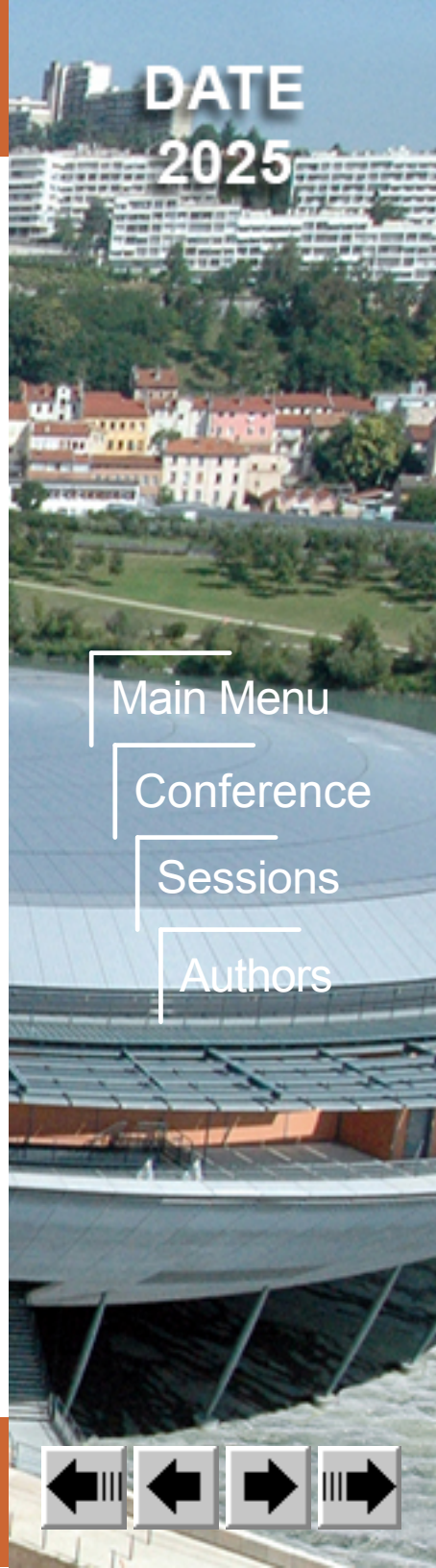
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Papers by Session

- Multi-Partner Project: Reverse Engineering Methods for Trusted Chip Design (RESEC)
  Bernhard Lippmann, Johanna Baehr, Alexander Hepp, and Horst Gieser
- Multi-Partner Project: Smart Sensor Analog Front-Ends Powered by Emerging Reconfigurable Devices (SENSOTERIC)
  Giulio Galderisi, Andreas Kramer, Andreas Fuchsberger, Jose Maria Gonzalez-Medina, Yuxuan He, Lee-Chi Hung, Marrit Jen Hong Li, Julian Kulenkampff, Maximilian Reuter, Lukas Wind, Masiar Sistani, Thomas Mikolajick, Bruno Neckel-Wesling, Marina Deng, Cristell Maneux, Pieter Harpe, Sonia Prado Lopez, Oskar Baumgartner, Chhandak Mukherjee, Eugenio Cantatore, Sandro Carrara, Klaus Hofmann, Walter M. Weber, and Jens Trommer
- Multi-Partner Project: Secure Hardware Accelerated Data Analytics for 6G Networks: The PRIVATEER Approach
  Ilias Papalamprou, Aimilios Leftheriotis, Apostolos Garos, Georgios Gardikis, Maria Christopoulou, George Xilouris, Lampros Argyriou, Antonia Karamatskou, Nikolaos Papadakis, Emmanouil Kalotychos, Nikolaos Chatzivasileiadis, Dimosthenis Masouros, George Theodoridis, and Dimitrios Soudris

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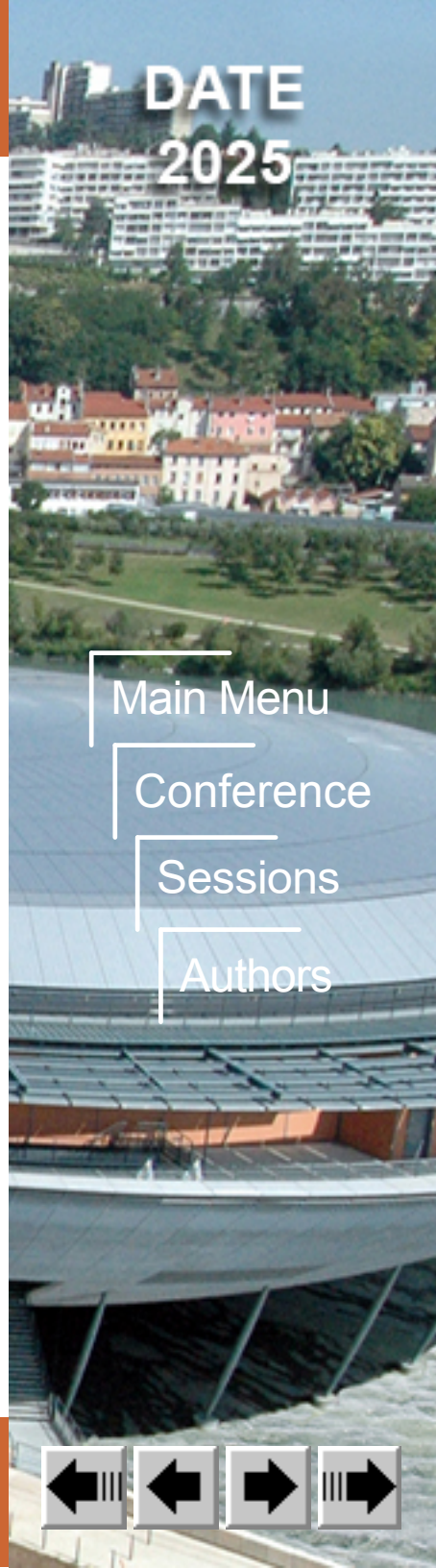
Papers by Session

Focus Session - Designing Secure Space Systems

- Designing Secure Space Systems

  Zain A. H. Hammadeh, Mohammad Hamad, Andrzej Olchawa, Milenko Starcik, Ricardo Fradique, Stefan Langhammer, Manuel Hoffmann, Florian Göhler, Daniel Lüdtke, Michael Felderer, and Sebastian Steinhorst

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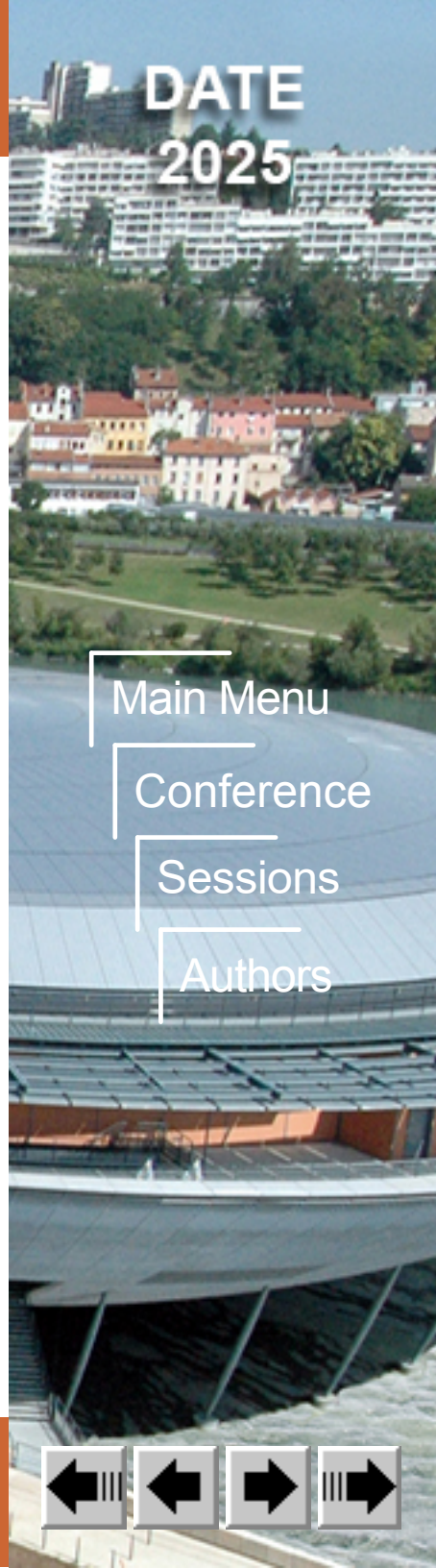


Papers by Session

Logical Analysis and Design

- Hybrid Exact and Heuristic Efficient Transistor Network Optimization for Multi-Output Logic
  Lang Feng, Rongjian Liang, and Hongxin Kong
- Maximum Fanout-Free Window Enumeration: Towards Multi-Output Sub-Structure Synthesis
  Ruofei Tang, Xuliang Zhu, Lei Chen, Xing Li, Xin Huang, Mingxuan Yuan, and Jianliang Xu
- SimGen: Simulation Pattern Generation for Efficient Equivalence Checking
  Carmine Rizzi, Sarah Brunner, Alan Mishchenko, and Lana Josipović
- ELMap: Area-Driven LUT Mapping with *k*-LUT Network Exact Synthesis
  Hongyang Pan, Keren Zhu, Fan Yang, Zhufei Chu, and Xuan Zeng
- Application of Formal Methods (SAT/SMT) to the Design of Constrained Codes
  Sunil Sudhakaran, Clark Barrett, and Mark Horowitz
- WideGate: Beyond Directed Acyclic Graph Learning in Subcircuit Boundary Prediction
  Jiawei Liu, Zhiyan Liu, Xun He, Jianwang Zhai, Zhengyuan Shi, Qiang Xu, Bei Yu, and Chuan Shi

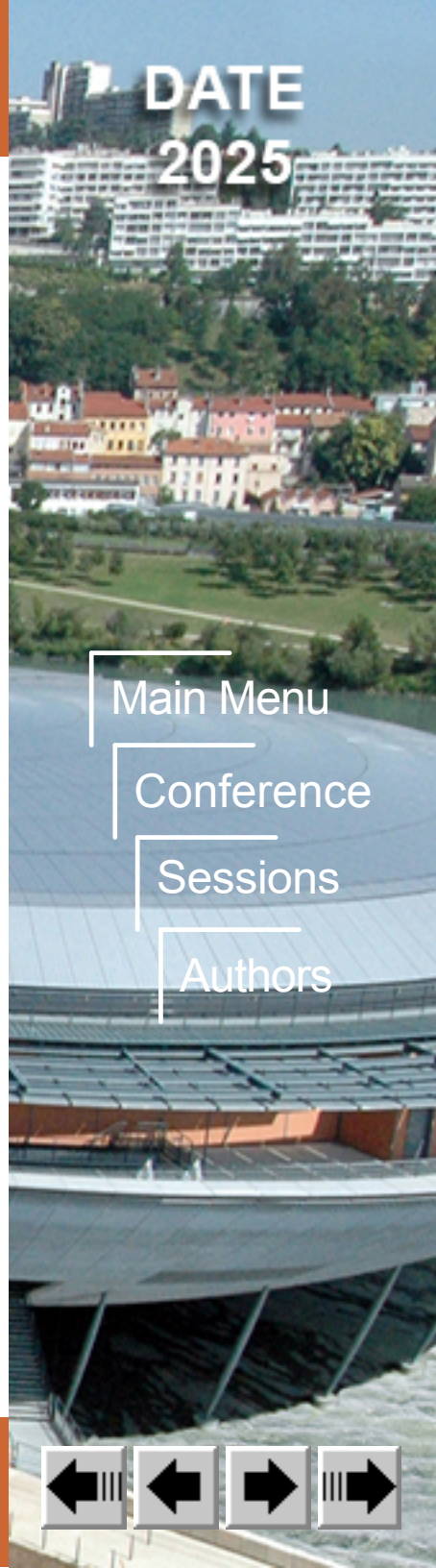
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Papers by Session

- Bias by Design: Diversity Quantification to Mitigate Structural Bias Effects in AIG Logic Optimization
  Isabella Venancia Gardner, Marcel Walter, Yukio Miyasaka, Robert Wille, and Michael Cochez
- Timing-Driven Approximate Logic Synthesis Based on Double-Chase Grey Wolf Optimizer
  Xiangfei Hu, Yuyang Ye, Tinghuan Chen, Hao Yan, and Bei Yu
- iRw: An Intelligent Rewriting
  Haisheng Zheng, Haoyuan Wu, Zhuolun He, Yuzhe Ma, and Bei Yu
- Automatic Routing for Photonic Integrated Circuits under Delay Matching Constraints
  Yuchao Wu, Weilong Guan, Yeyu Tong, and Yuzhe Ma
- ML-Based AIG Timing Prediction to Enhance Logic Optimization
  Wenjing Jiang, Jin Yan, and Sachin S. Sapatnekar

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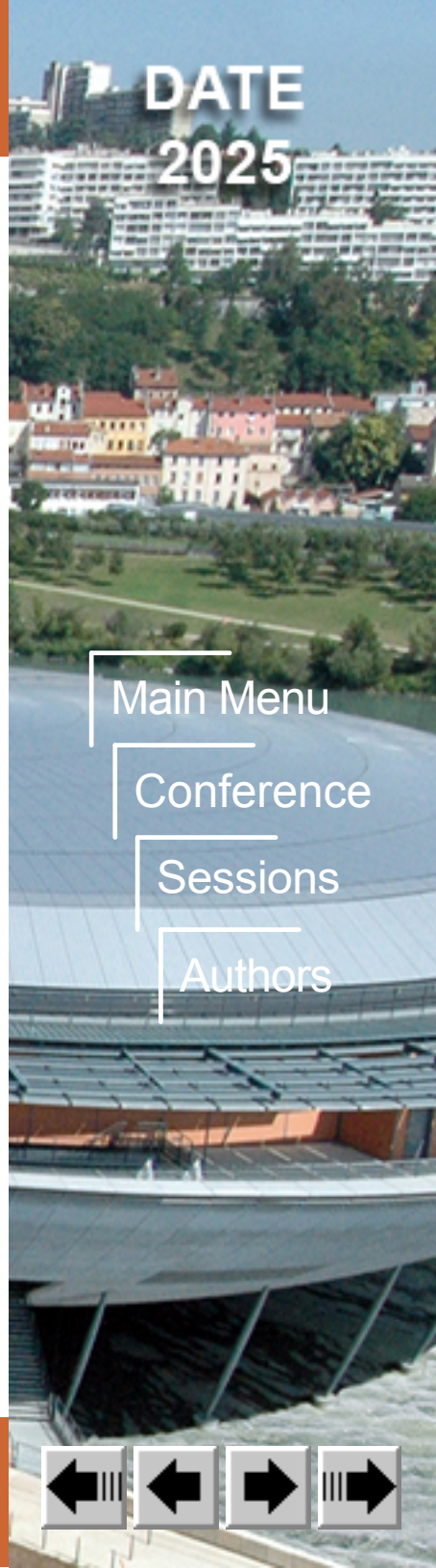


Papers by Session

Design and Test for Machine Learning and Machine Learning for Design and Test

- HyAtten: Hybrid Photonic-Digital Architecture for Accelerating Attention Mechanism
  Huize Li, Dan Chen, and Tulika Mitra
- SEGA-DCIM: Design Space Exploration-Guided Automatic Digital CIM Compiler with Multiple Precision Support
  Haikang Diao, Haoyi Zhang, Jiahao Song, Haoyang Luo, Yibo Lin, Runsheng Wang, Yuan Wang, and Xiyuan Tang
- SoftmAP: Software-Hardware Co-Design for Integer-Only Softmax on Associative Processors
  Mariam Rakka, Jinhao Li, Guohao Dai, Ahmed Eltawil, Mohammed E. Fouda, and Fadi Kurdahi
- Comprehensive RISC-V Floating-Point Verification: Efficient Coverage Models and Constraint-Based Test Generation
  Tianyao Lu, Anlin Liu, Bingjie Xia, and Peng Liu
- WinAcc: Window-Based Acceleration of Neural Networks using Block Floating Point
  Xin Ju, Jun He, Mei Wen, Jing Feng, Yasong Cao, Junzhong Shen, Zhaoyun Chen, and Yang Shi

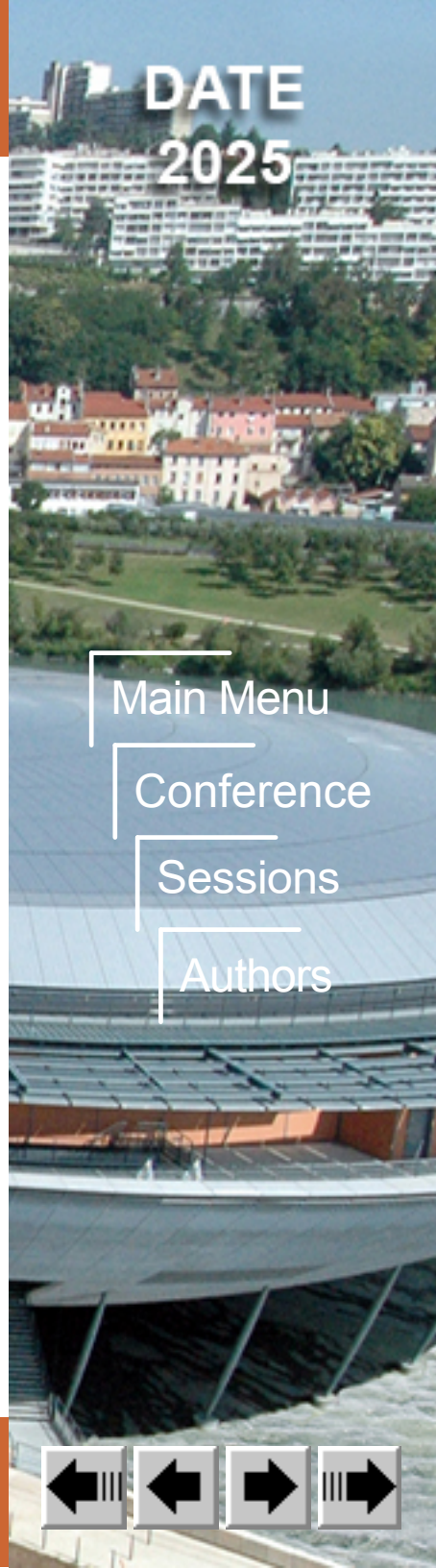
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Papers by Session

- SACPlace: Multi-Agent Deep Reinforcement Learning for Symmetry-Aware Analog Circuit Placement
  Lei Cai, Guojing Ge, Guibo Zhu, Jixin Zhang, Jinqiao Wang, Bowen Jia, and Ning Xu
- Linearization of Quadrature Digital Power Amplifiers by Neural Network of ULR_LSTM: Unsupervised Learning Residual LSTM
  Jiayu Yang, Luyi Guo, Yicheng Li, Wang Wang, Zixu Li, Manni Li, Zijian Huang Yinyin Lin, Yun Yin, and Hongtao Xu
- Compatibility Graph Assisted Automatic Hardware Trojan Insertion Framework
  Gaurav Kumar, Ashfaq Hussain Shaik, Anjum Riaz, Yamuna Prasad, and Satyadev Ahlawat
- Towards Robust RRAM-Based Vision Transformer Models with Noise-Aware Knowledge Distillation
  Wenyong Zhou, Zhengwu Liu, Taiqiang Wu, Chenchen Ding, Yuan Ren, and Ngai Wong
- HyIMC: Analog-Digital Hybrid In-Memory Computing SoC for High-Quality Low-Latency Speech Enhancement
  Wanru Mao, Hanjie Liu, Guangyao Wang, Tianshuo Bai, Jingcheng Gu, Han Zhang, Xitong Yang, Aifei Zhang, Xiaohang Wei, Meng Wang, and Wang Kang

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Papers by Session

Design and Test for Analog and Mixed-Signal Circuits / Systems / MEMS

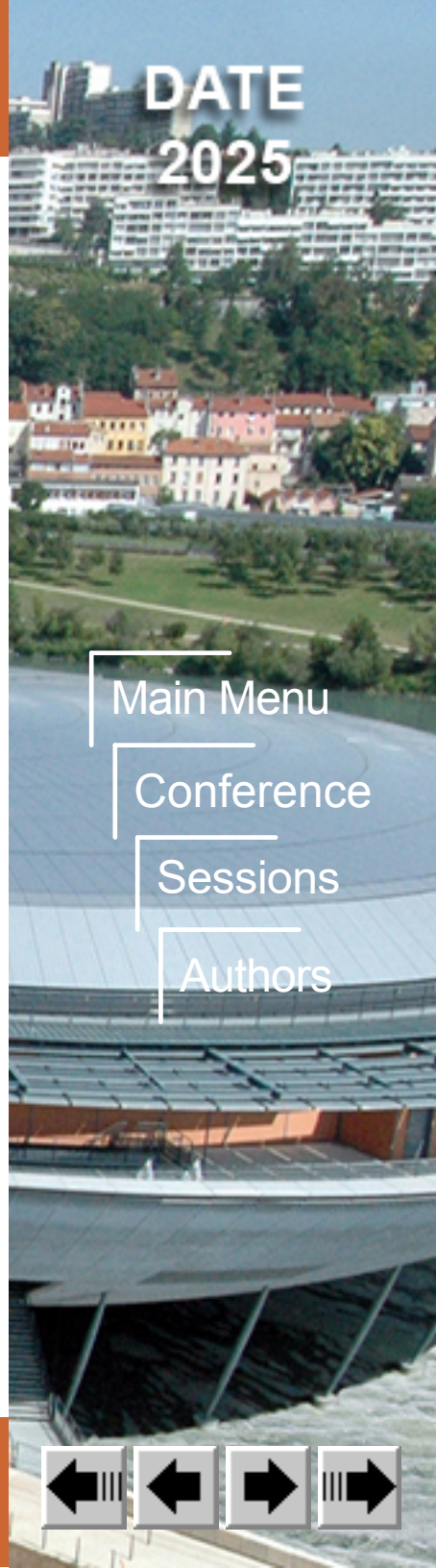
- INTO-OA: Interpretable Topology Optimization for Operational Amplifiers
  Jinyi Shen, Fan Yang, Li Shang, Zhaori Bi, Changhao Yan, Dian Zhou, and Xuan Zeng
- Effective Analog ICs Floorplanning with Relational Graph Neural Networks and Reinforcement Learning
  Davide Basso, Luca Bortolussi, Mirjana Videnovic-Misic, and Husni Habal
- Formally Verifying Analog Neural Networks with Device Mismatch Variations
  Yasmine Abu-Haeyeh, Thomas Bartelsmeier, Tobias Ladner, Matthias Althoff, Lars Hedrich, and Markus Olbrich
- Post-Layout Automated Optimization for Capacitor Array in Digital-To-Time Converter
  Hefei Wang, Jianghao Su, Junhe Xue, Haoran Lyu, Junhua Zhang, Longyang Lin, Kai Chen, Lijuan Yang, and Shenghua Zhou
- Time-Domain 3D Electromagnetic Fields Estimation Based on Physics-Informed Deep Learning Framework
  Huifan Zhang, Yun Hu, and Pingqiang Zhou

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Papers by Session

- TPC-GAN: Batch Topology Synthesis for Performance-Compliant Operational Amplifiers using Generative Adversarial Networks
  YuHao Leng, Jinglin Han, Yining Wang, and Peng Wang
- Nanoelectromechanical Binary Comparator for Edge-Computing Applications
  Victor Marot, Manu Bala Krishnan, Mukesh Kumar Kulsreshath, Elliott Worsey, Roshan Weerasekera, and Dinesh Pamunuwa
- Clock and Power Supply-Aware High Accuracy Phase Interpolator Layout Synthesis
  Siou-Sian Lin, Shih-Yu Chen, Yu-Ping Huang, Tzu-Chuan Lin, Hung-Ming Chen, and Wei-Zen Chen
- ML-Based Fast and Accurate Performance Modeling and Prediction for High-Speed Memory Interfaces across Different Technologies
  Taehoon Kim, Minjeong Kim, Hankyu Chi, Byungjun Kang, Eunji Song, and Woo-Seok Choi
- Accelerating OTA Circuit Design: Transistor Sizing Based on a Transformer Model and Precomputed Lookup Tables
  Subhadip Ghosh, Endalk Y. Gebru, Chandramouli V. Kashyap, Ramesh Harjani, and Sachin S. Sapatnekar

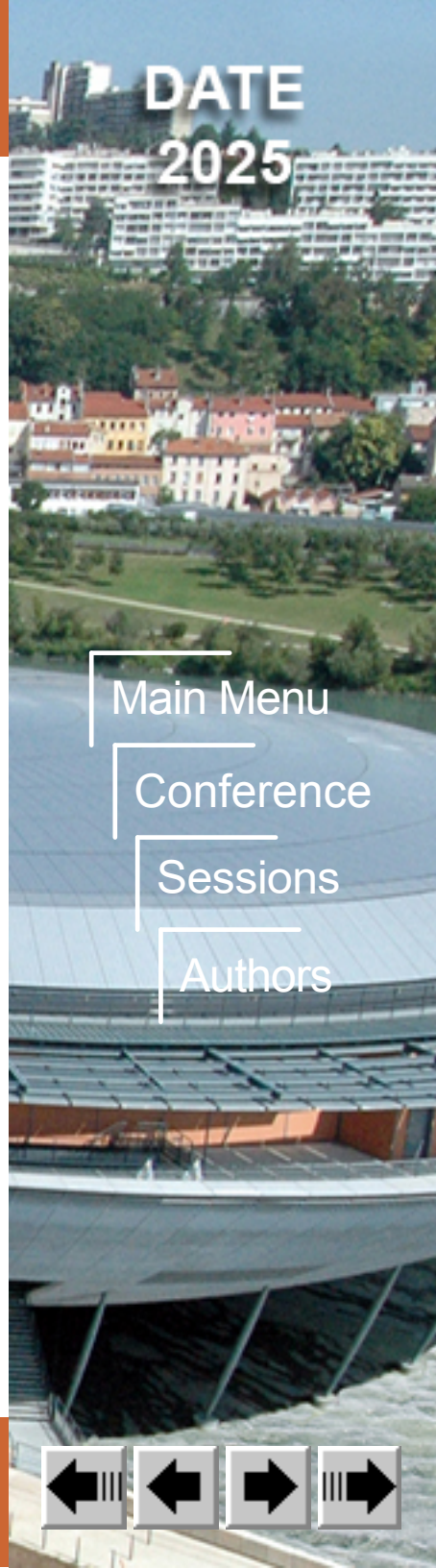
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Papers by Session

- A 10ps-Order Flexible Resolution Time-to-Digital Converter with Linearity Calibration and Legacy FPGA
  Kentaroh Katoh, Toru Nakura, and Haruo Kobayashi

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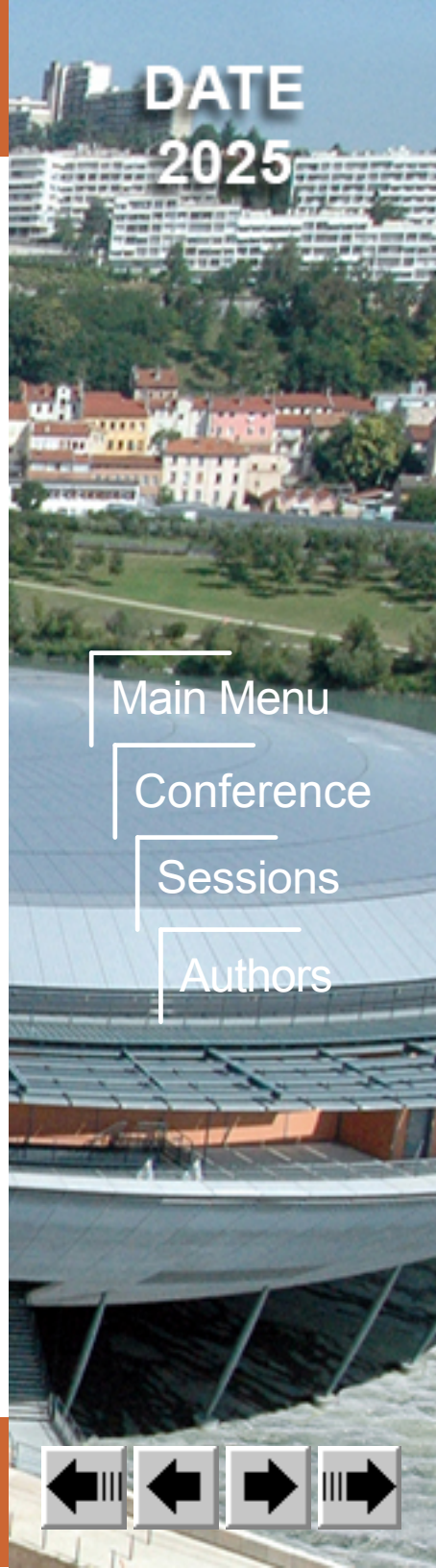


Papers by Session

Design for On-Chip Interconnects

- HiPerNoC: A High-Performance Network-on-Chip for Flexible and Scalable FPGA-Based SmartNICs
  Klajd Zyla, Marco Liess, Thomas Wild, and Andreas Herkersdorf
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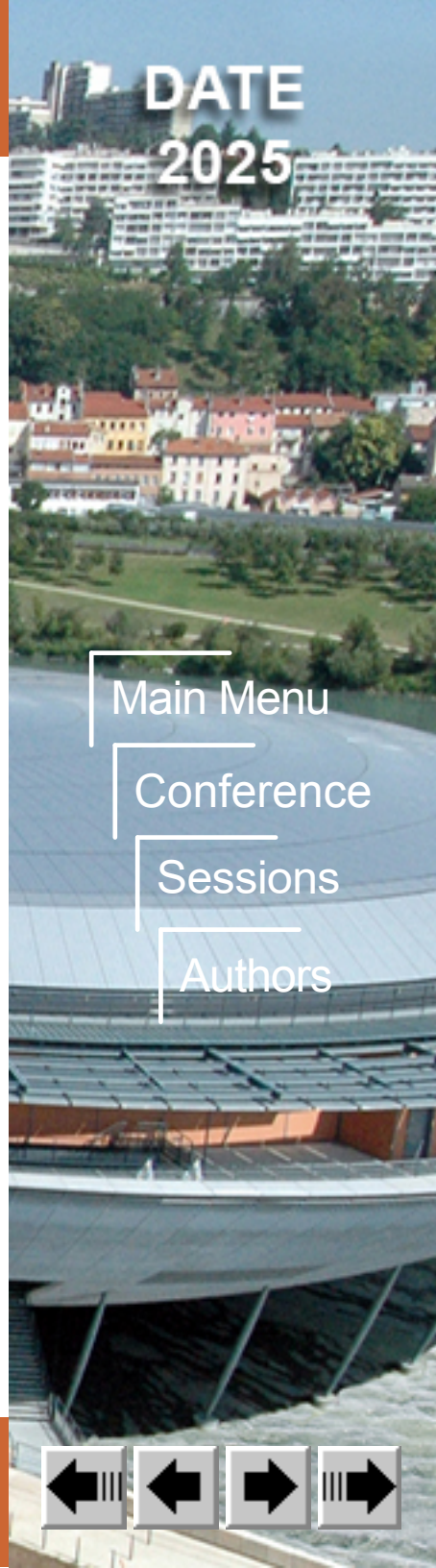
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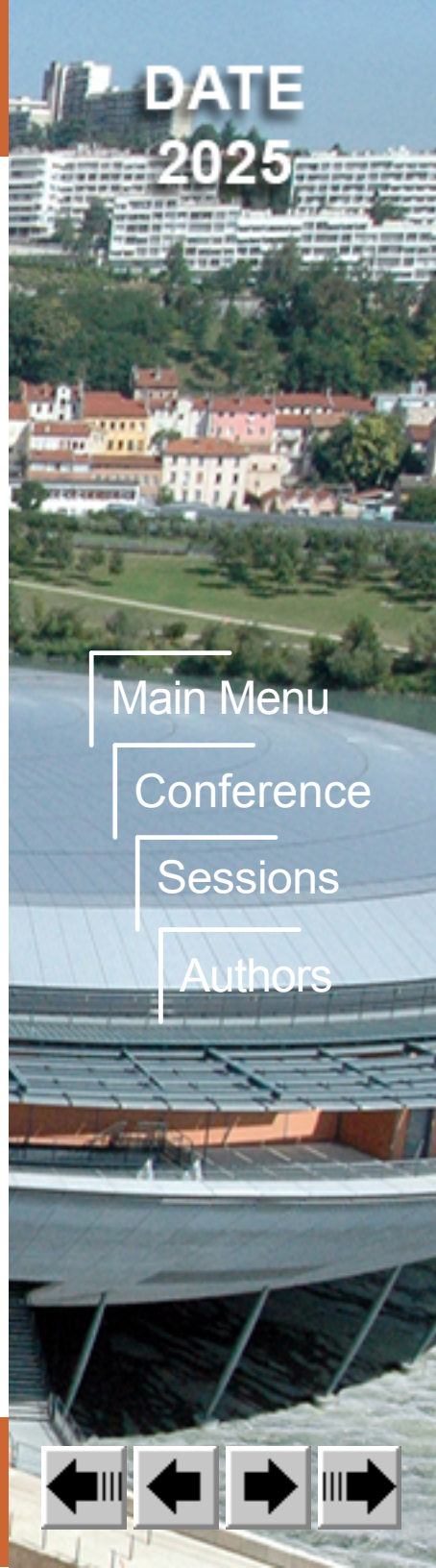


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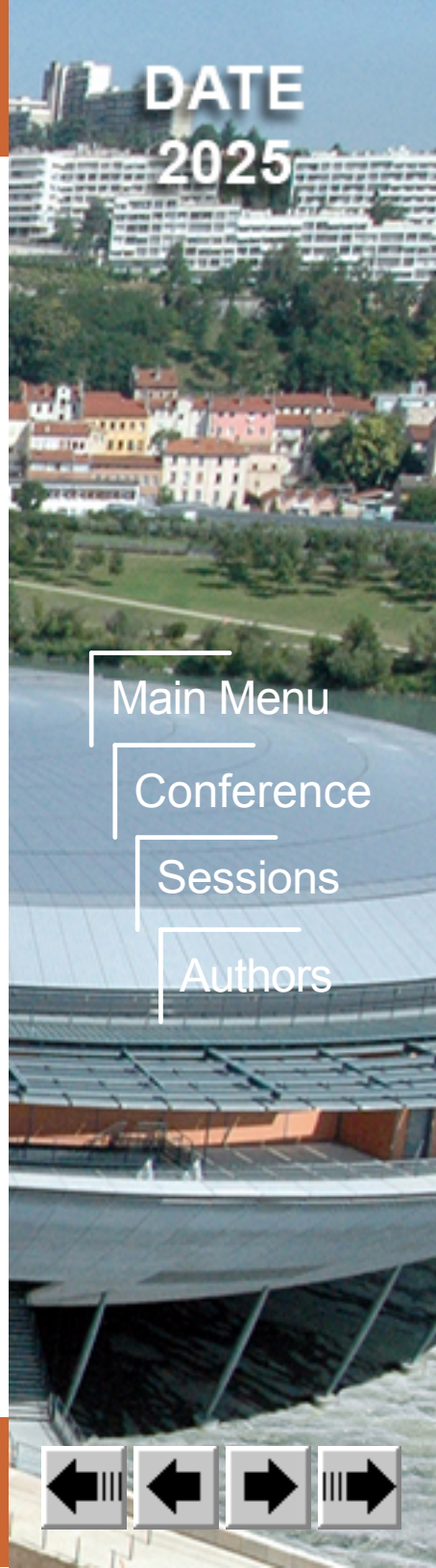
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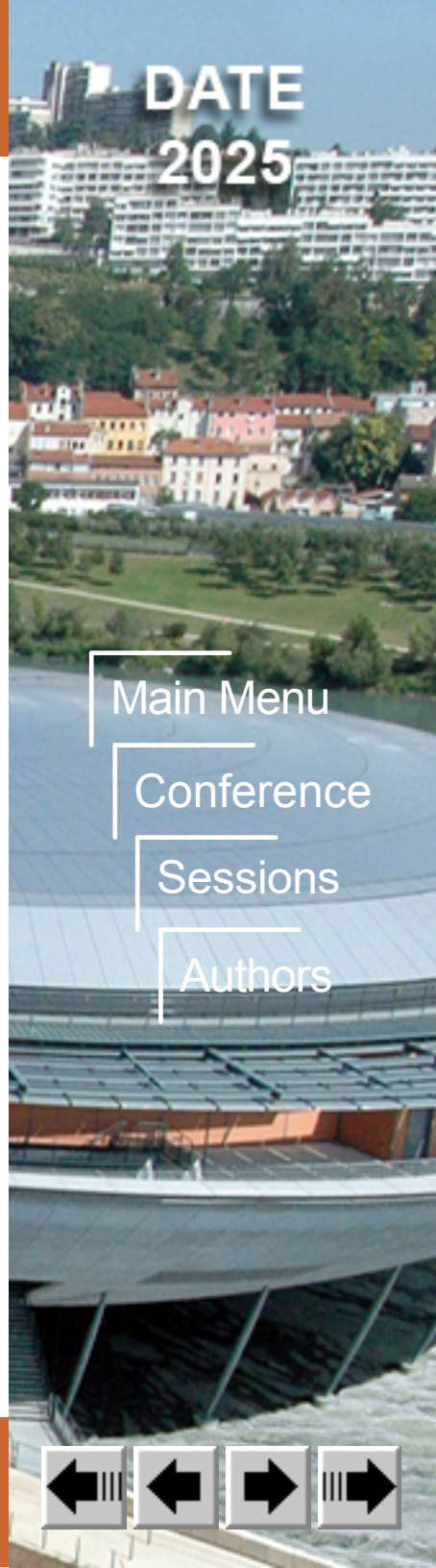


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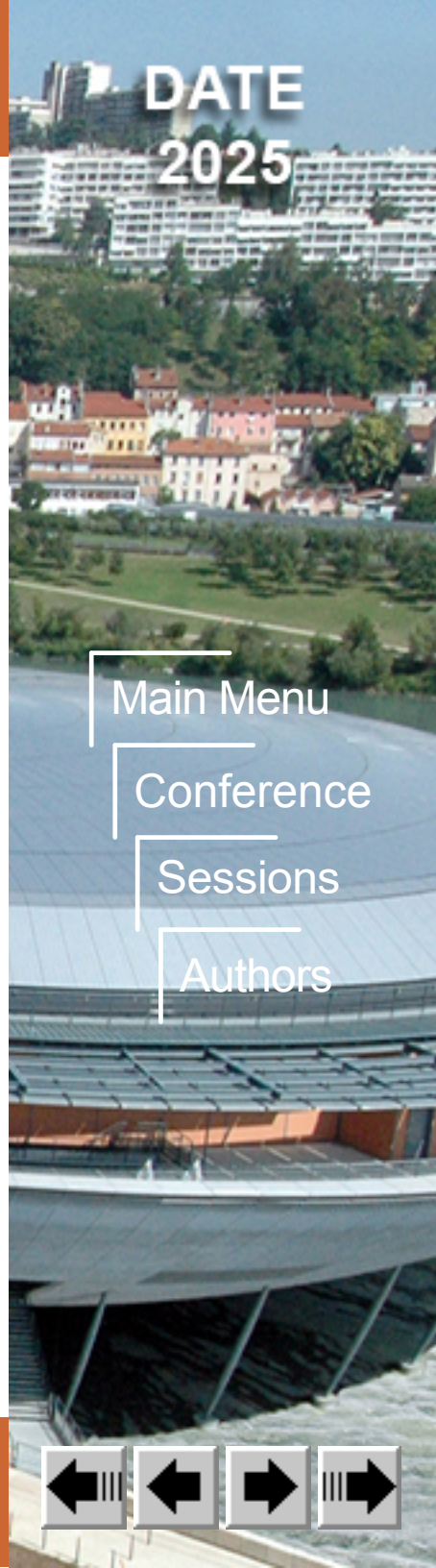
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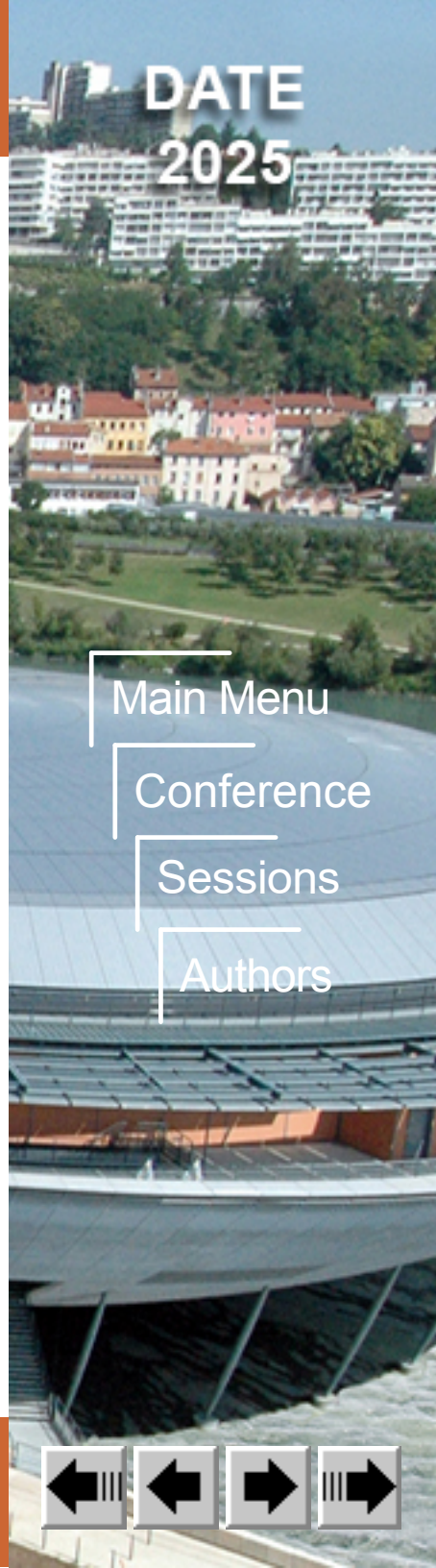


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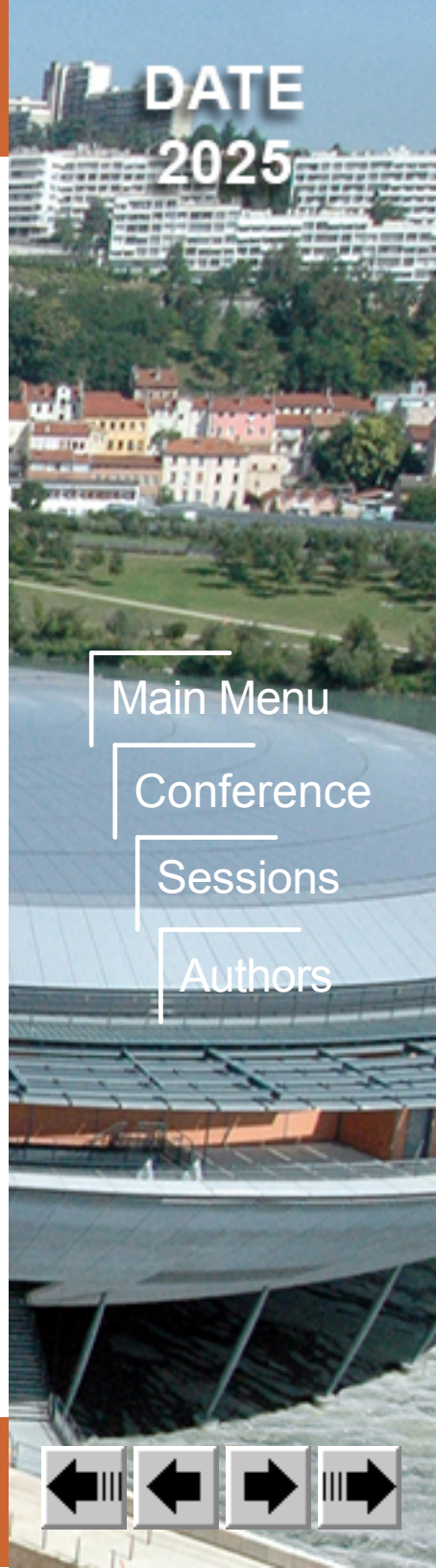
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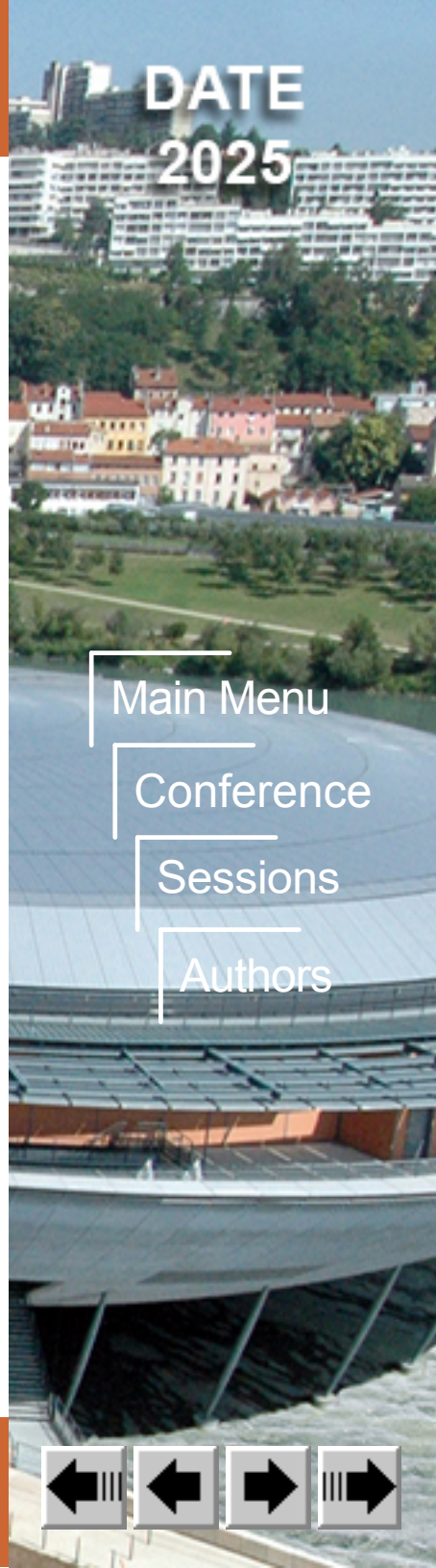


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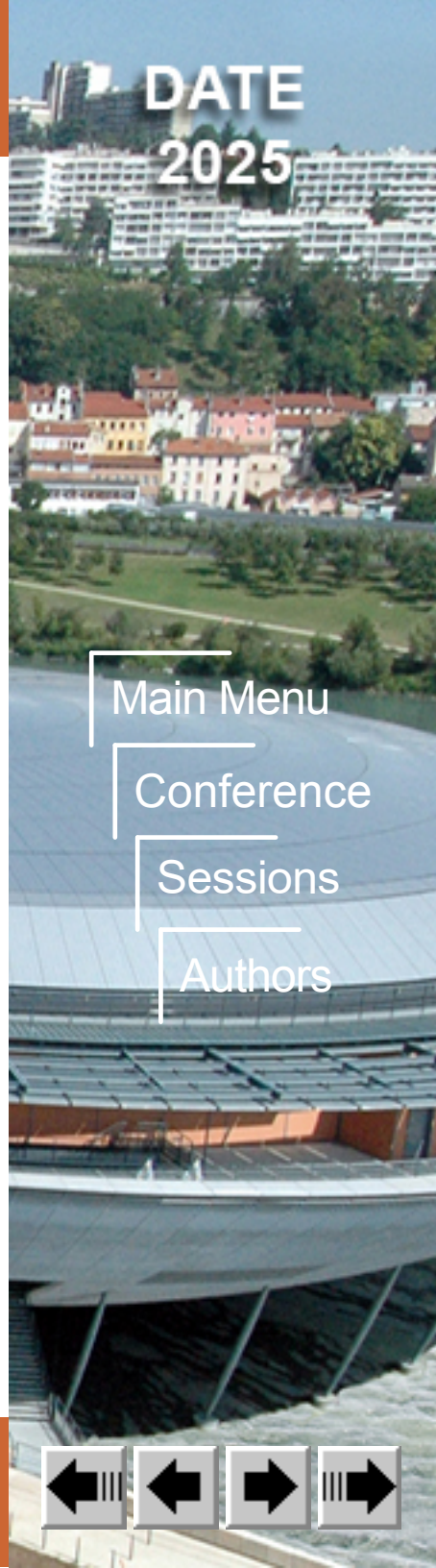
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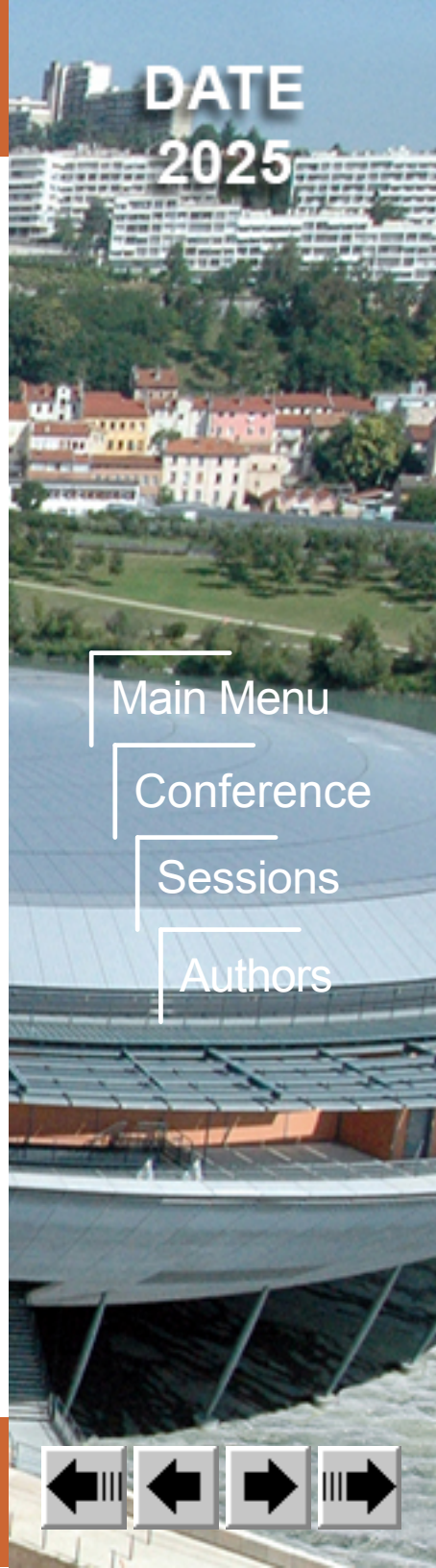


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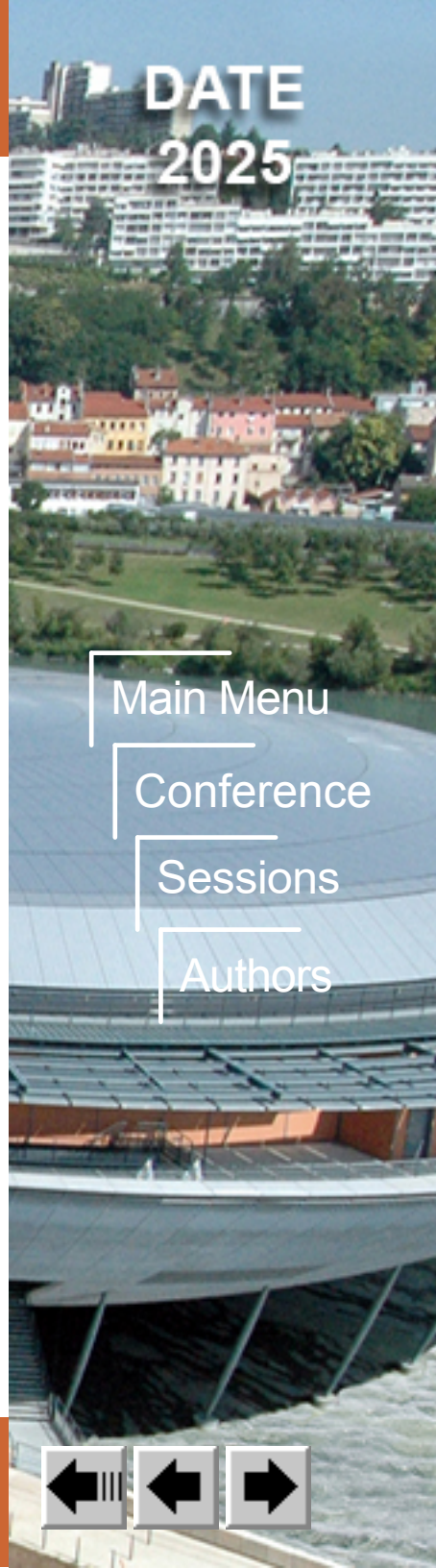
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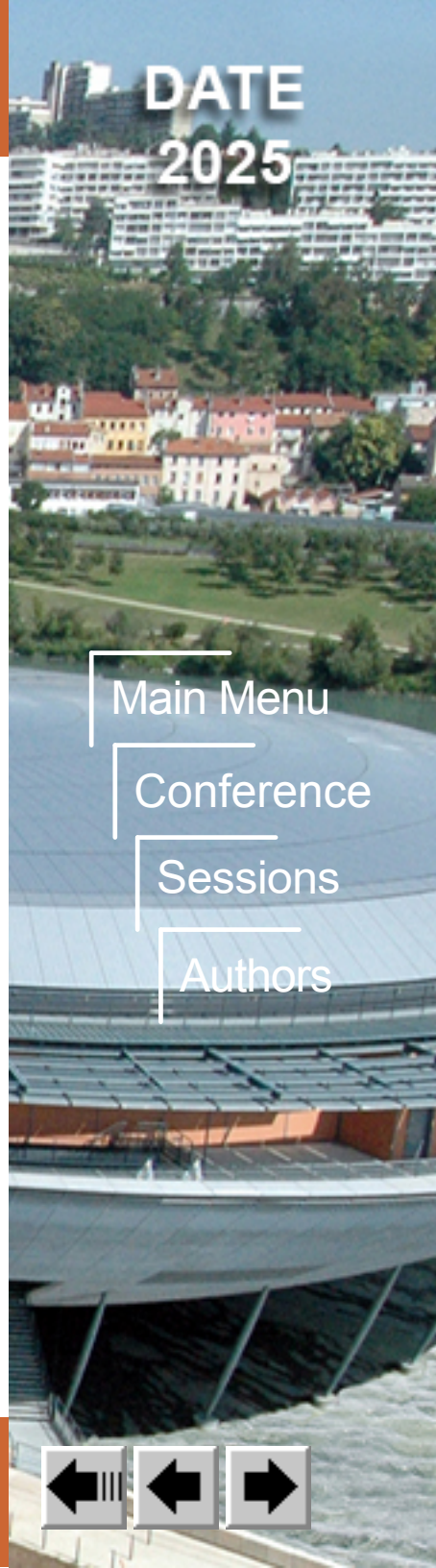
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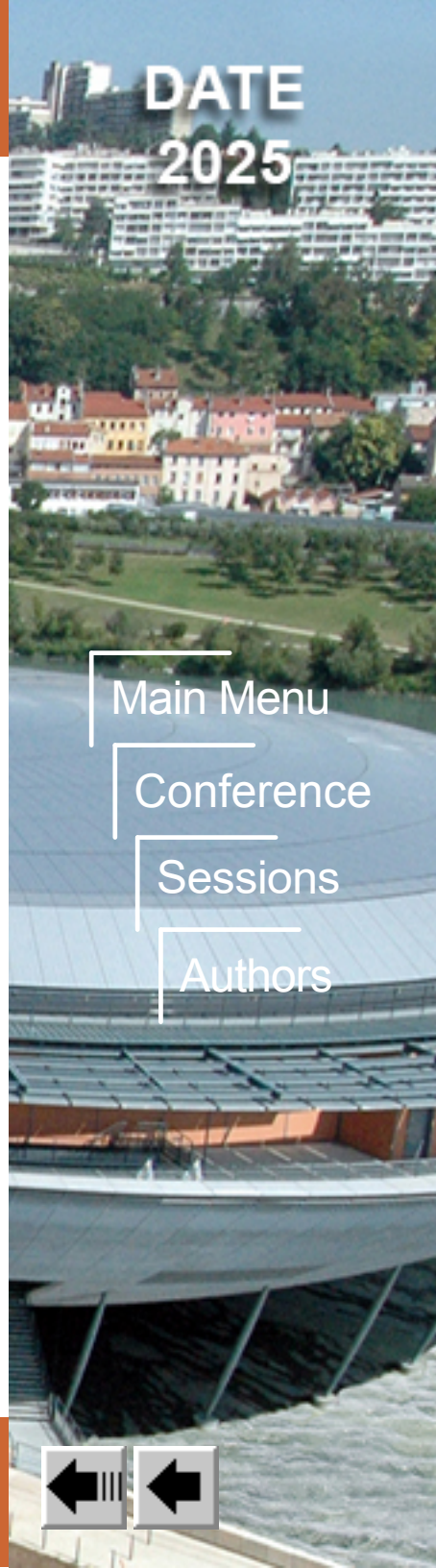
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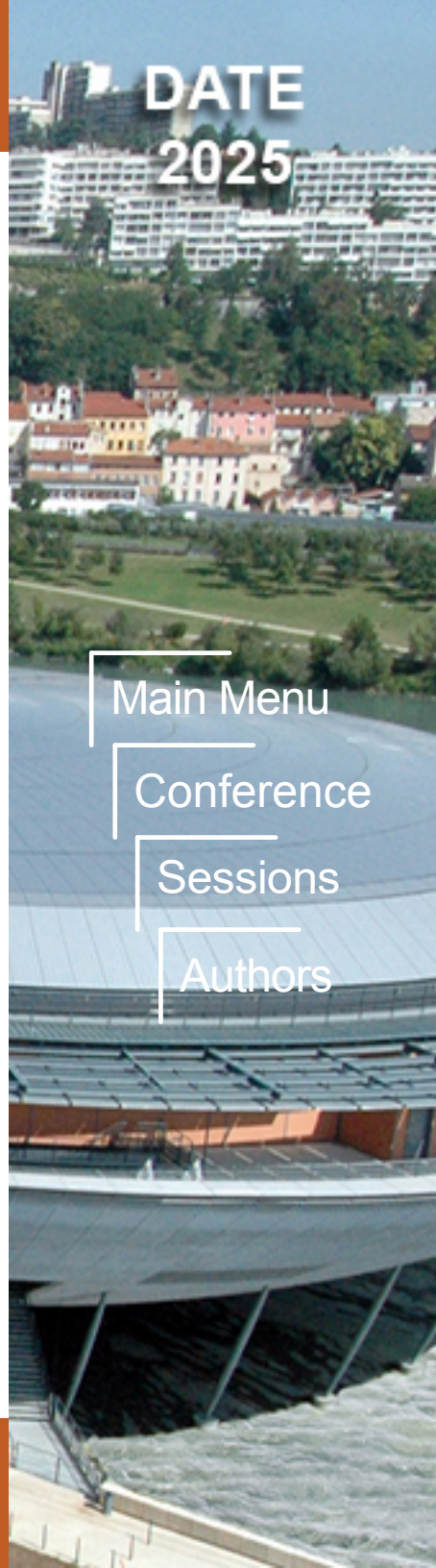
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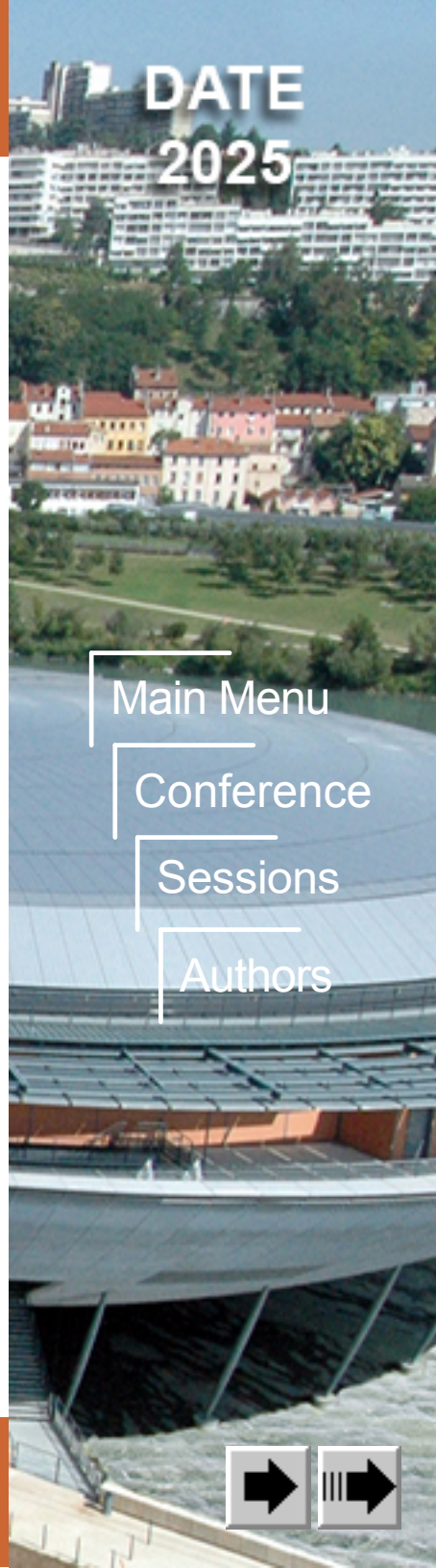
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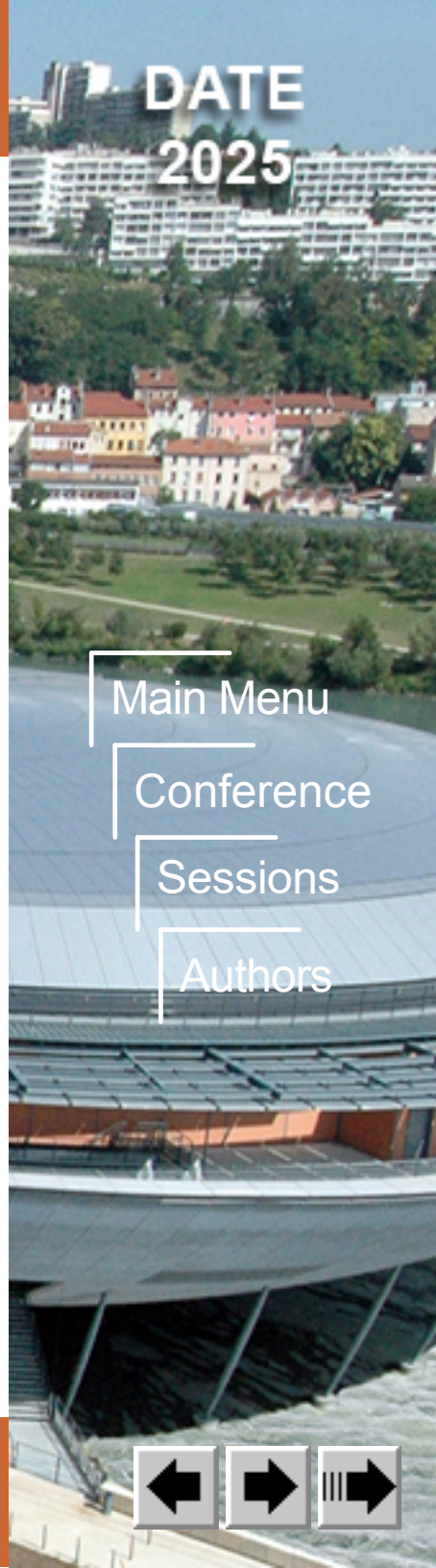
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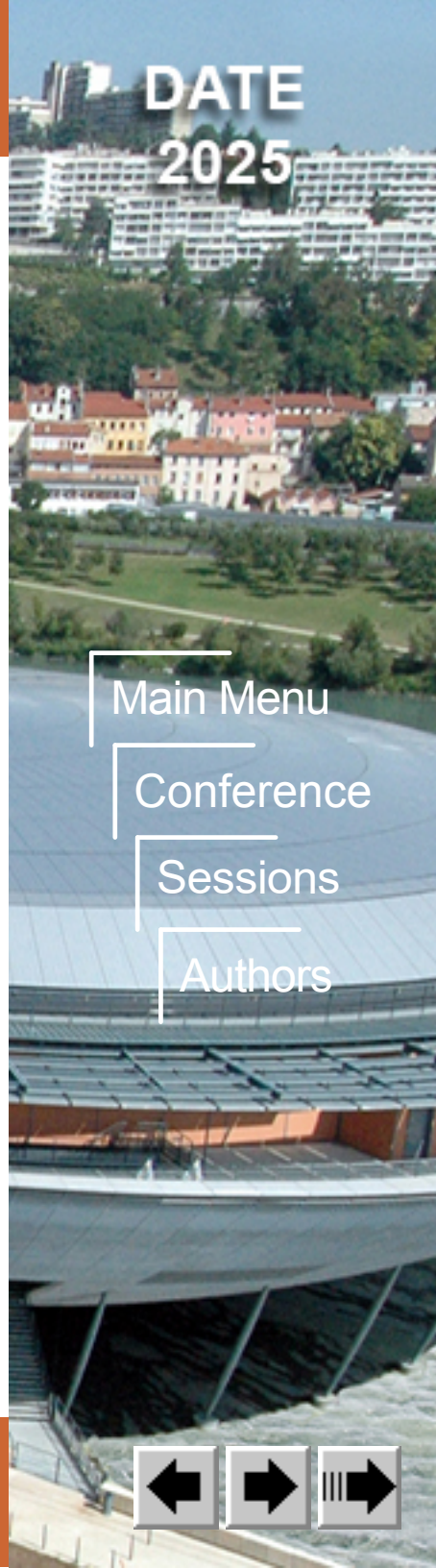
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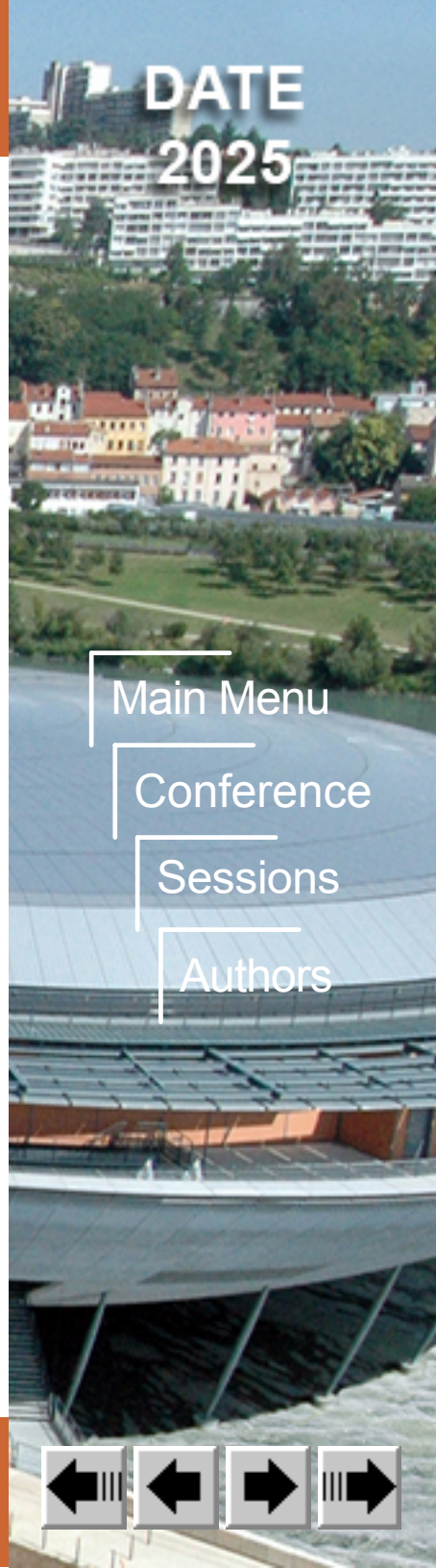
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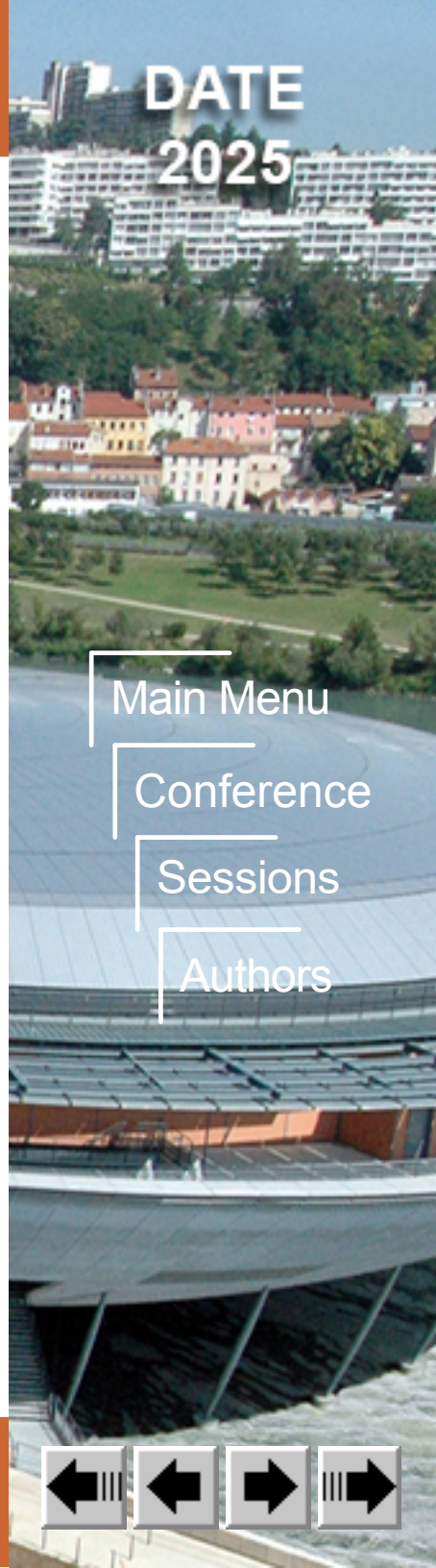
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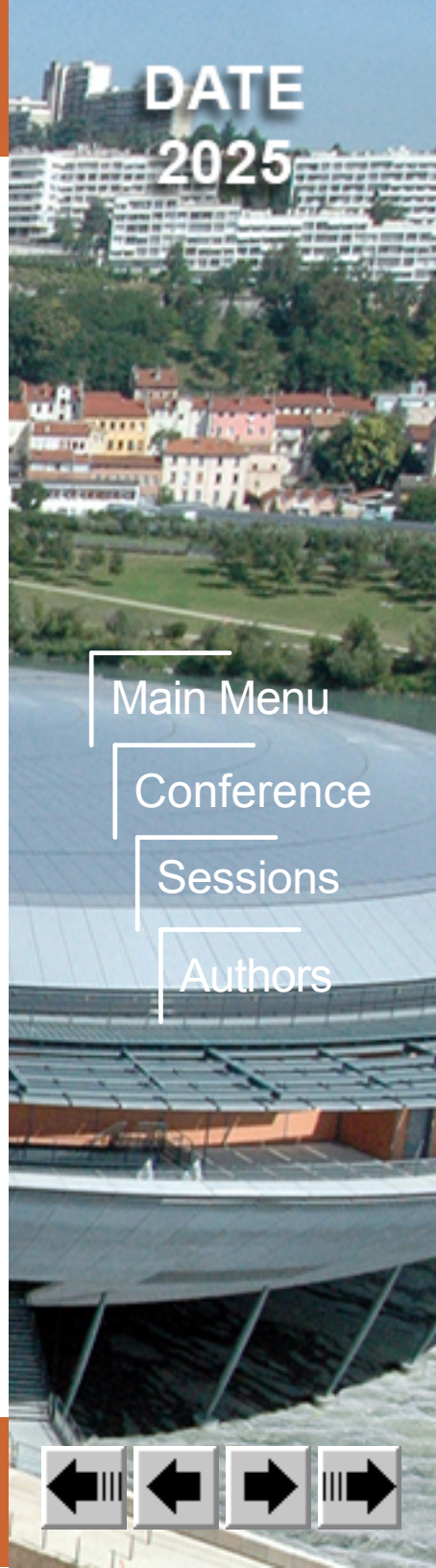
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- Chakrabarty, Krishnendu
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- Chakraborty, Soham
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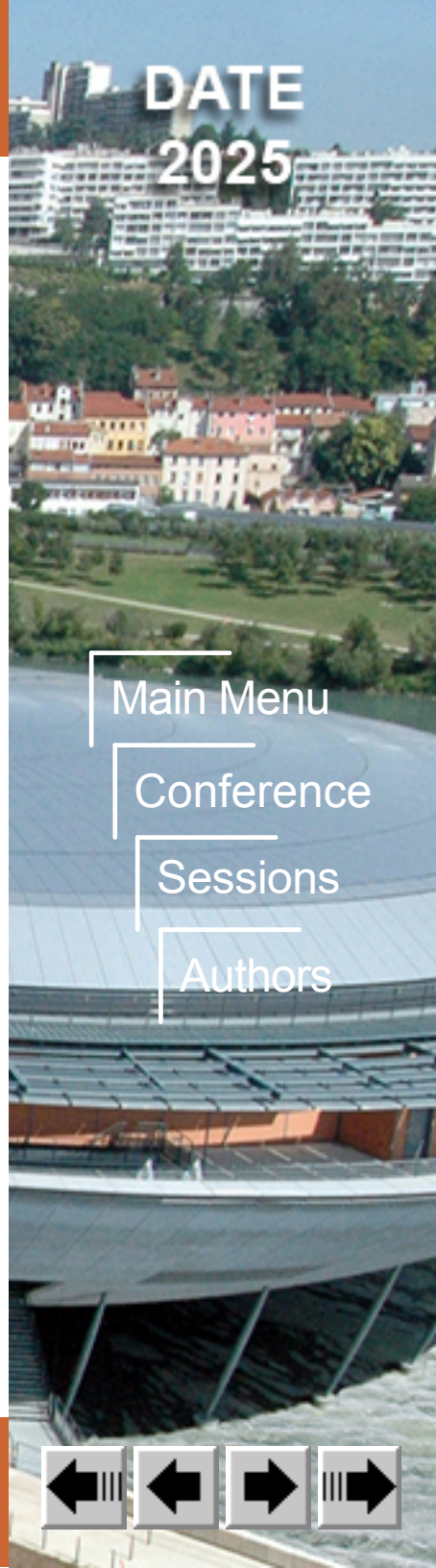
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- Chen, Jintao
- Chen, Kai
- Chen, Kuan-Hsun
- Chen, Lei
- Chen, Li-Wei
- Chen, Luke
- Chen, Peiyu
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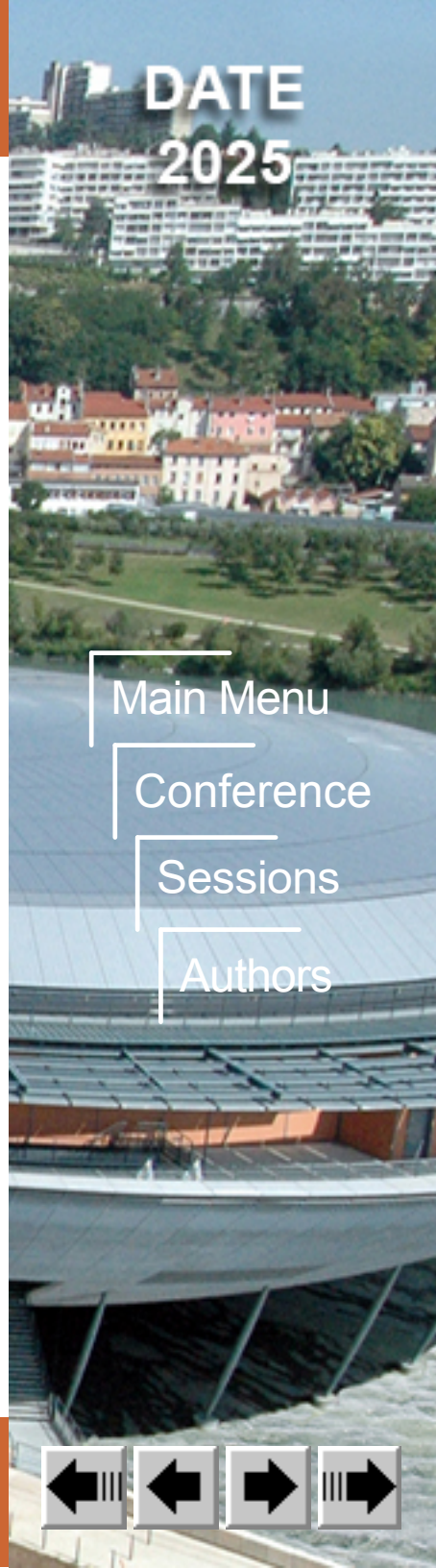
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- Chen, Zhaoyun
- Chen, Zhengrui
- Chen, Zhonghao
- Chen, Zhuo
- Chen, Ziang
- Chen, Ziming
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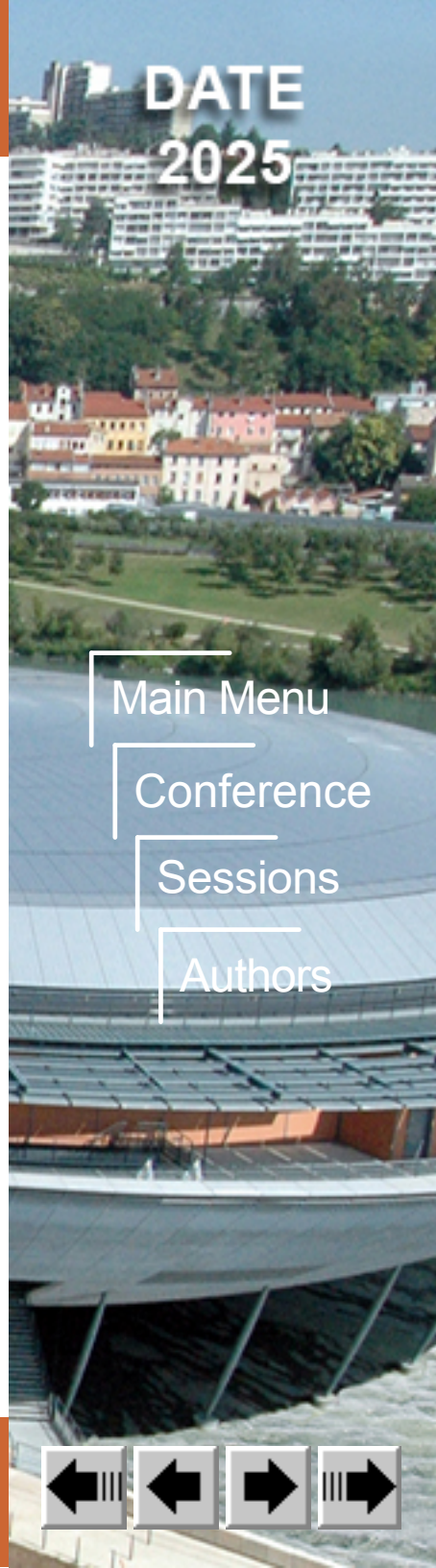
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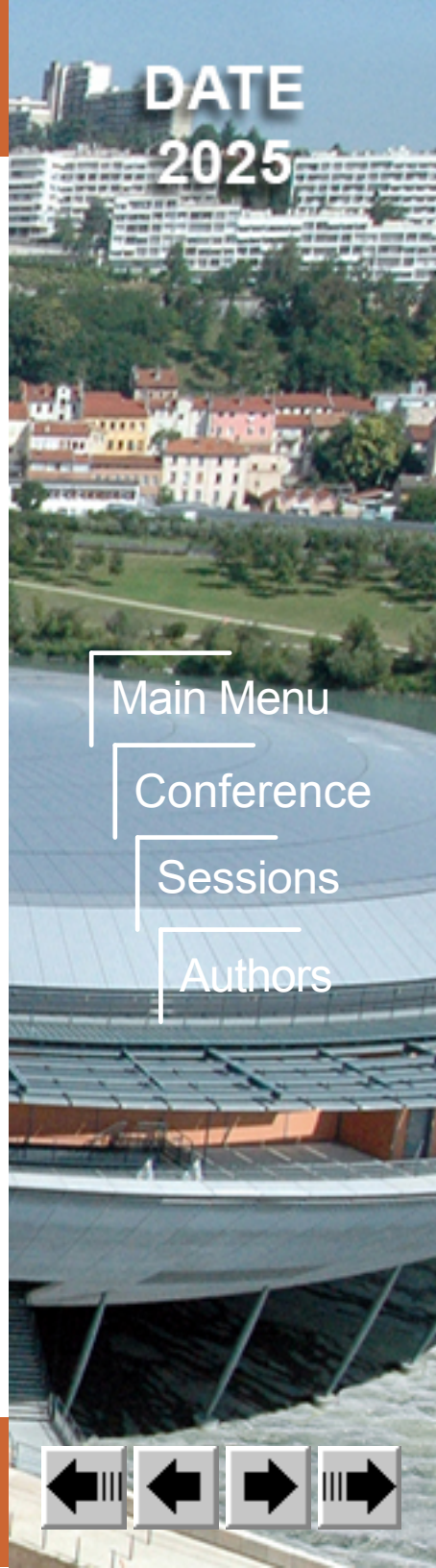
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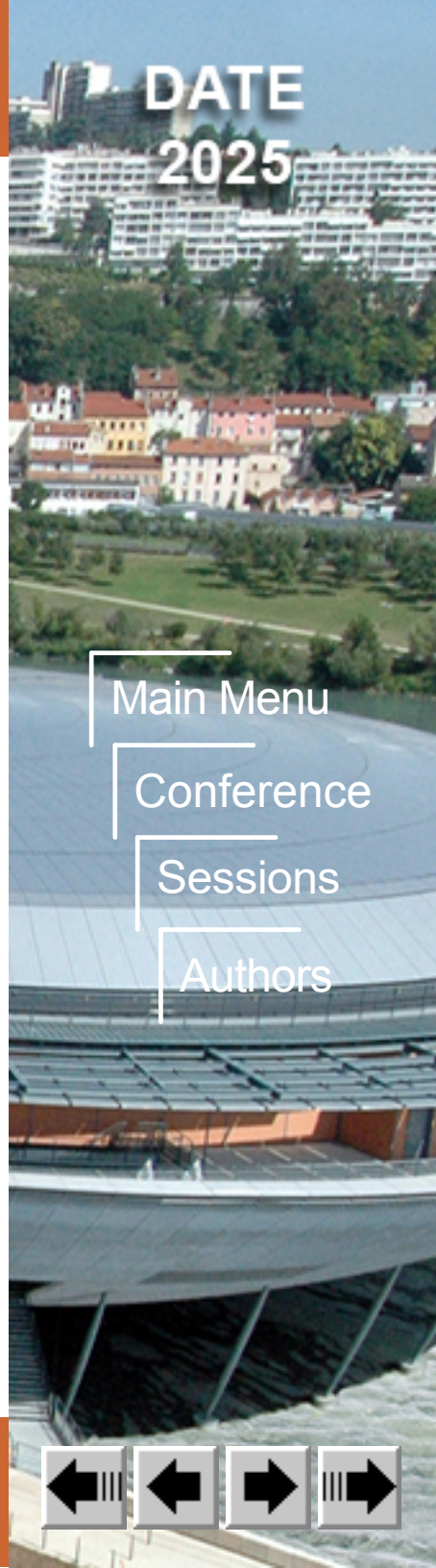
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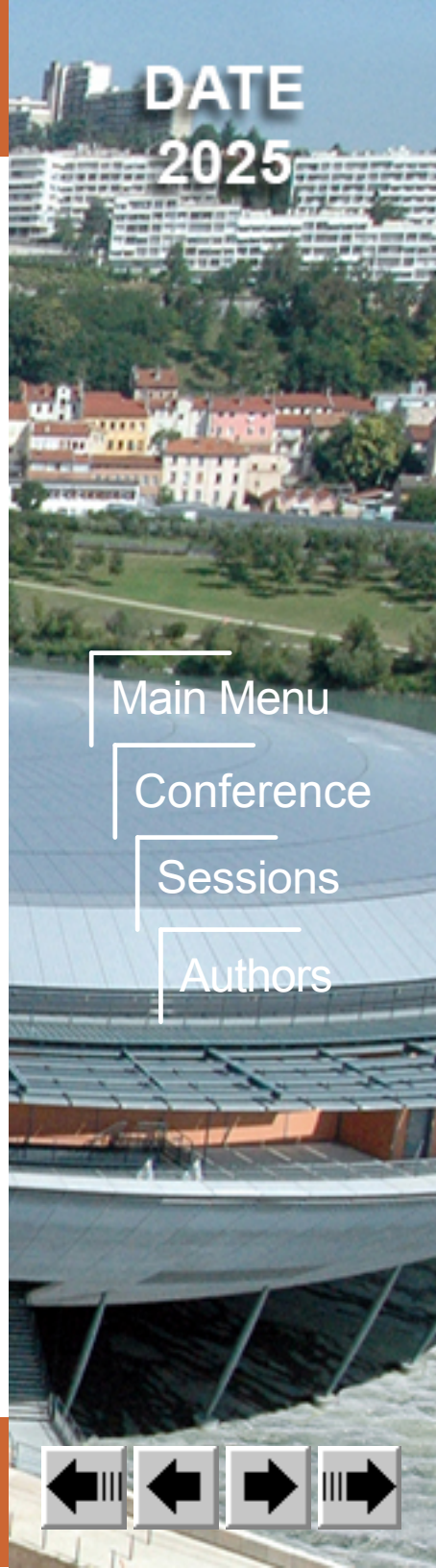
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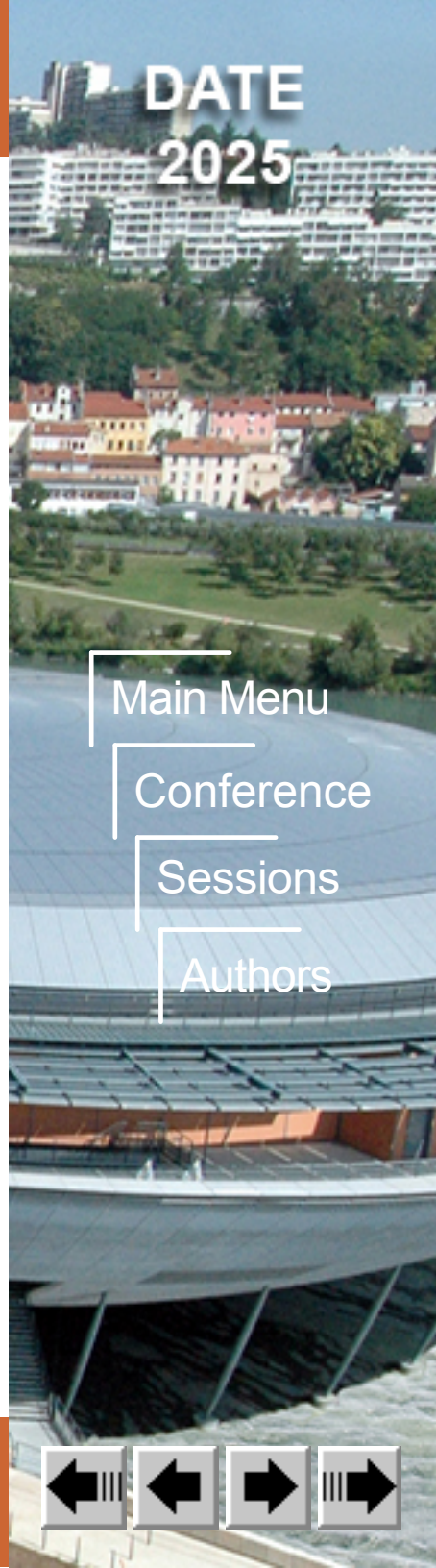
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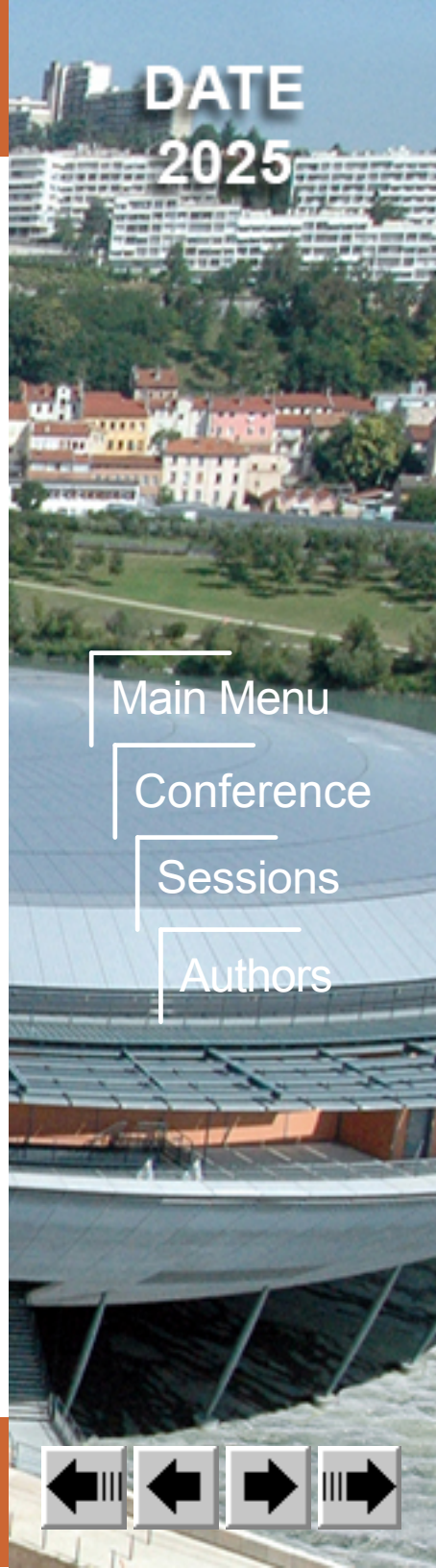
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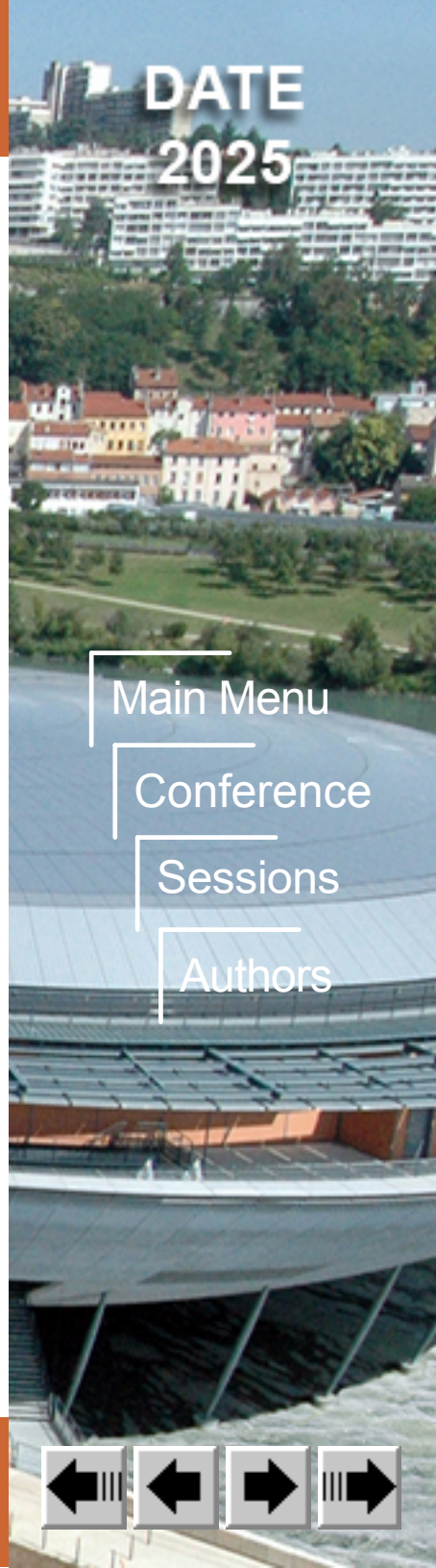
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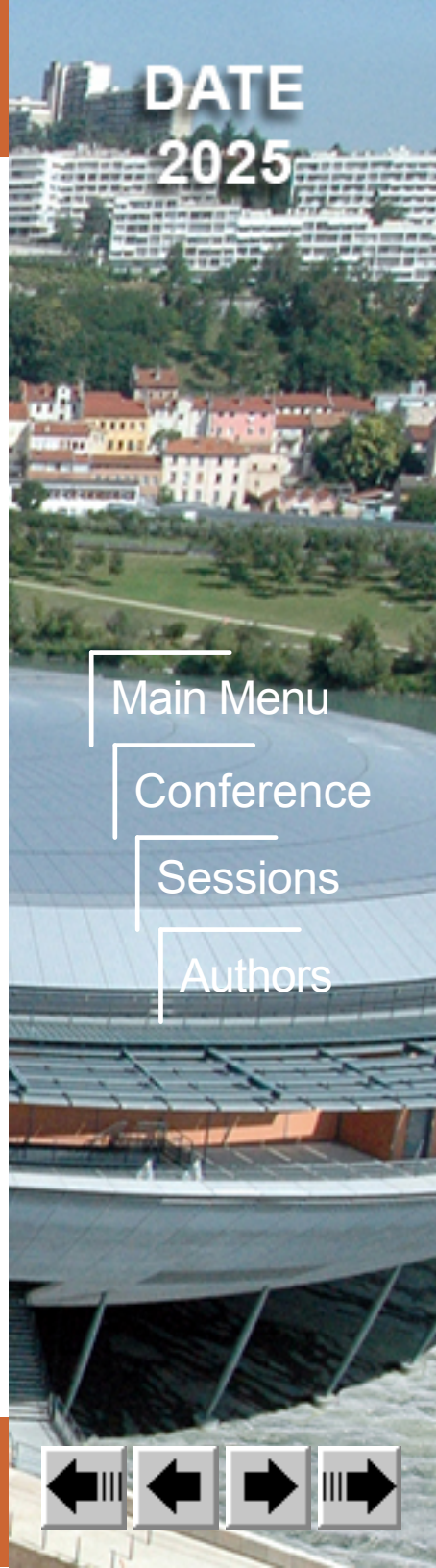
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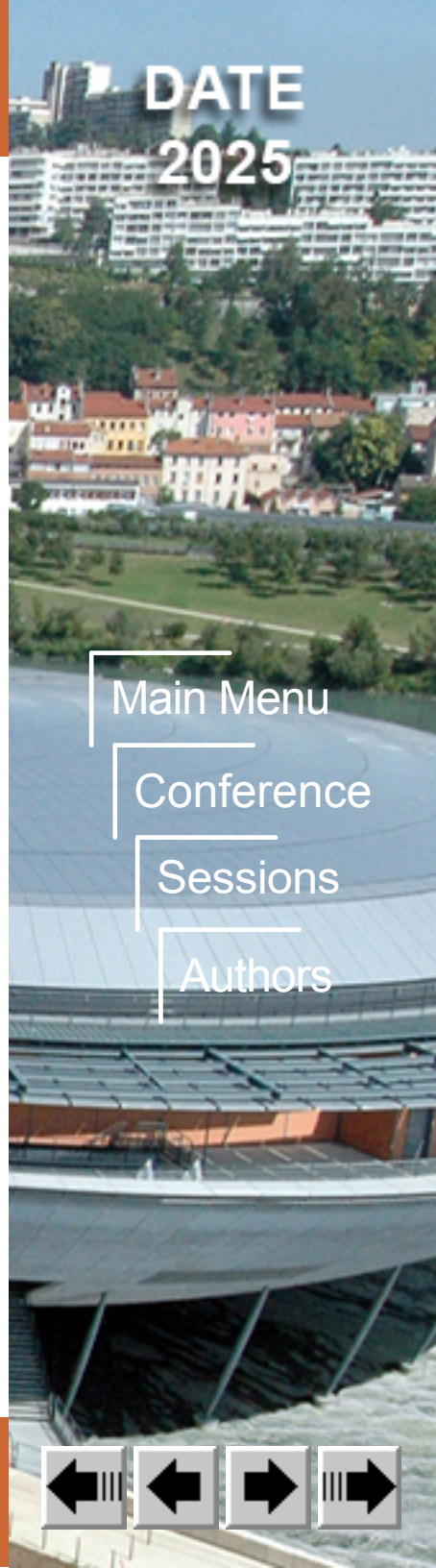
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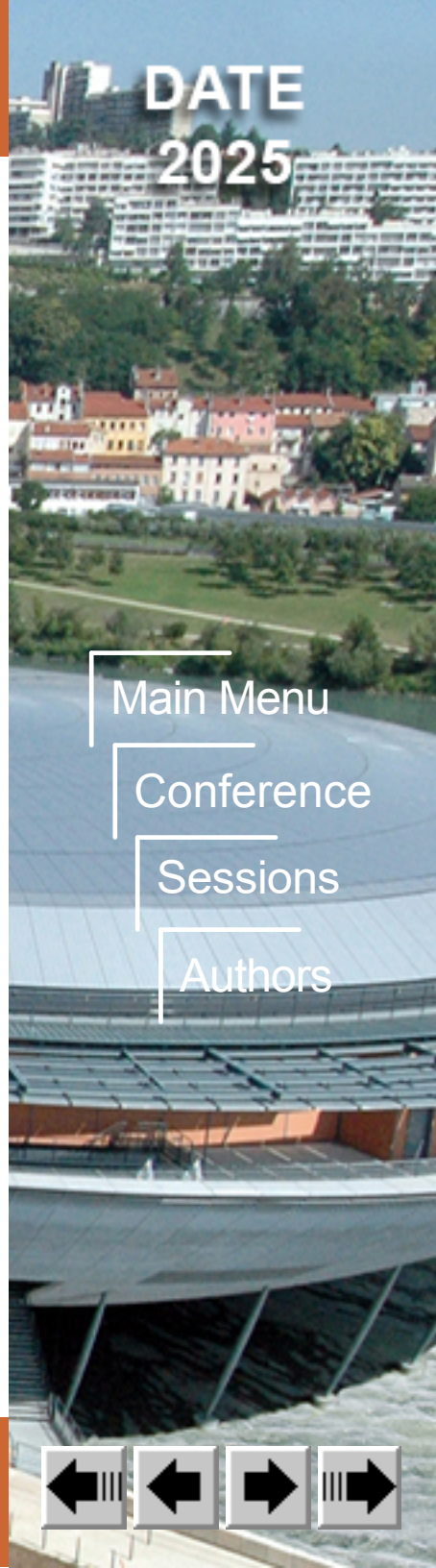
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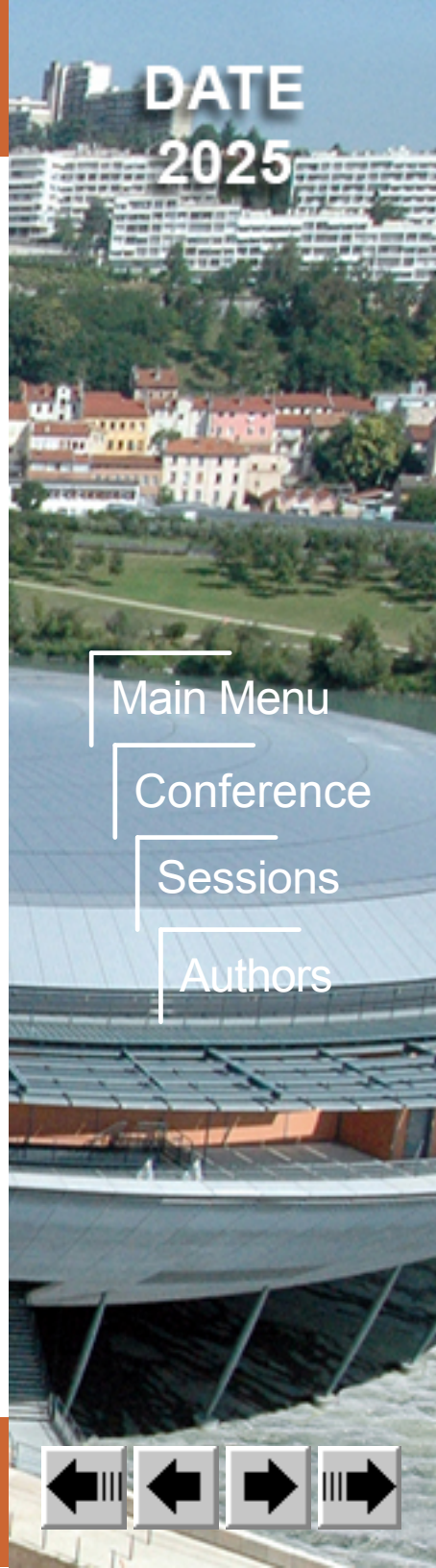
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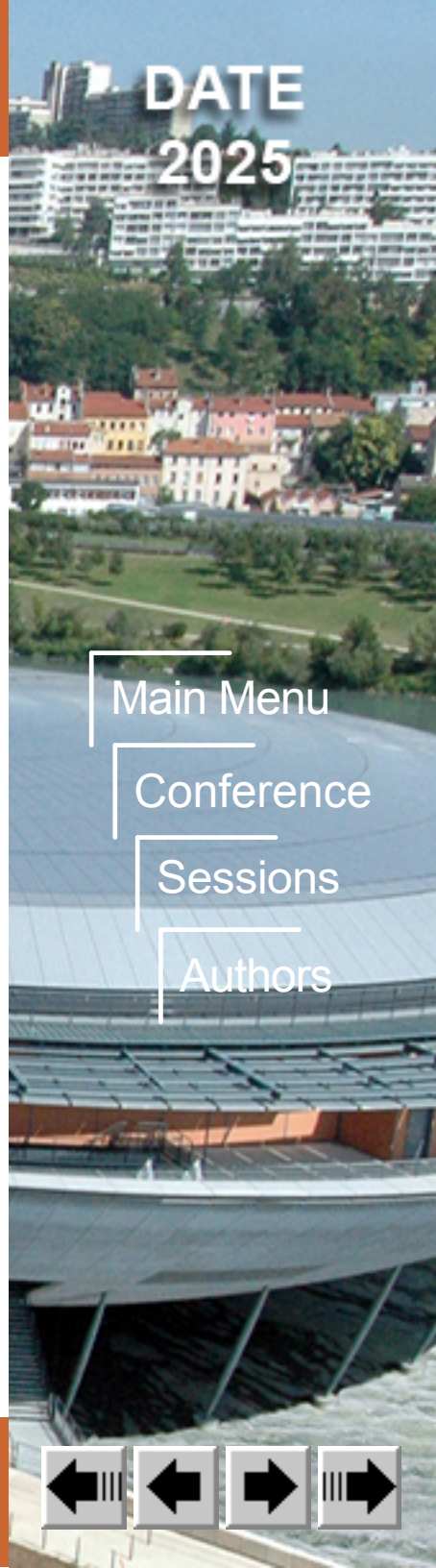
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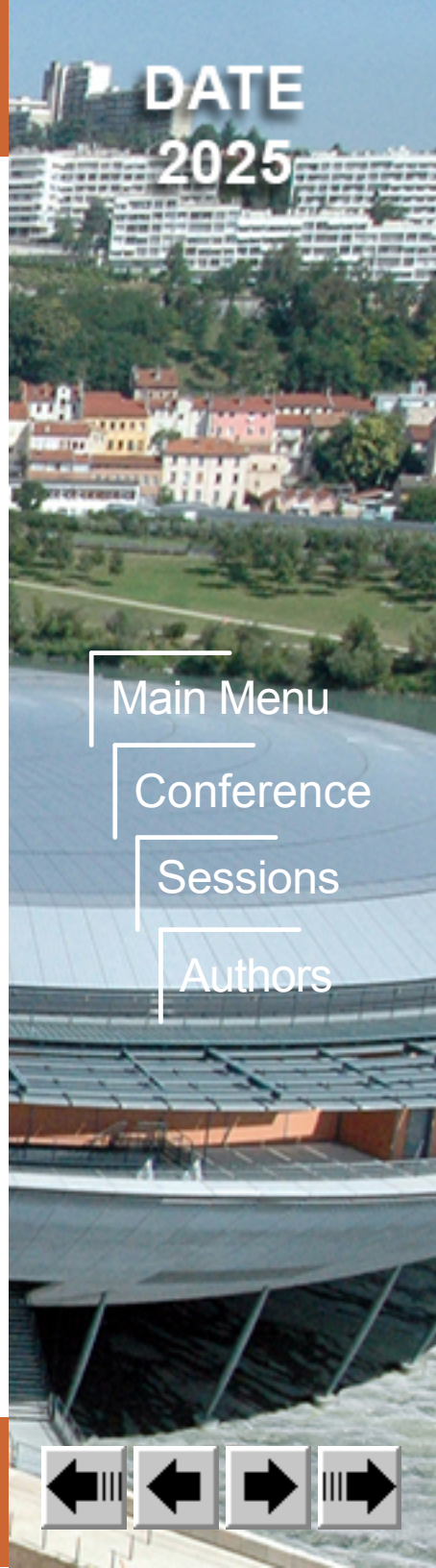
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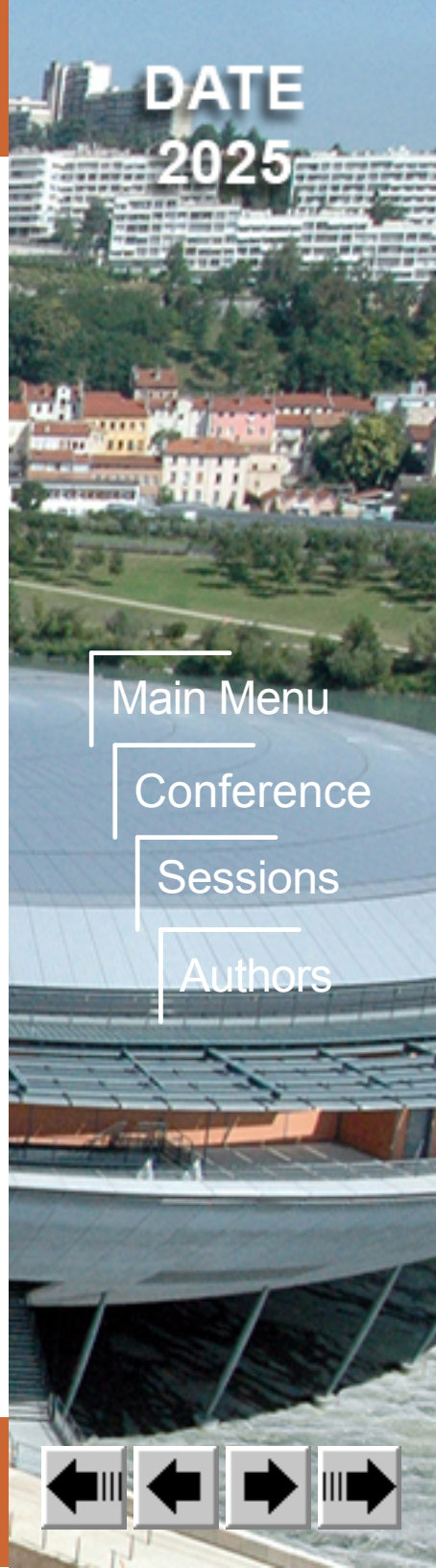
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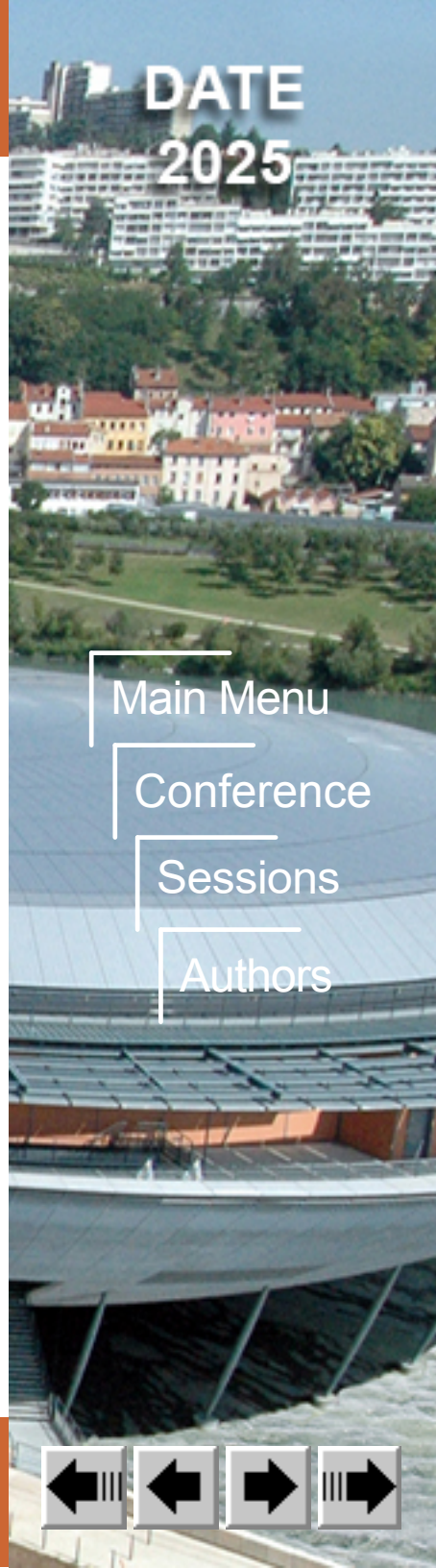
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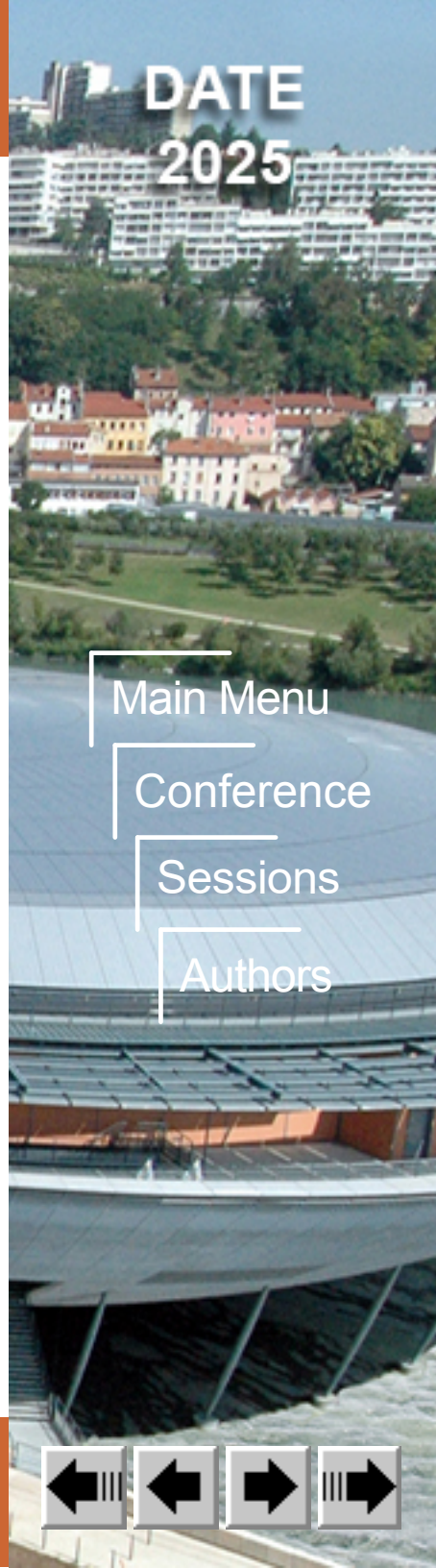
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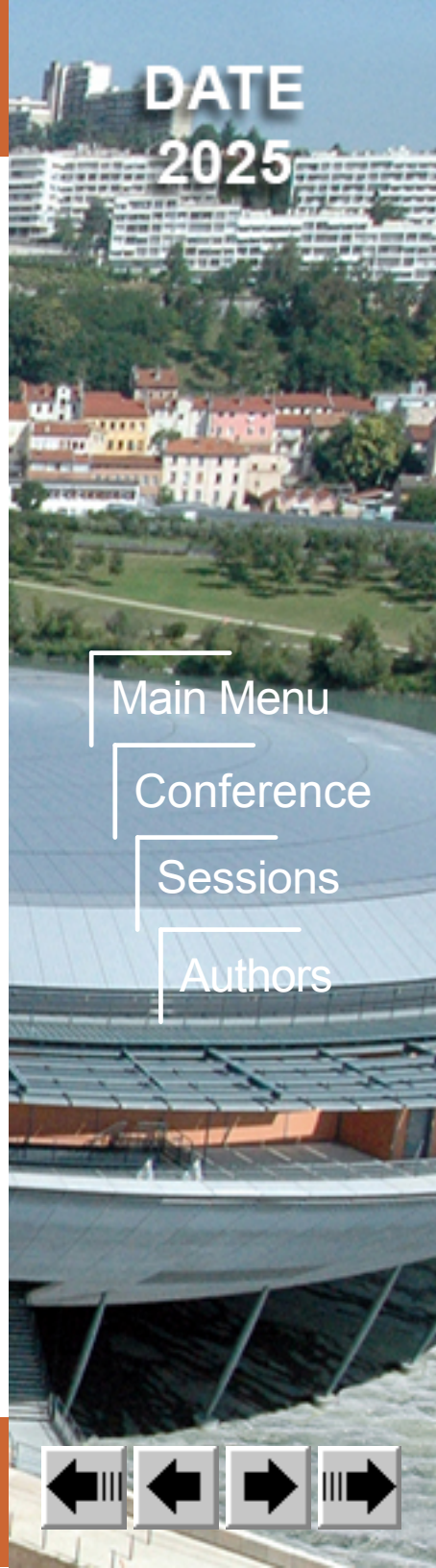
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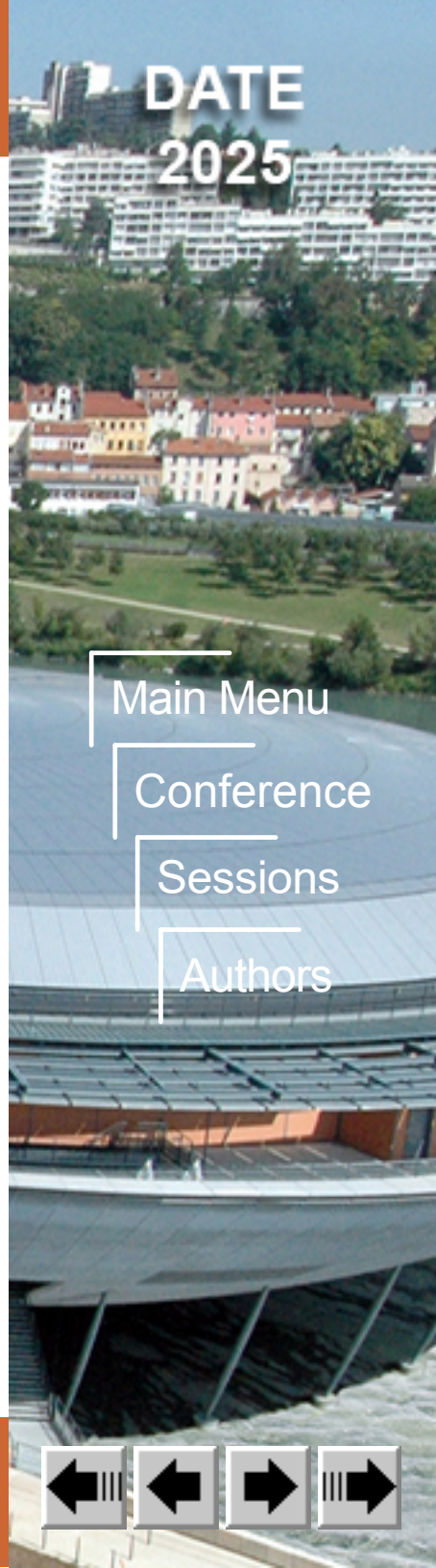
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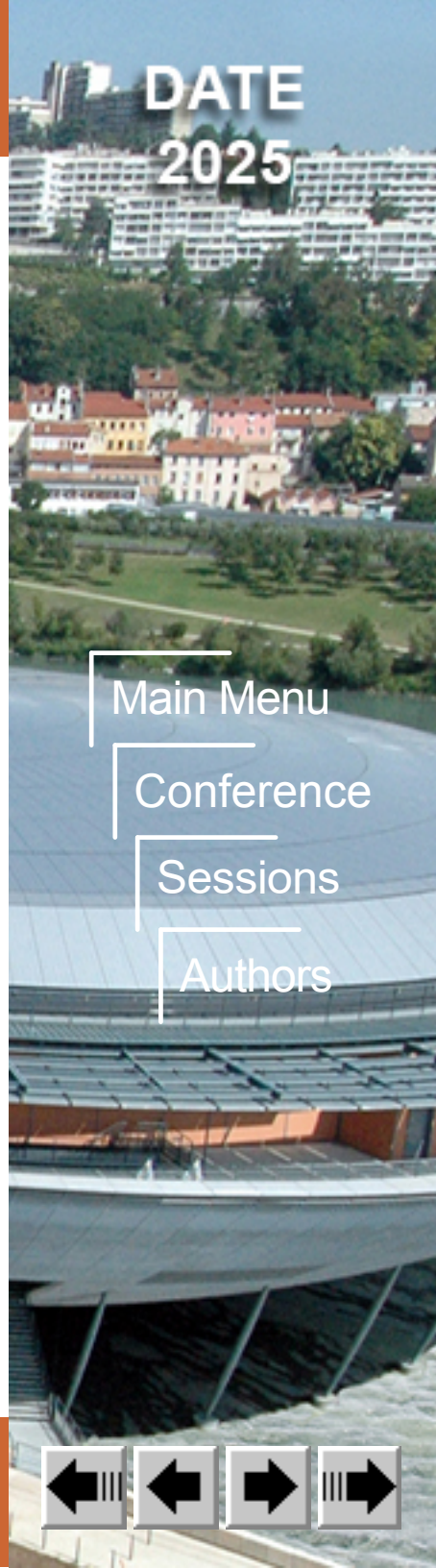
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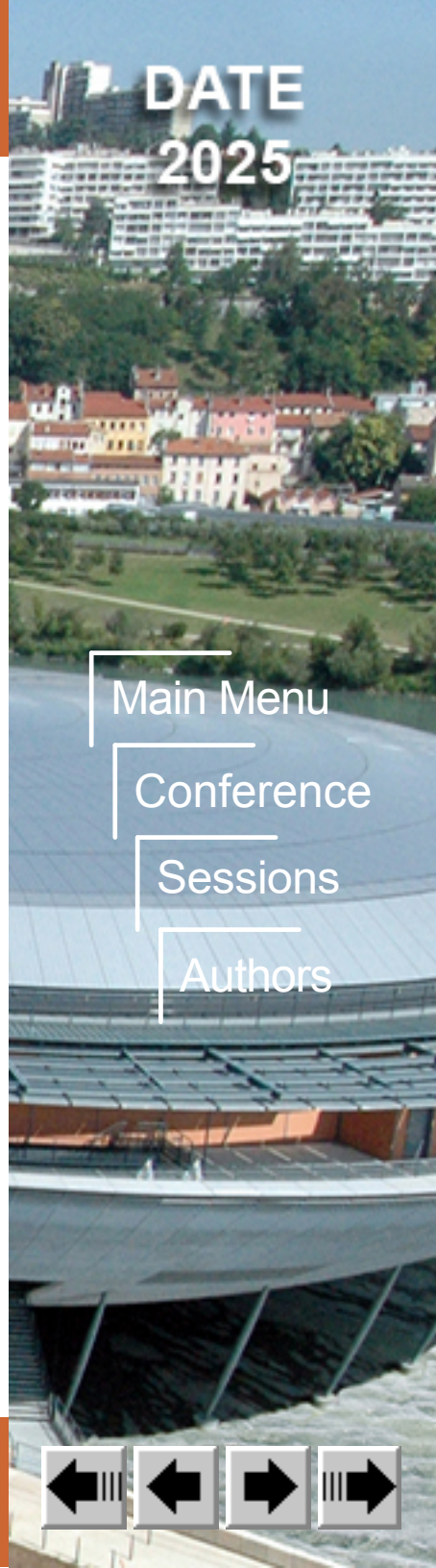
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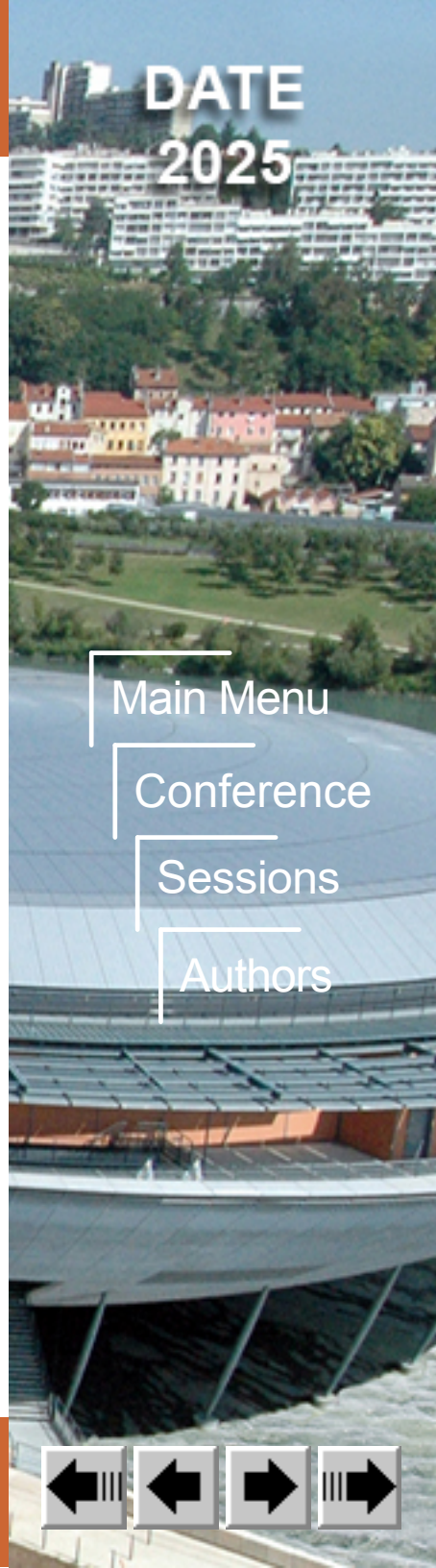
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- Li, Yuan
- Li, Yuecheng
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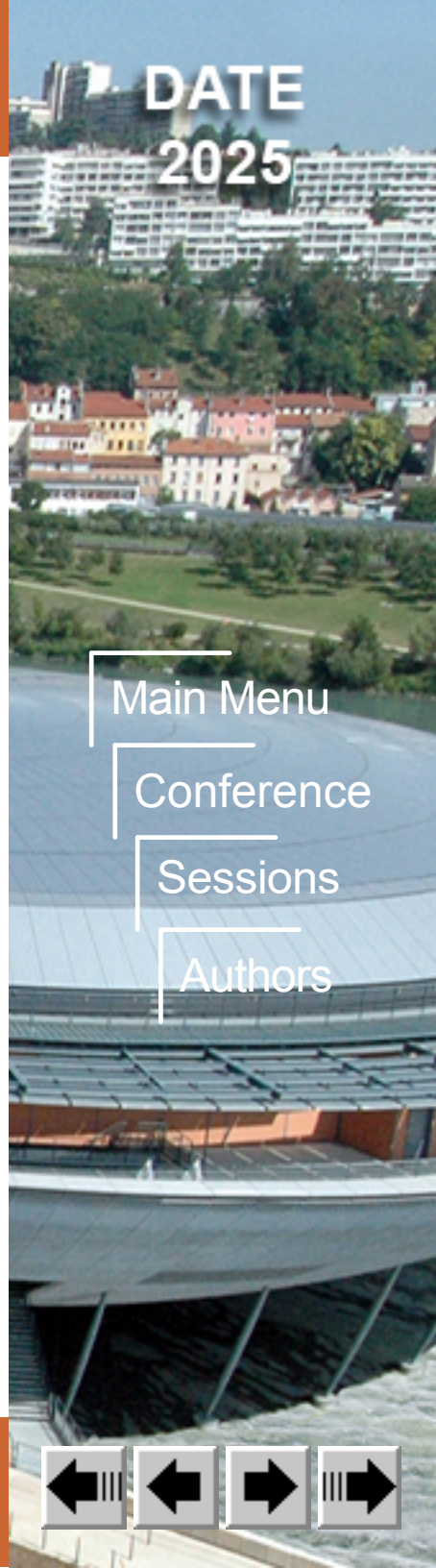
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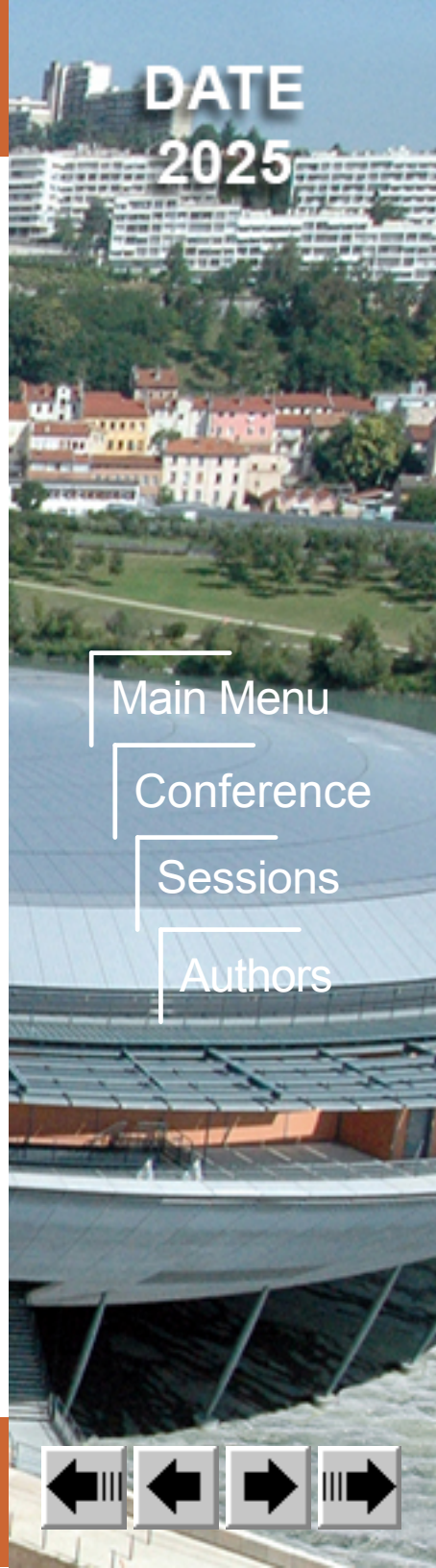
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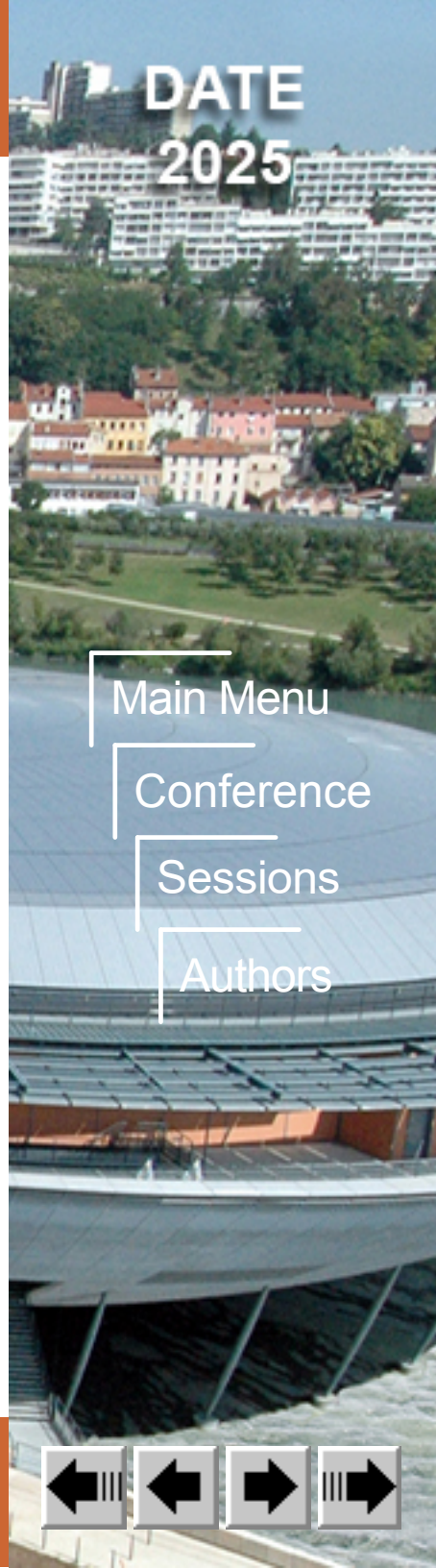
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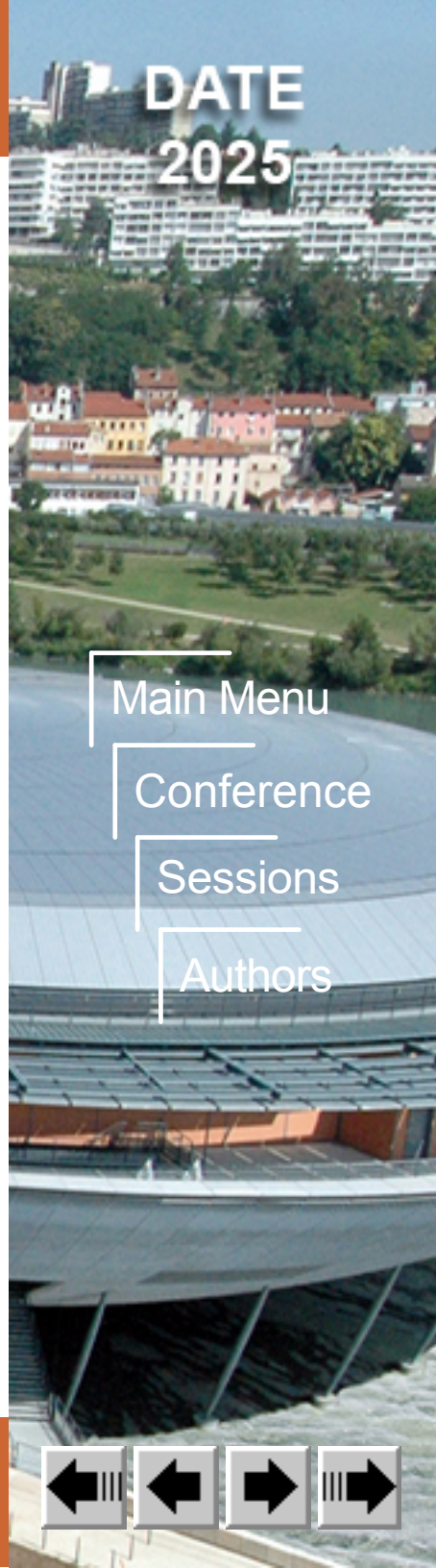
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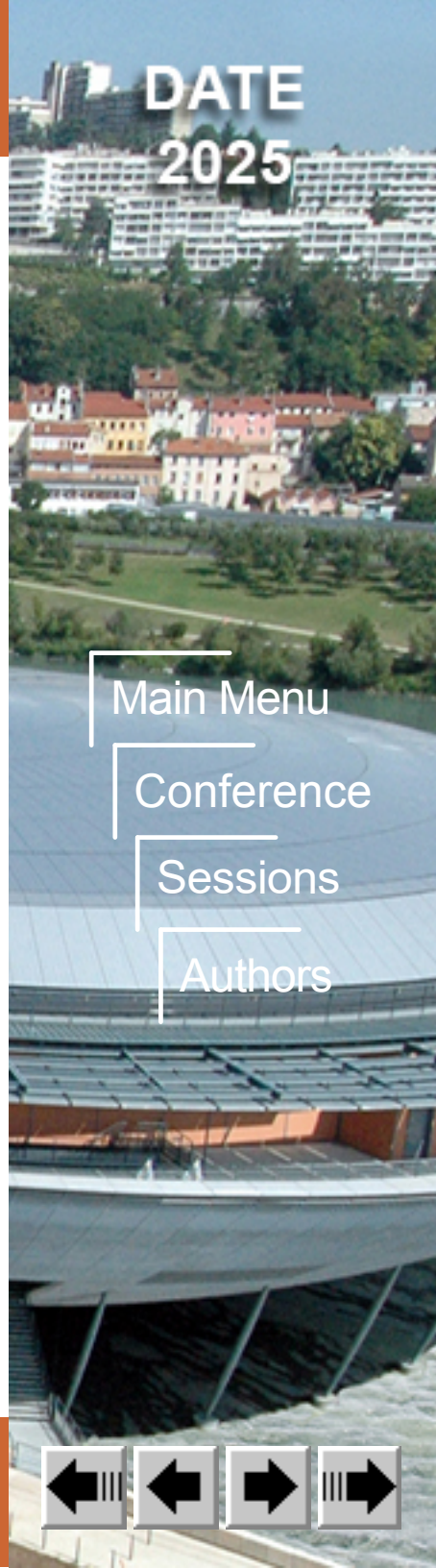
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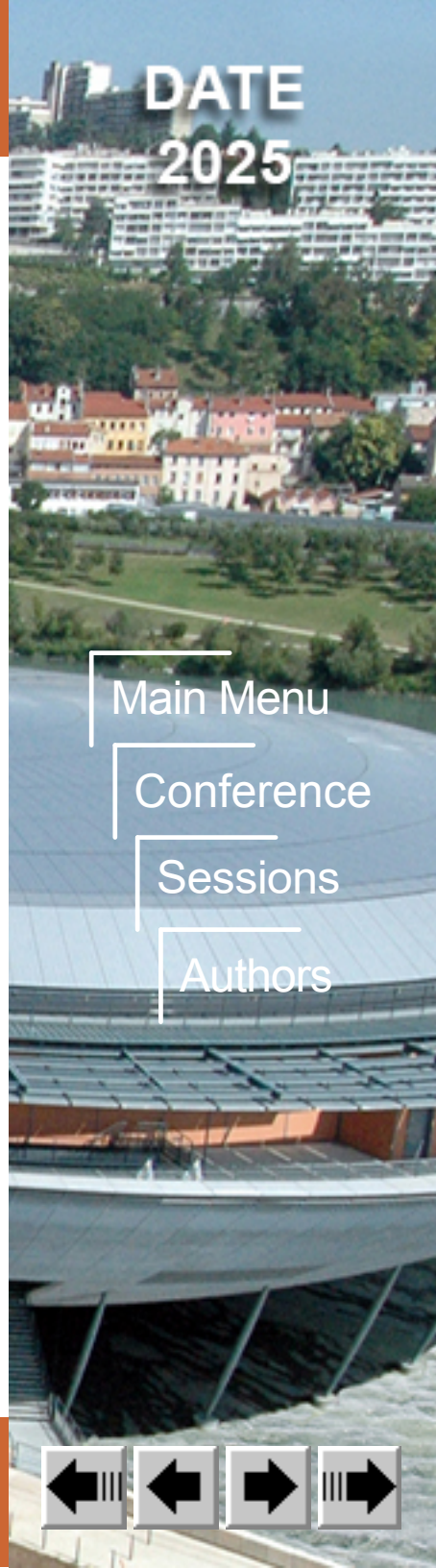
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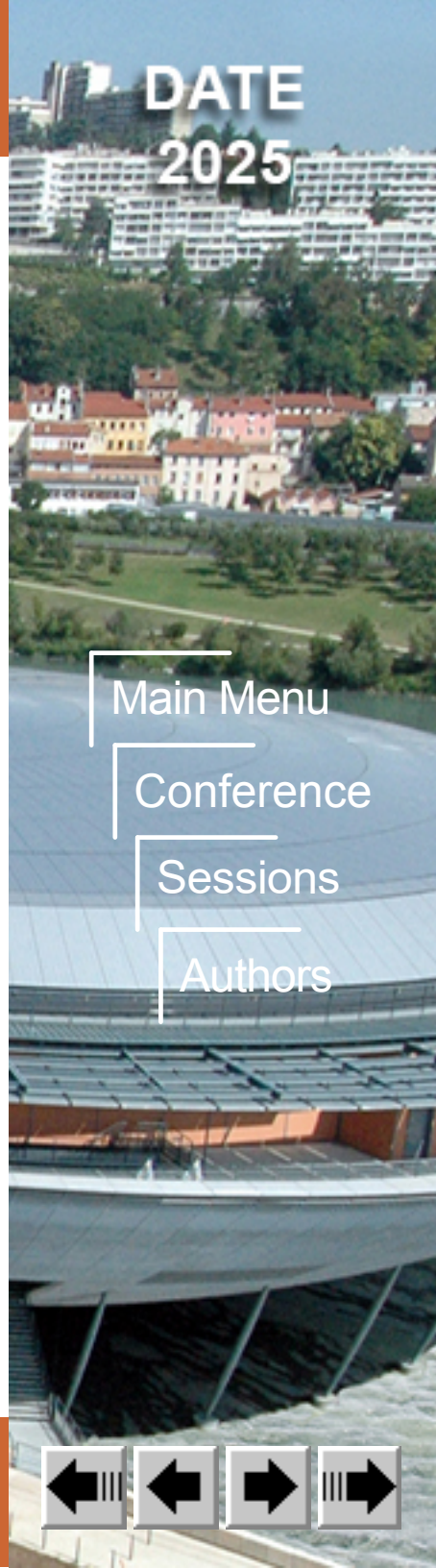
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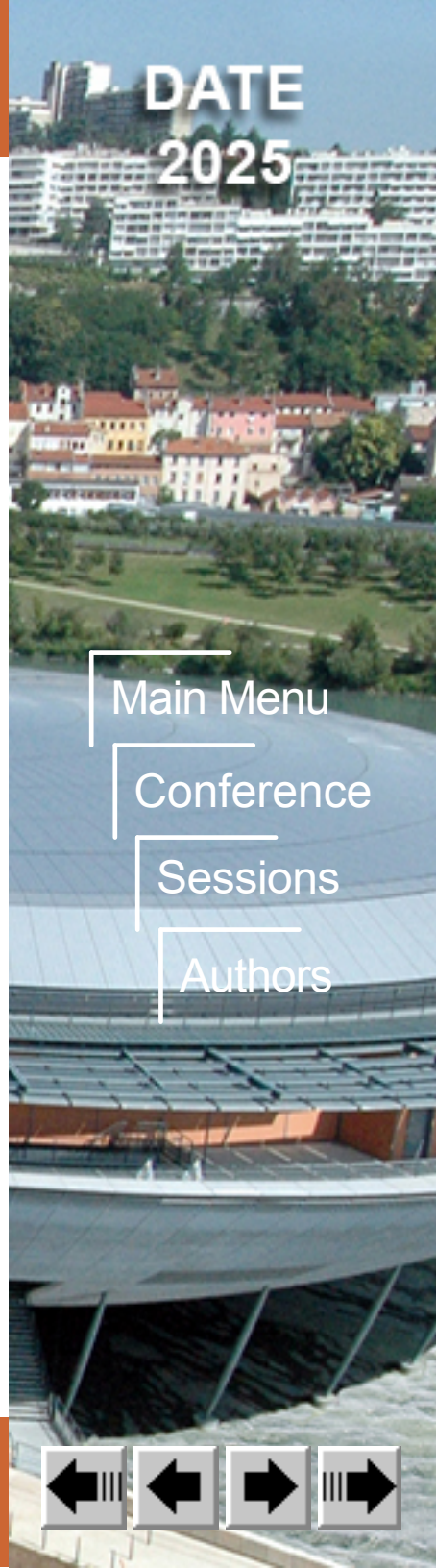
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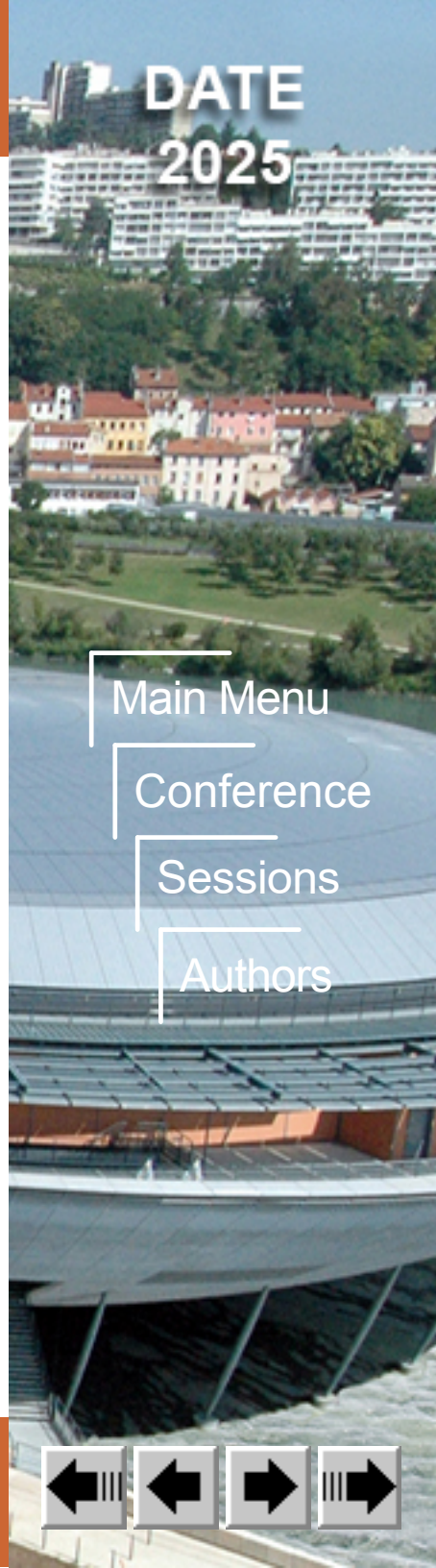
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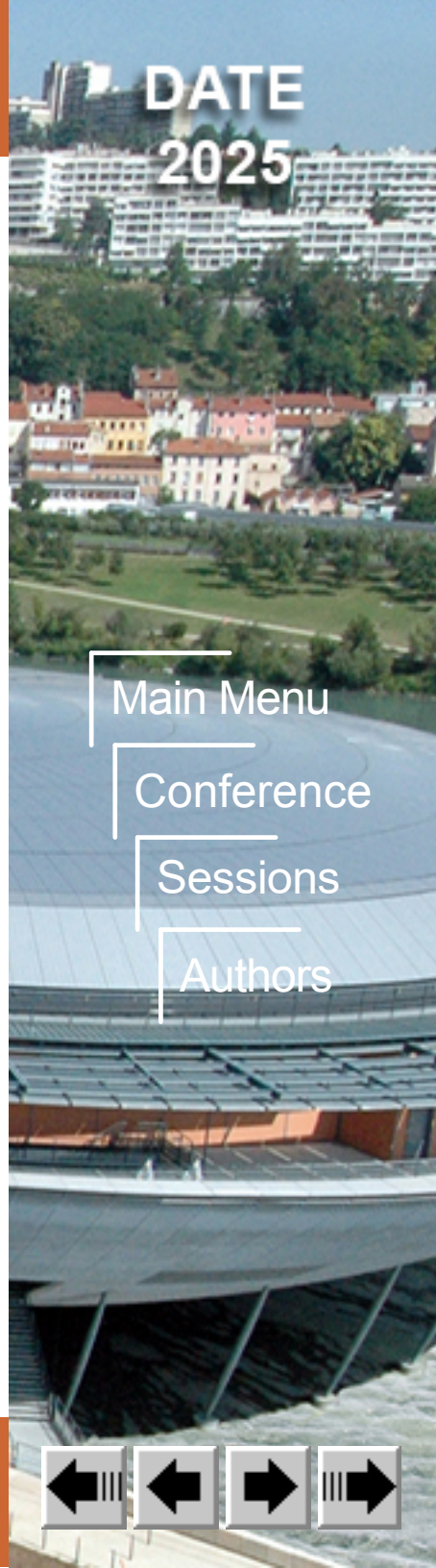
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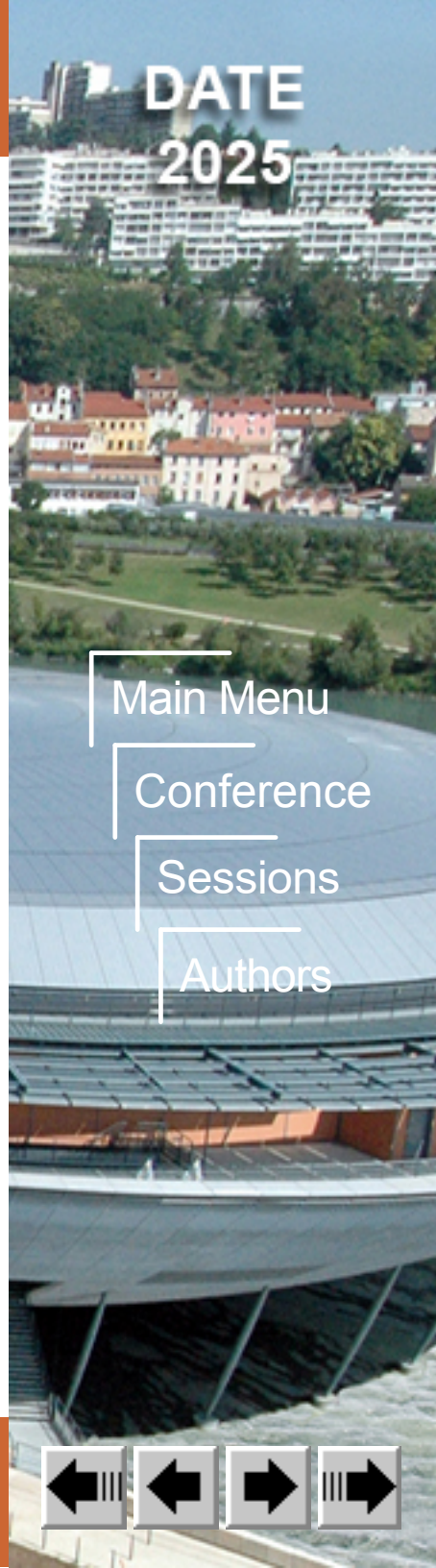
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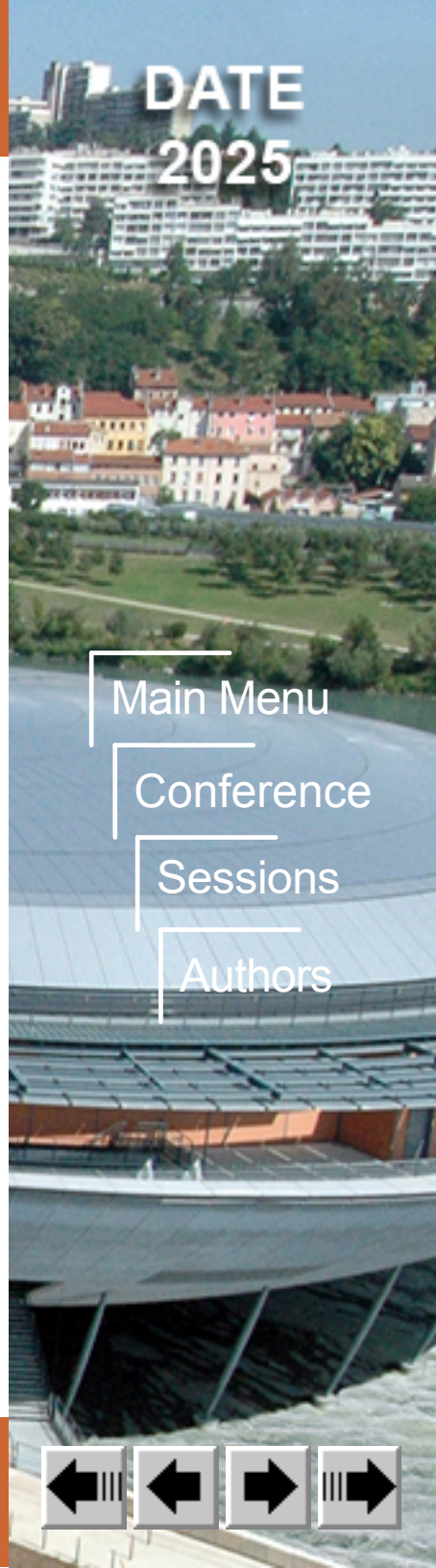
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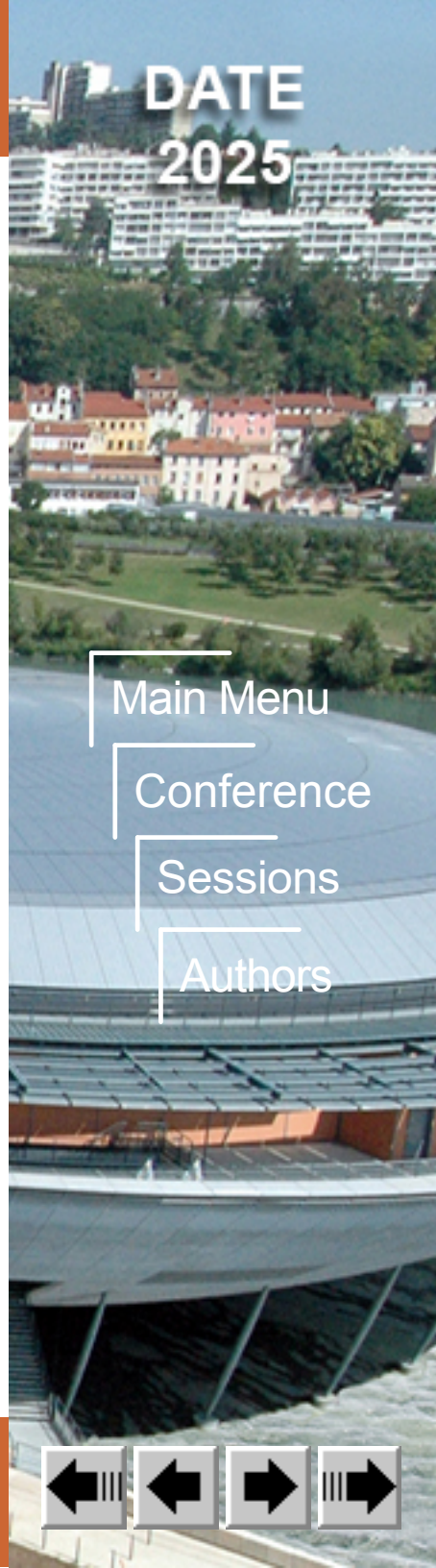
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- Qin, Aoxiang
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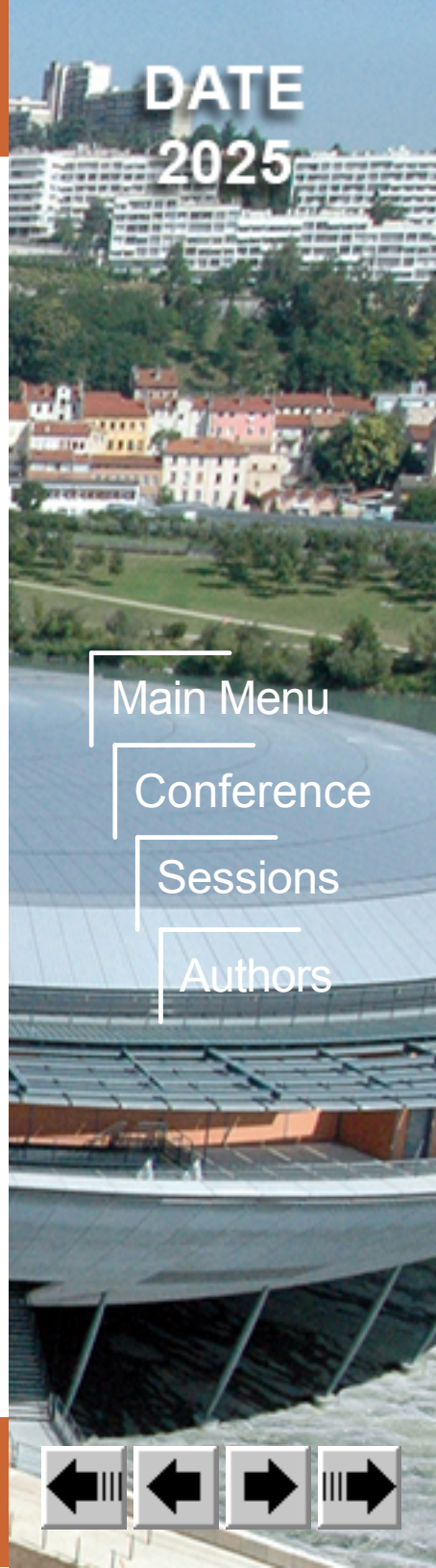
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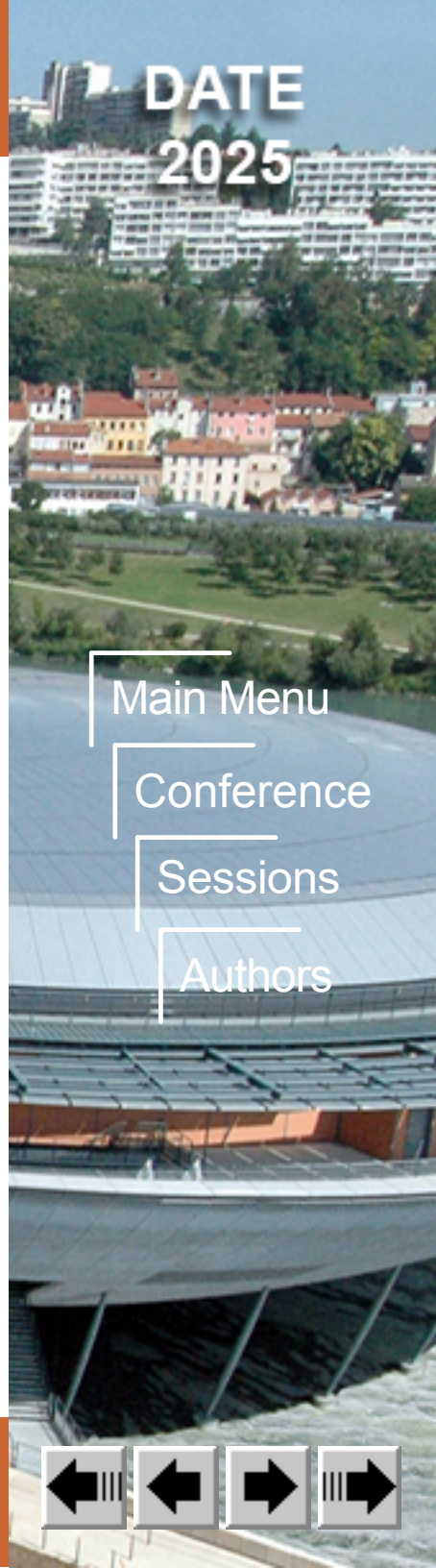
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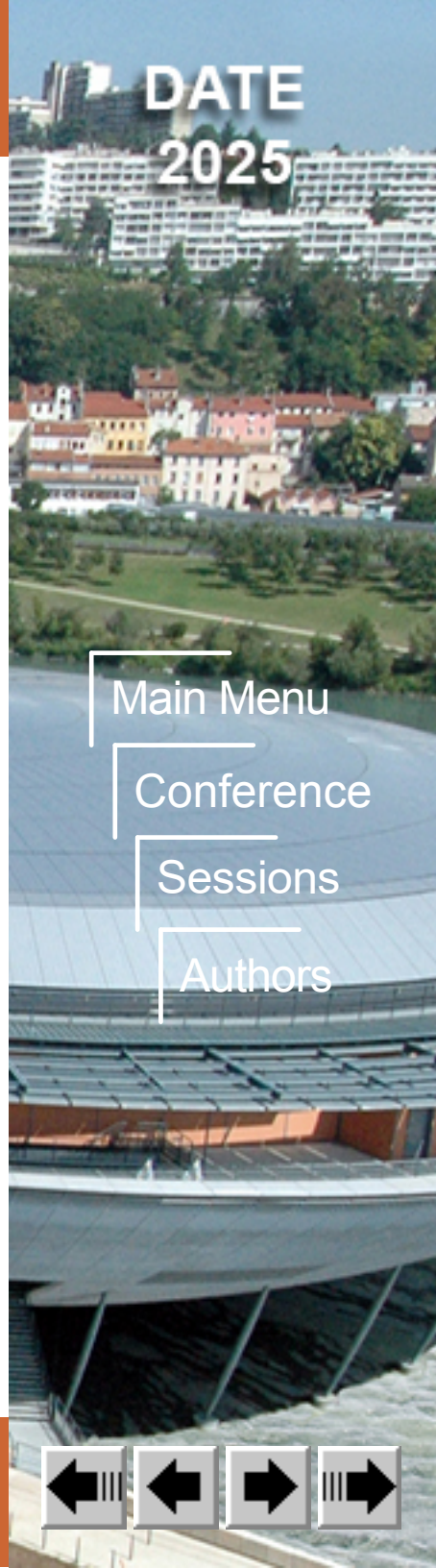
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- Schmid, Ludwig
- Schmid, Patrick
- Schmid, Ulrich
- Schmidt, Heidemarie
- Schneider, Christopher
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- Schulz, Martin

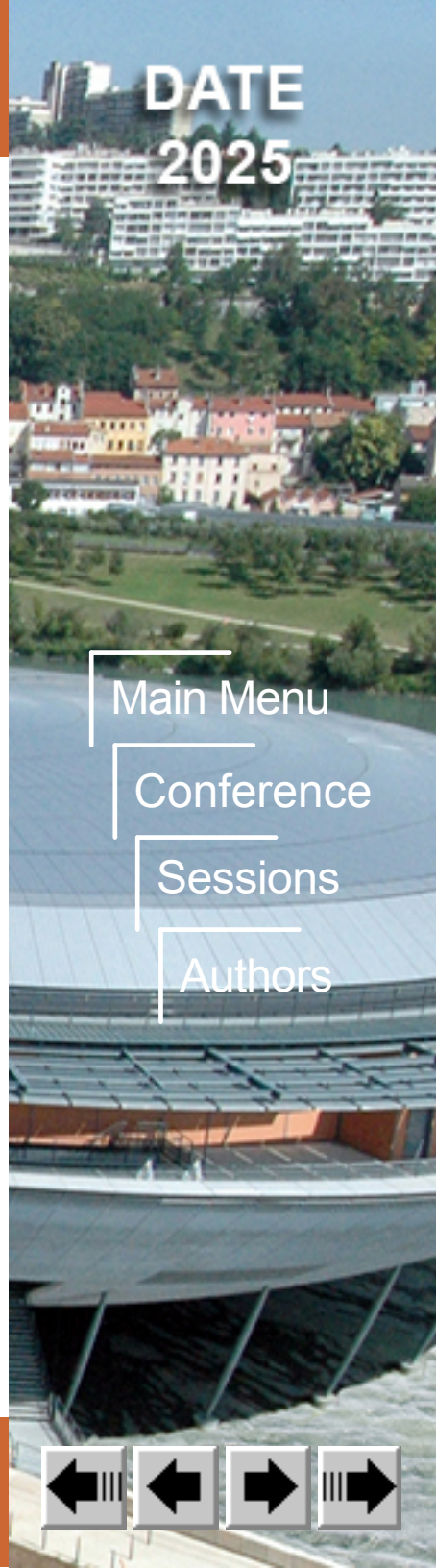
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- Shen, Chaoyao
- Shen, Chun-Wei
- Shen, Diyou
- Shen, Guobin
- Shen, Jinyi
- Shen, John Paul
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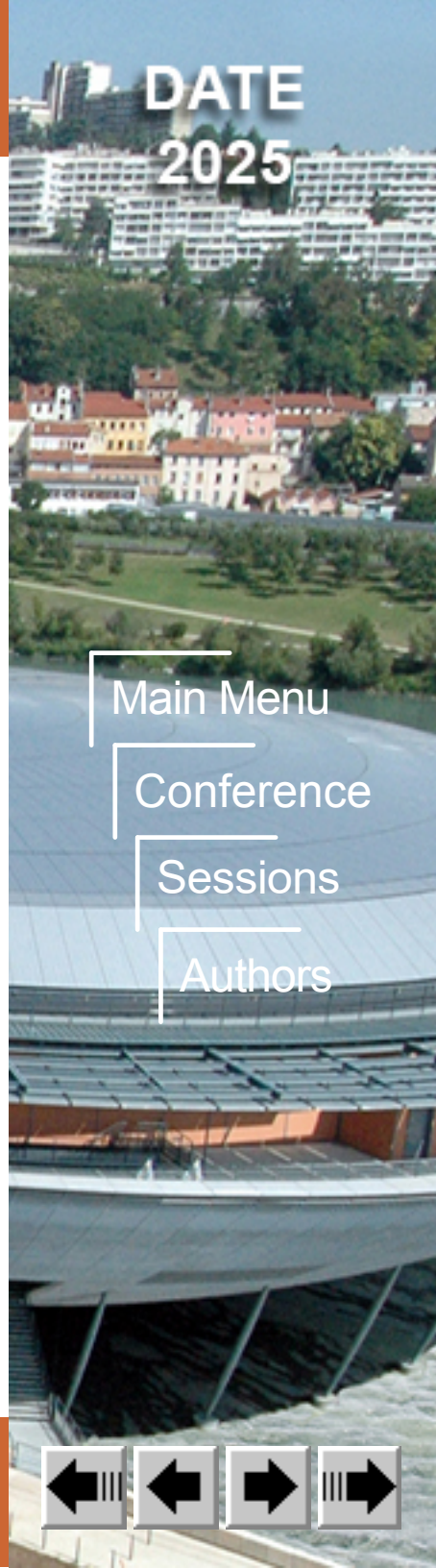
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- Shinde, Shweta
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- Sigl, Georg
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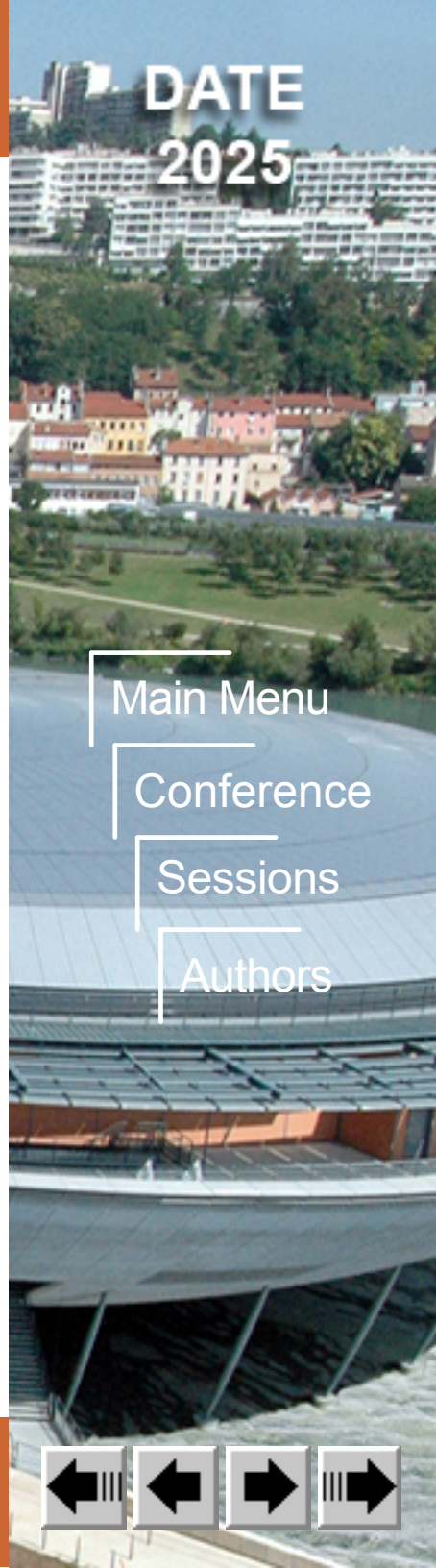
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- Sotiropoulos, Aris
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- Soudris, Dimitrios
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- Sousa, Leonel

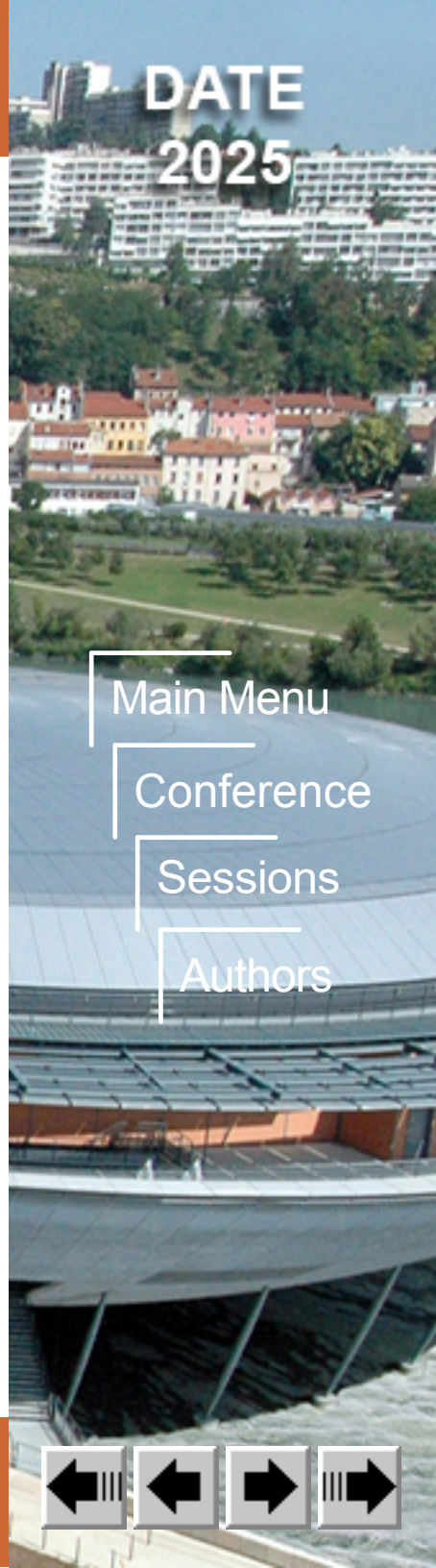
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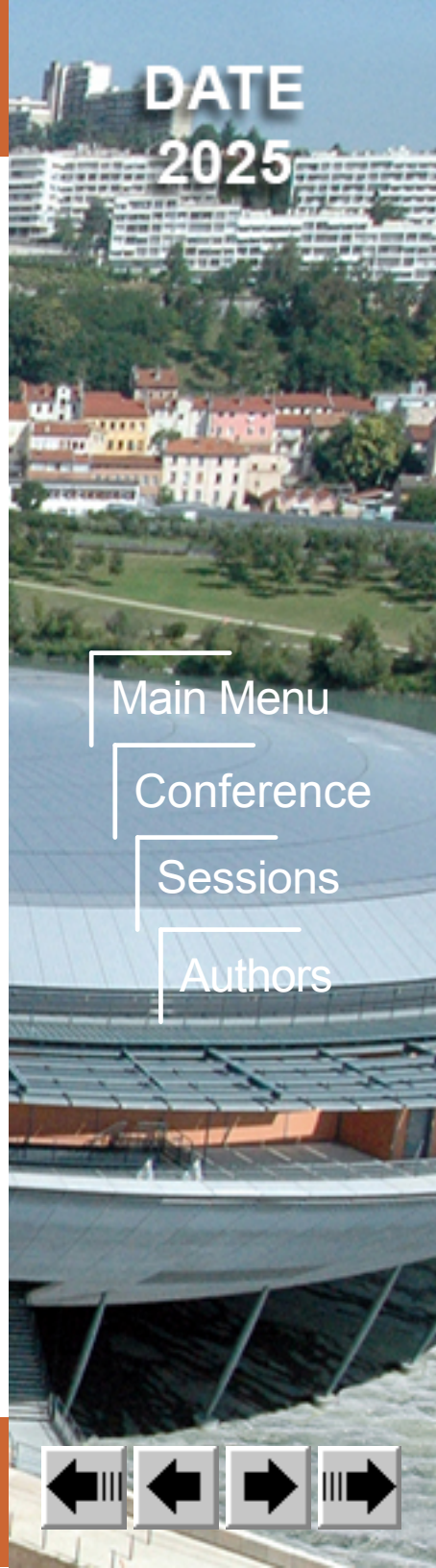
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- Tang, Hao
- Tang, Jiaping
- Tang, Minjin
- Tang, Ningzhi
- Tang, Ruofei
- Tang, Shidi
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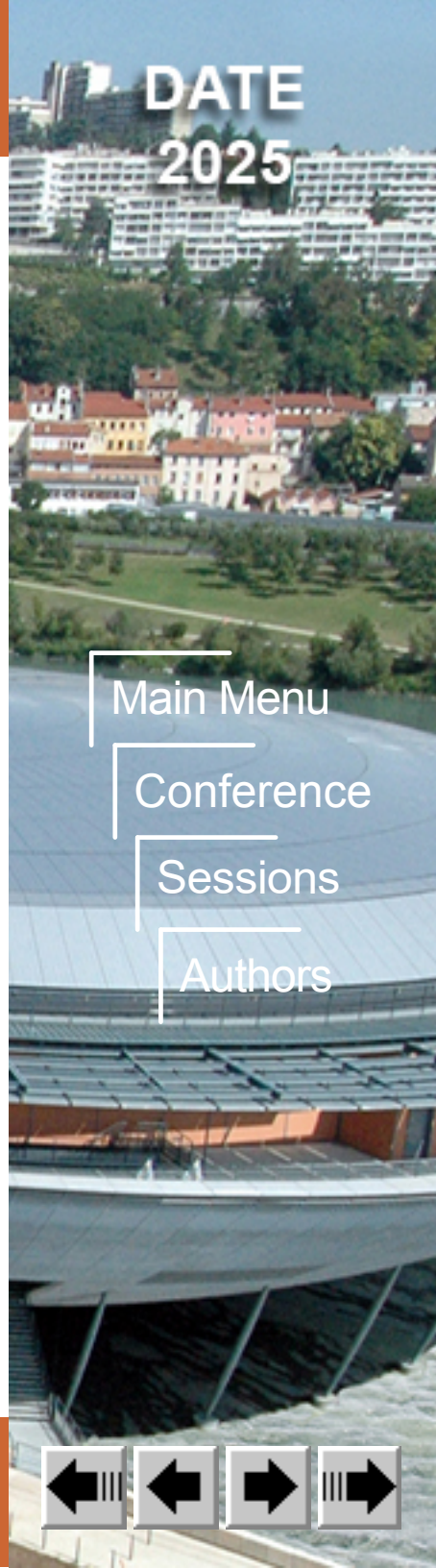
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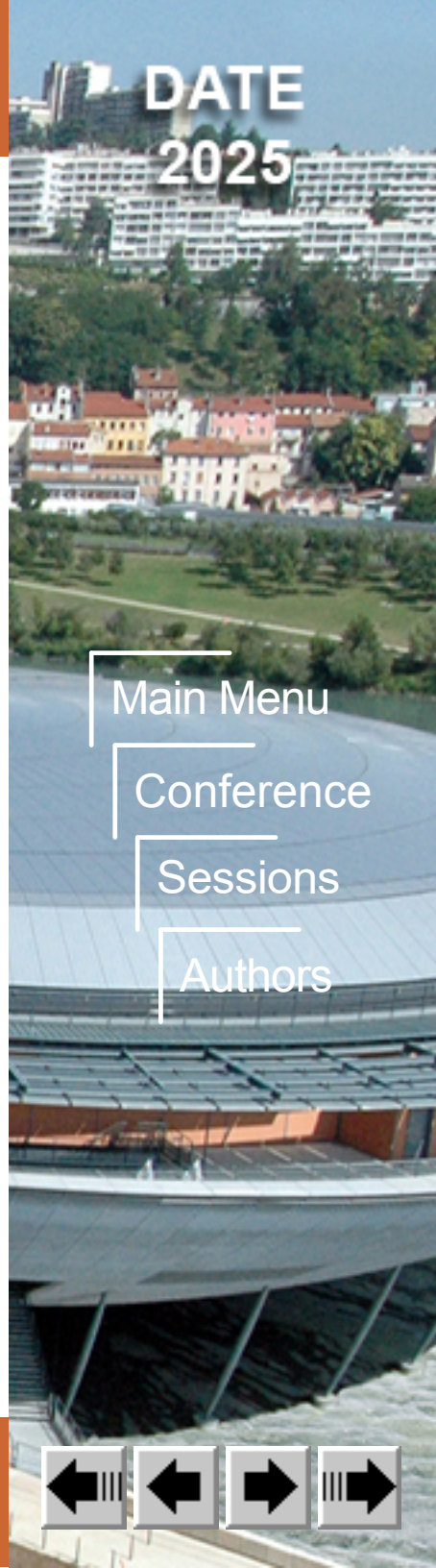
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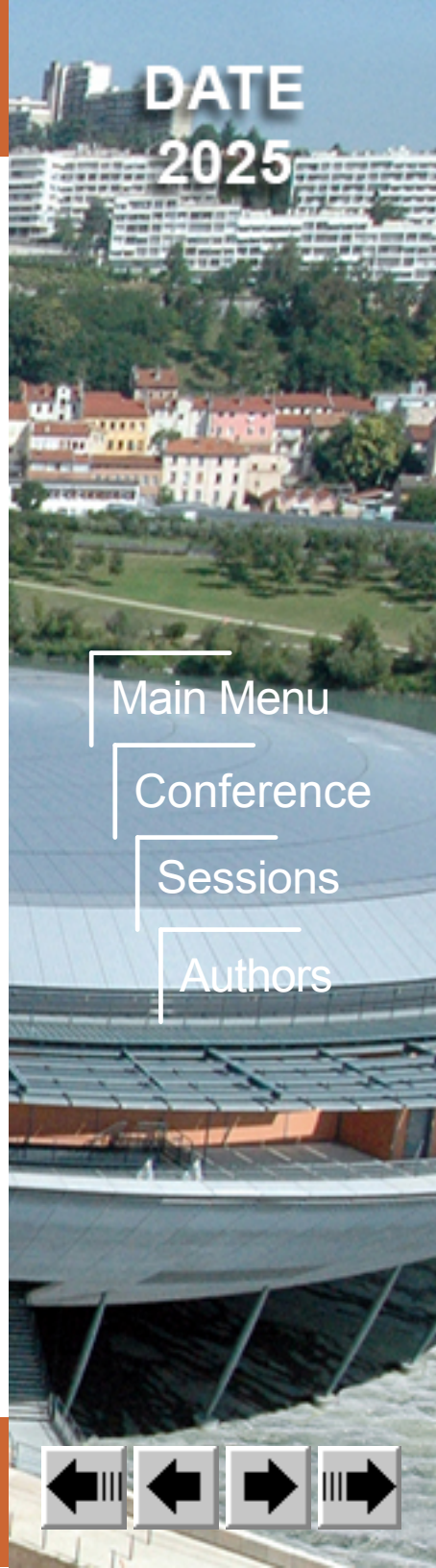
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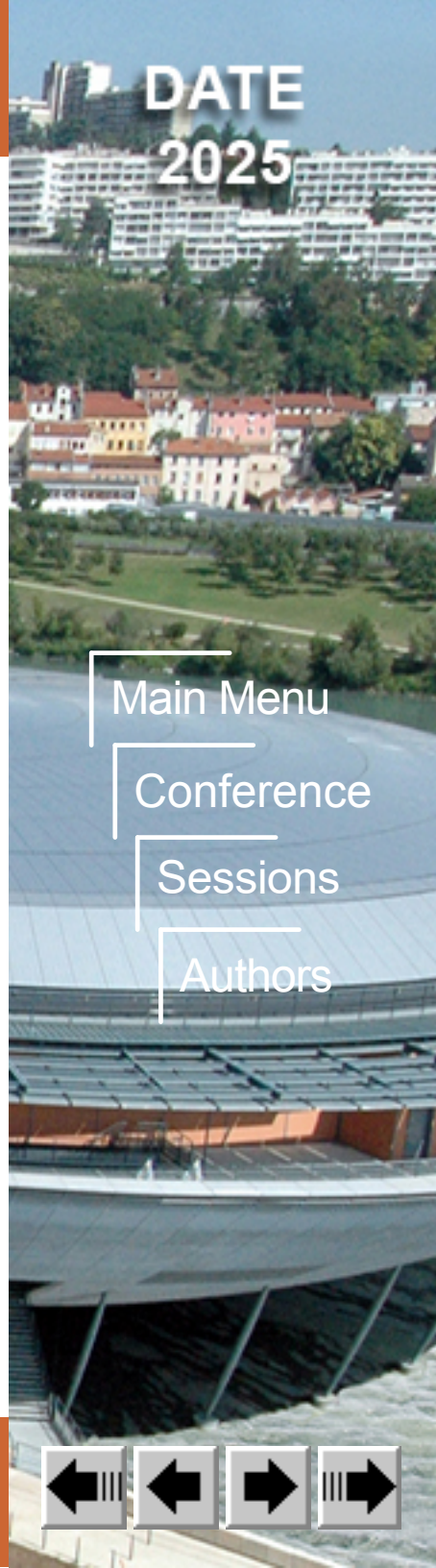
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- Wang, Jinqiao
- Wang, Jinquan
- Wang, Ke
- Wang, Kun
- Wang, Leyan
- Wang, Liang
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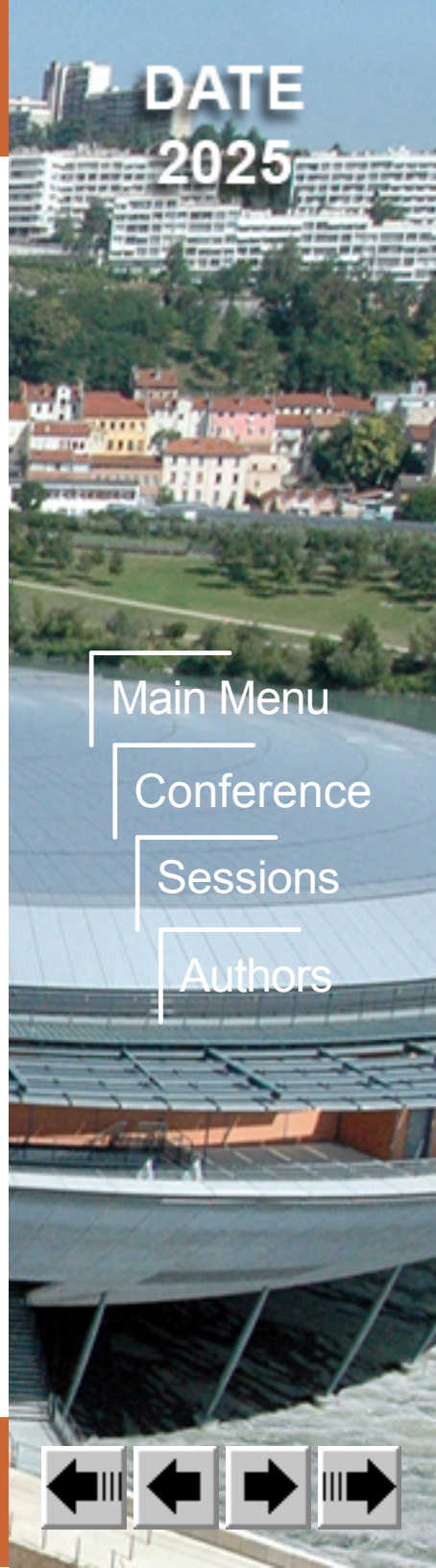
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- Wang, Yichuan
- Wang, Yining
- Wang, Yongwen
- Wang, Youwen
- Wang, Yu Chen
- Wang, Yuan
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- Wang, Yuhan

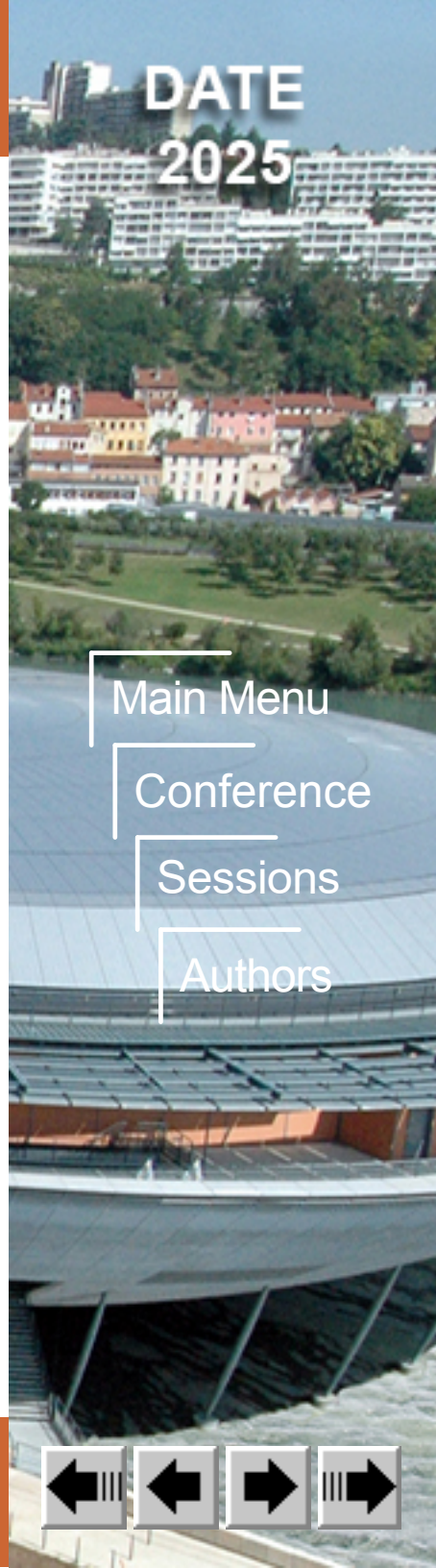
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- Weinstock, Jan Henrik
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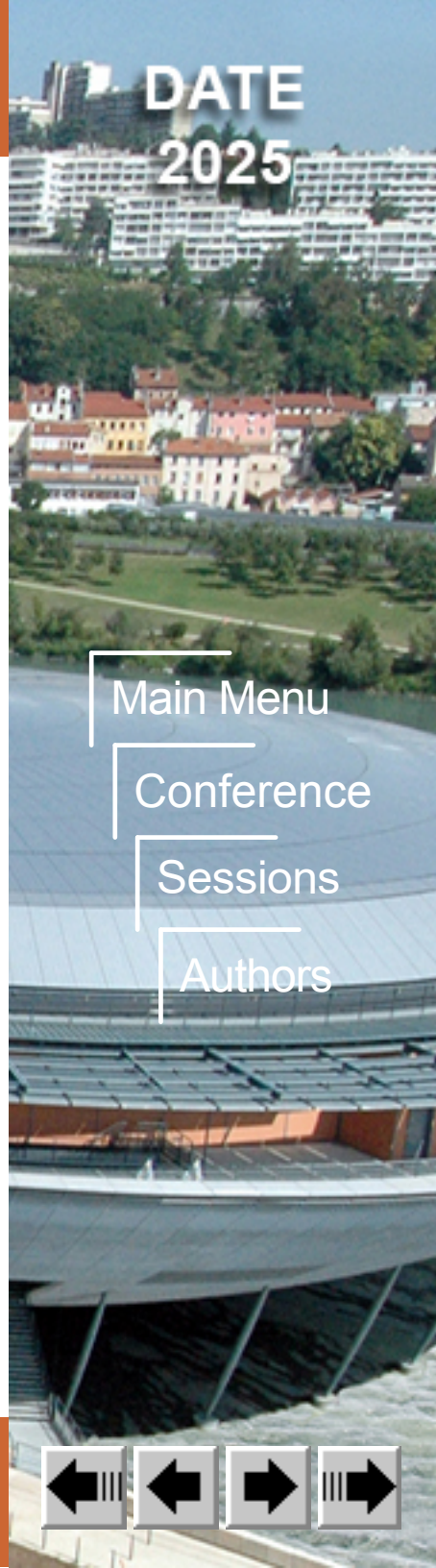
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- Xiao, Xun
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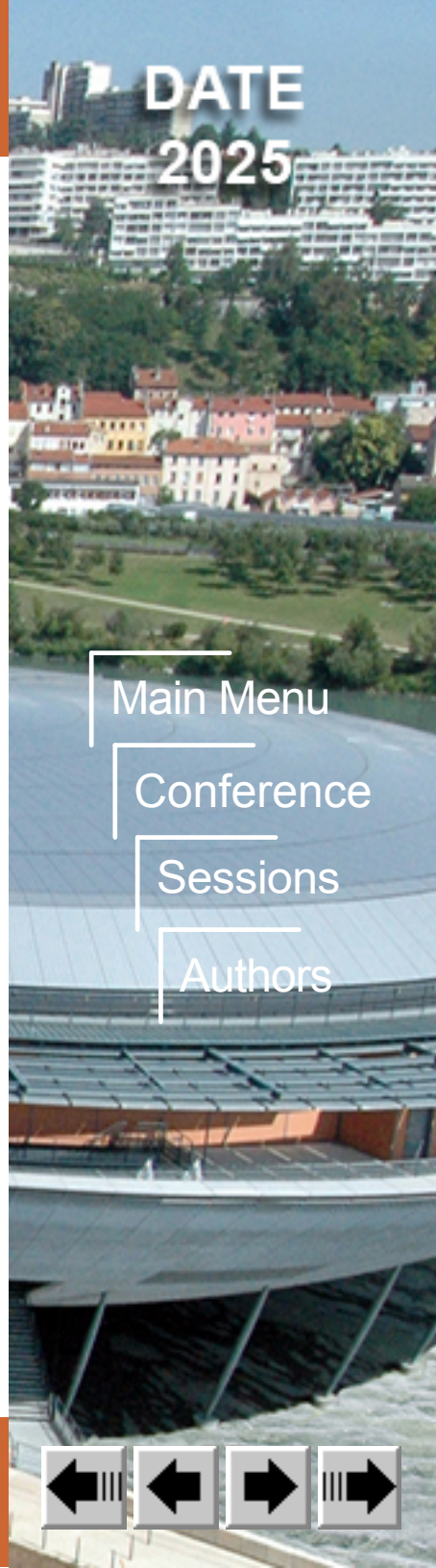
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- Xu, Weikai
- Xu, Weixia
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- Xu, Yuanchao
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- Xue, Ke
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- Xue, Yufei
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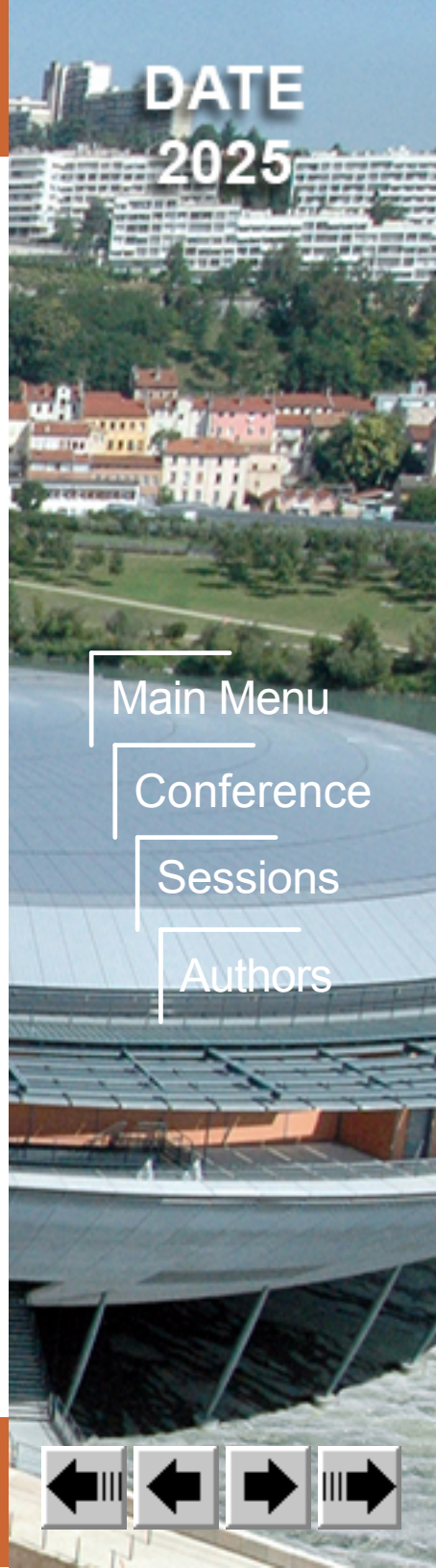
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- Yang, Lita
- Yang, Ning
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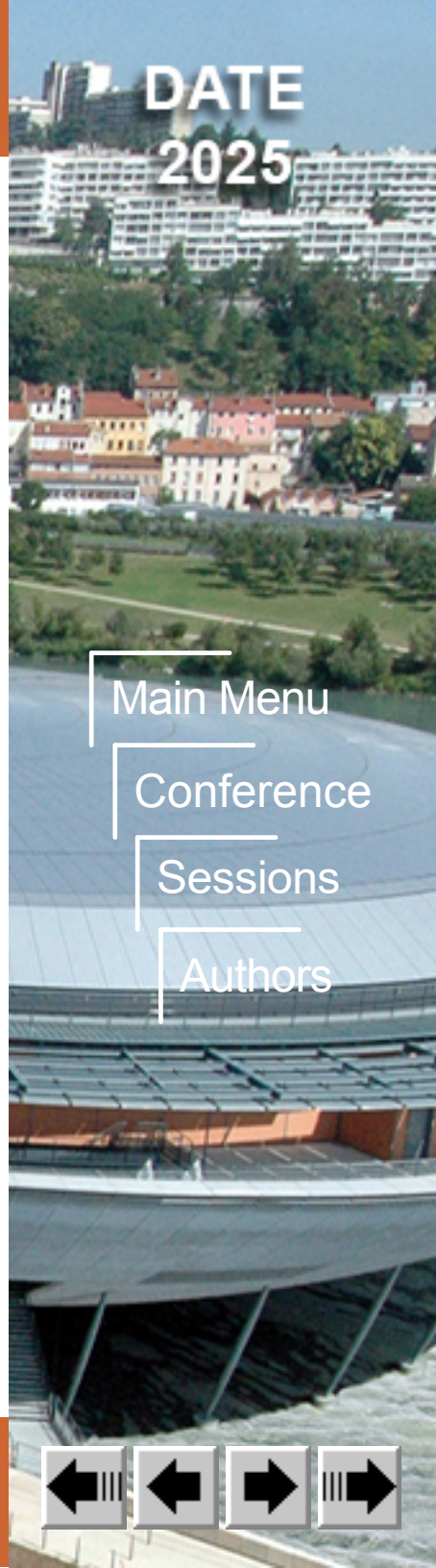
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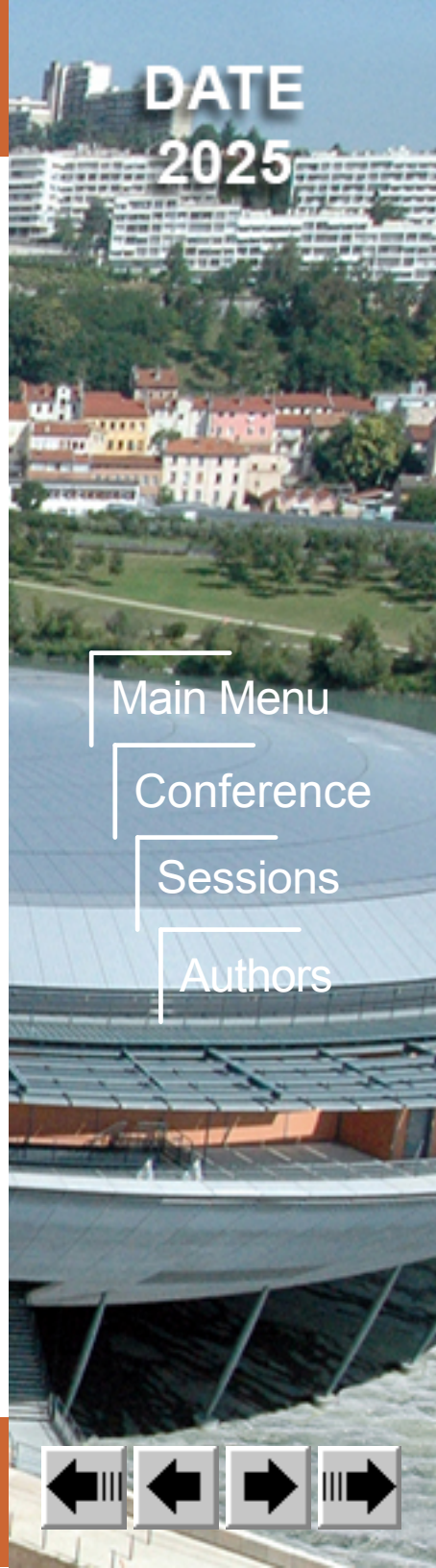
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- Zeng, Yue

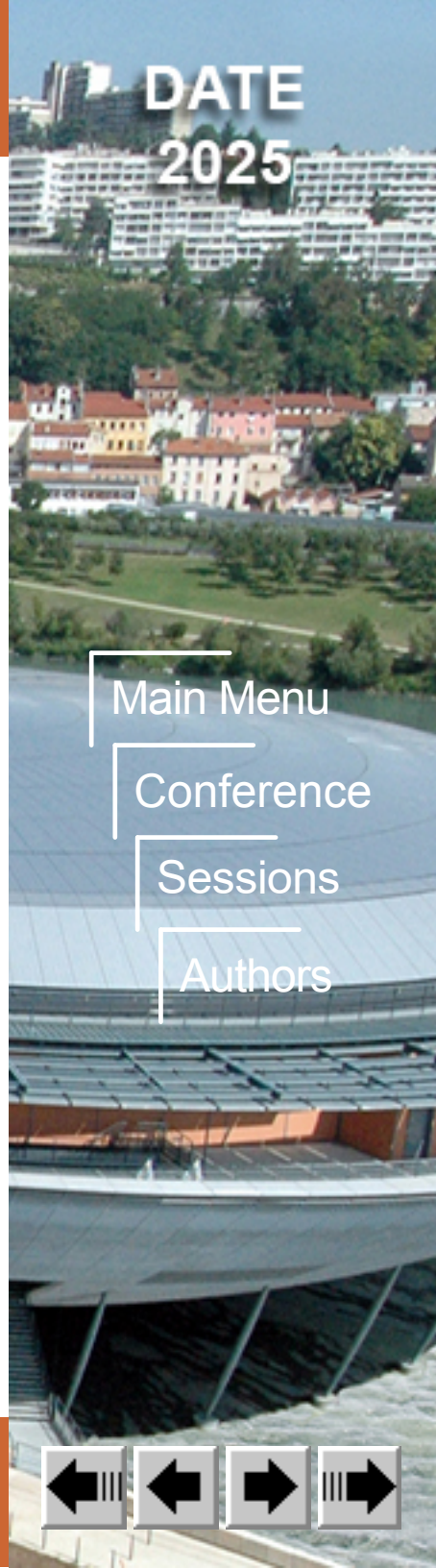
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- Zhang, Han
- Zhang, Hao
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- Zhang, Meng
- Zhang, Qian
- Zhang, Qing
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- Zhang, Runhua

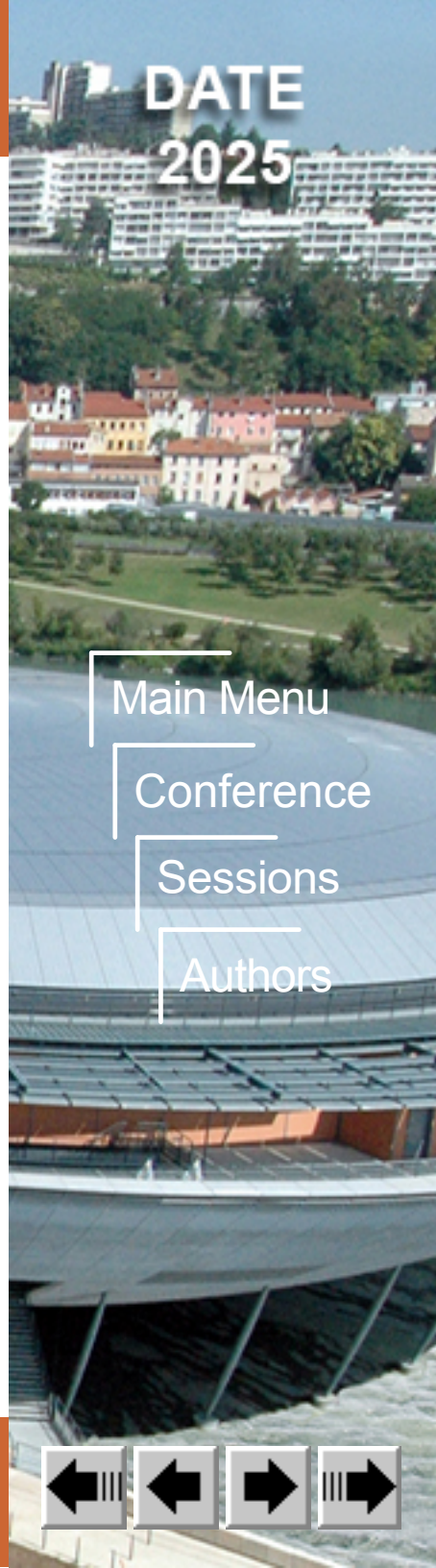
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- Zhang, Yanqing
- Zhang, Yichao
- Zhang, Yifan
- Zhang, Yipu
- Zhang, Yong
- Zhang, Yucheng
- Zhang, Yuhang
- Zhang, Yujie
- Zhang, Yunxiang
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- Zhang, Zhengya
- Zhang, Zhenya
- Zhang, Zhiyuan
- Zhang, Zicheng
- Zhao, Dongcheng
- Zhao, Guannan
- Zhao, Haibin
- Zhao, Hengrui
- Zhao, Hongxiao
- Zhao, Jianjun
- Zhao, Junping

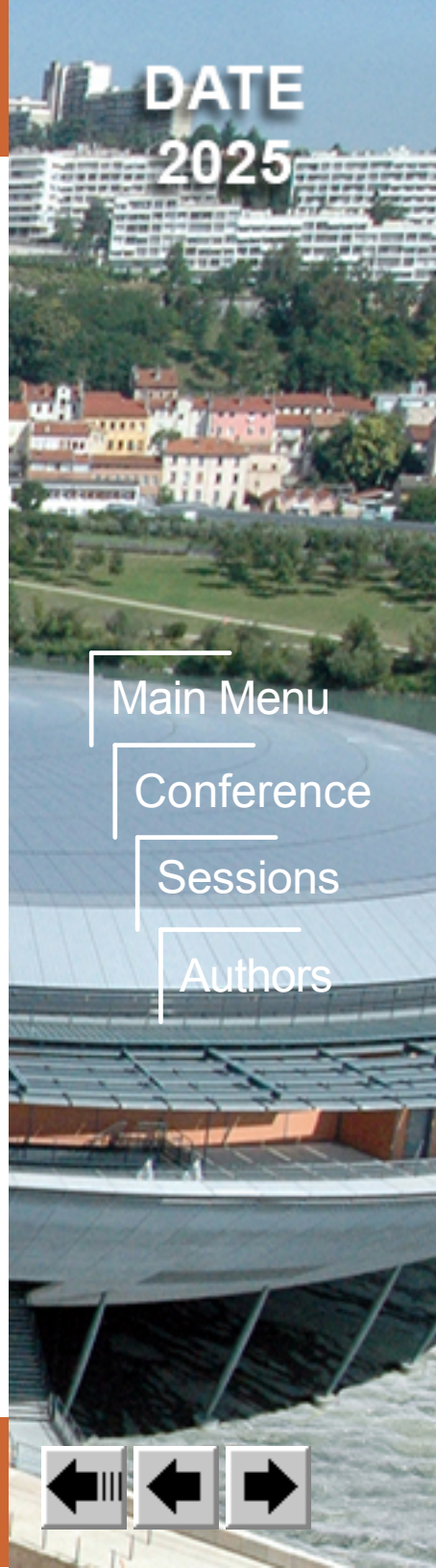
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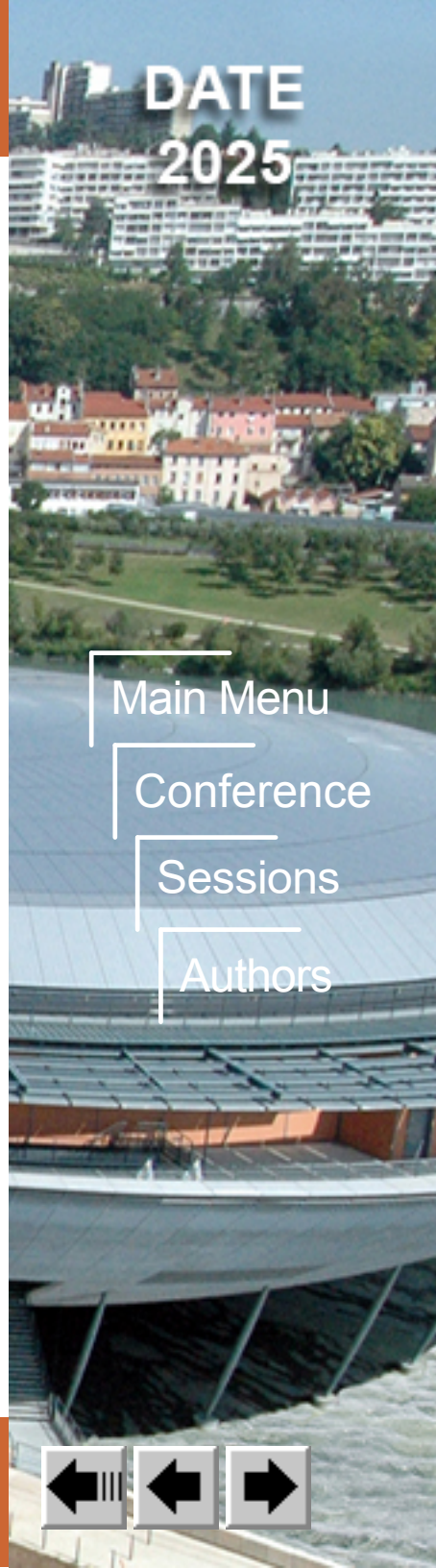
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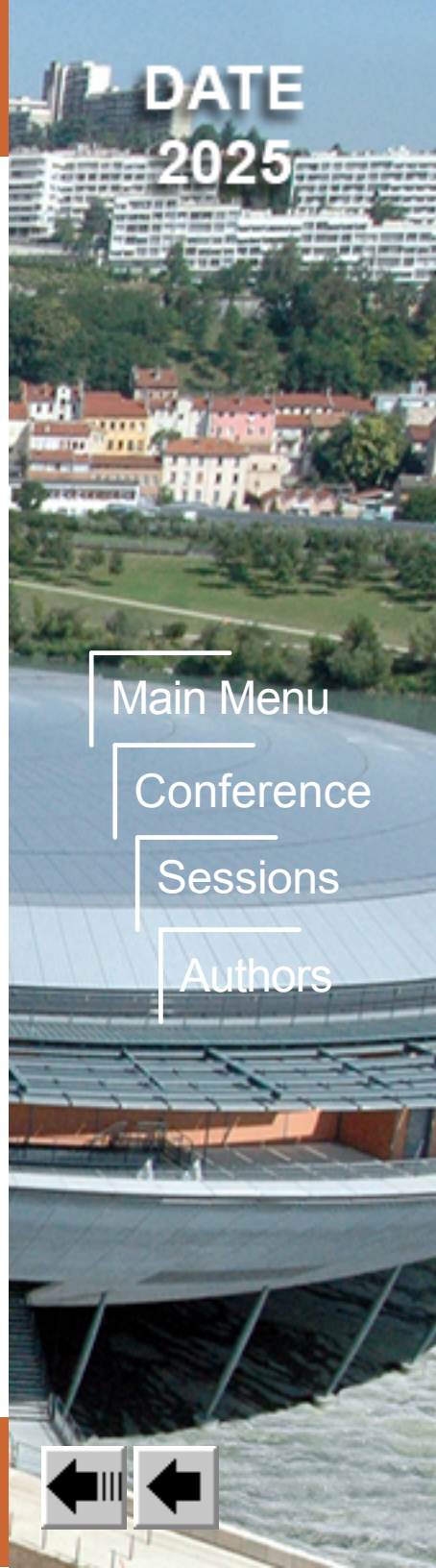
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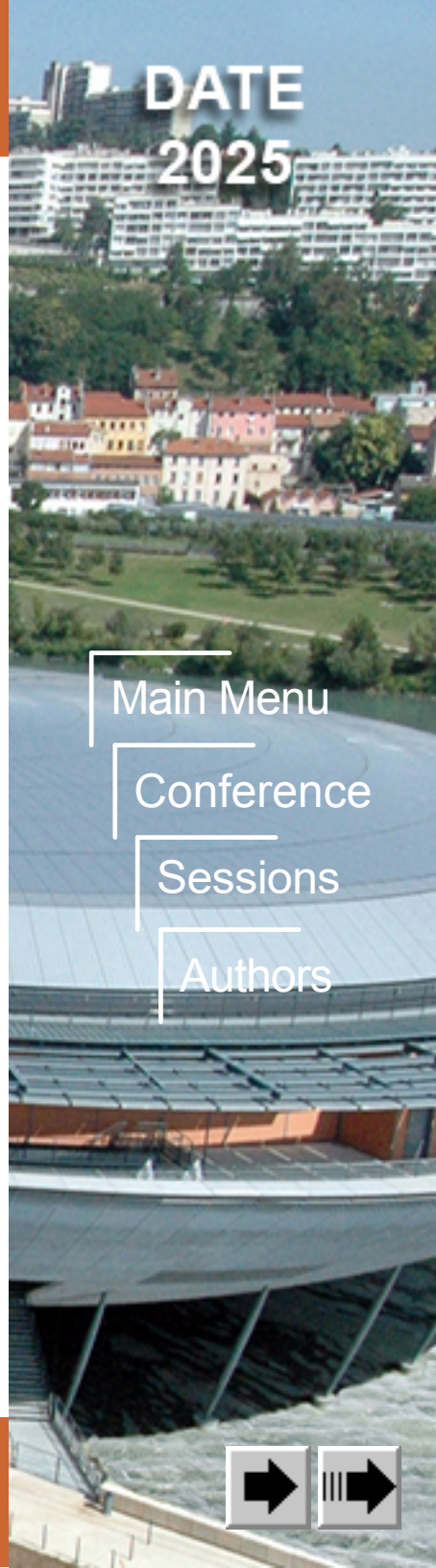
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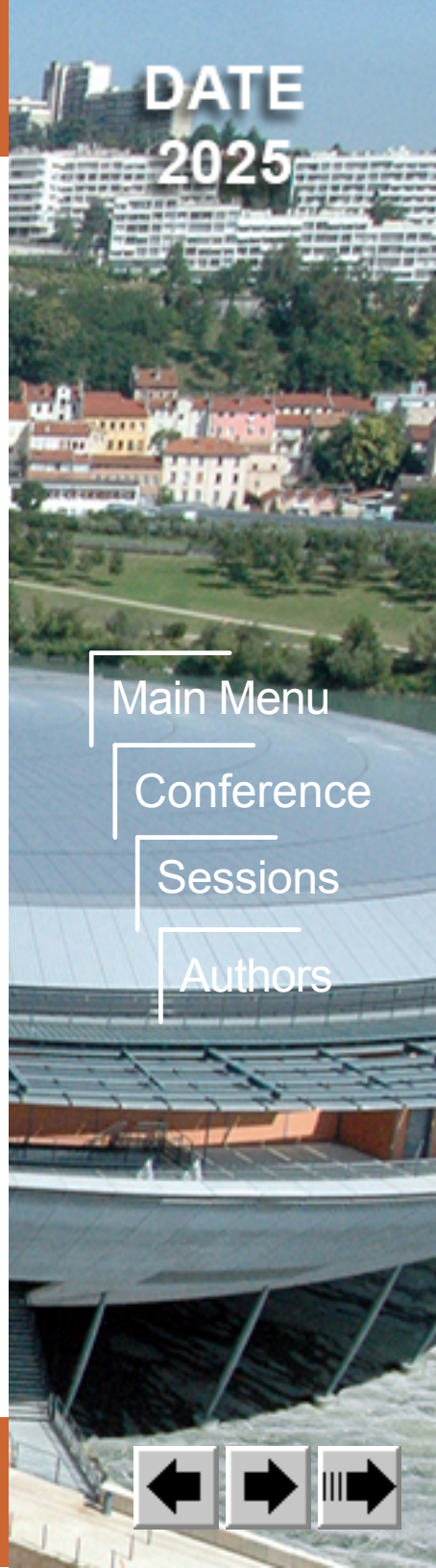
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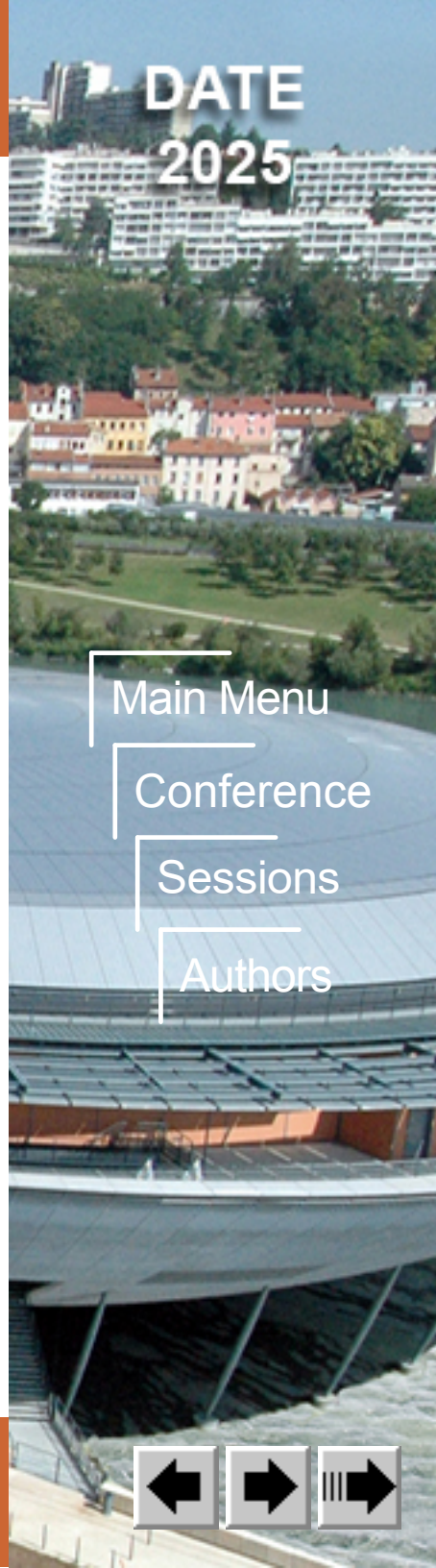
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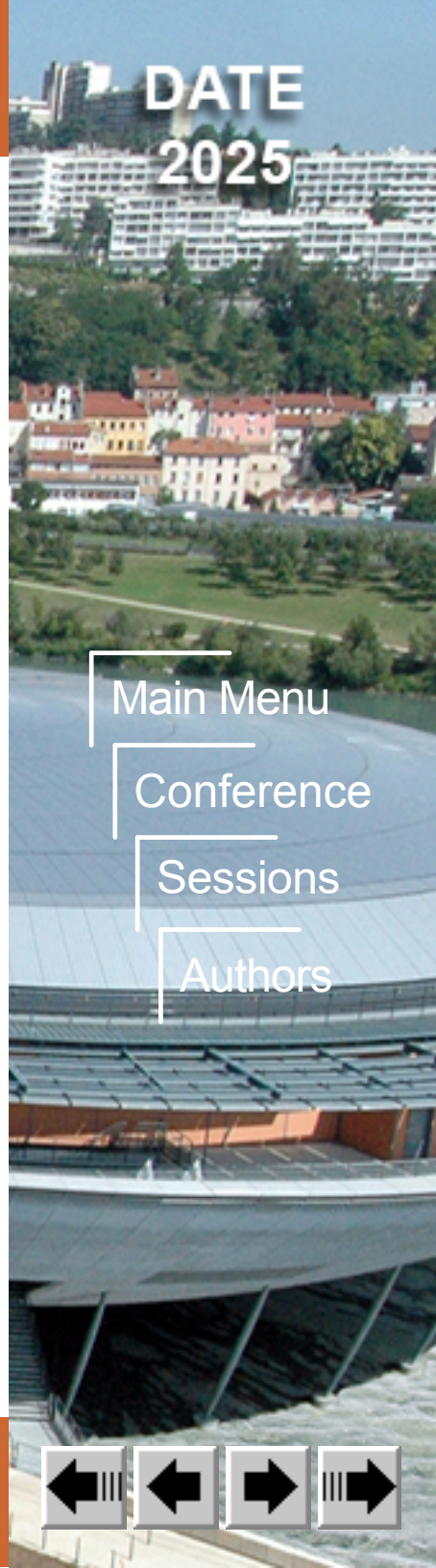
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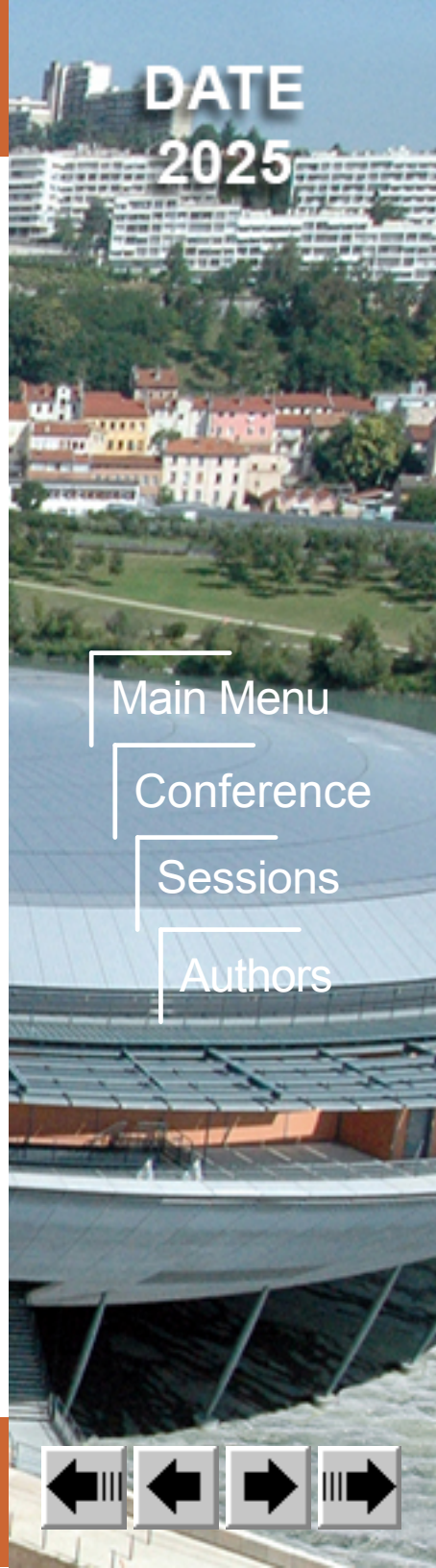
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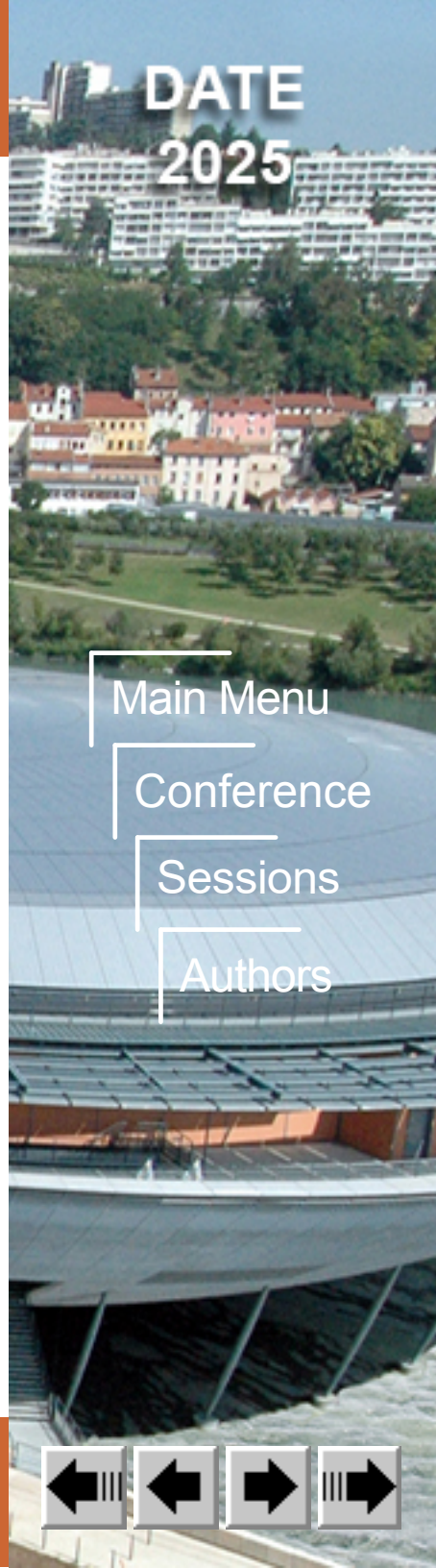
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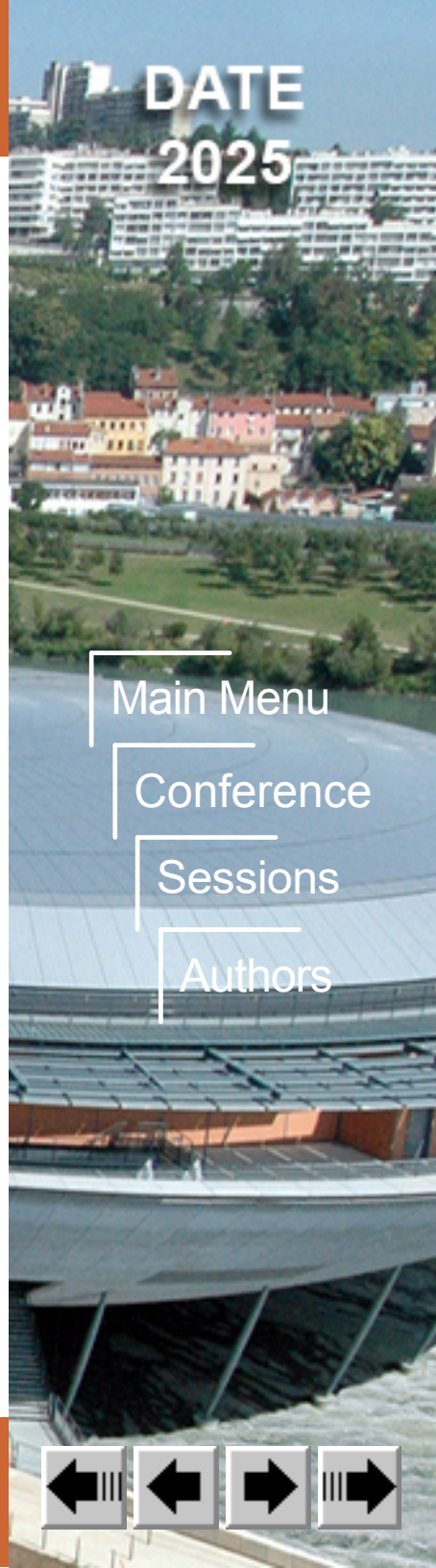
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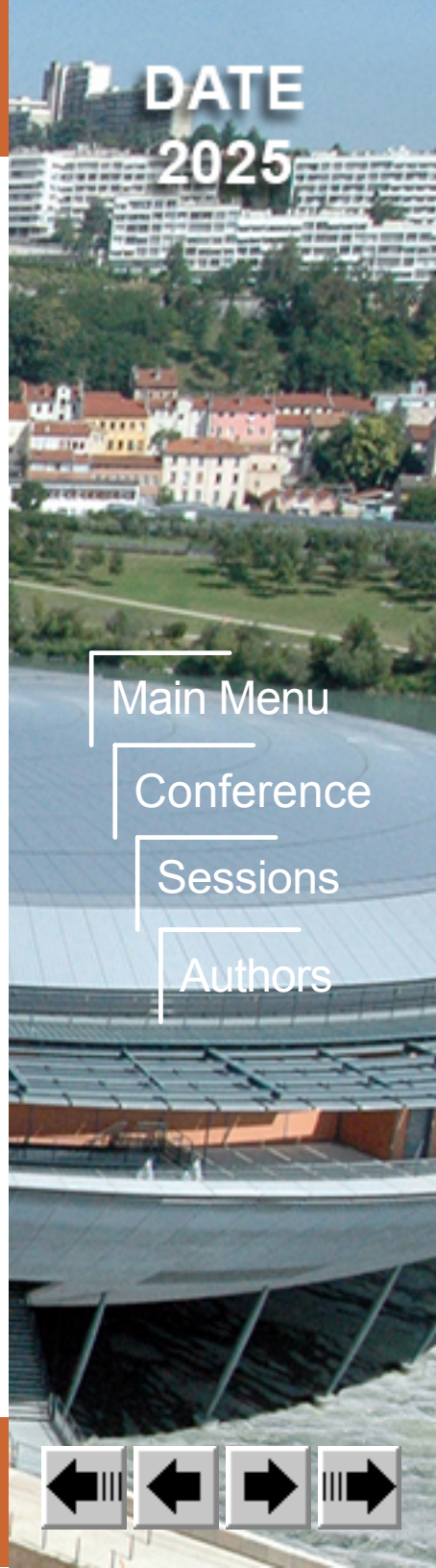
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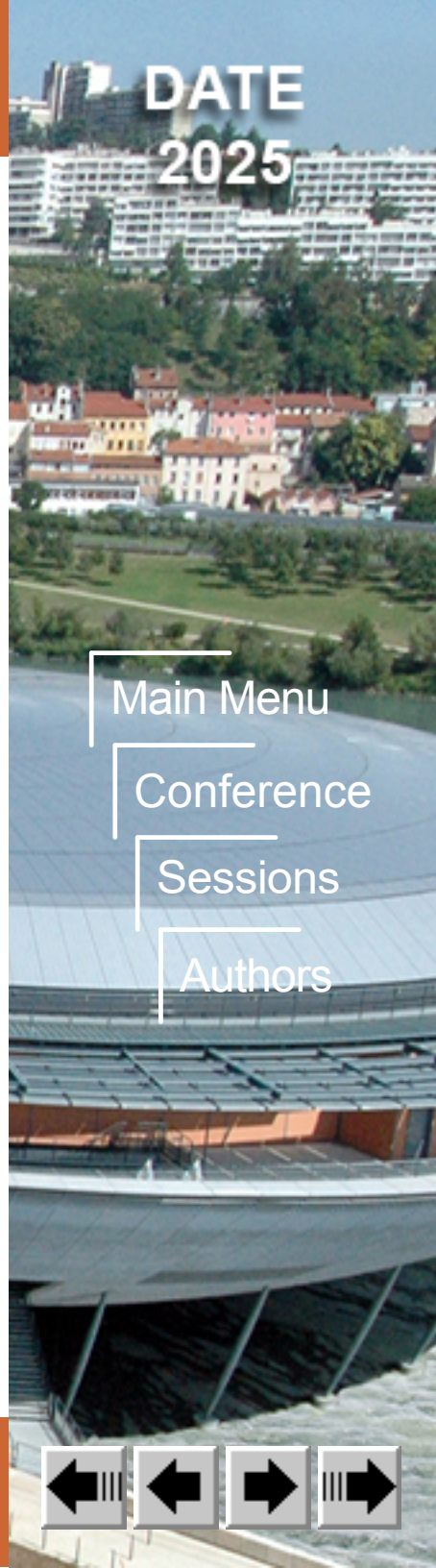
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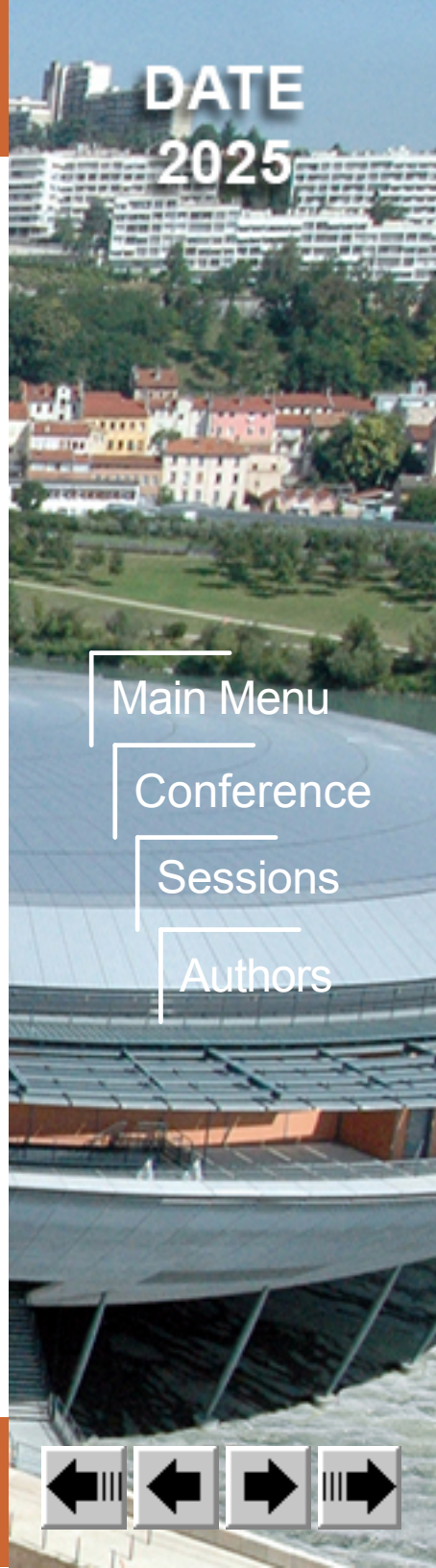
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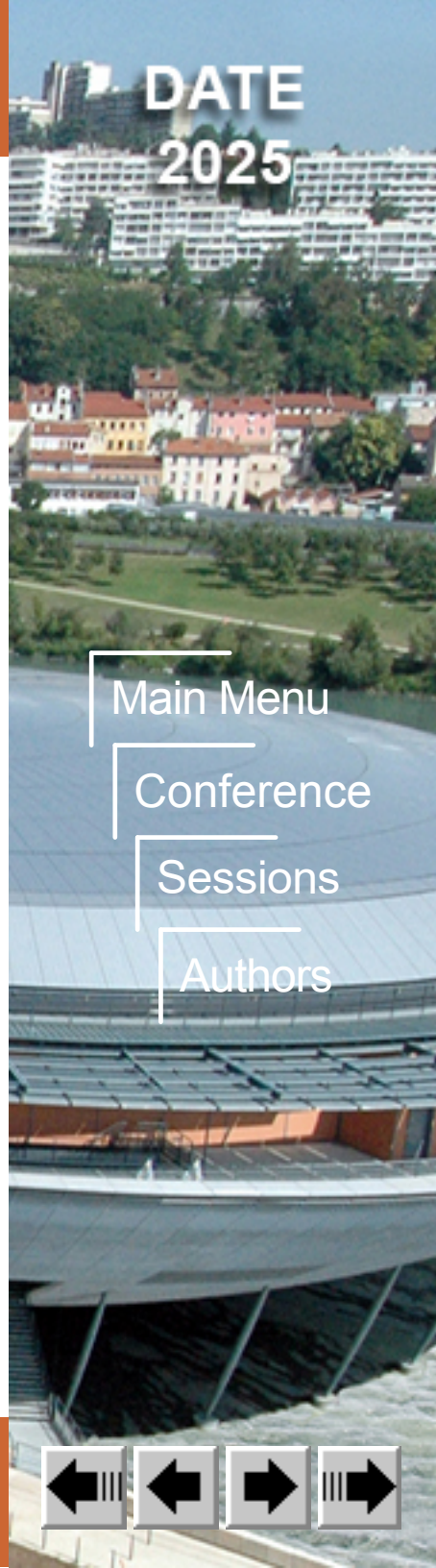
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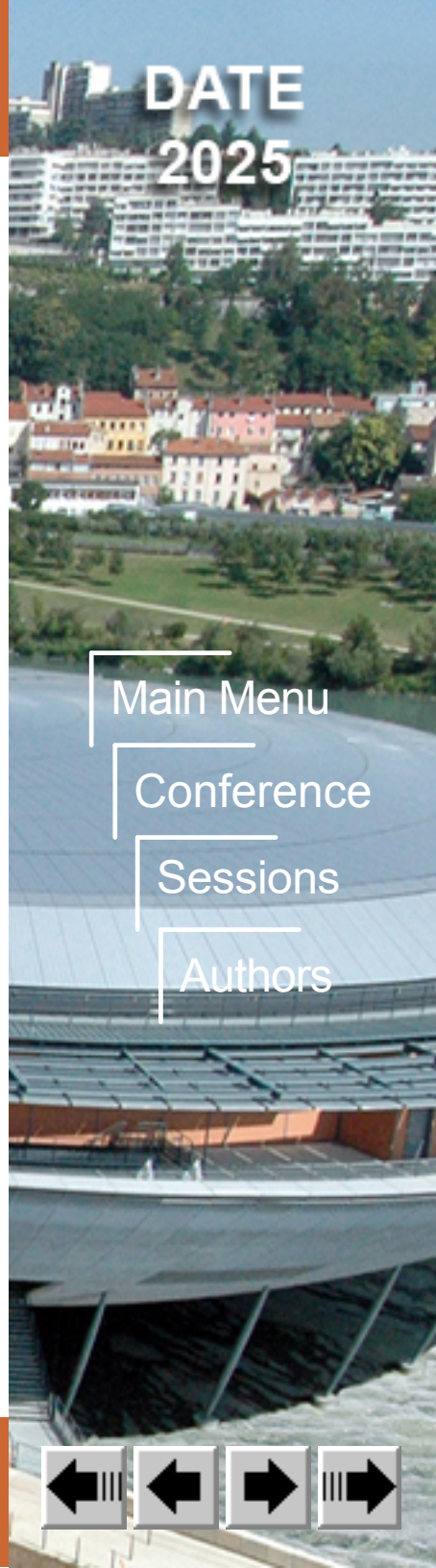
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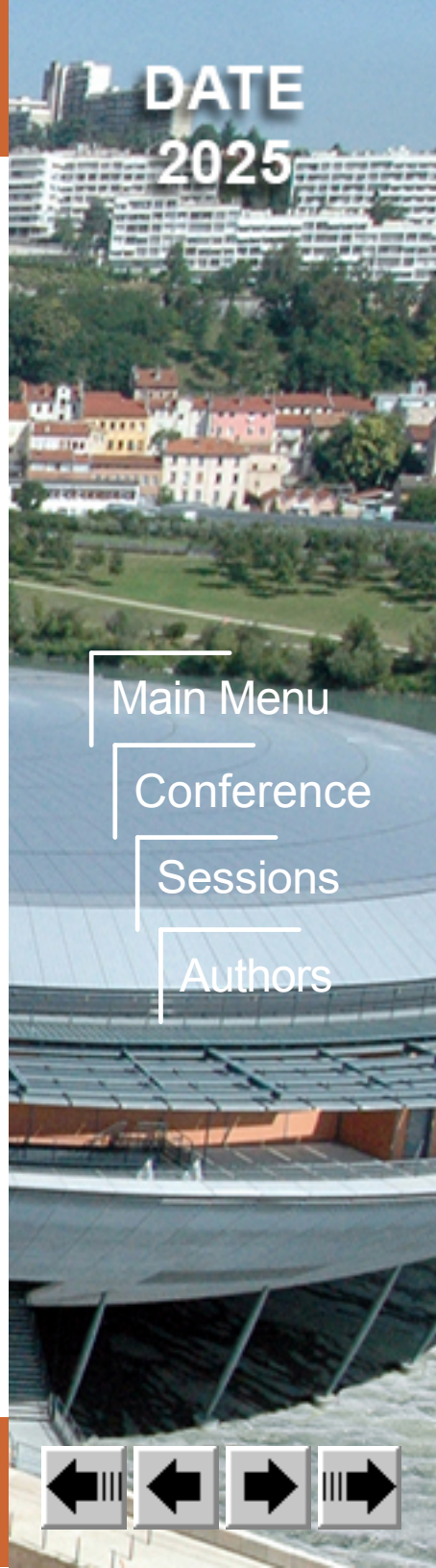
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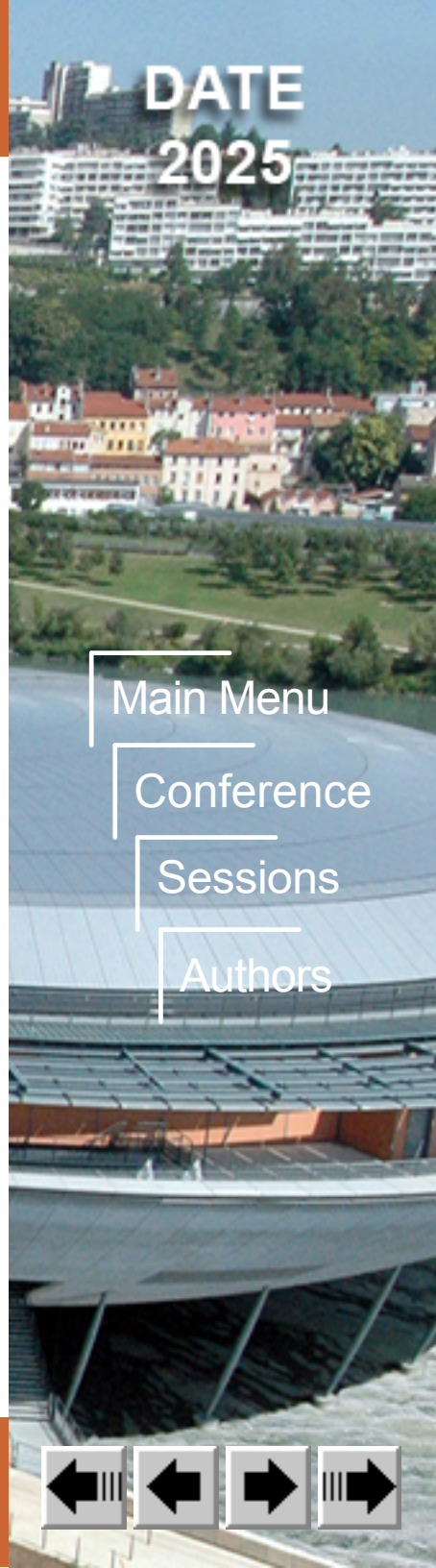
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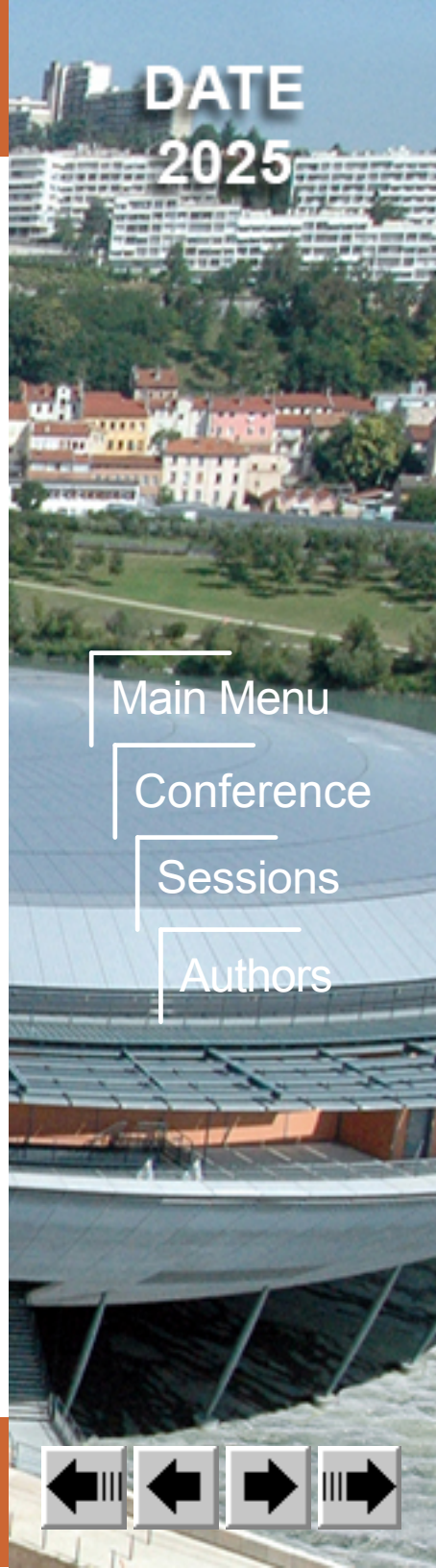
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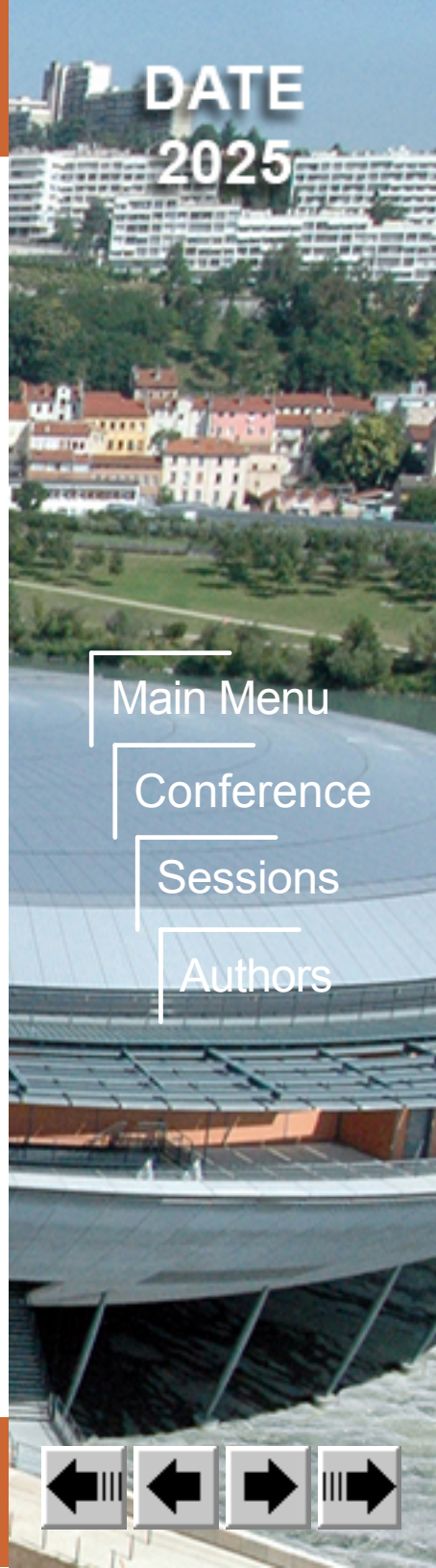
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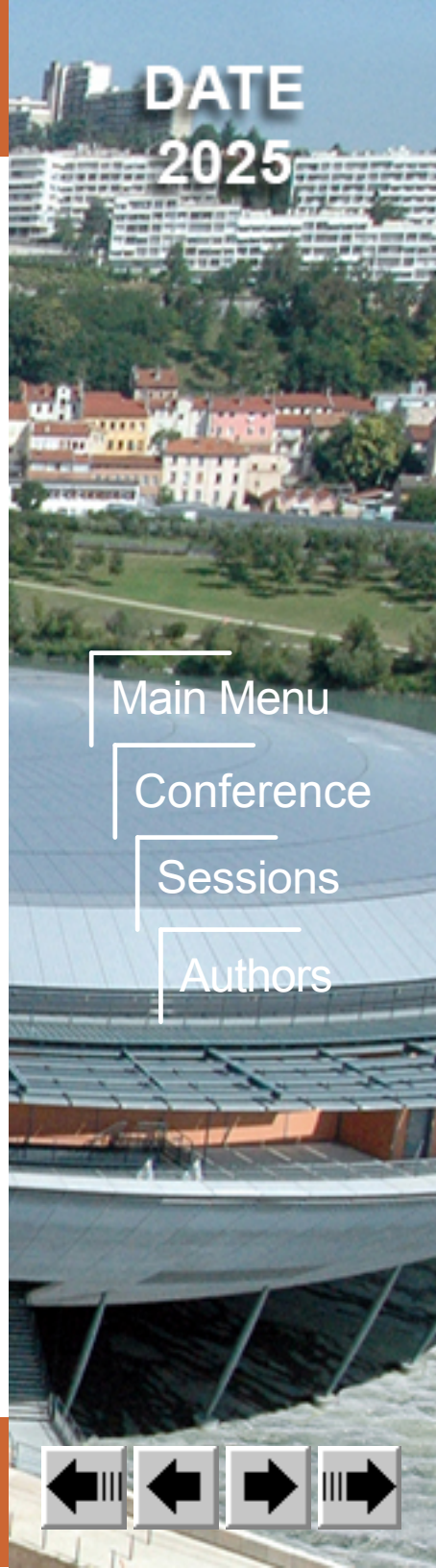
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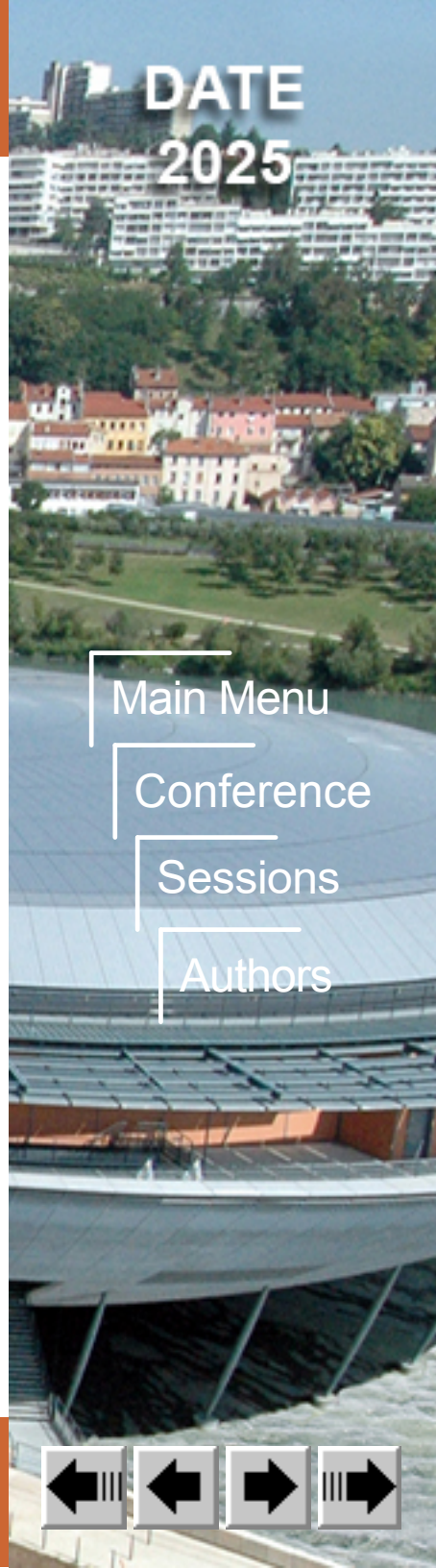
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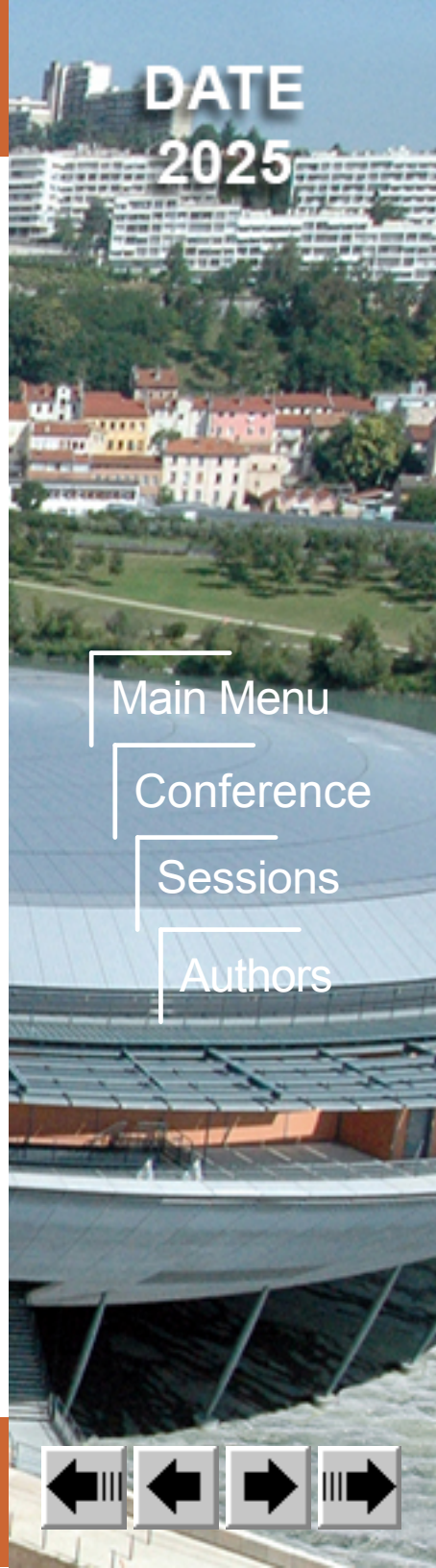
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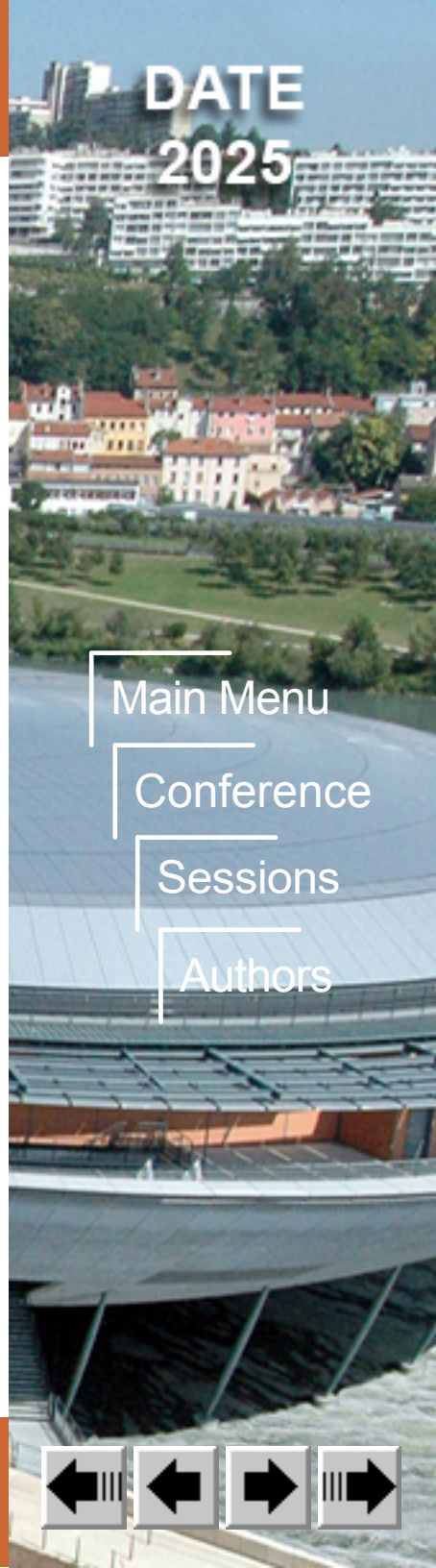
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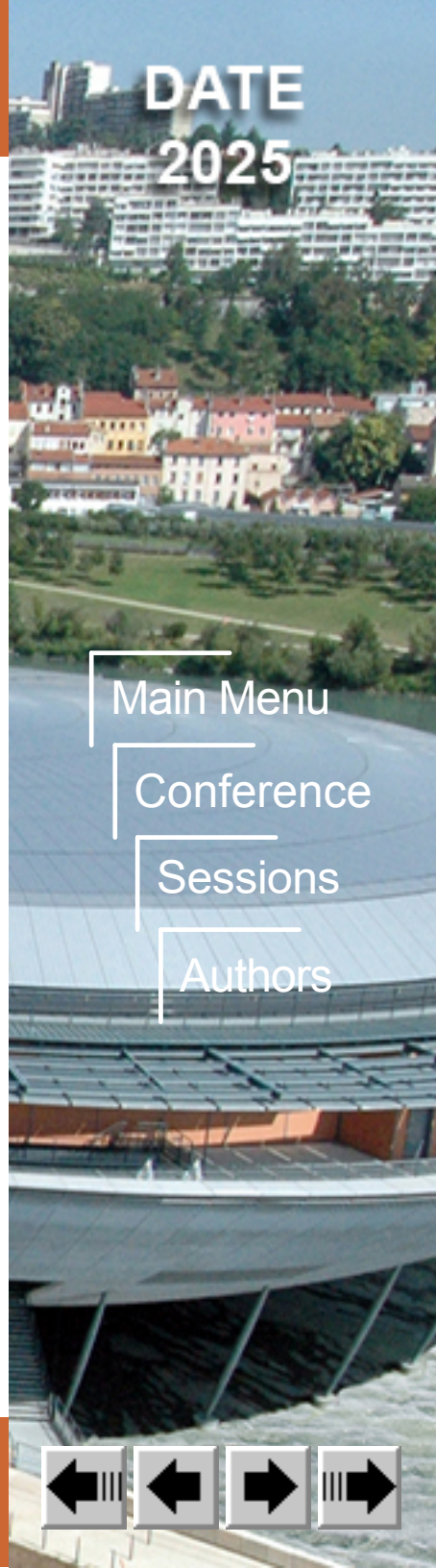
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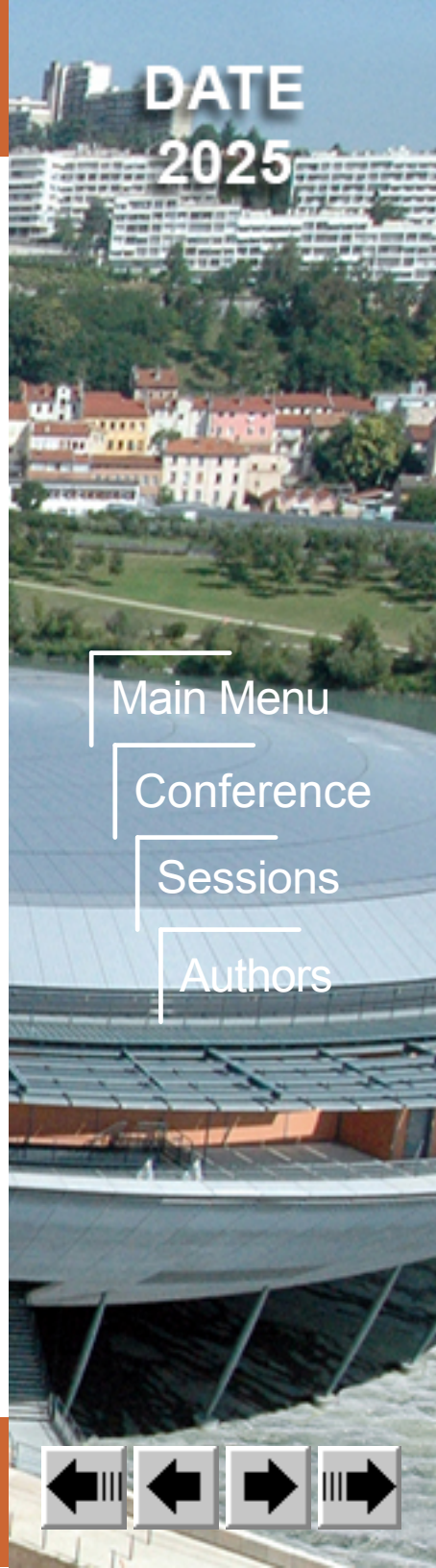
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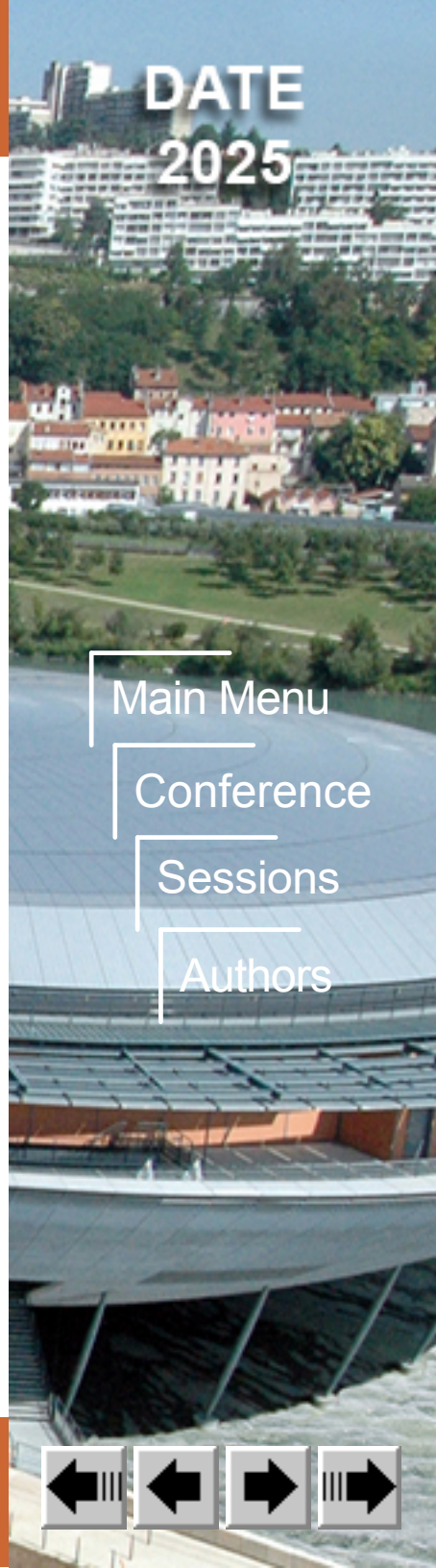
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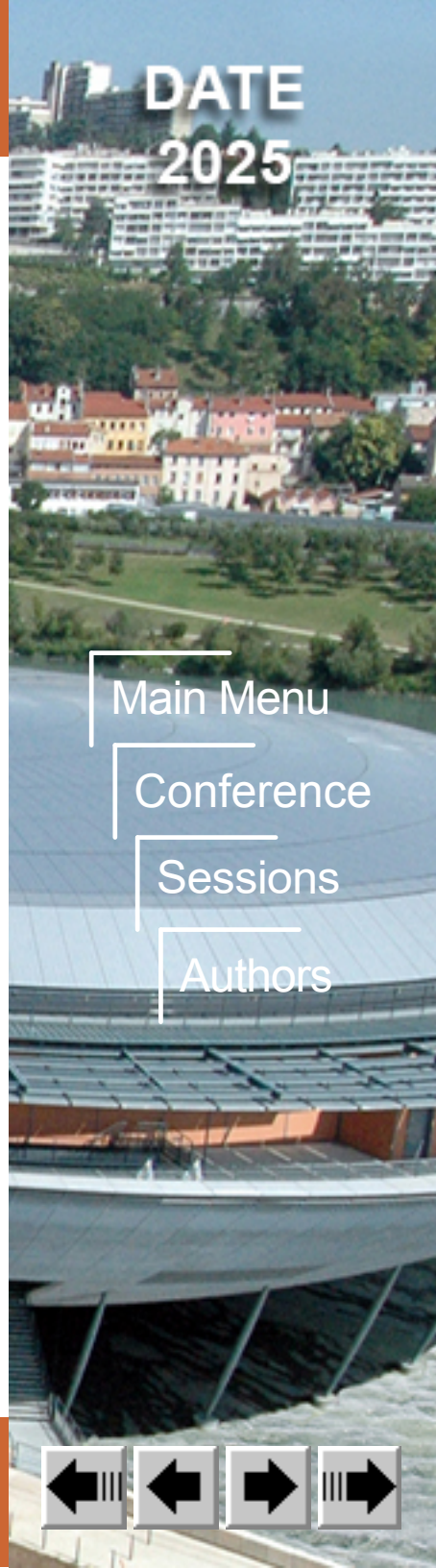
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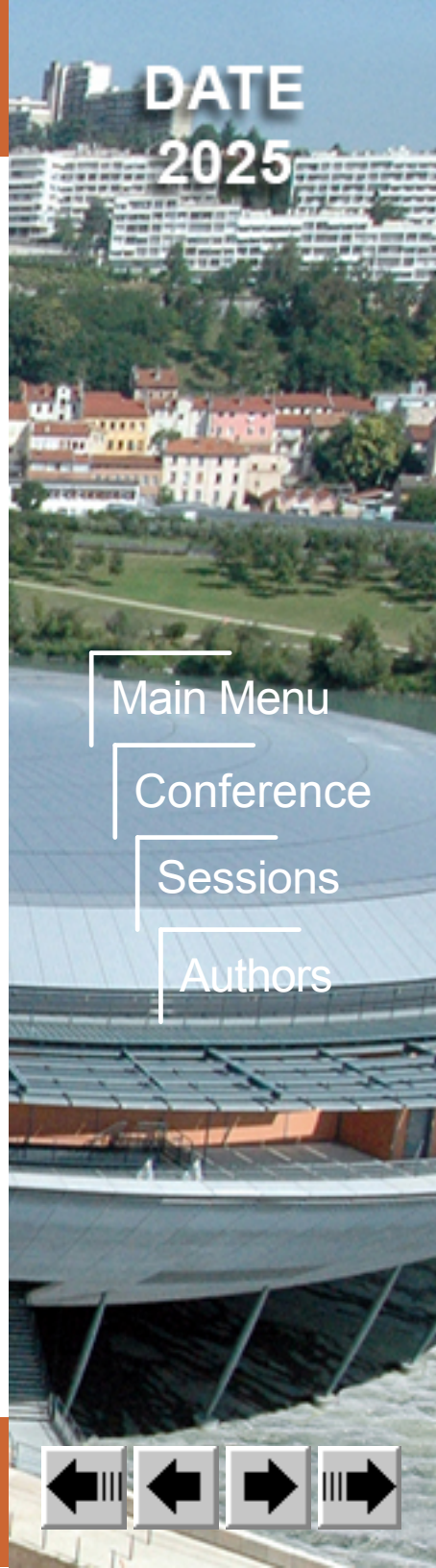
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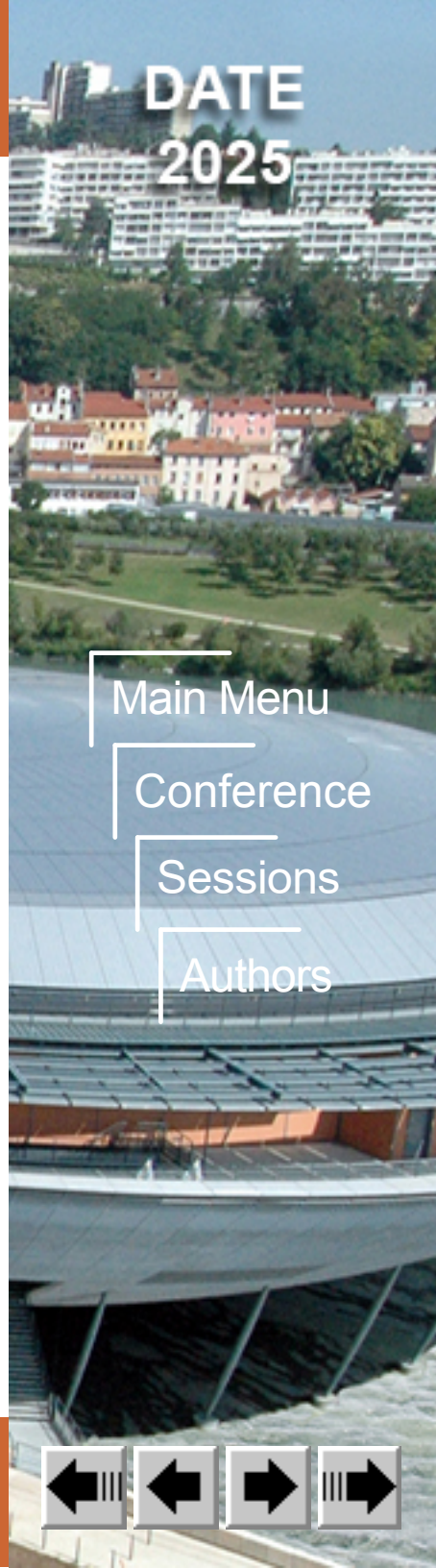
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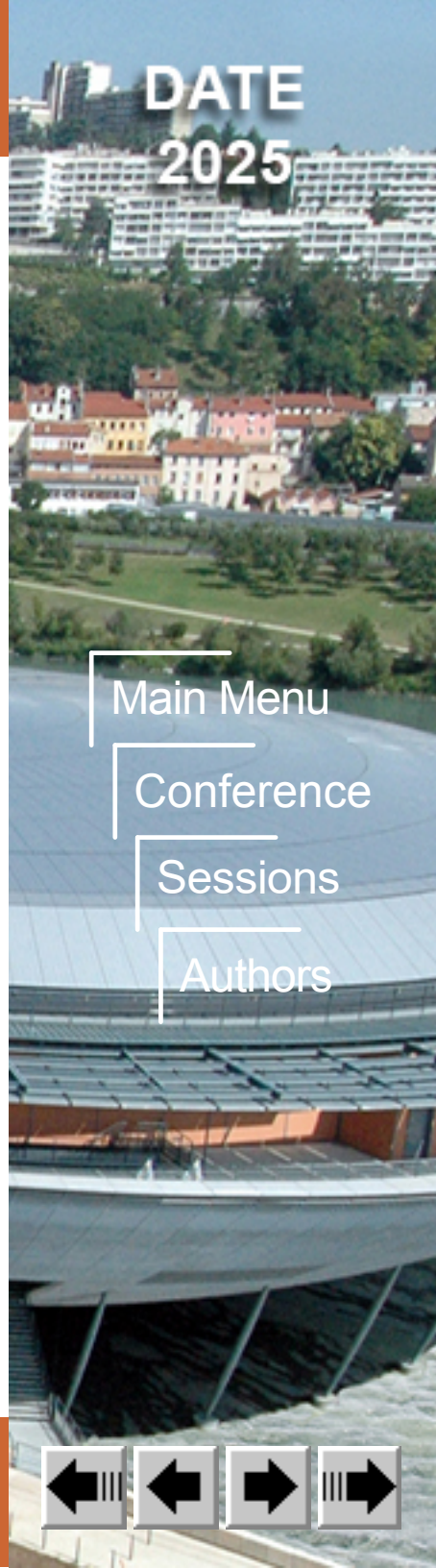
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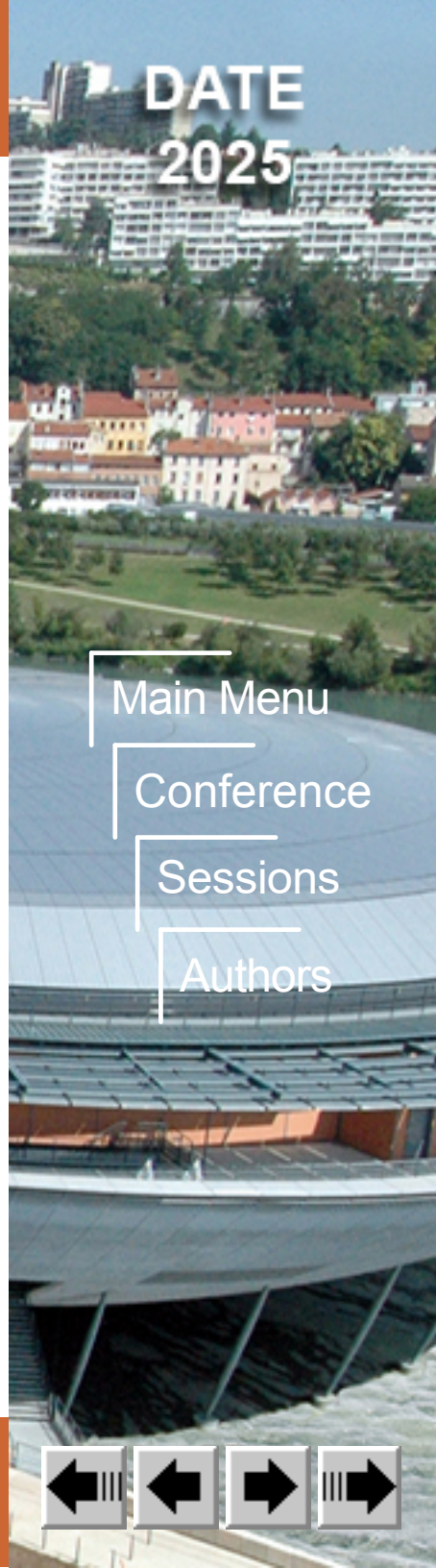
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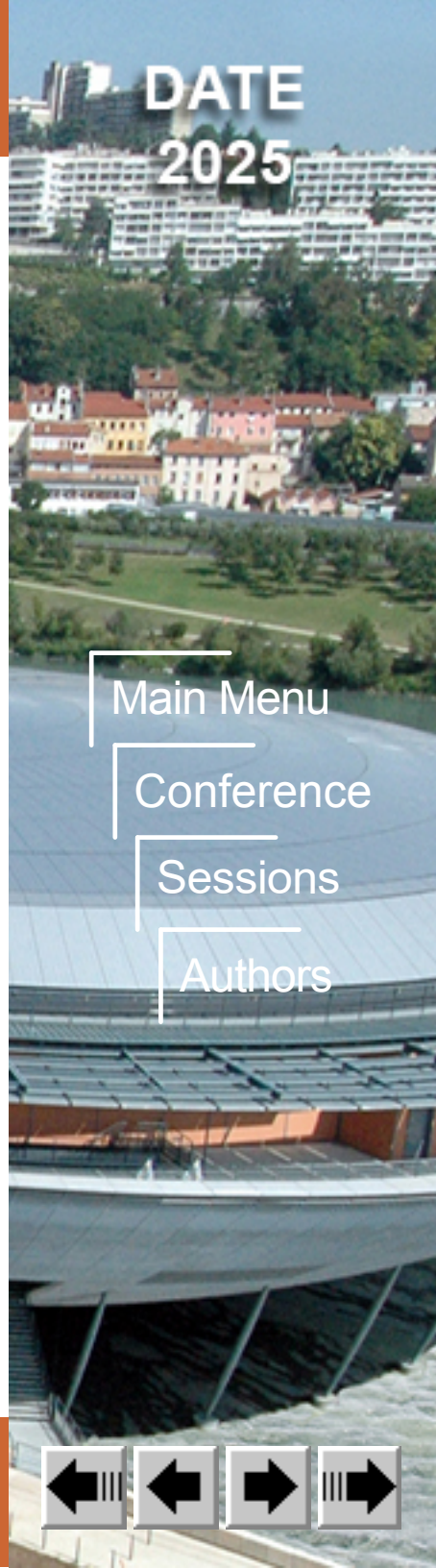
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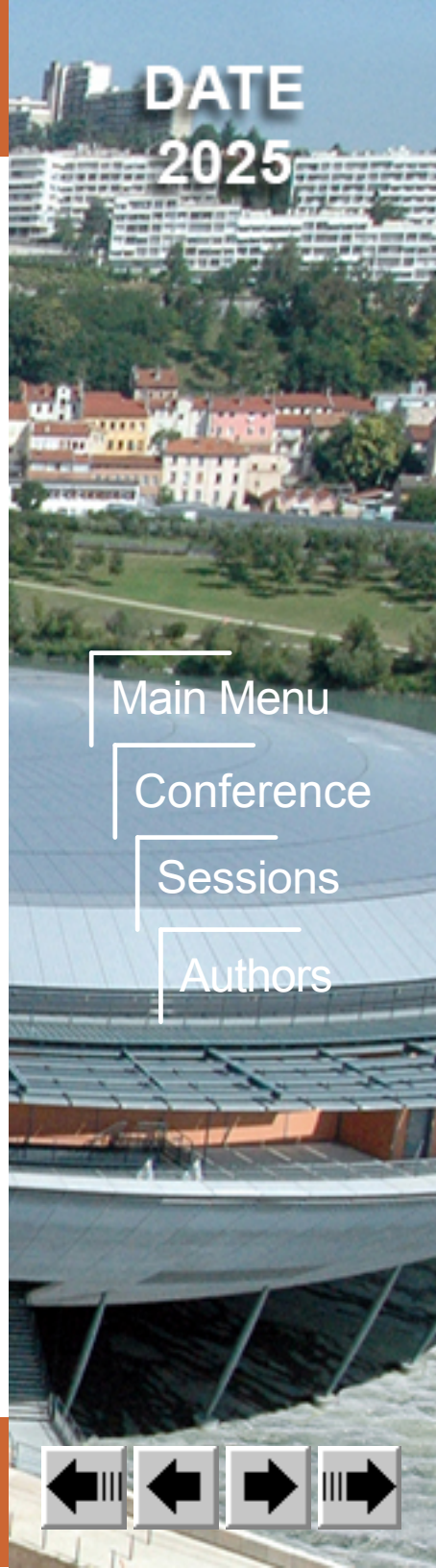
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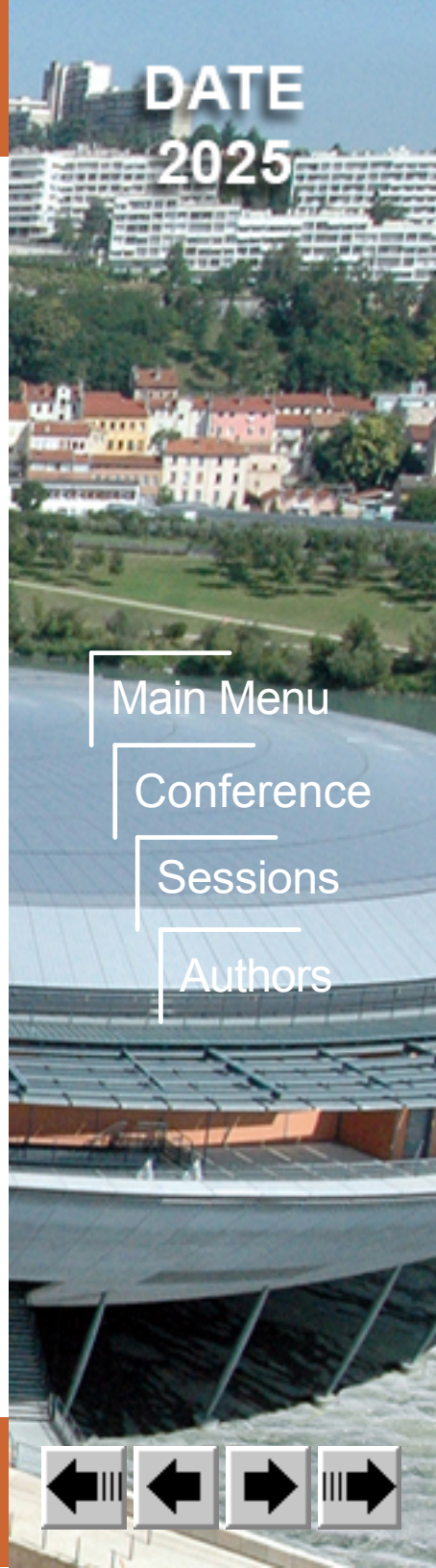
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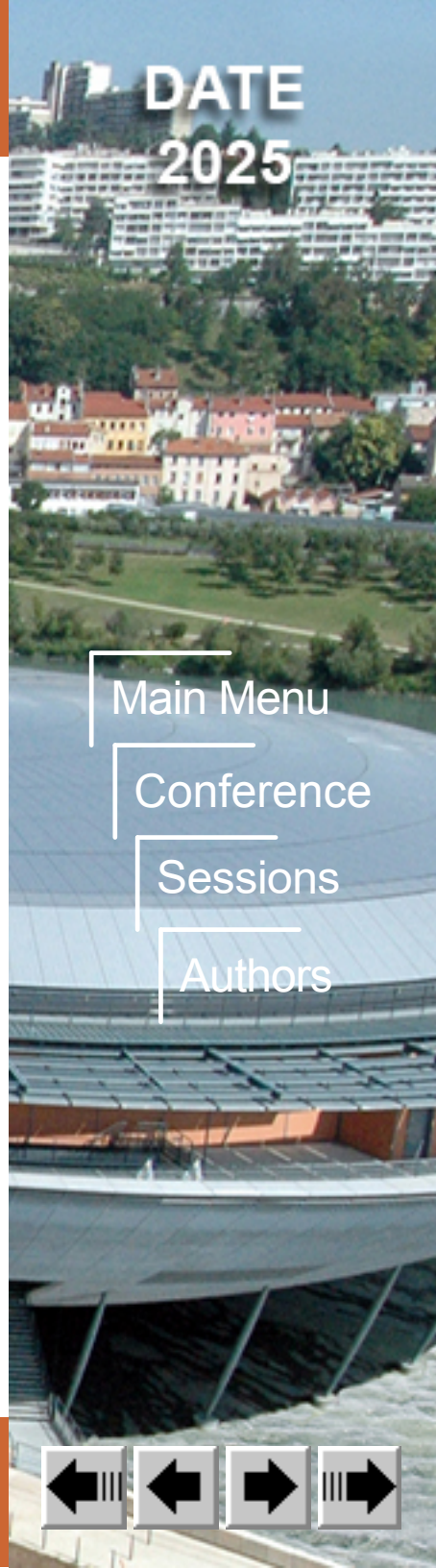
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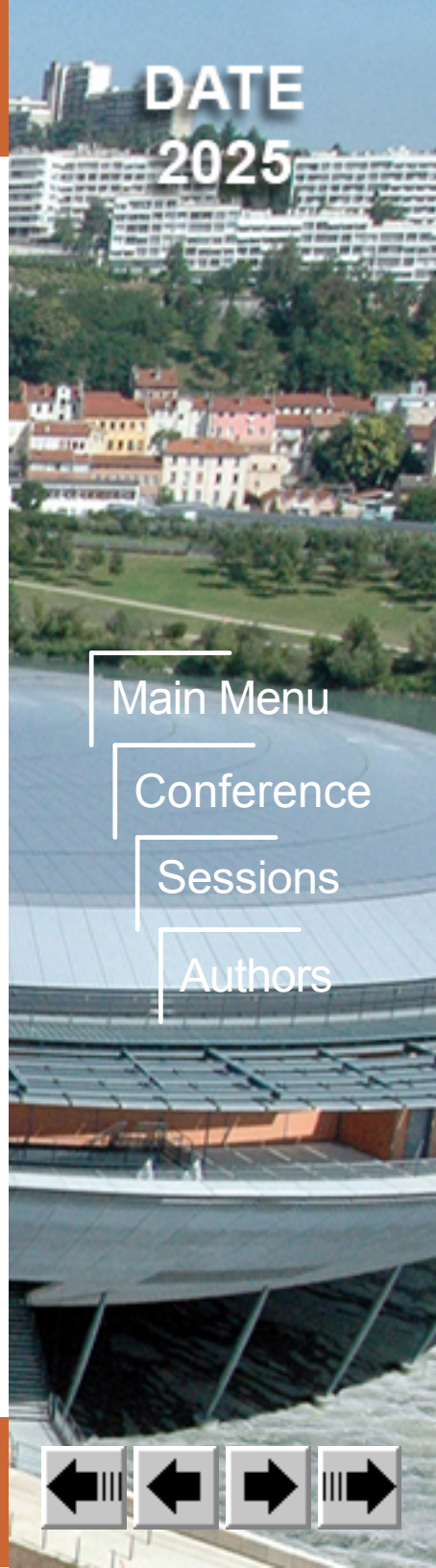
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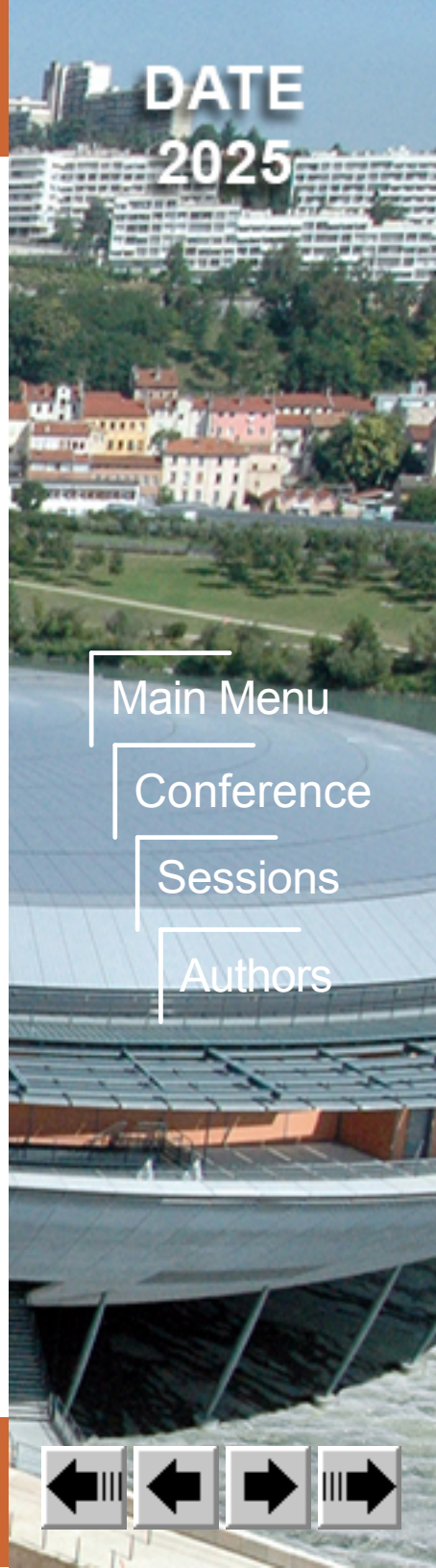
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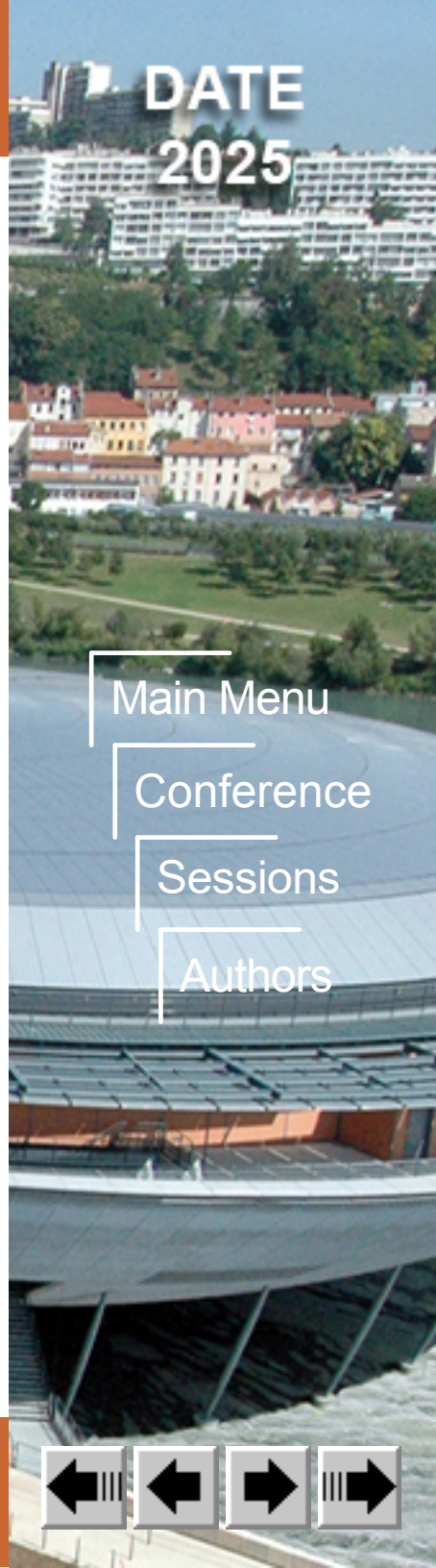
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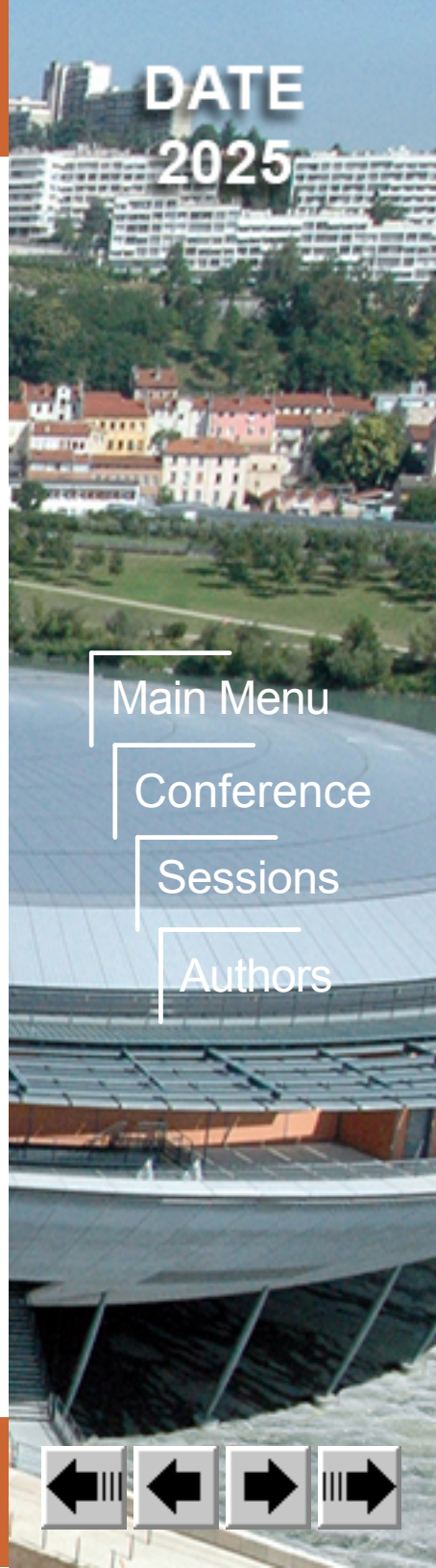
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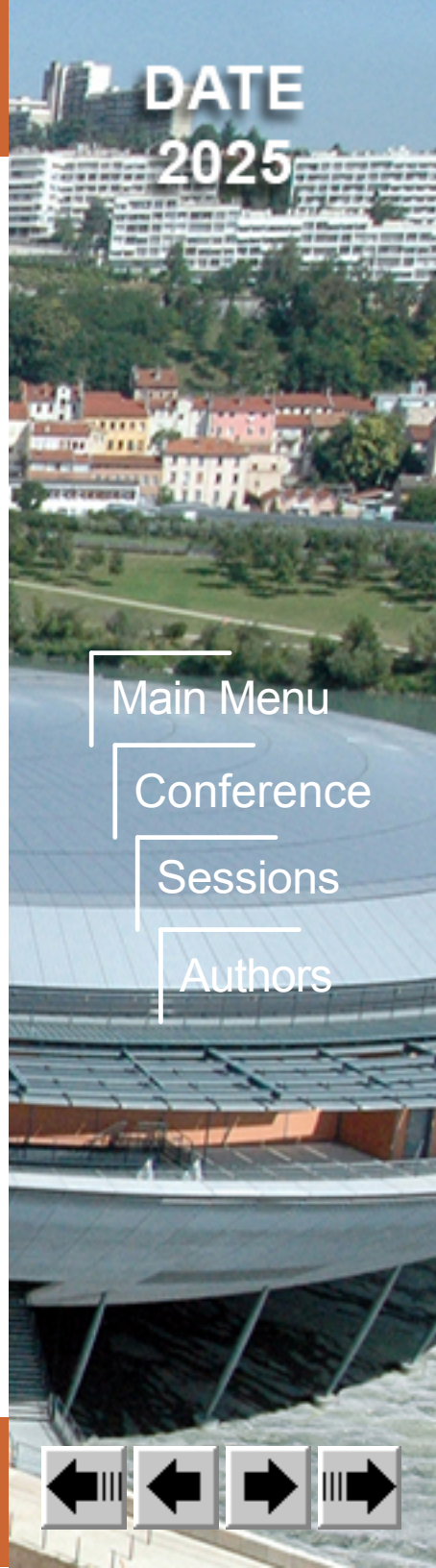
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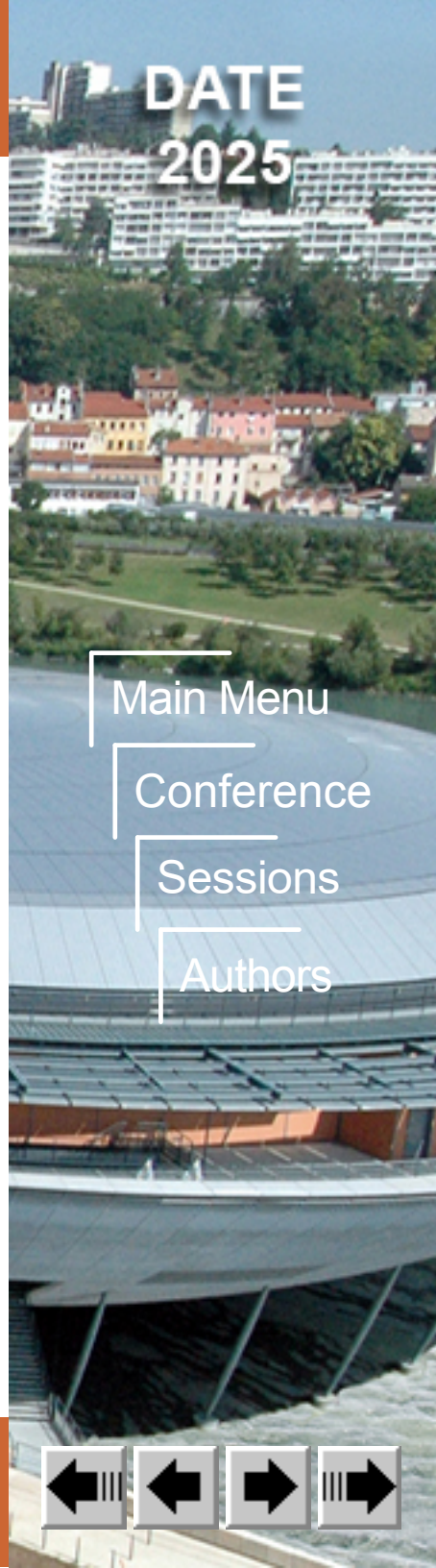
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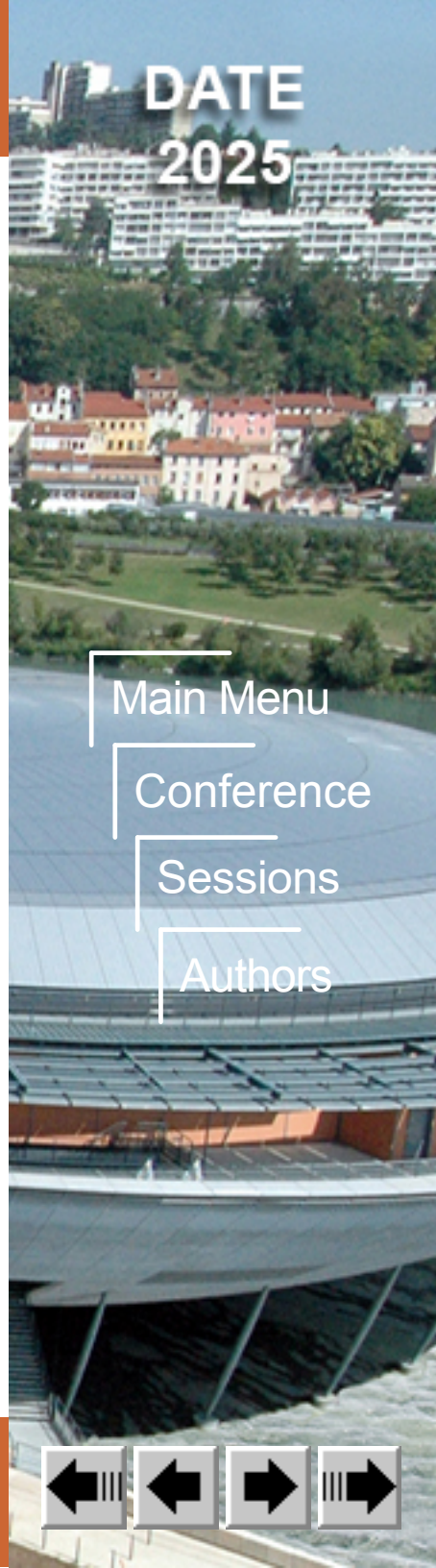
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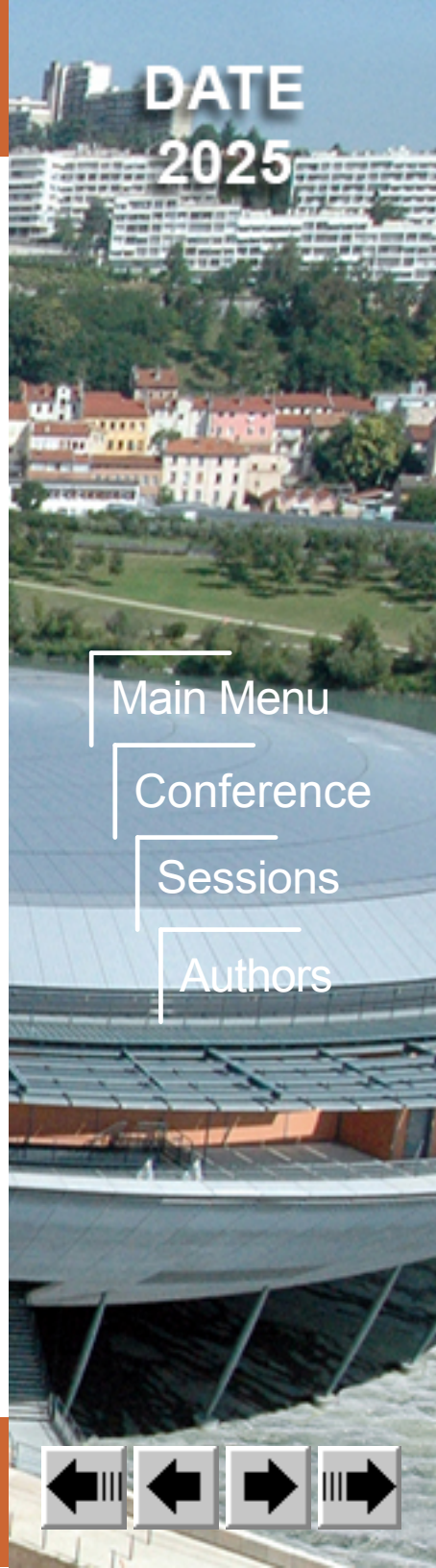
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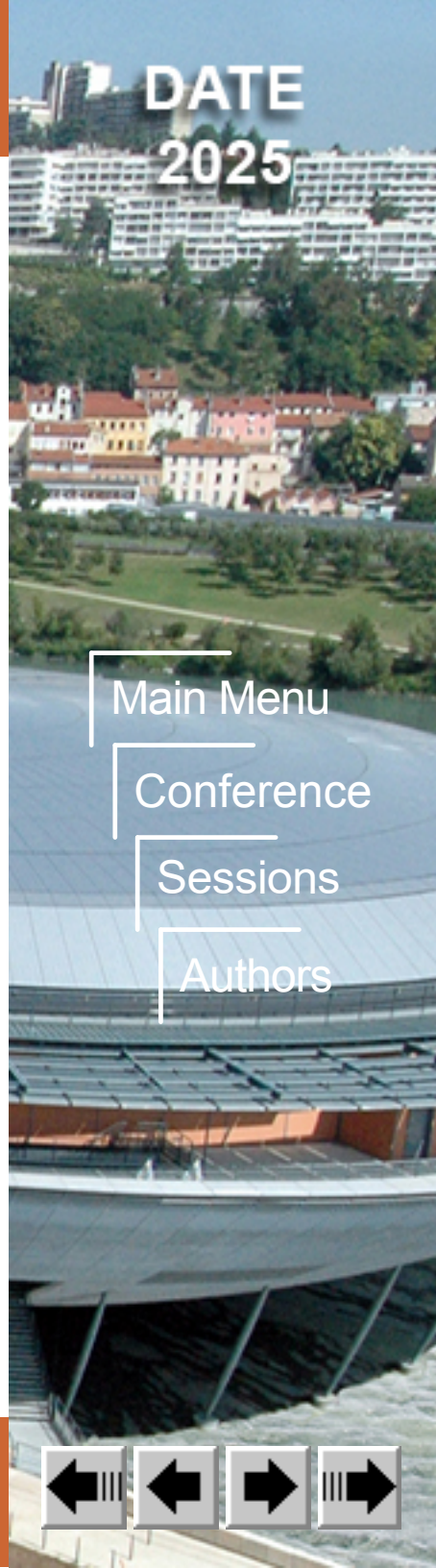
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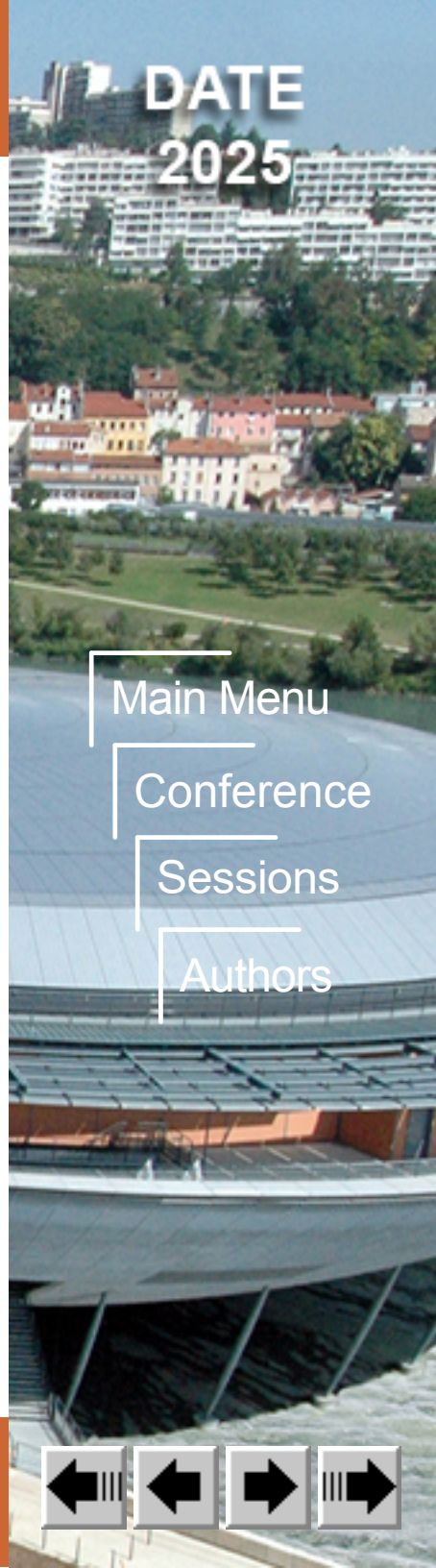
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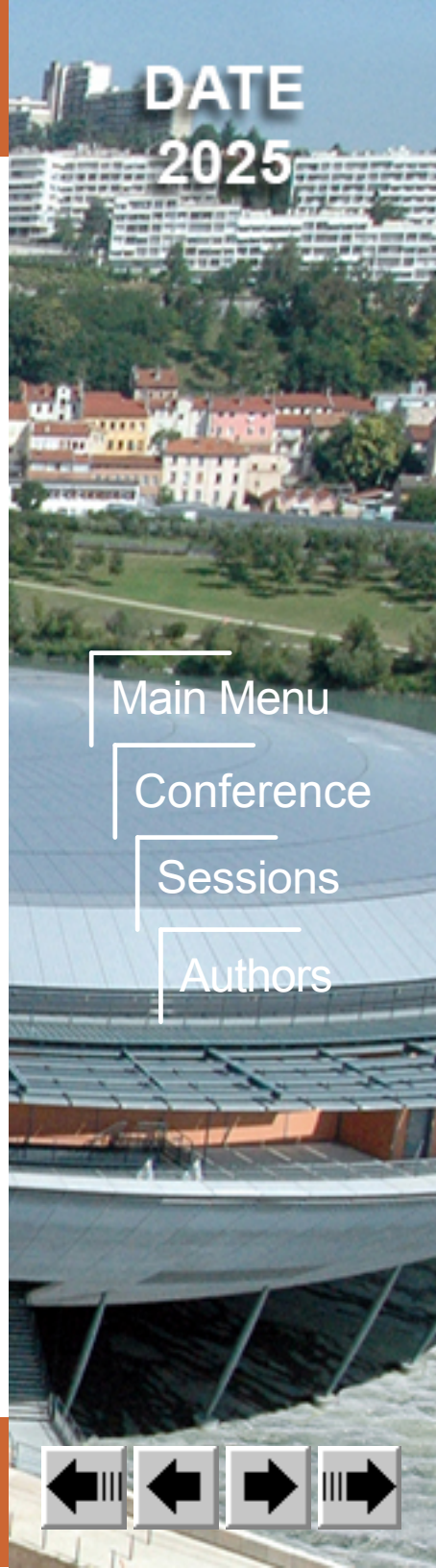
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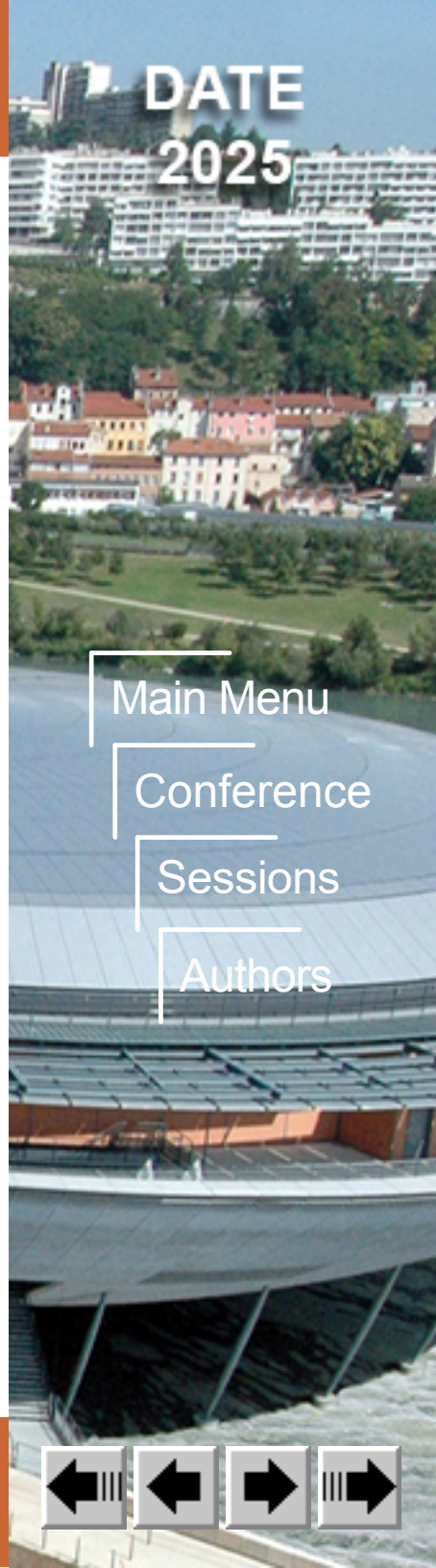
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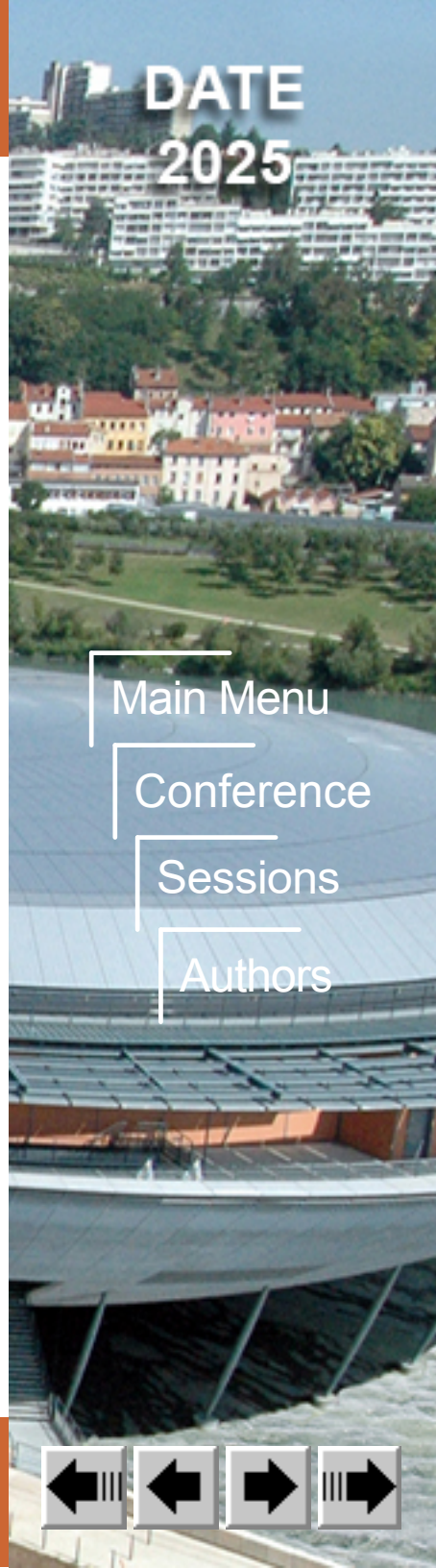
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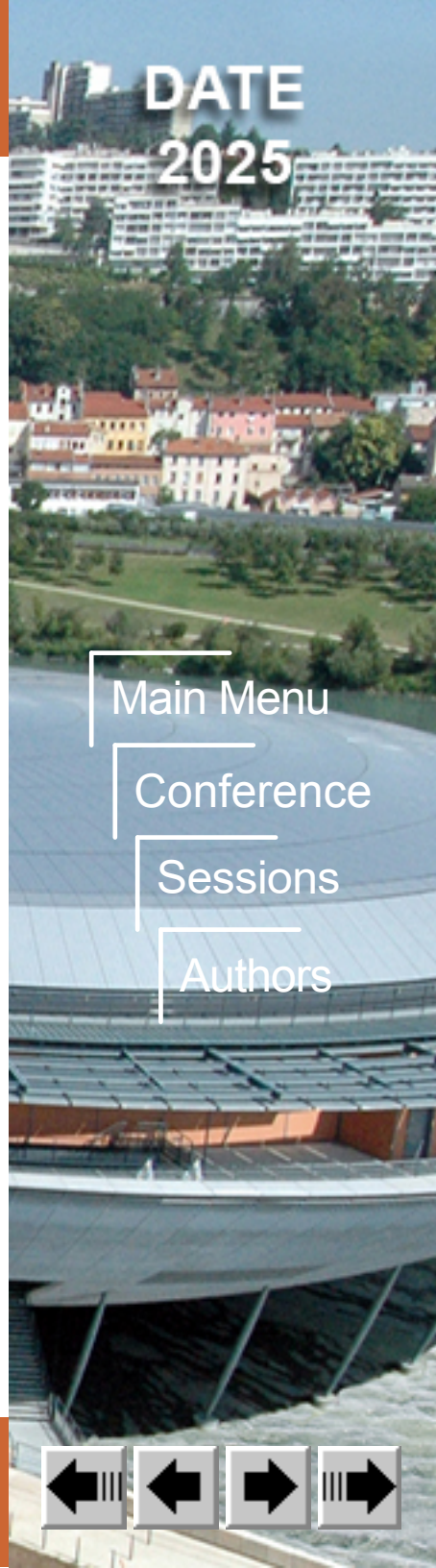
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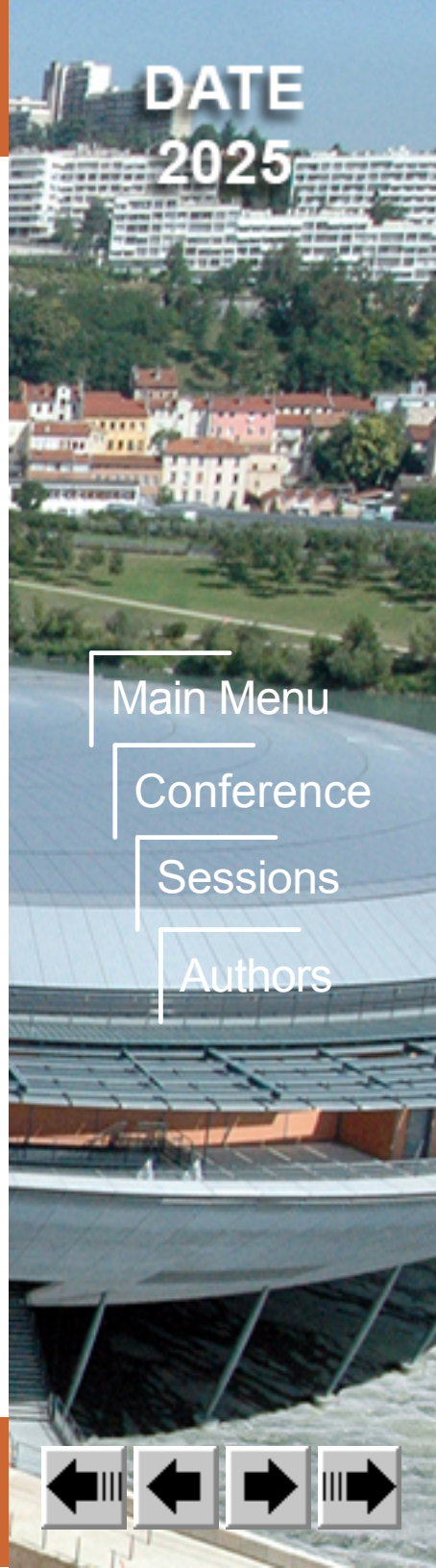
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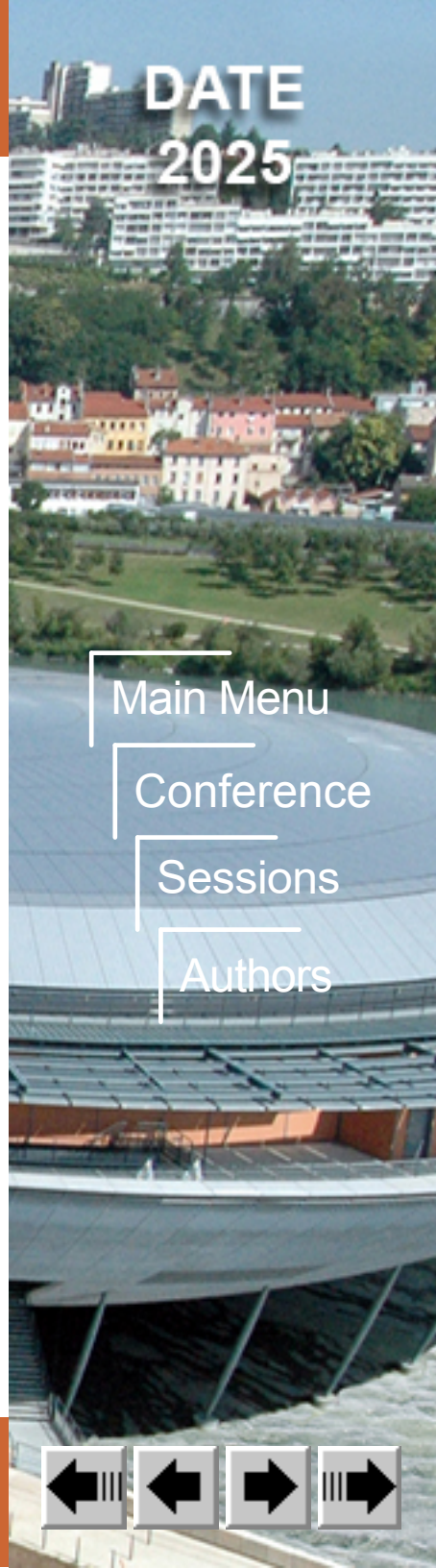
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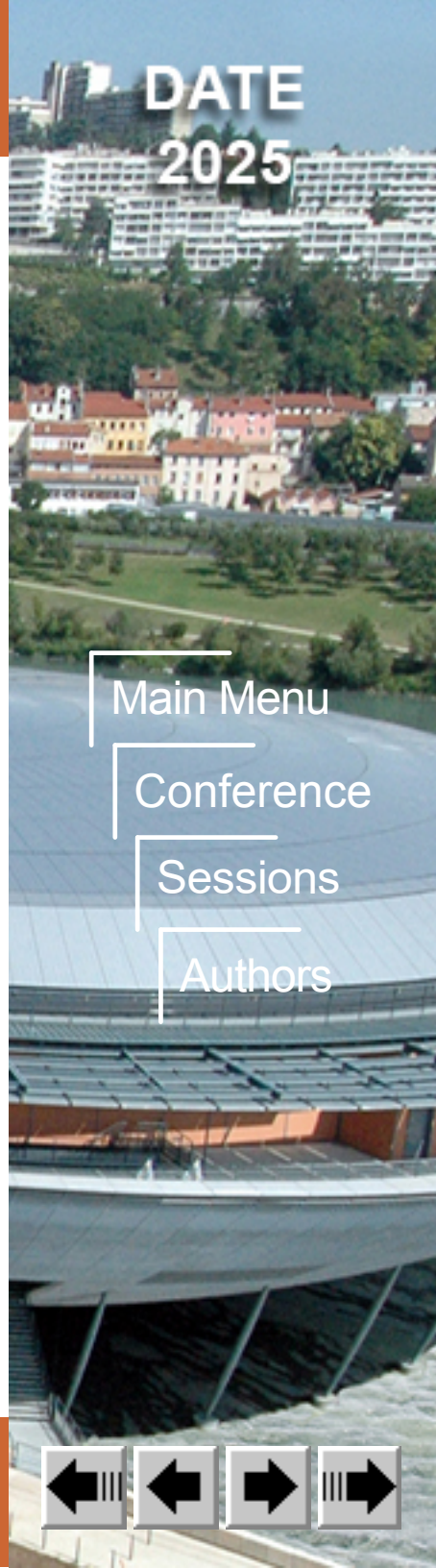
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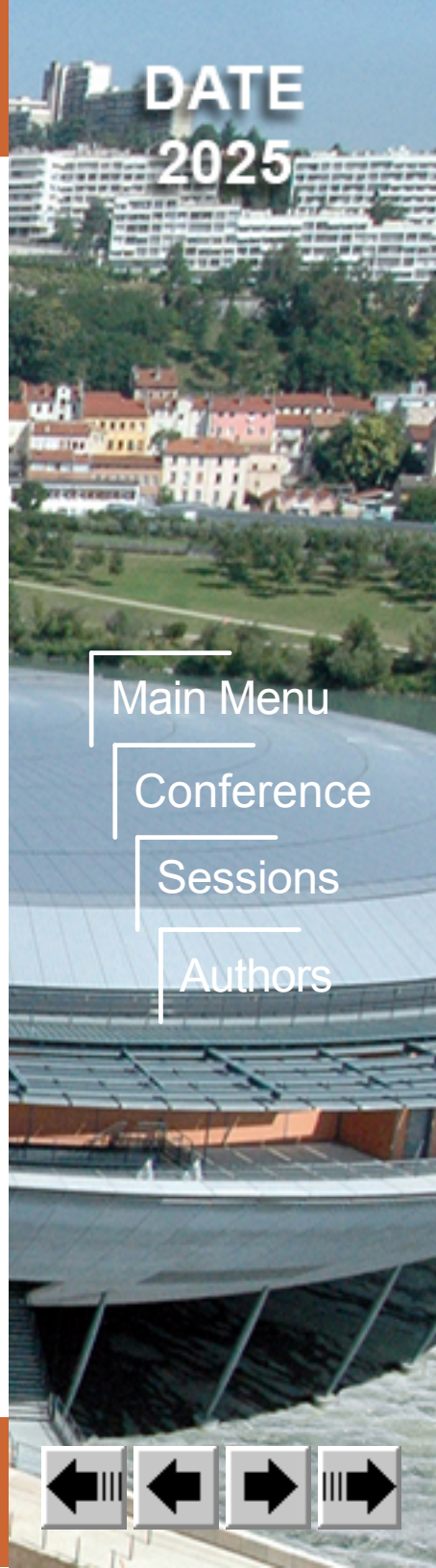
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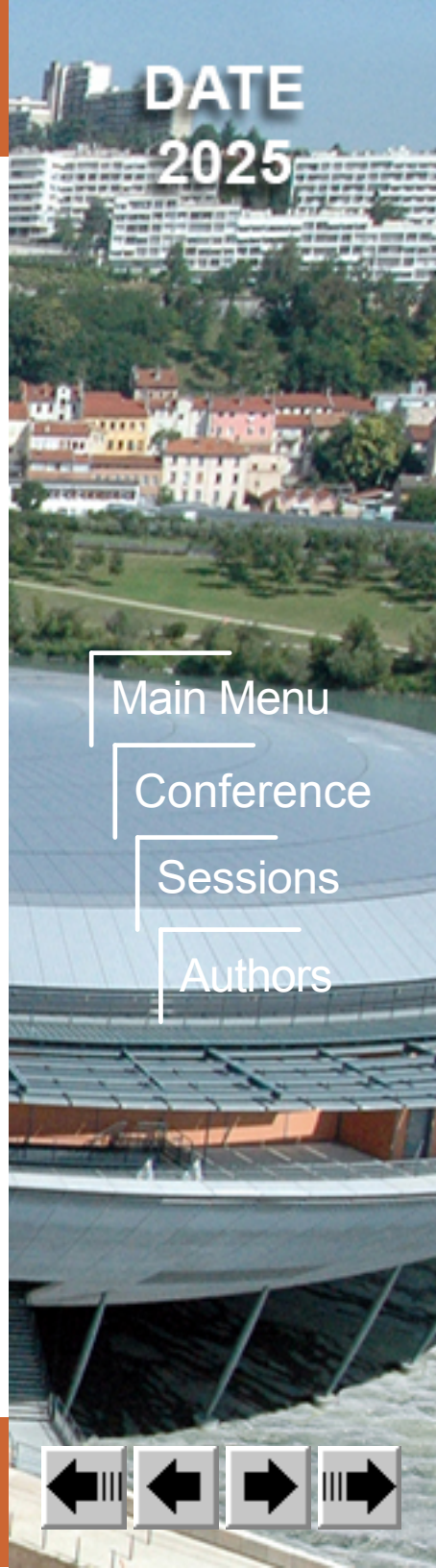
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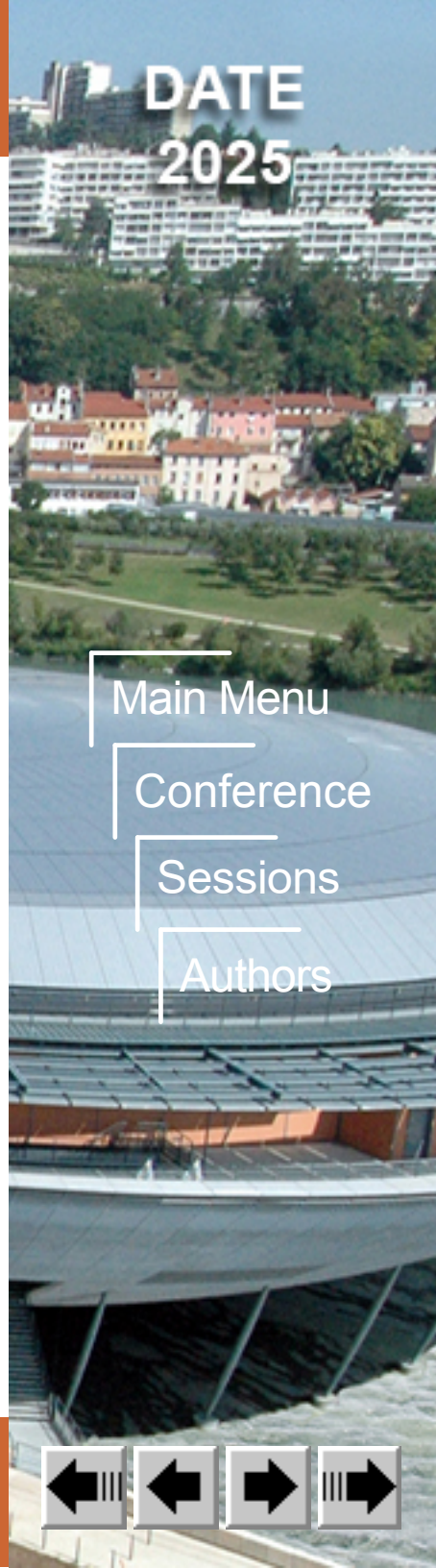
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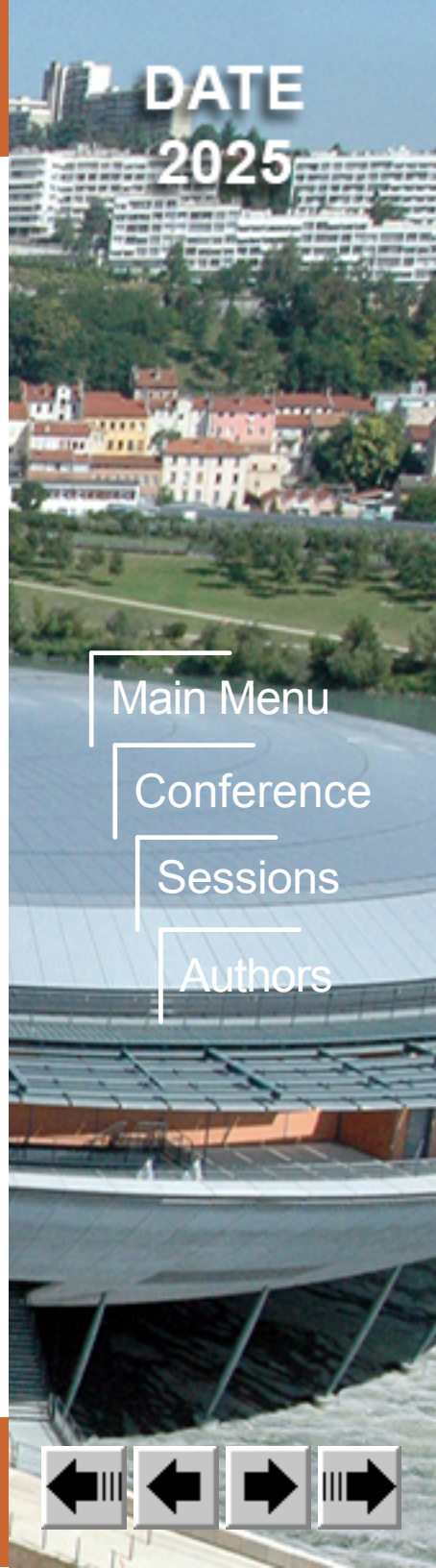
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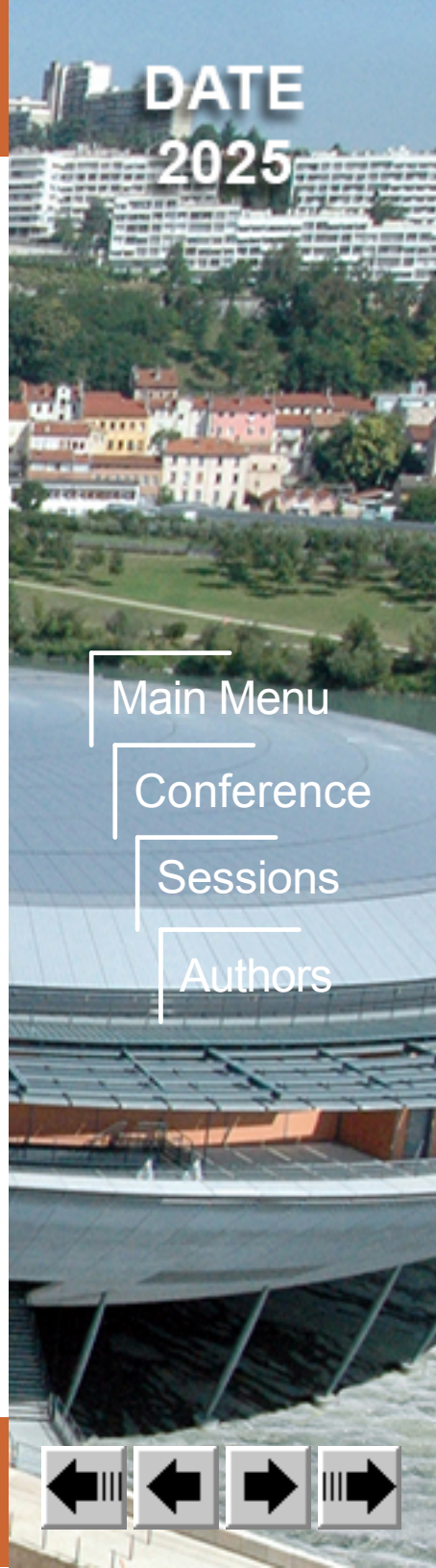
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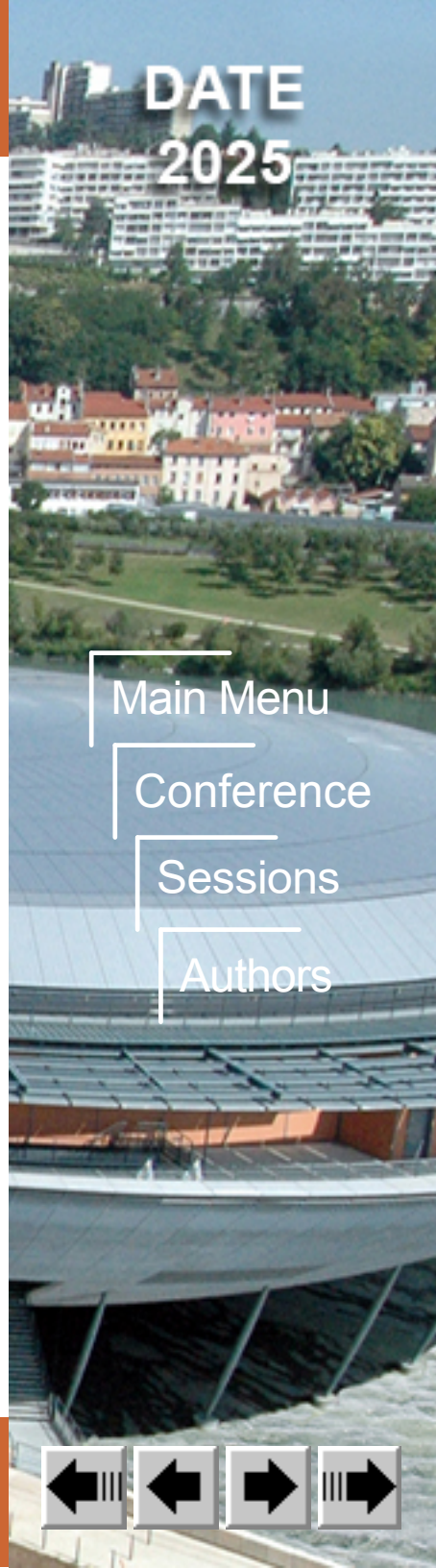
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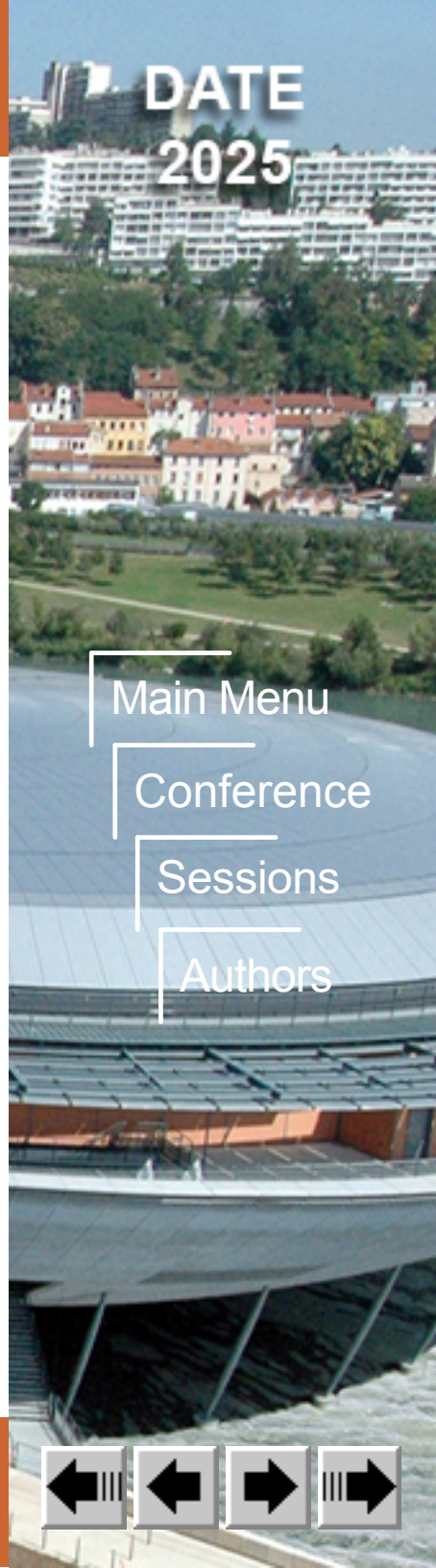
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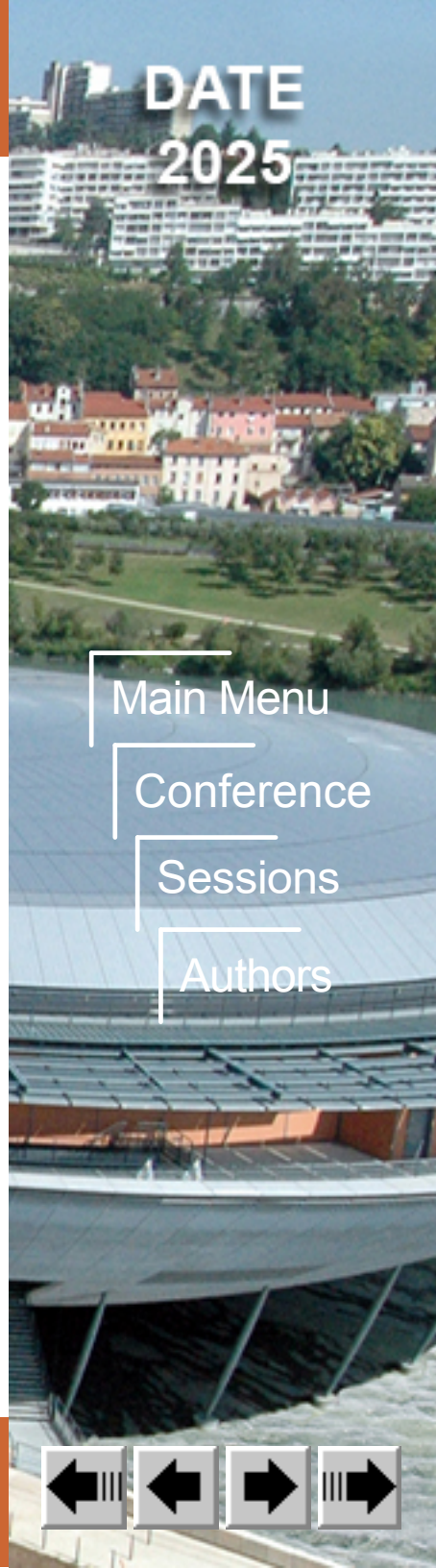
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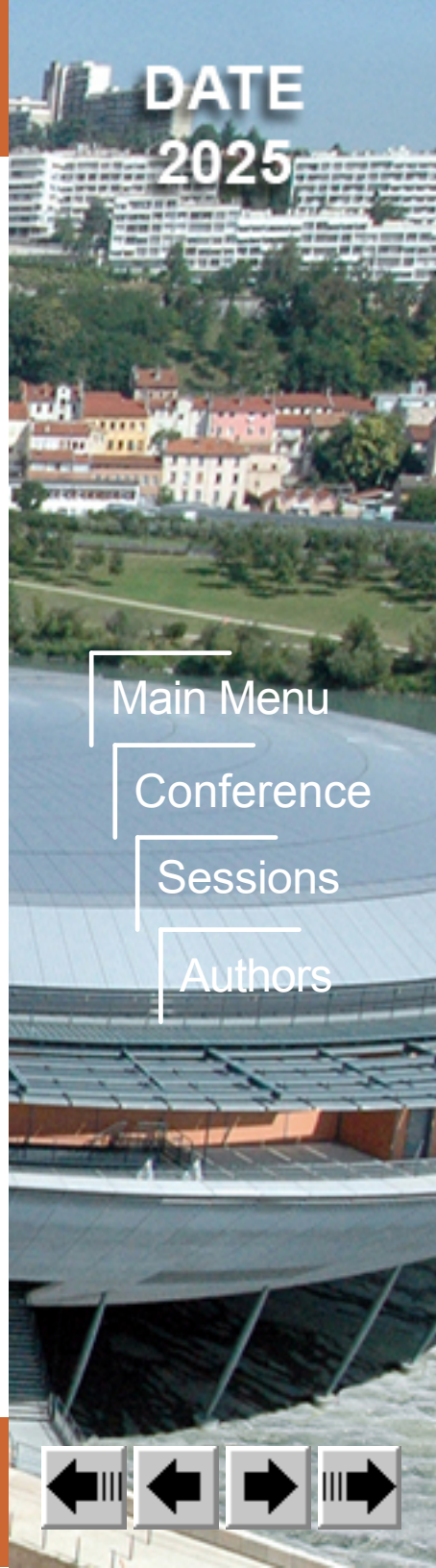
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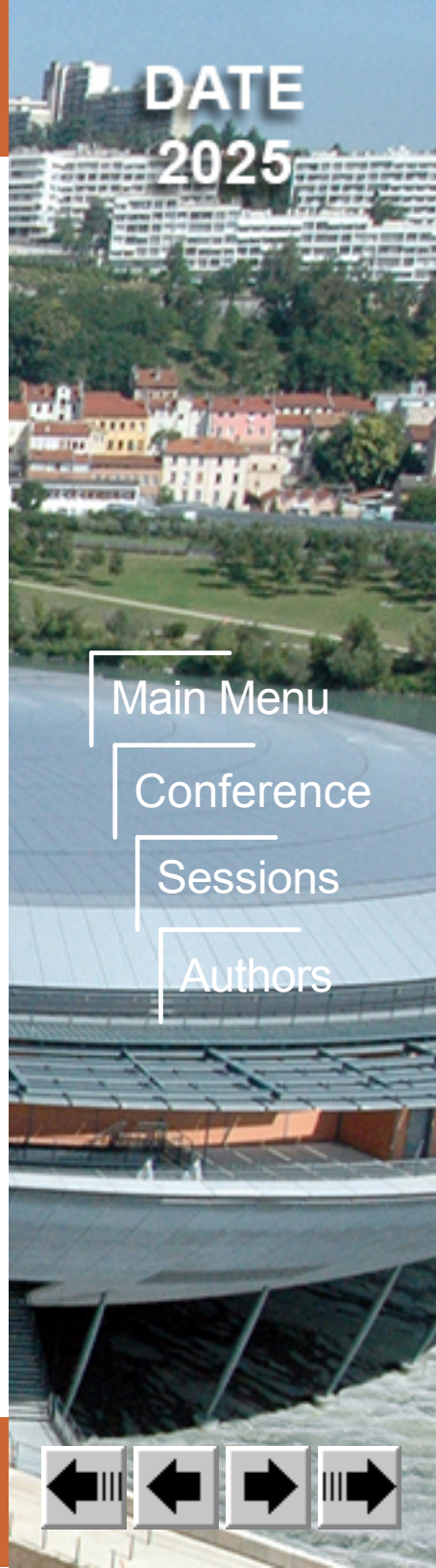
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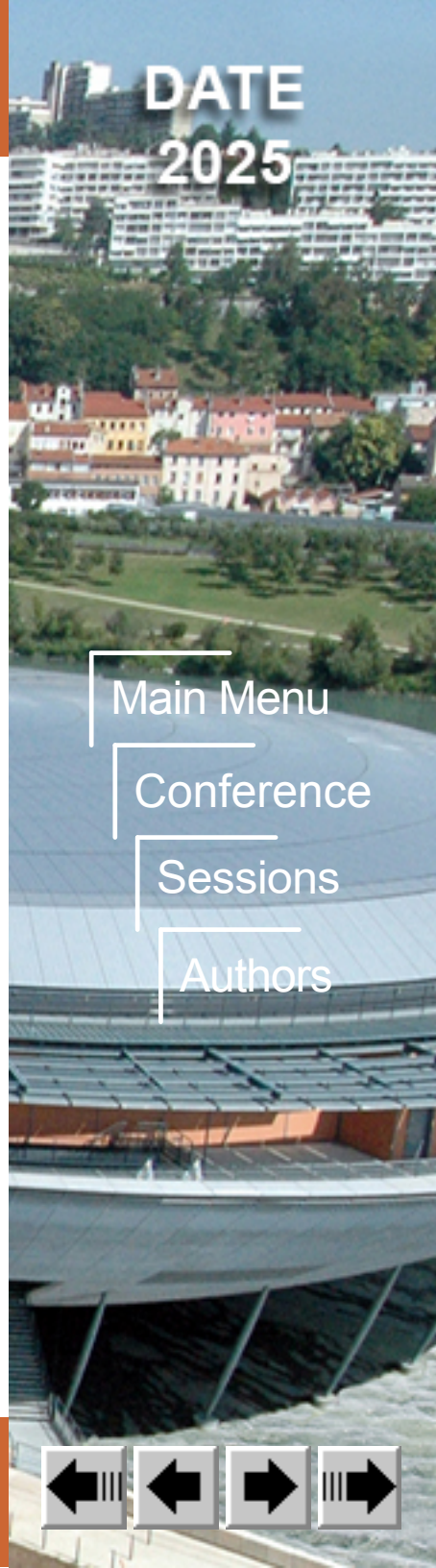
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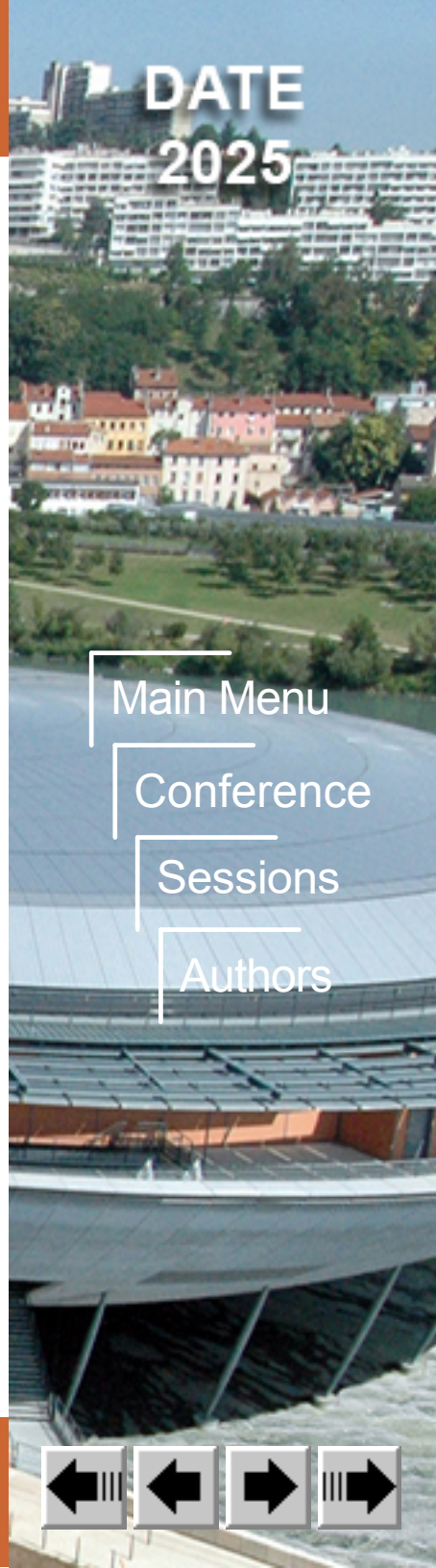
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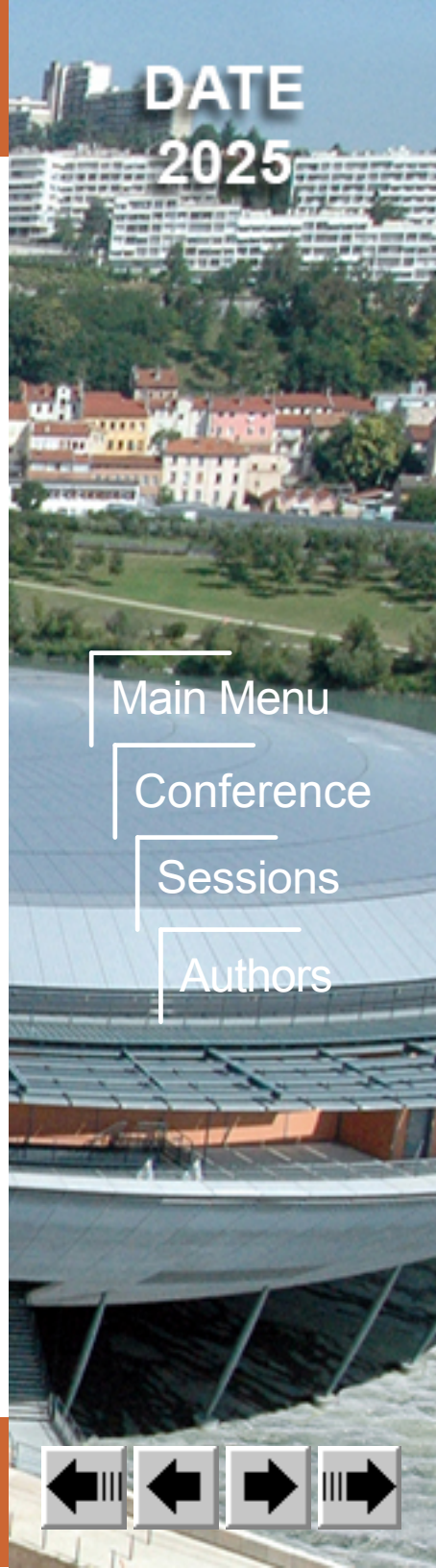
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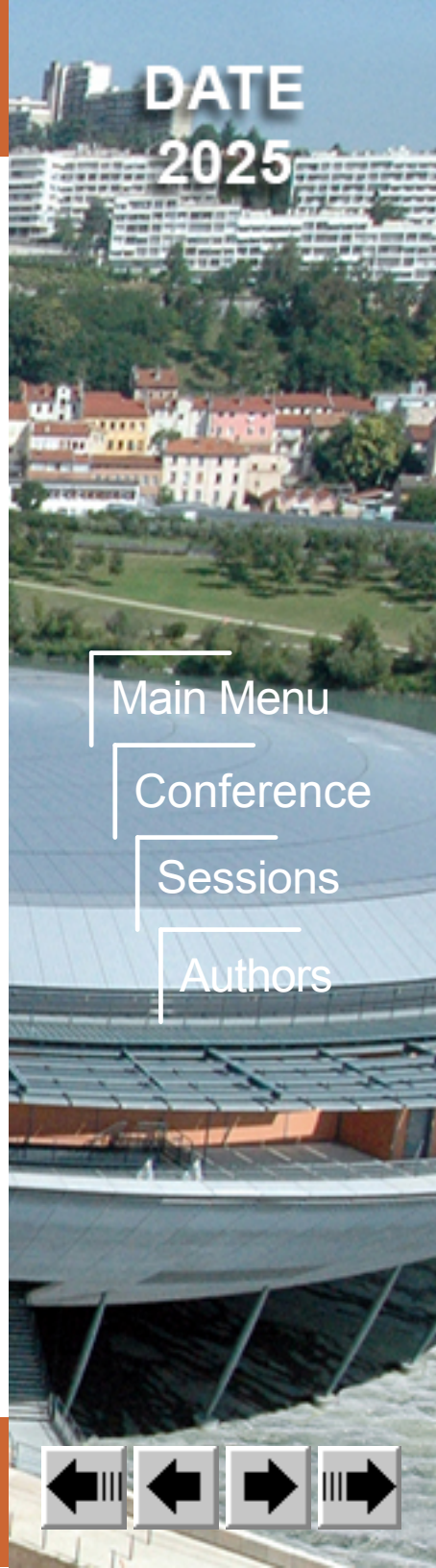
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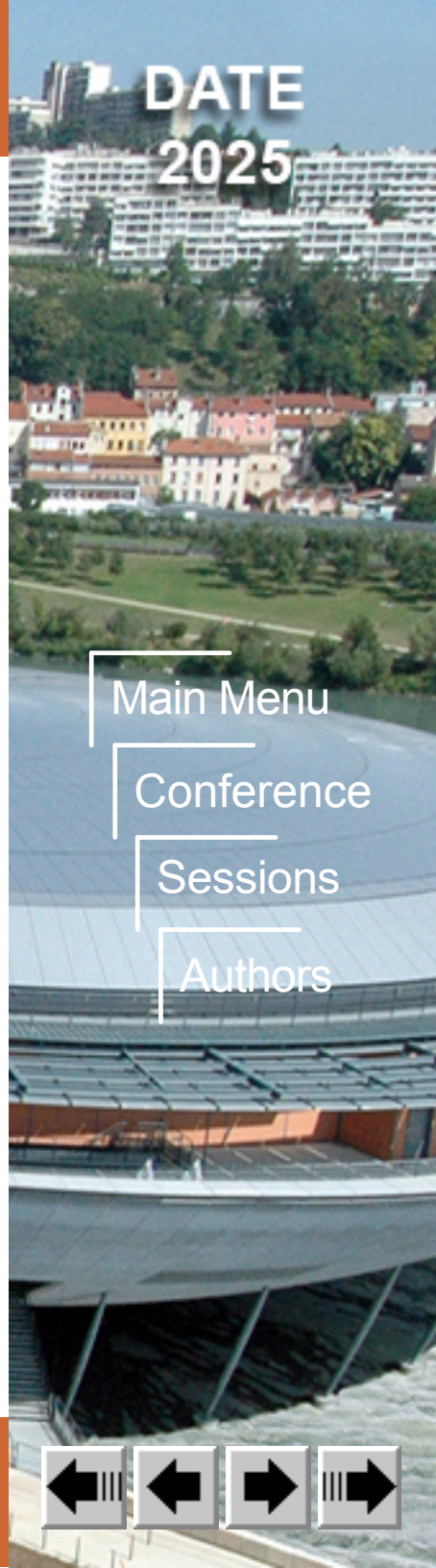
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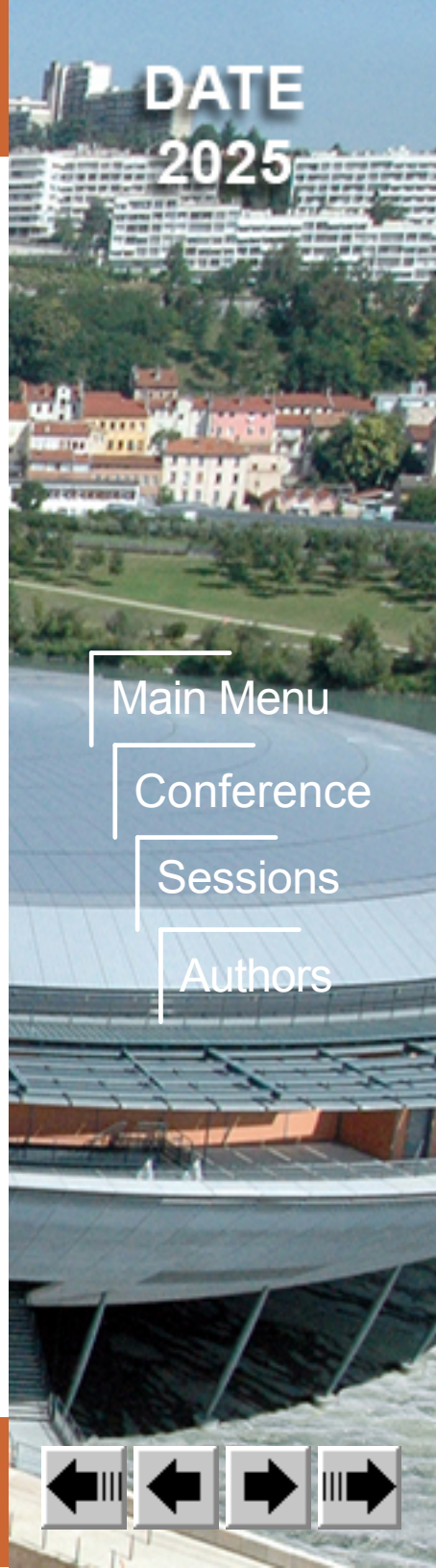
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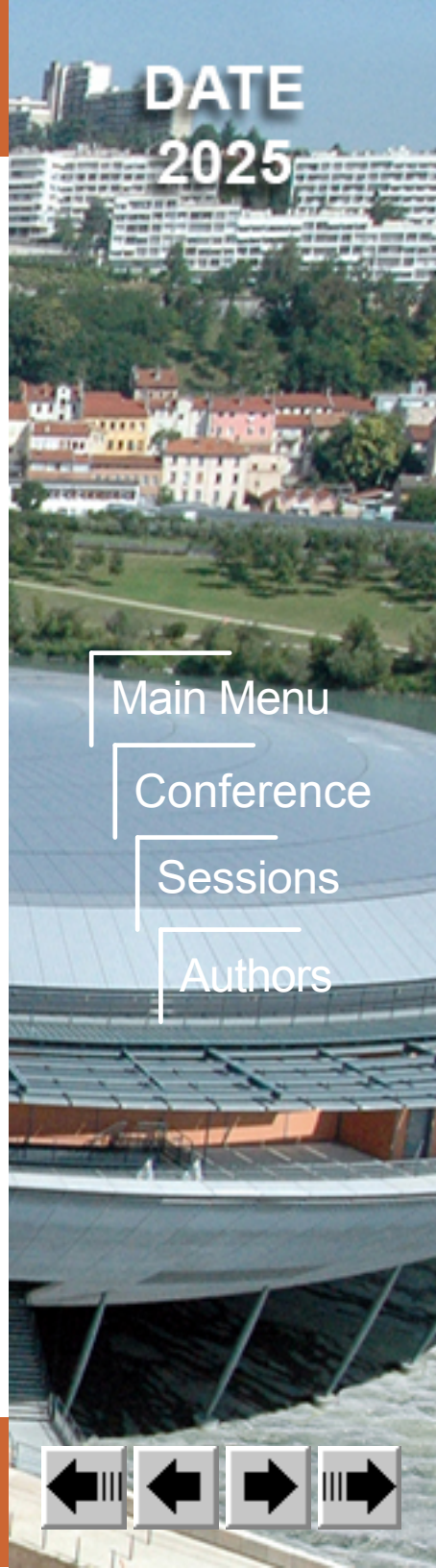
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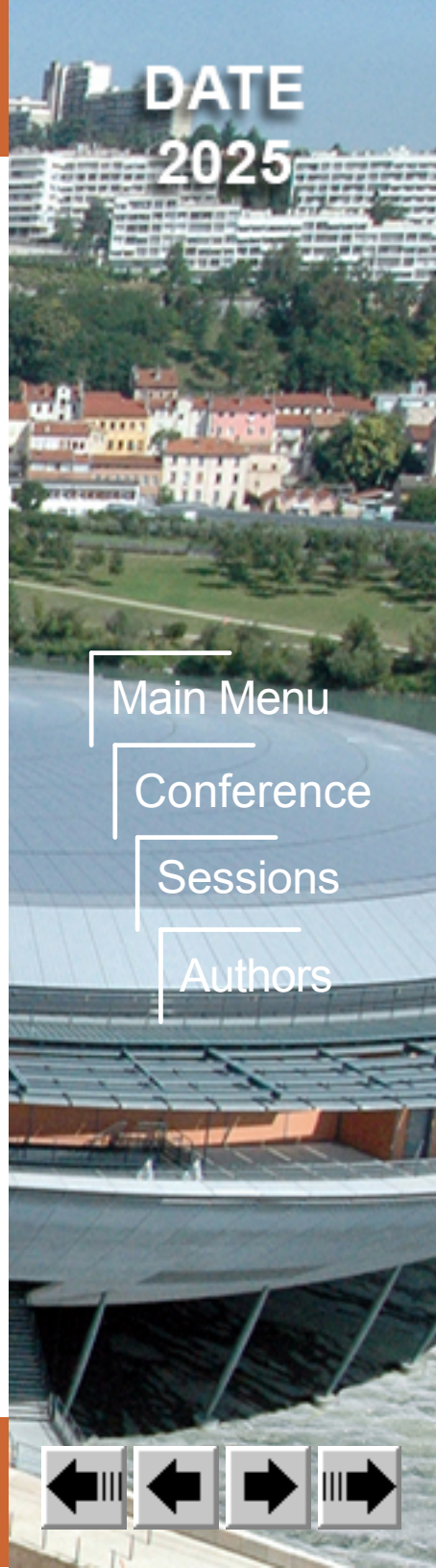
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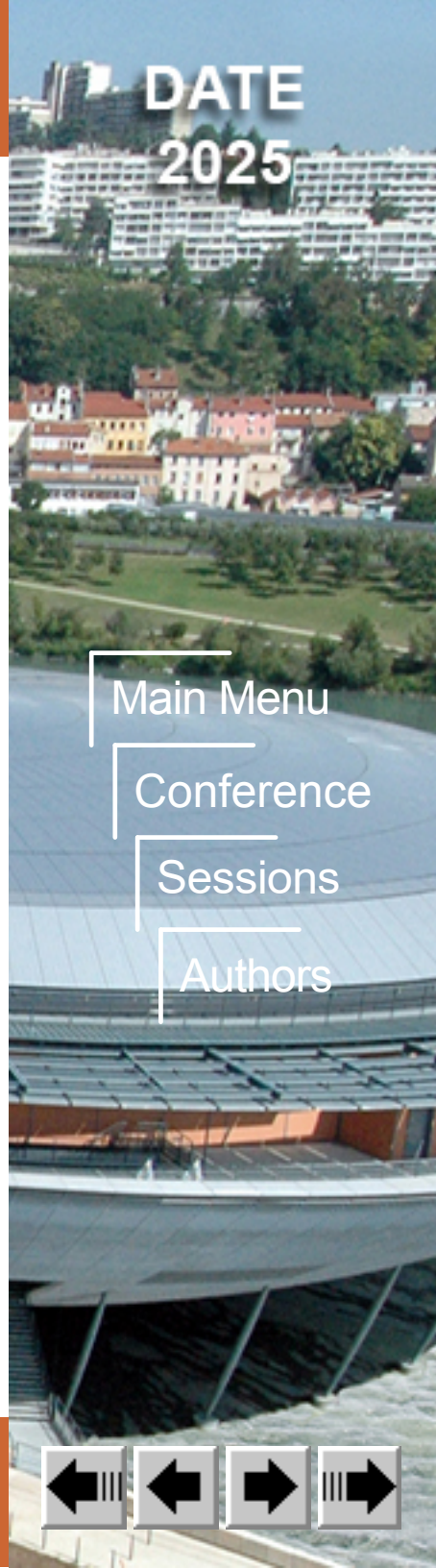
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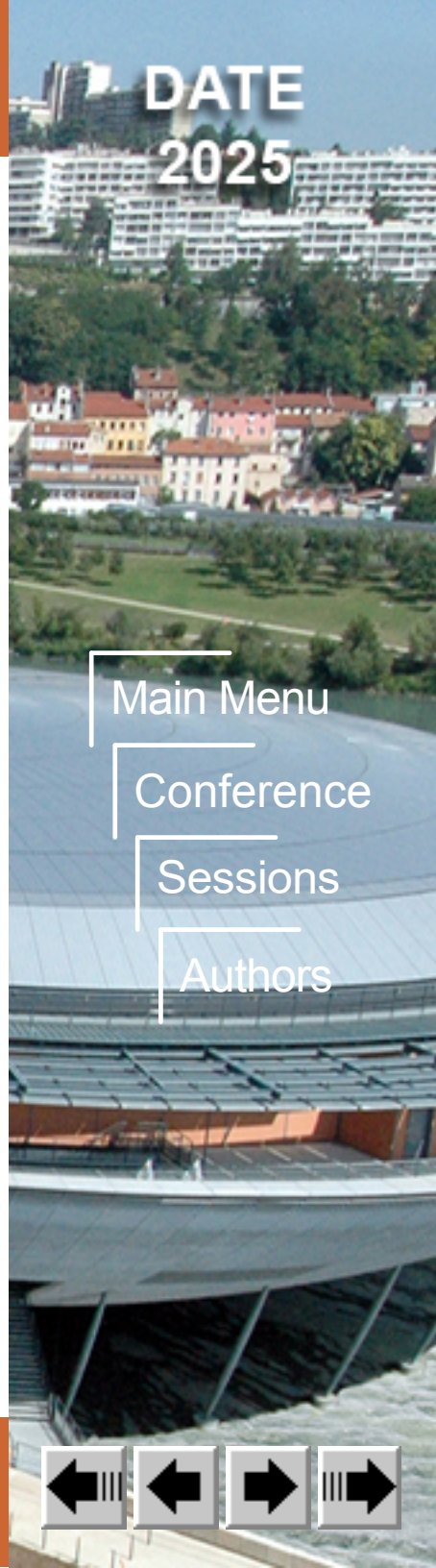
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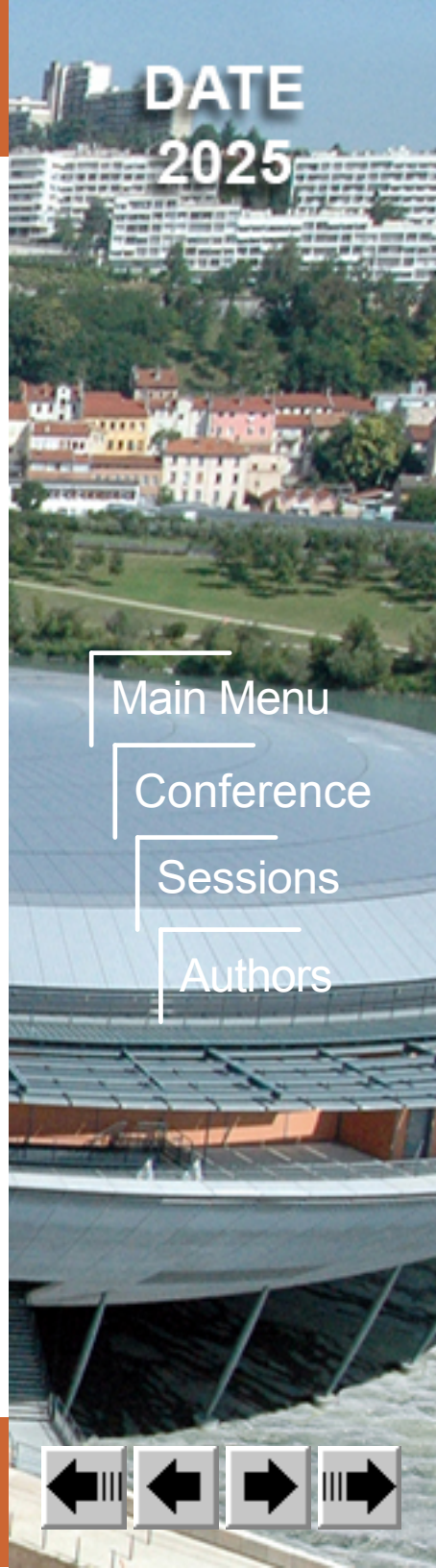
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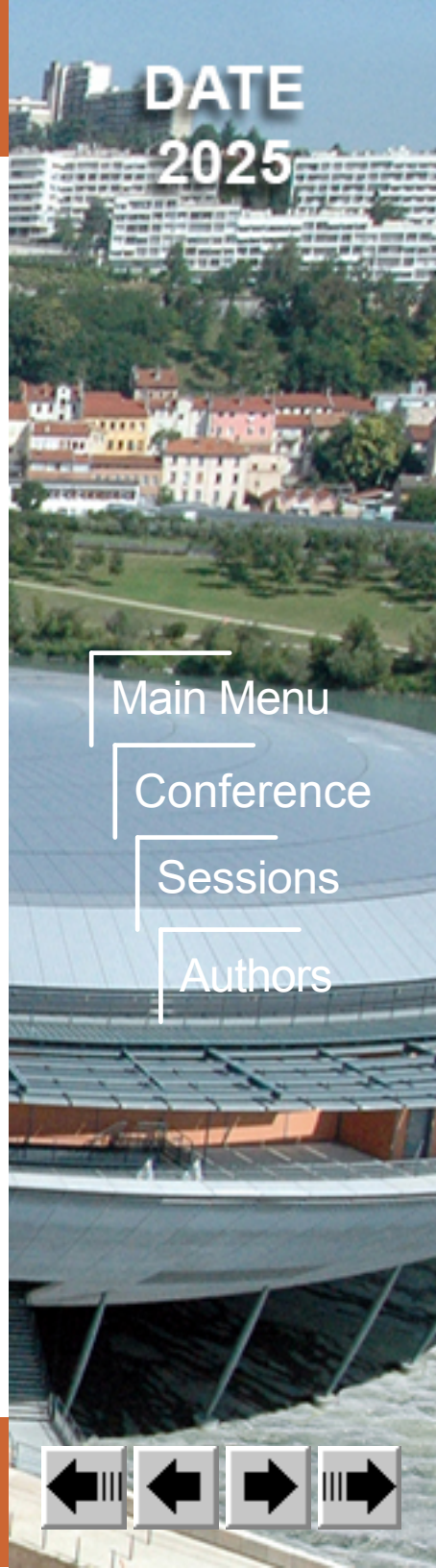
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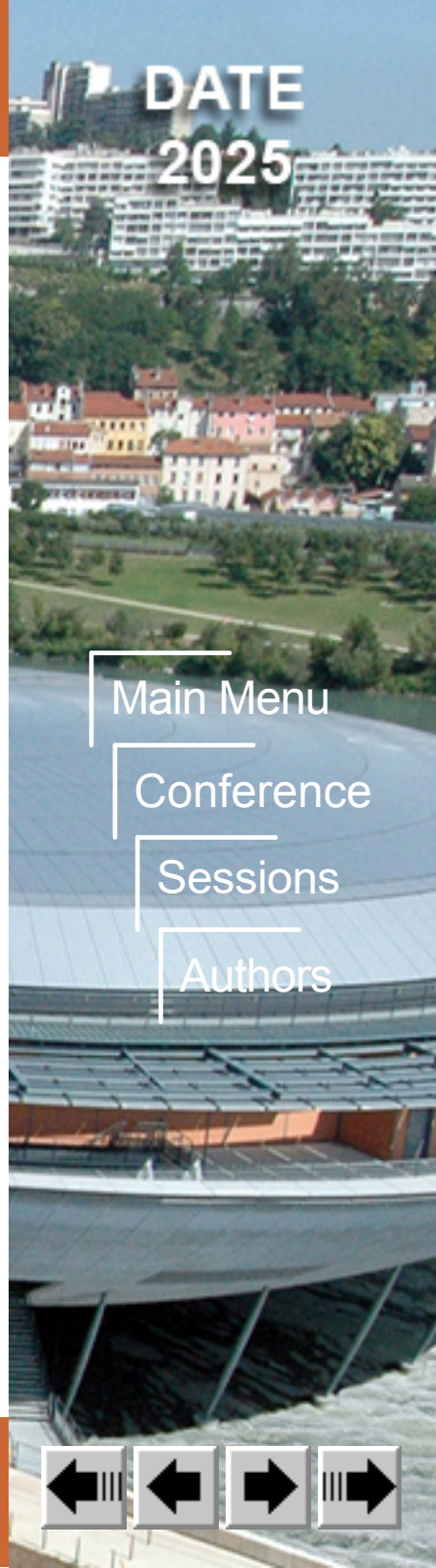
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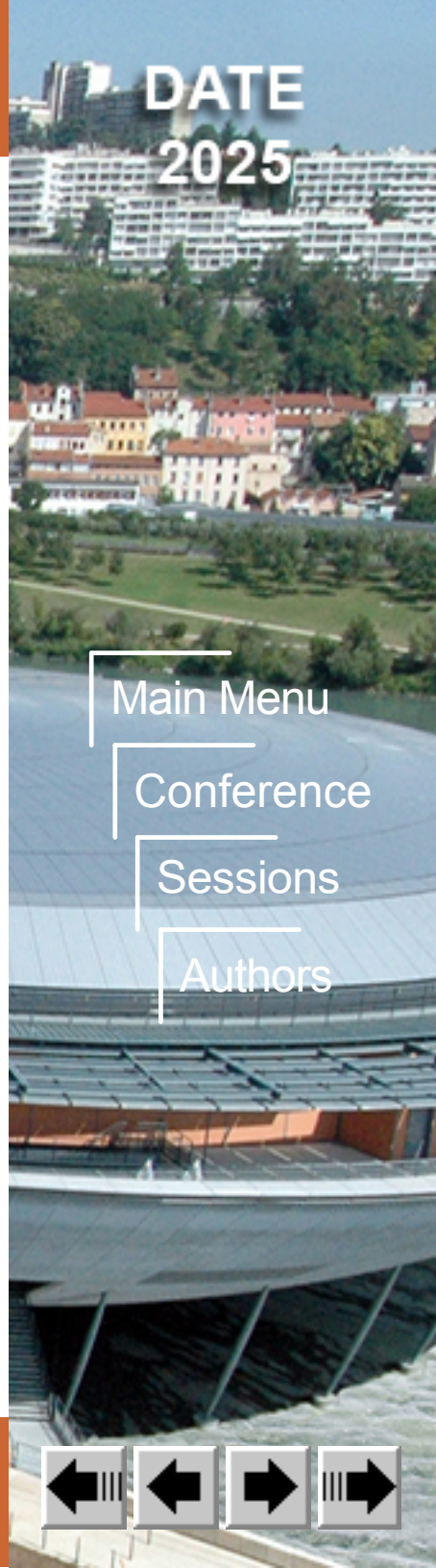
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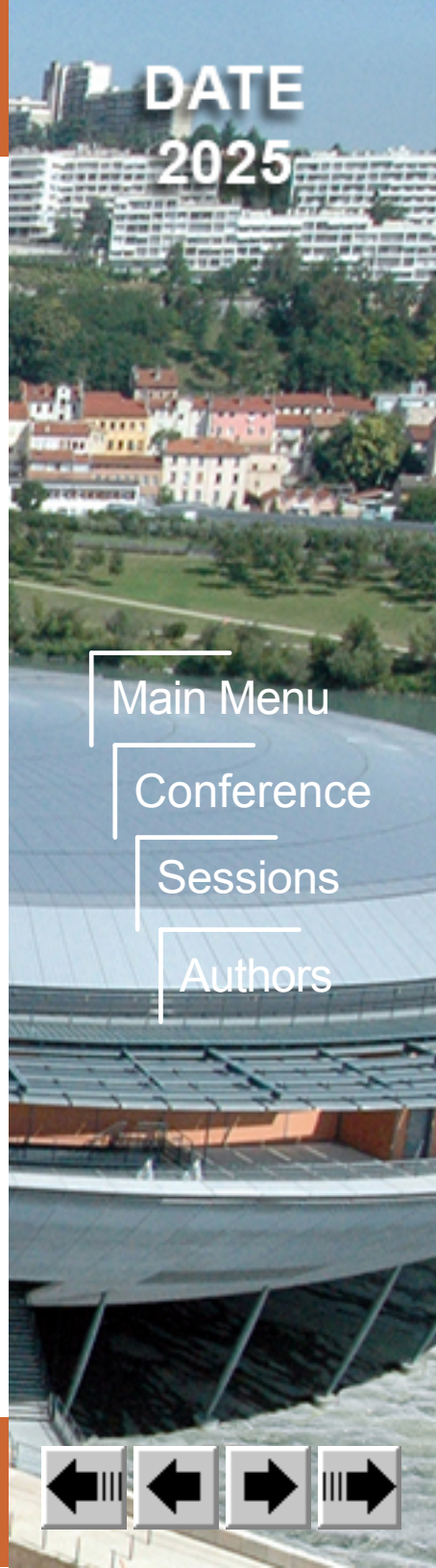
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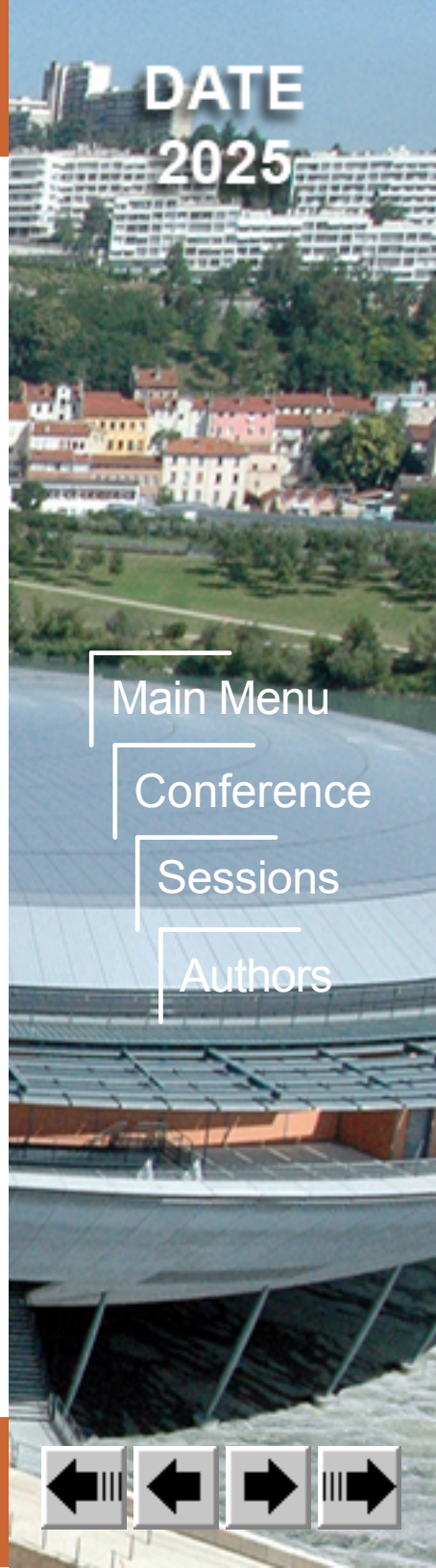
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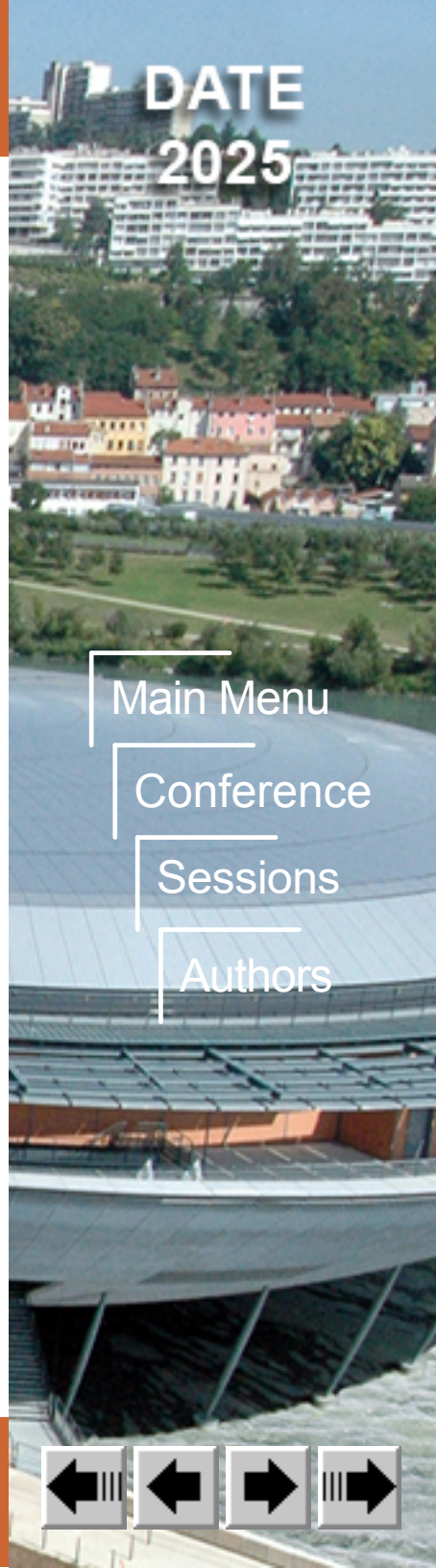
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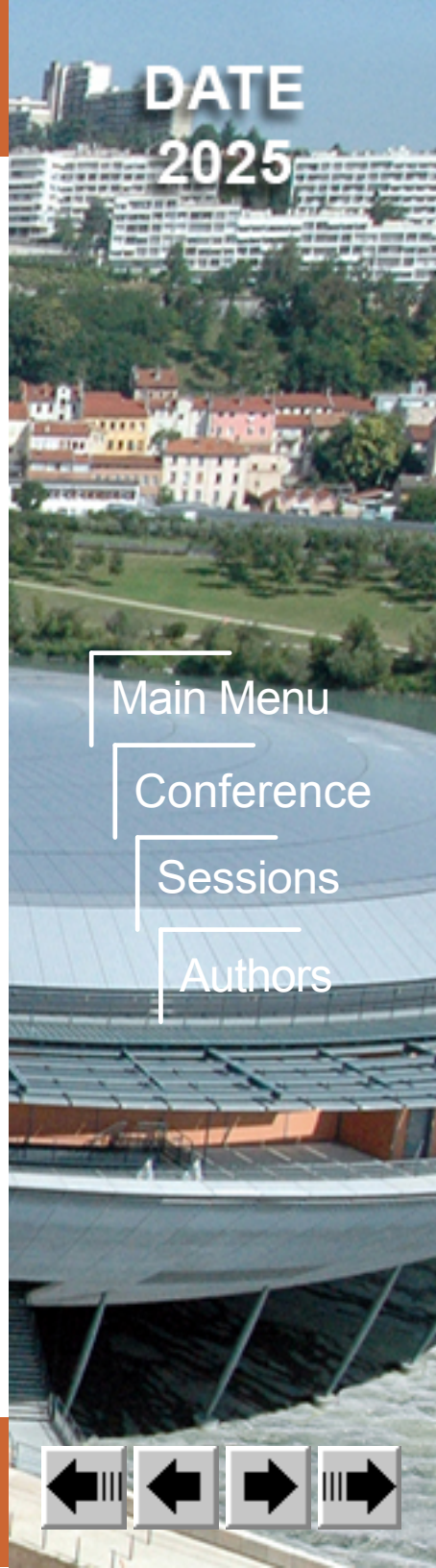
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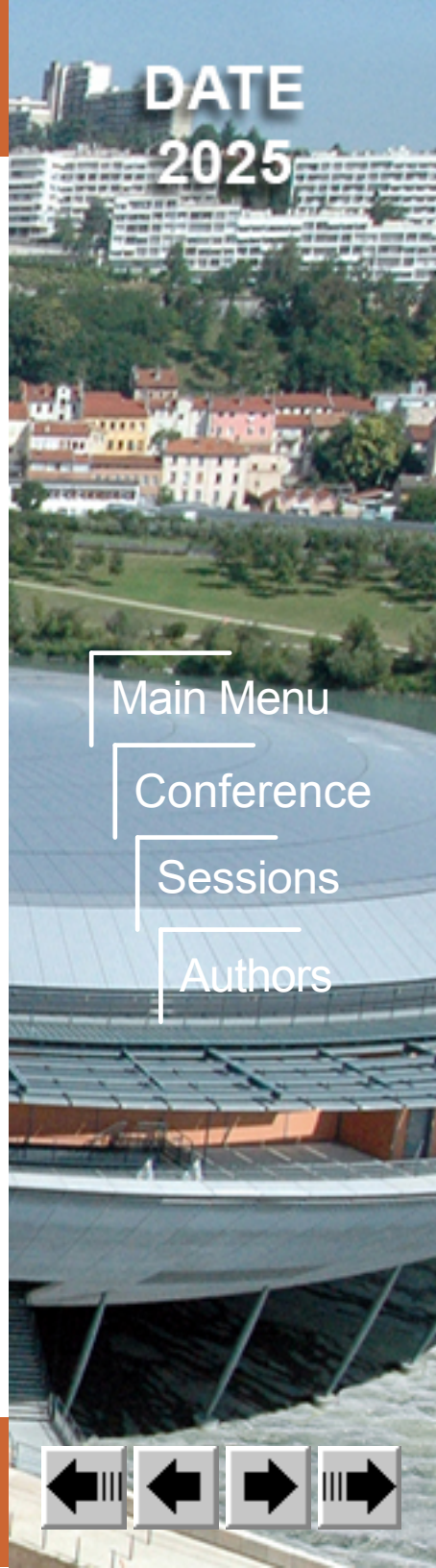
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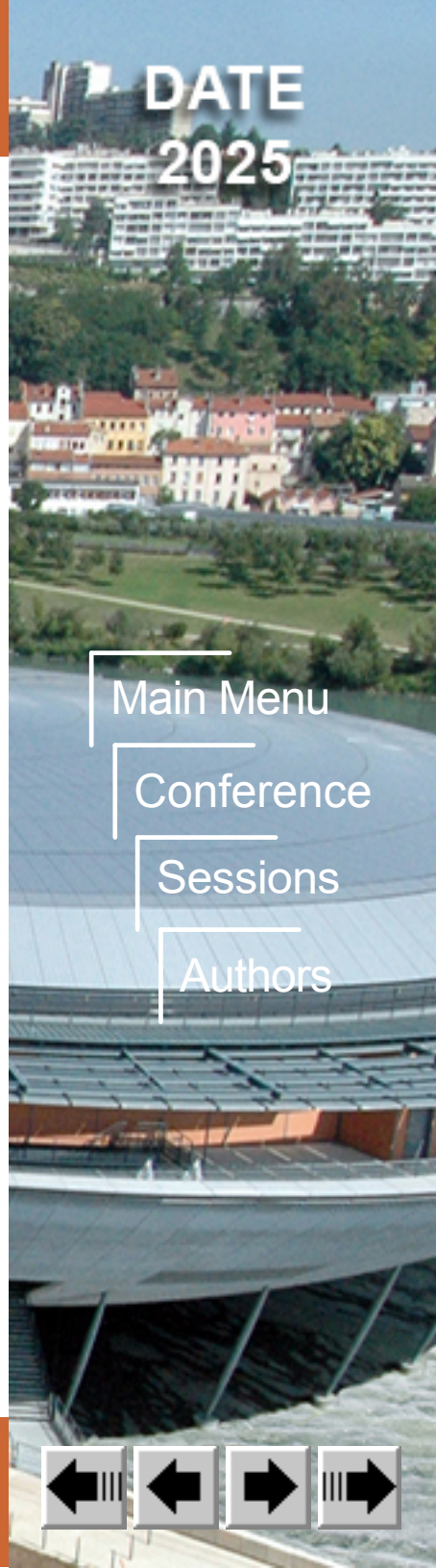
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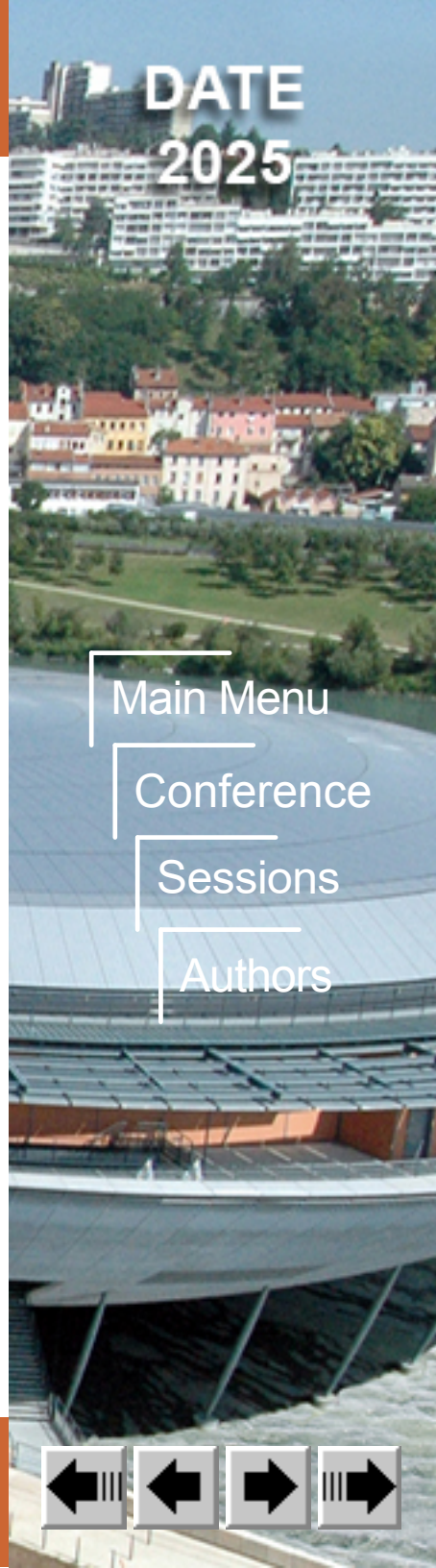
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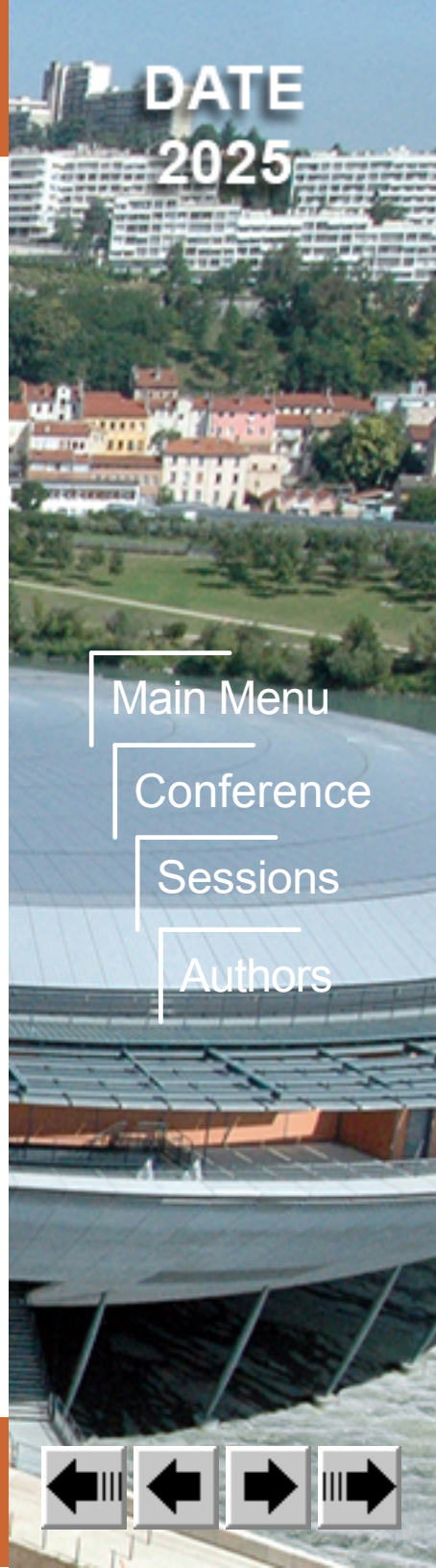
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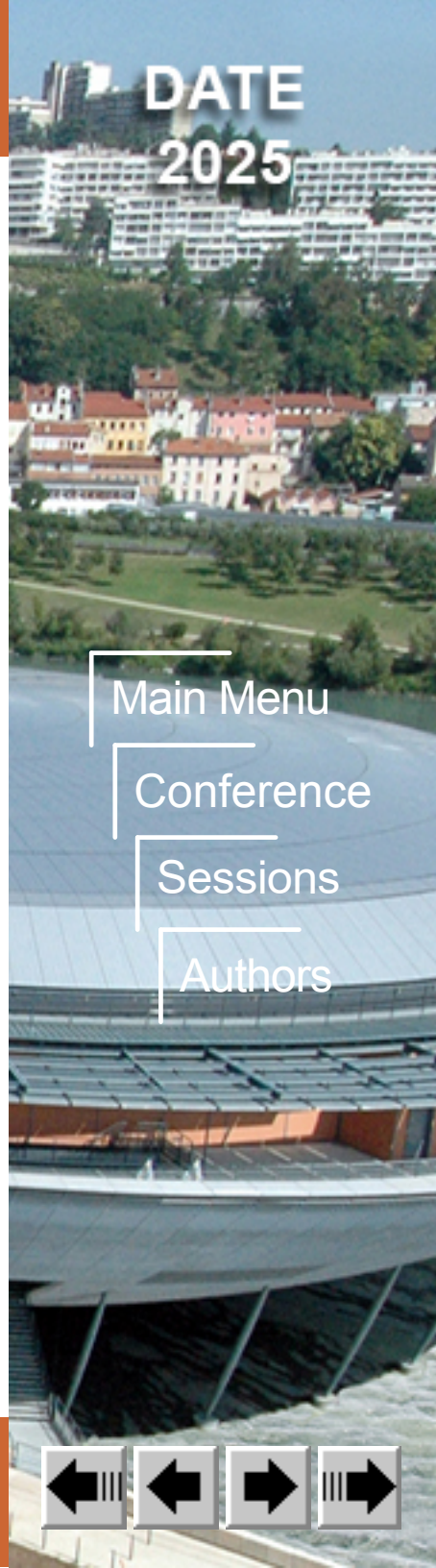
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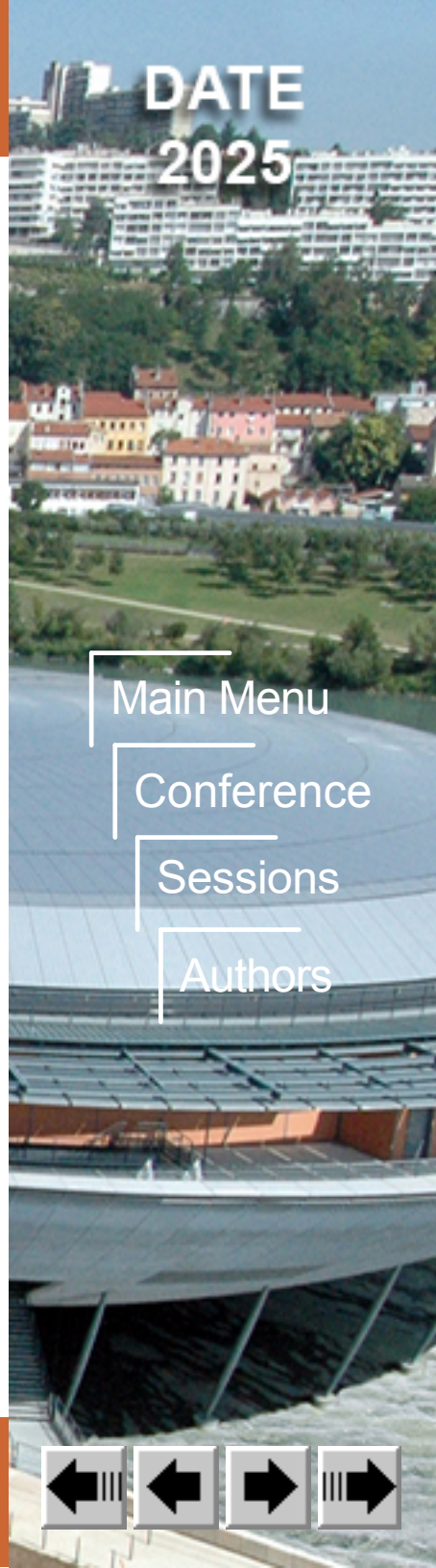
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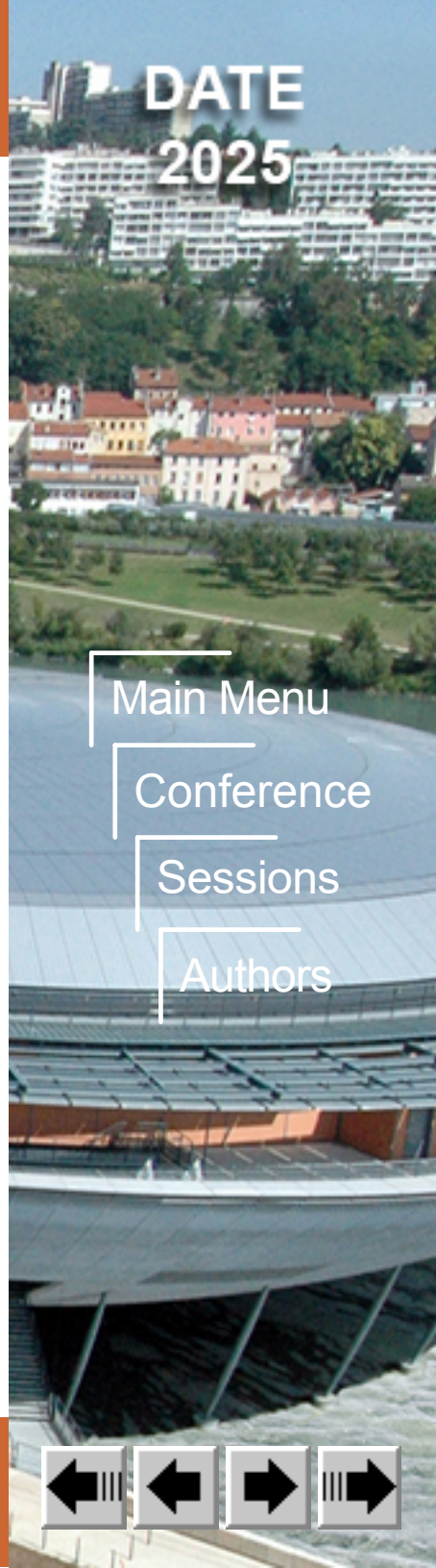
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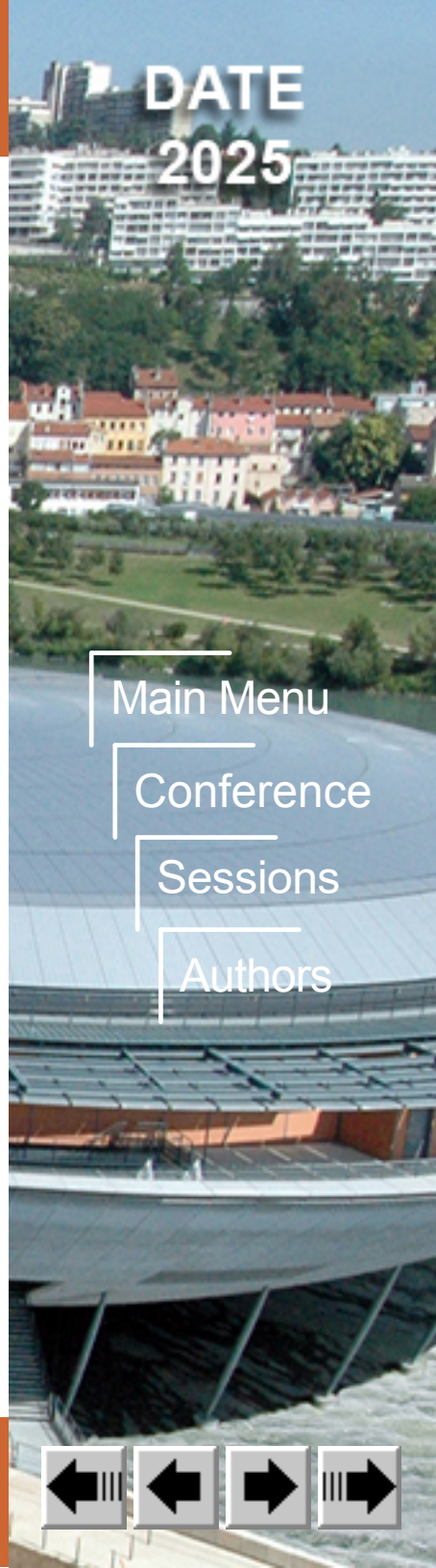
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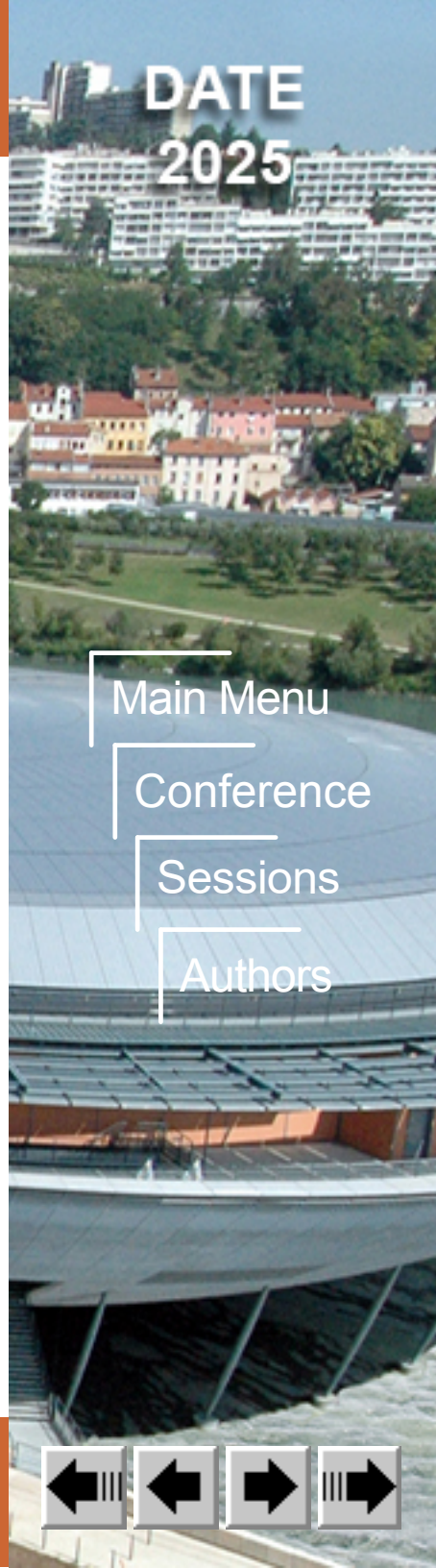
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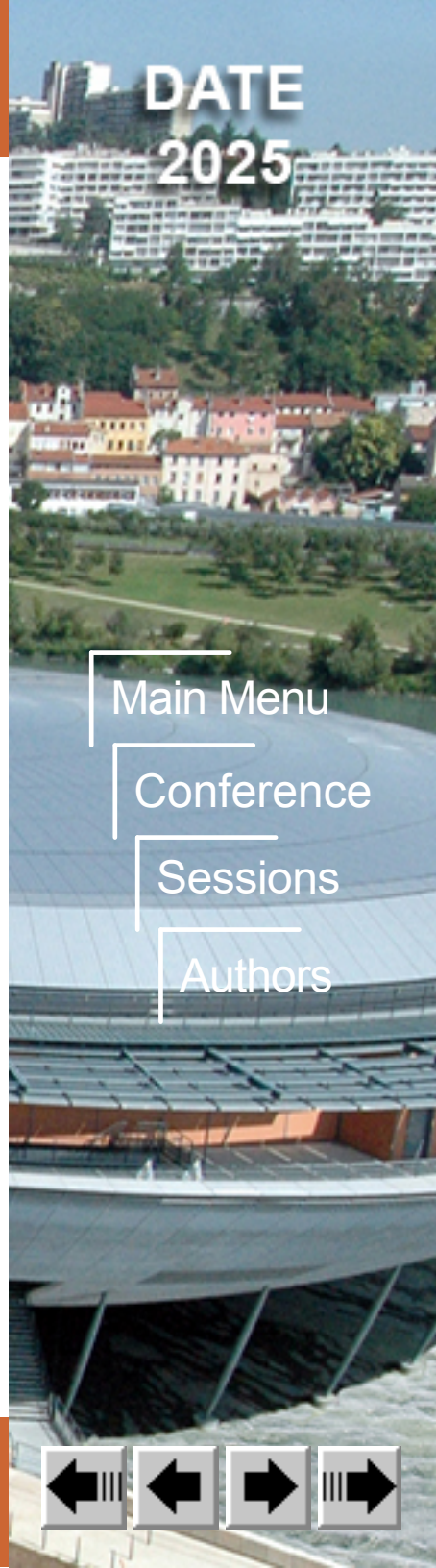
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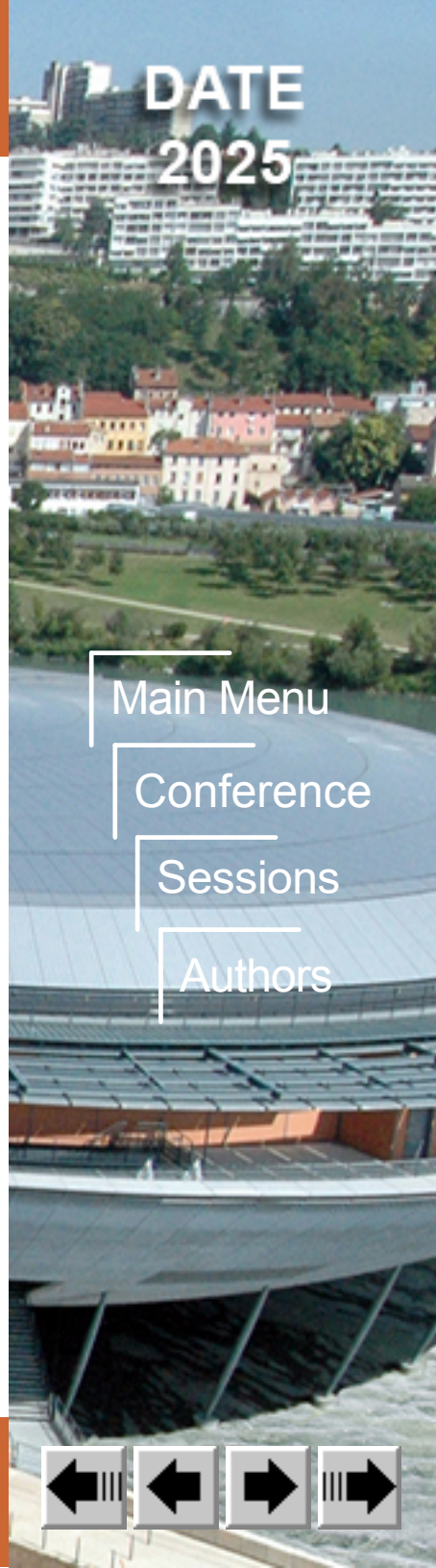
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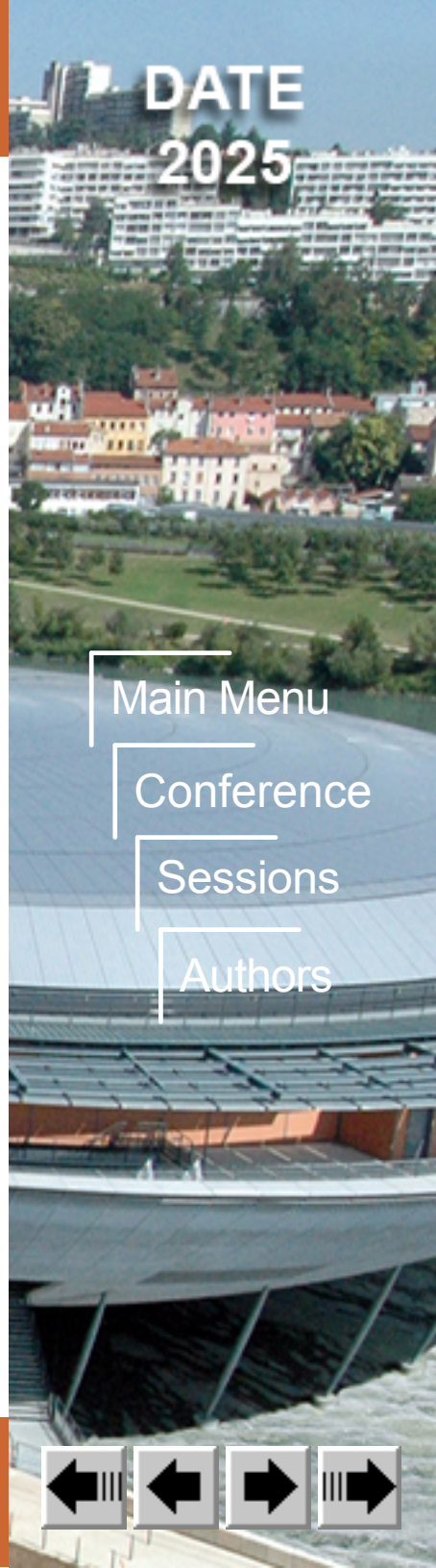
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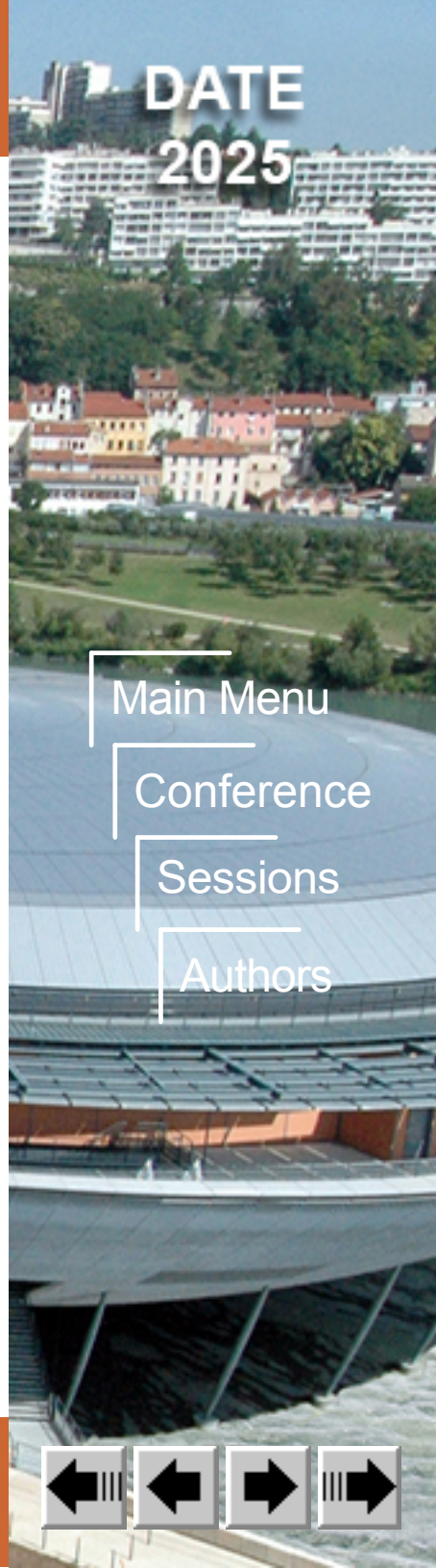
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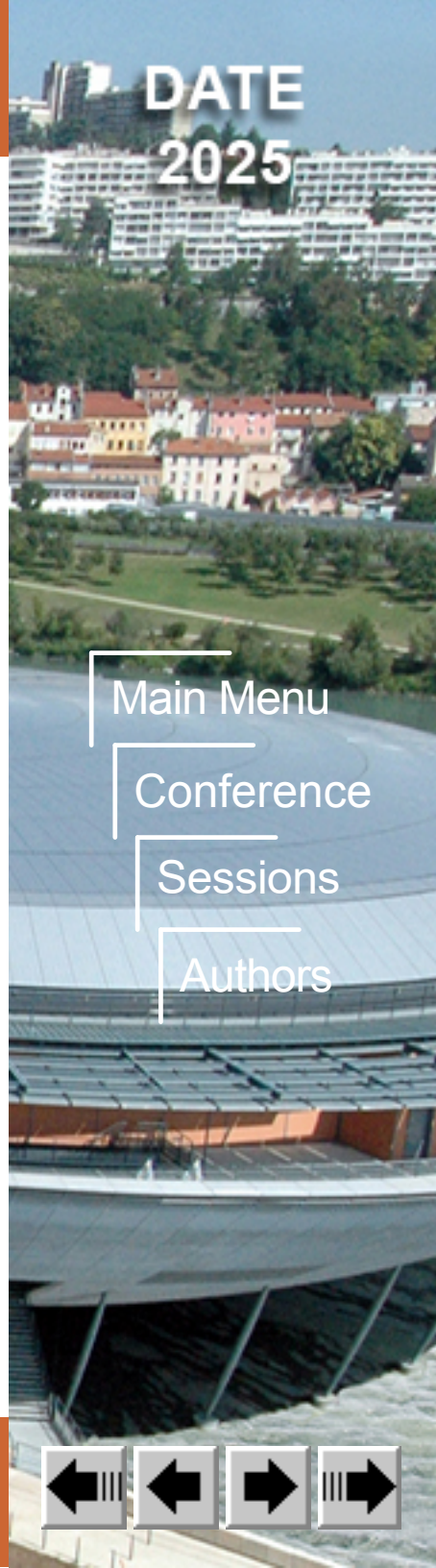
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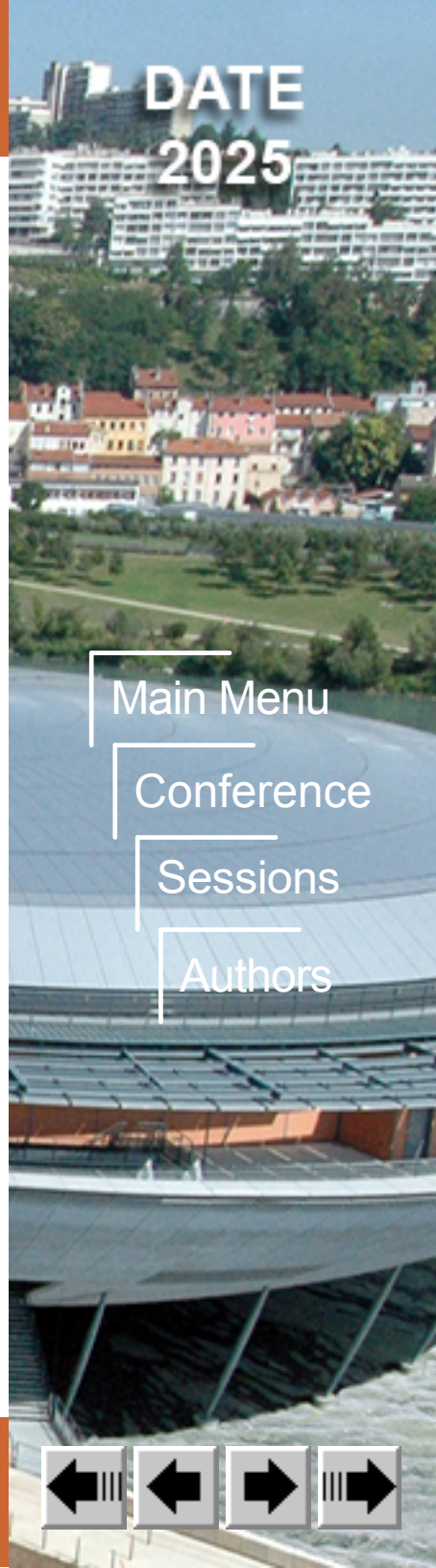
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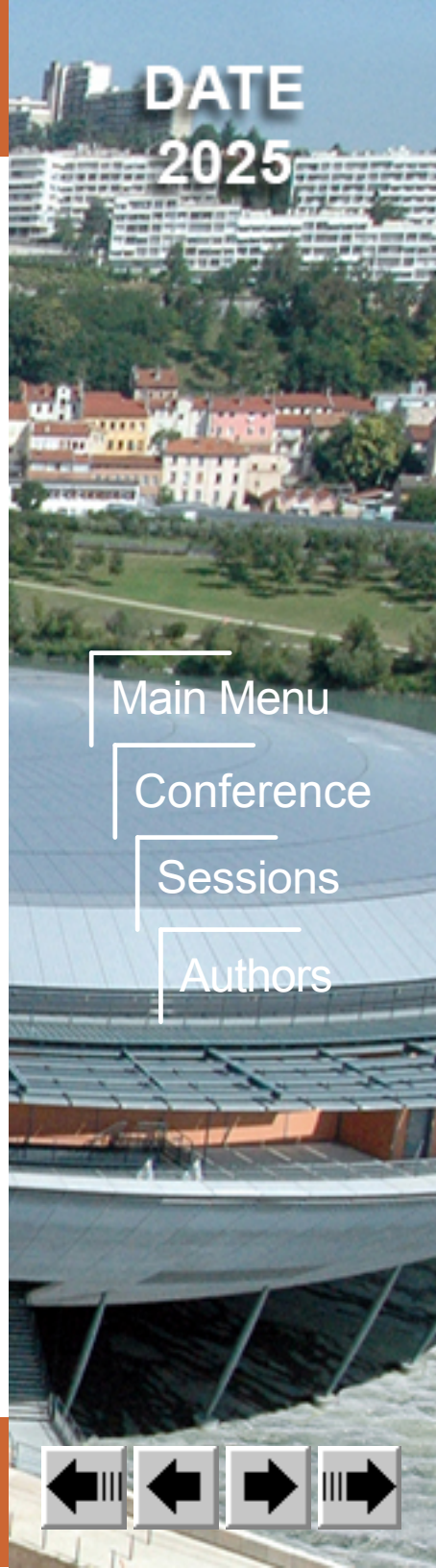
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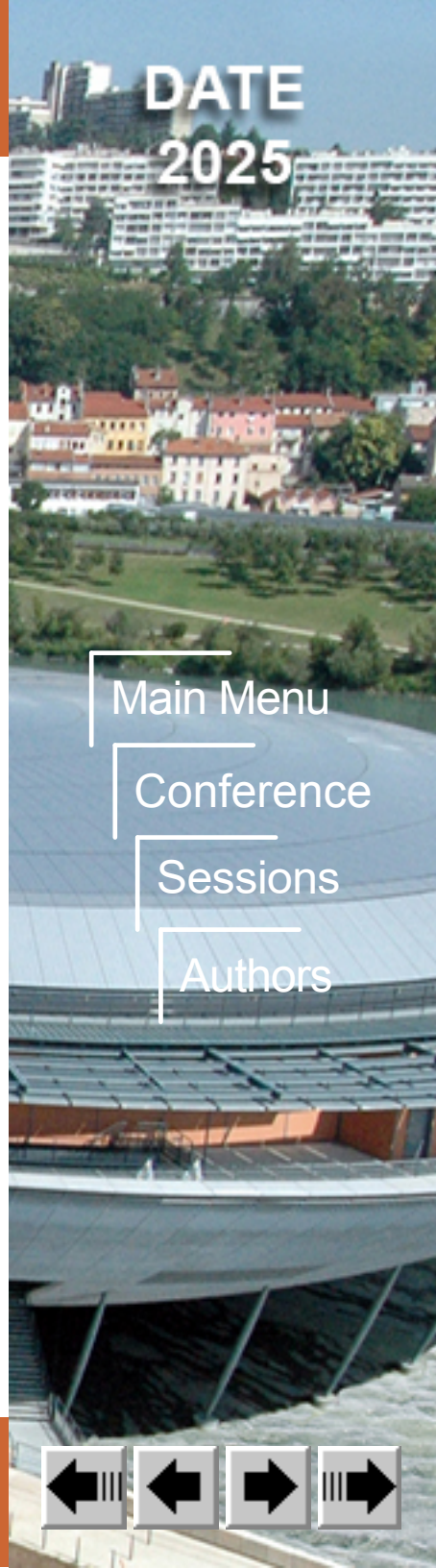
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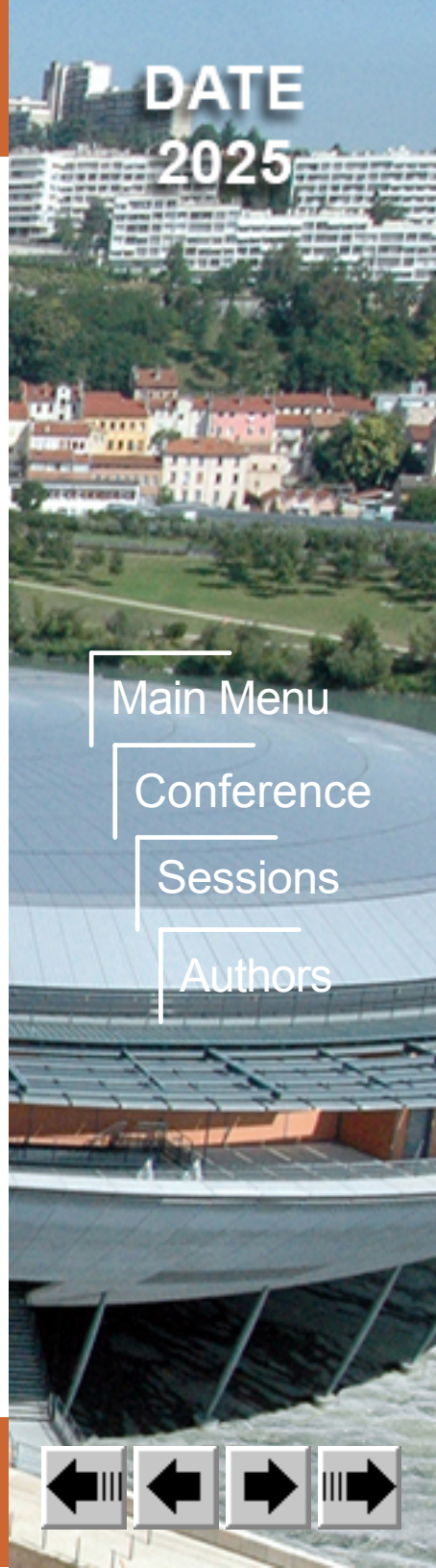
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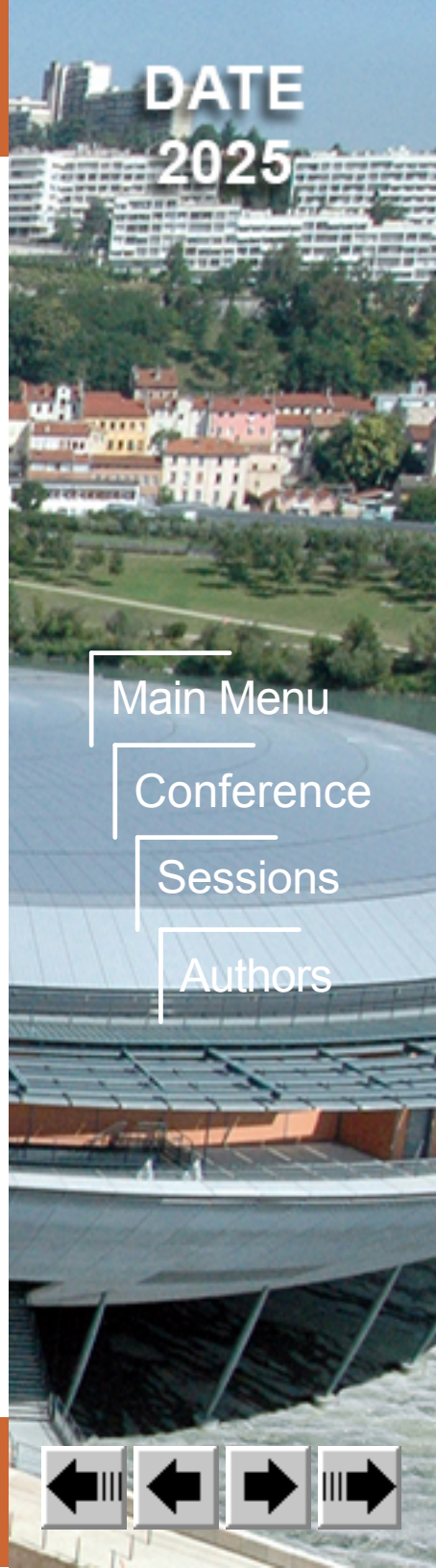
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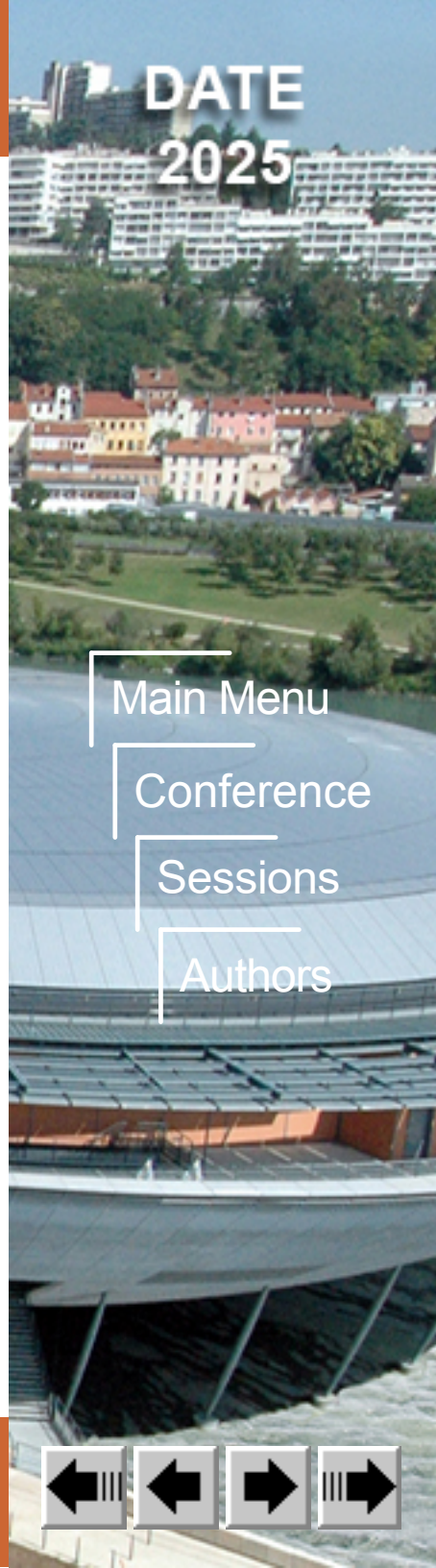
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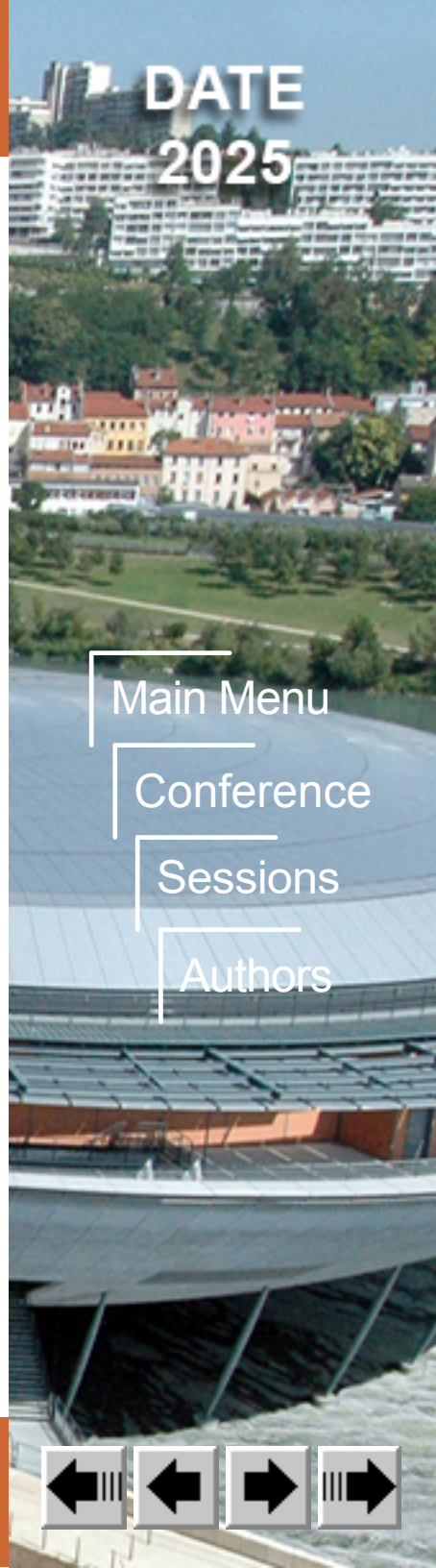
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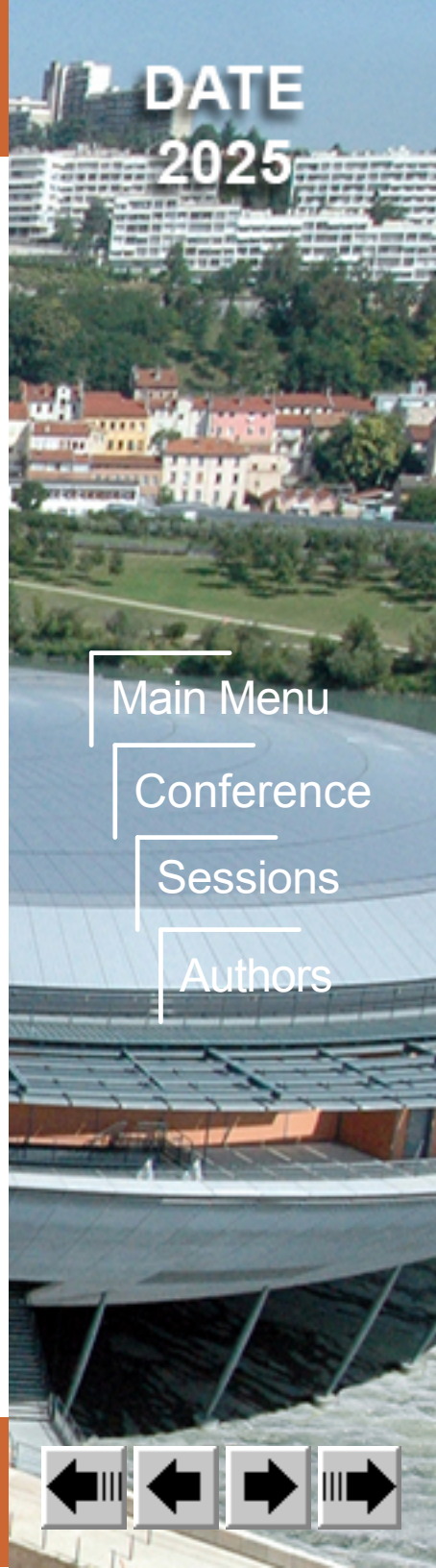
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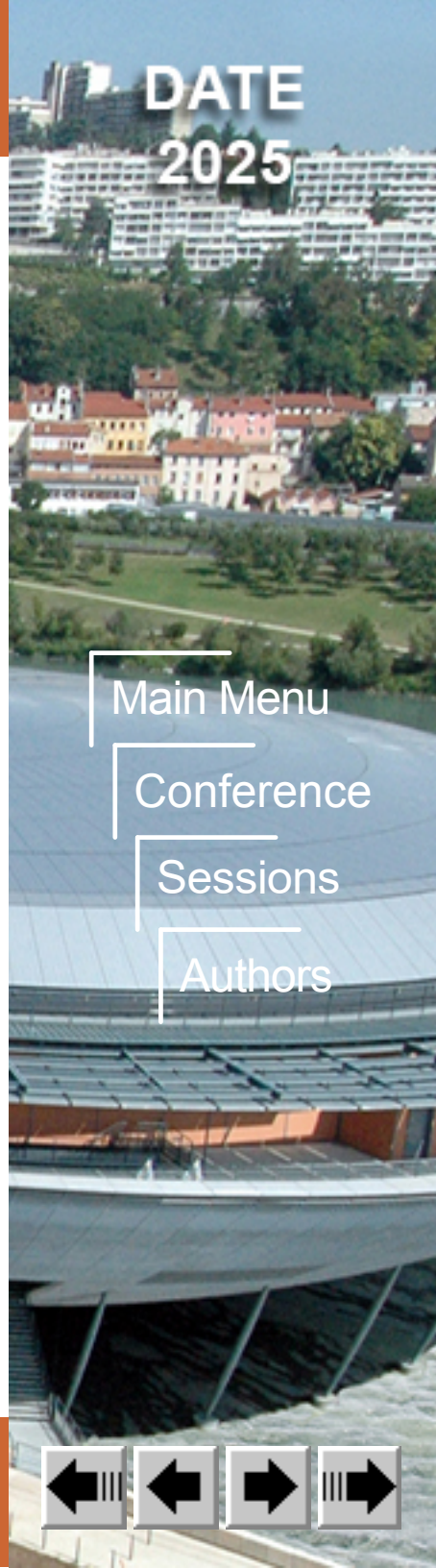
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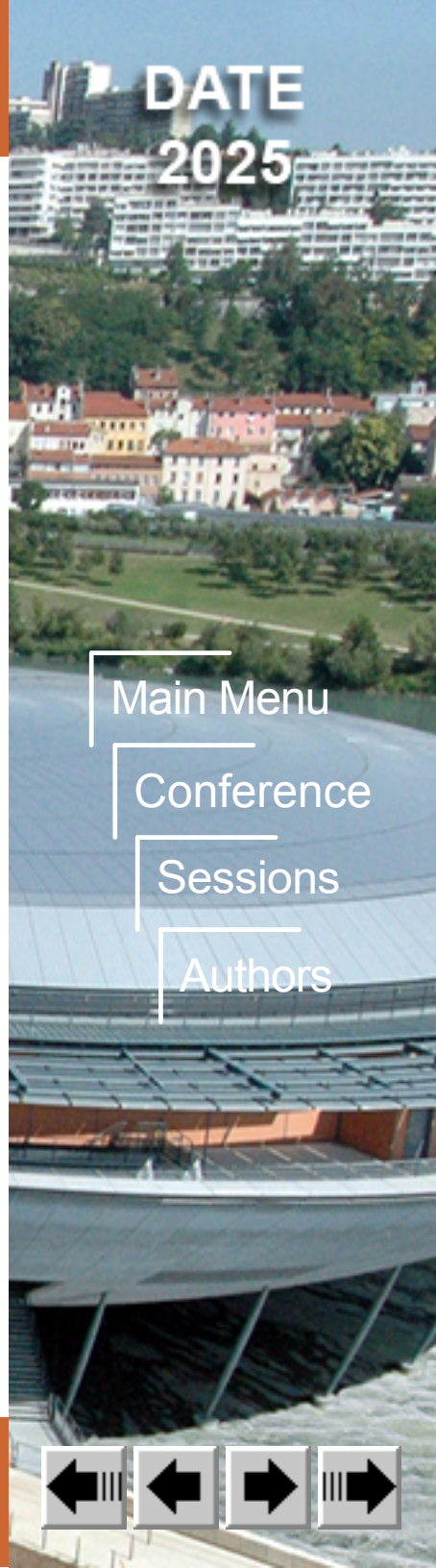
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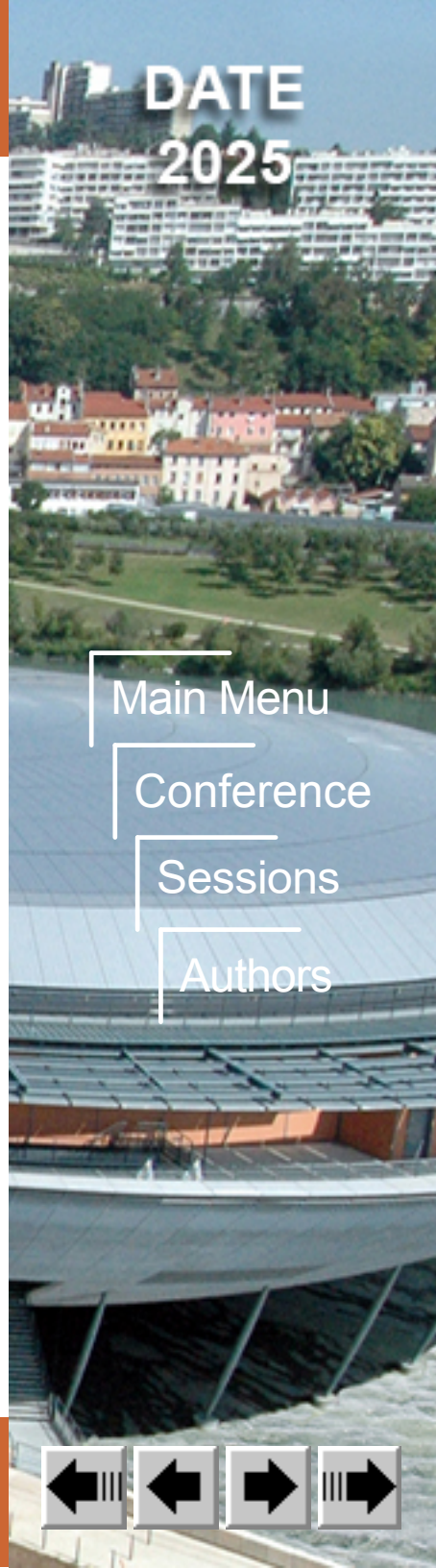
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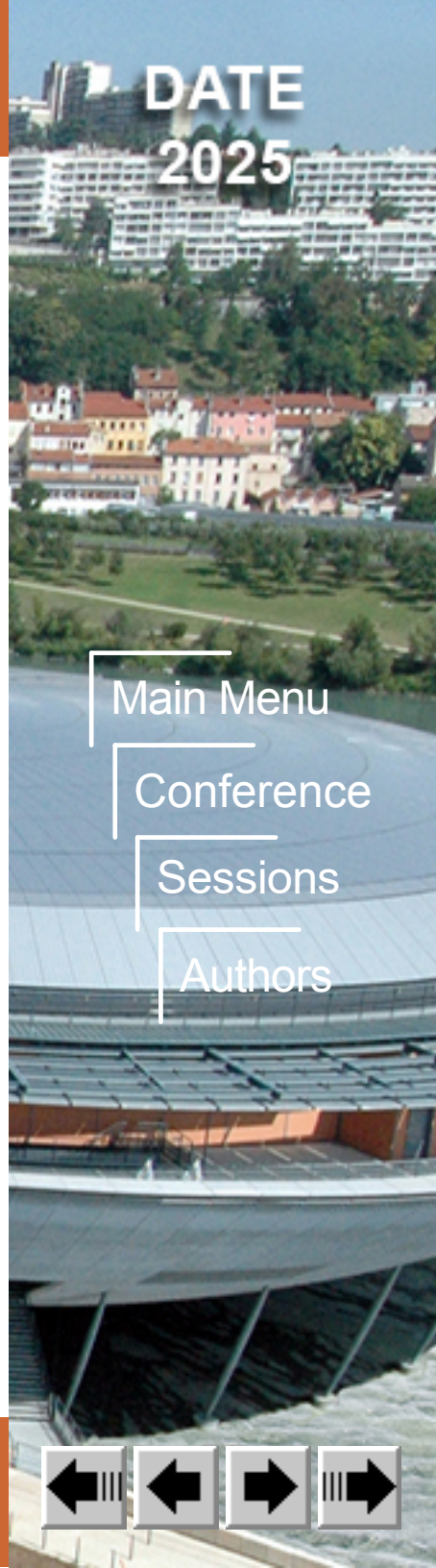
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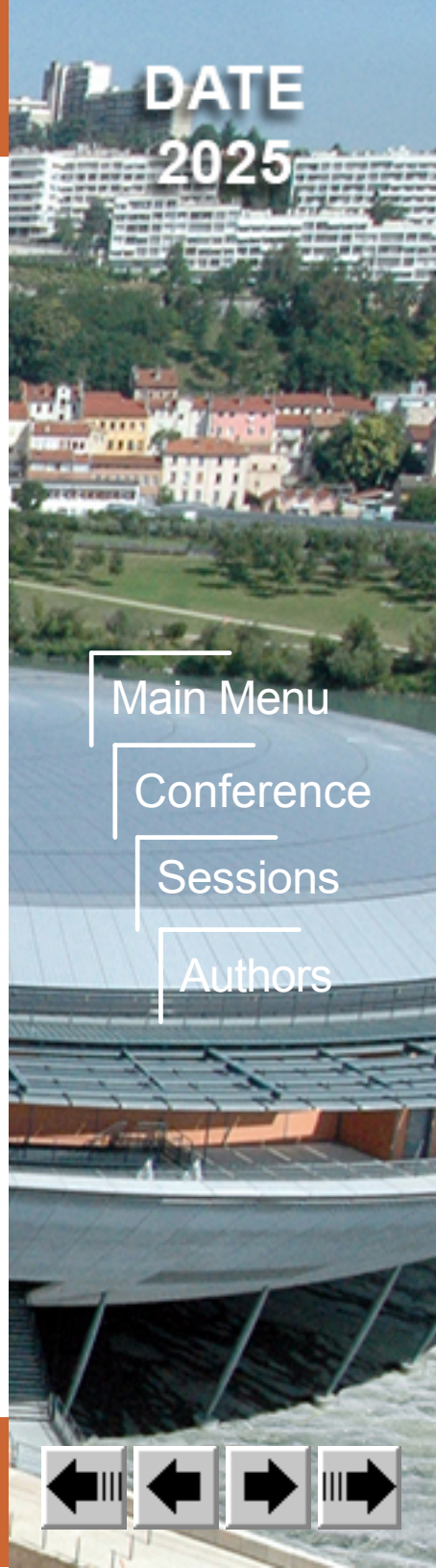
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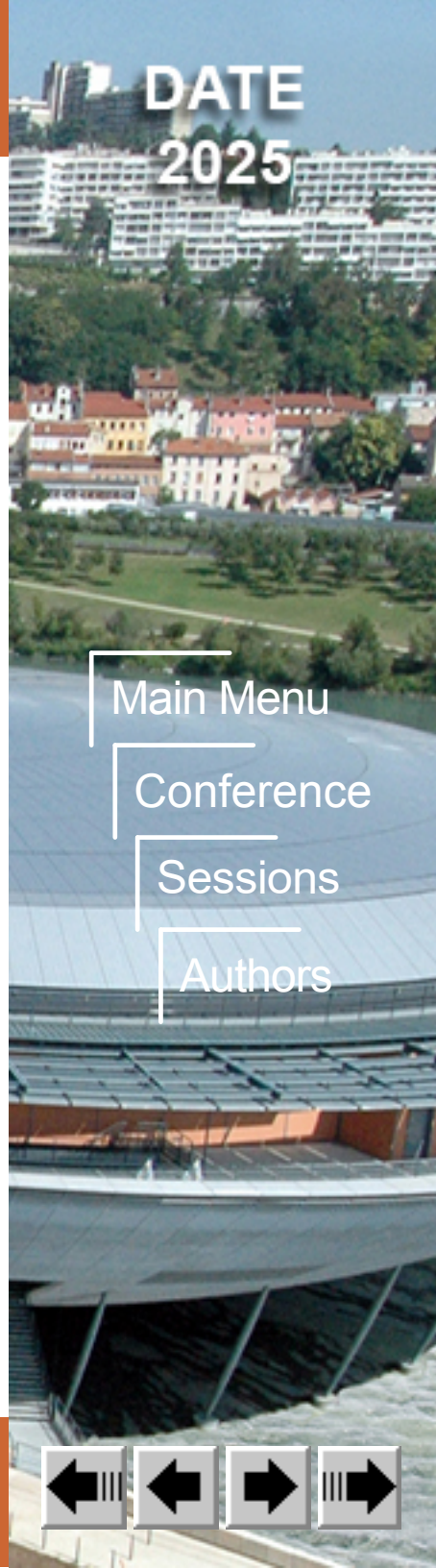
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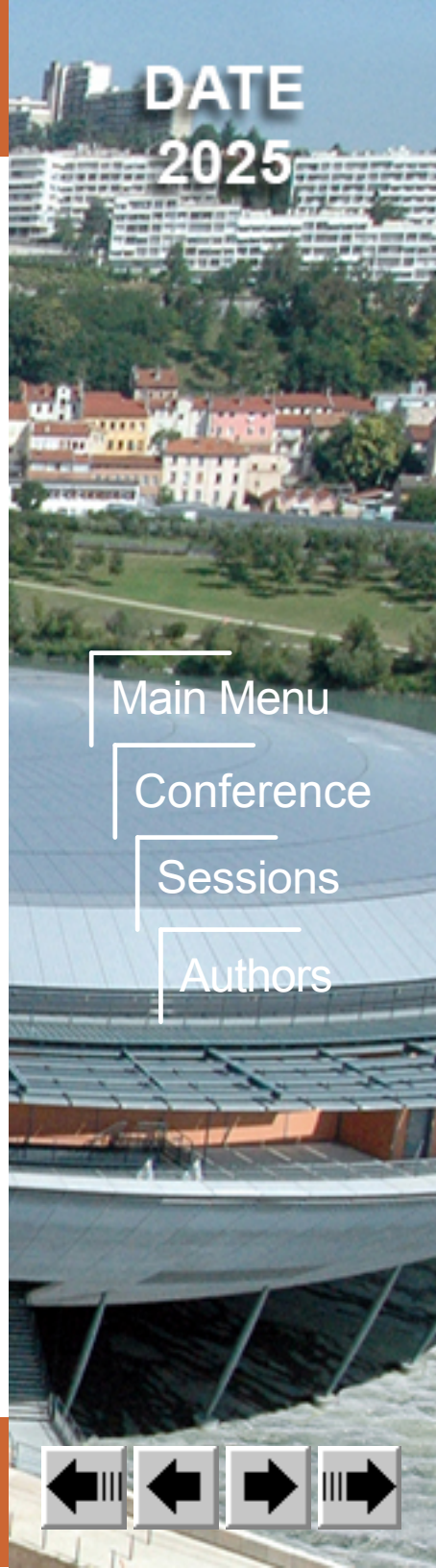
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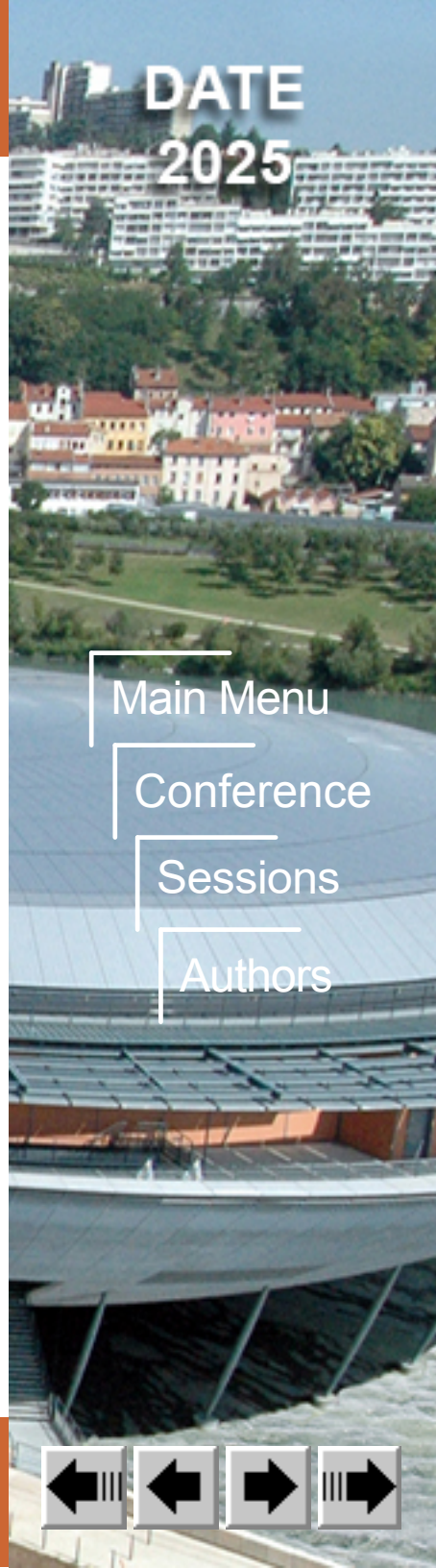
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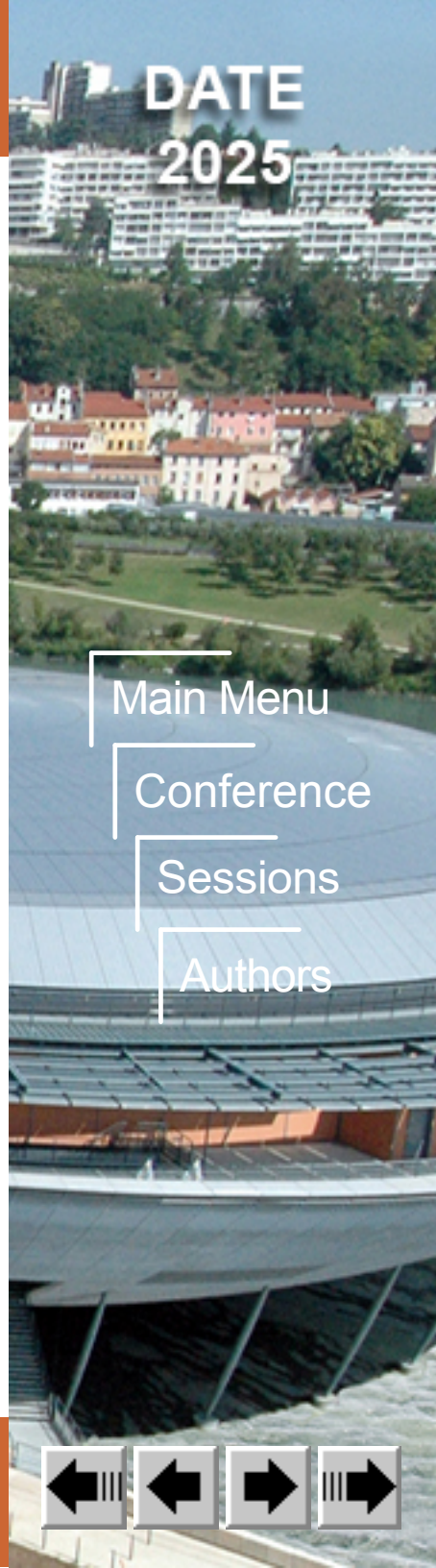
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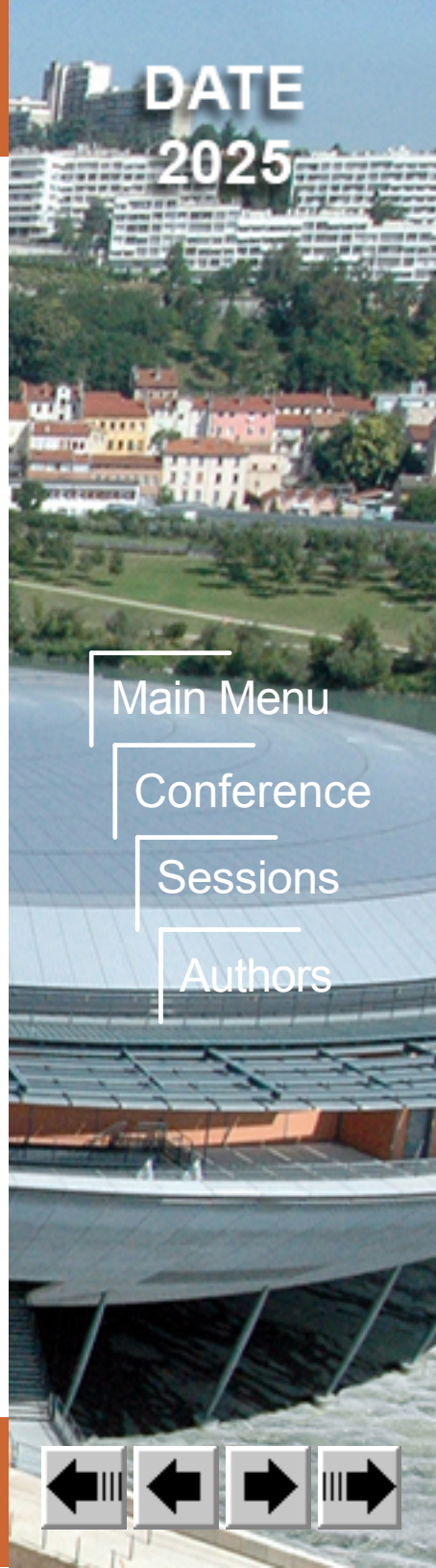
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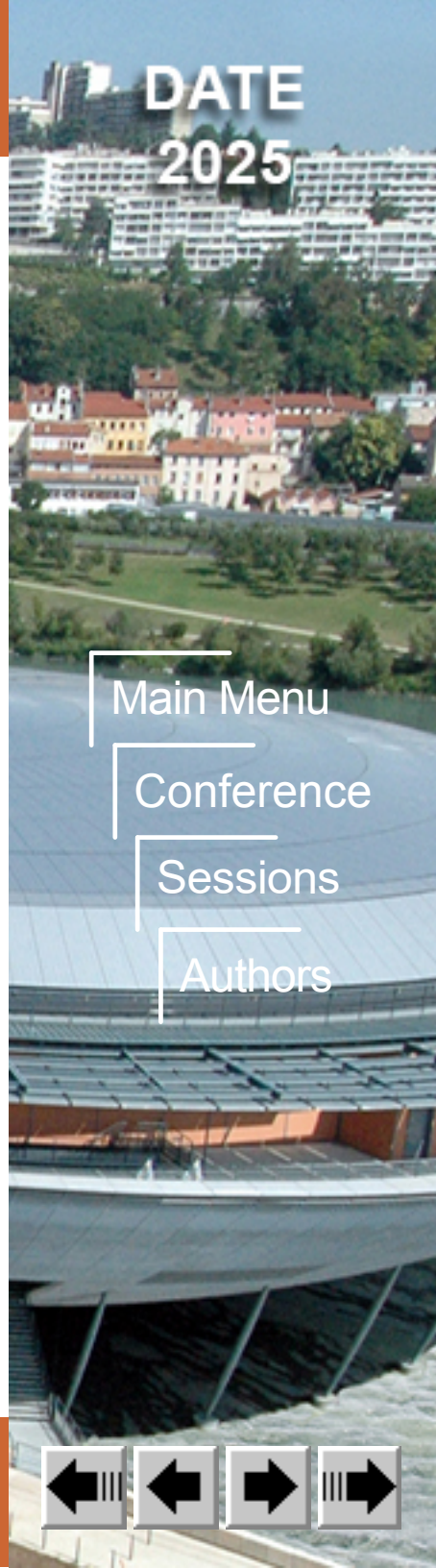
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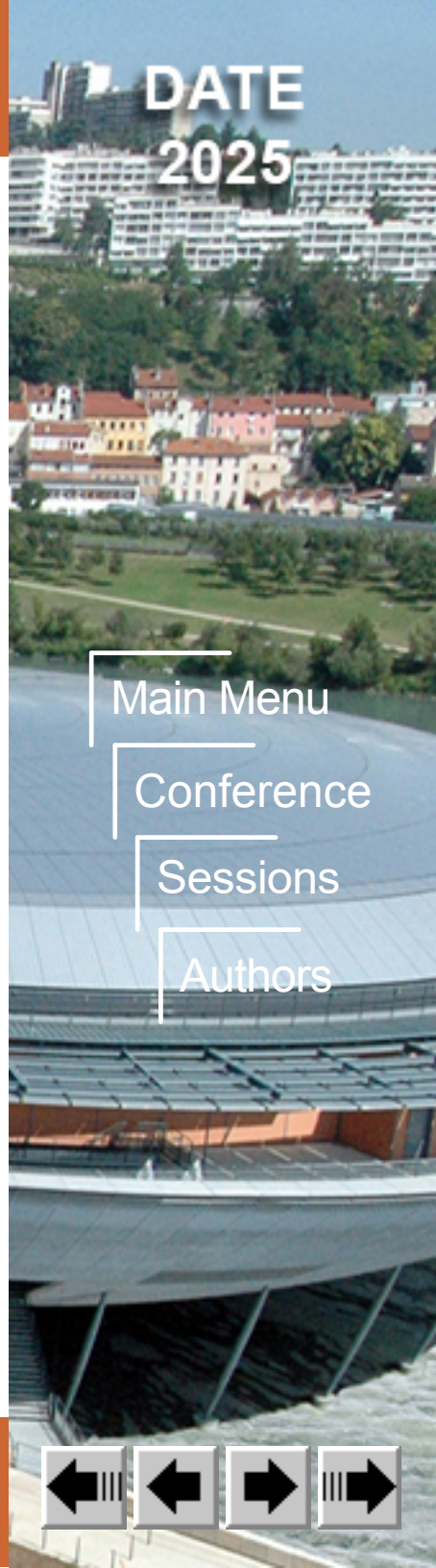
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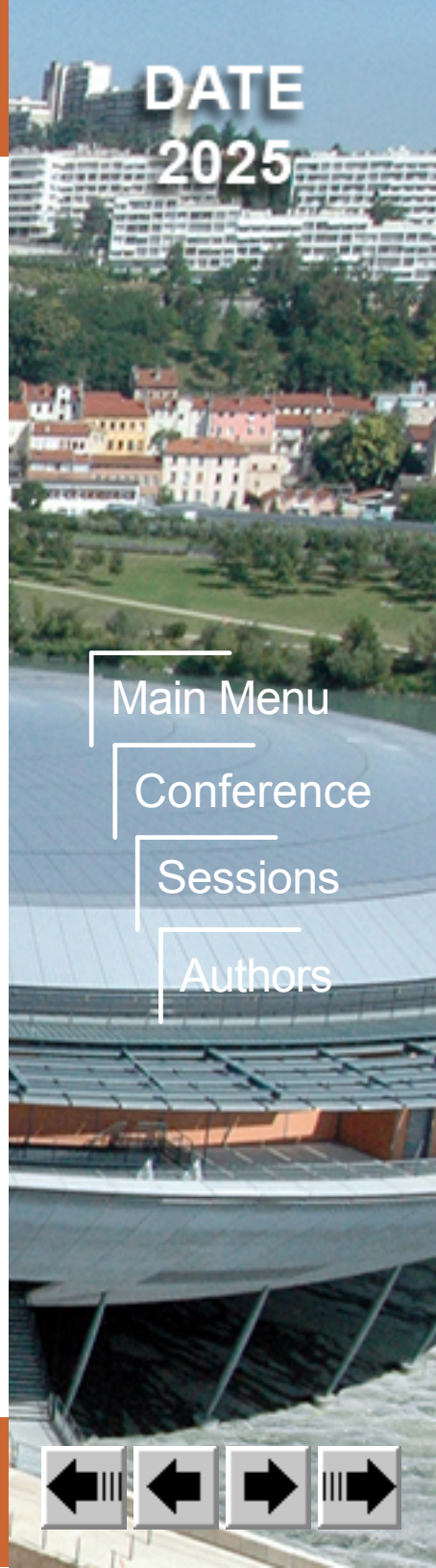
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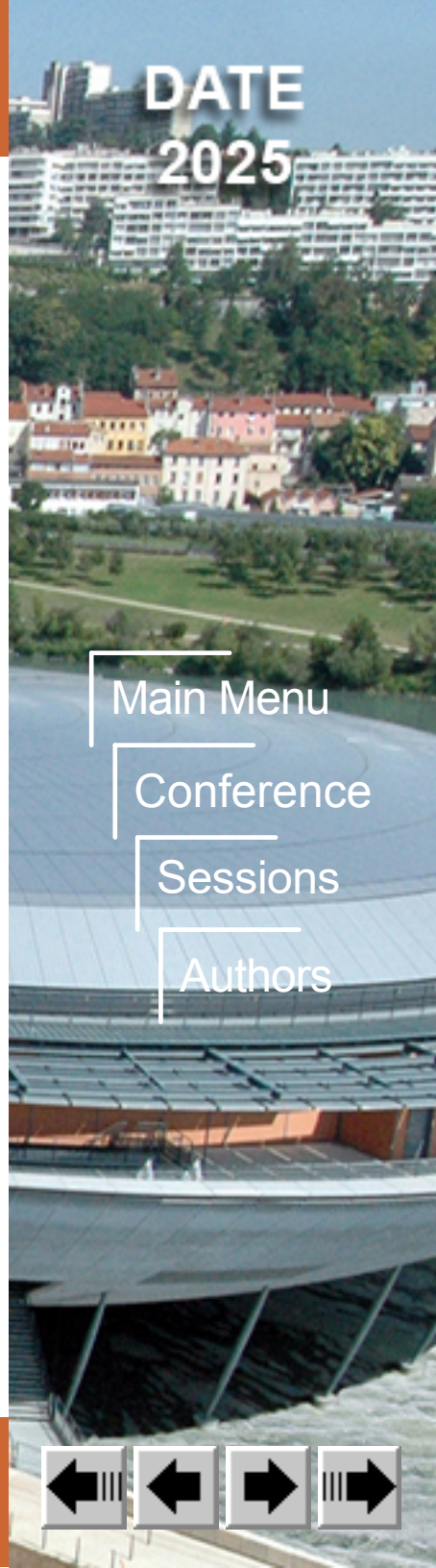
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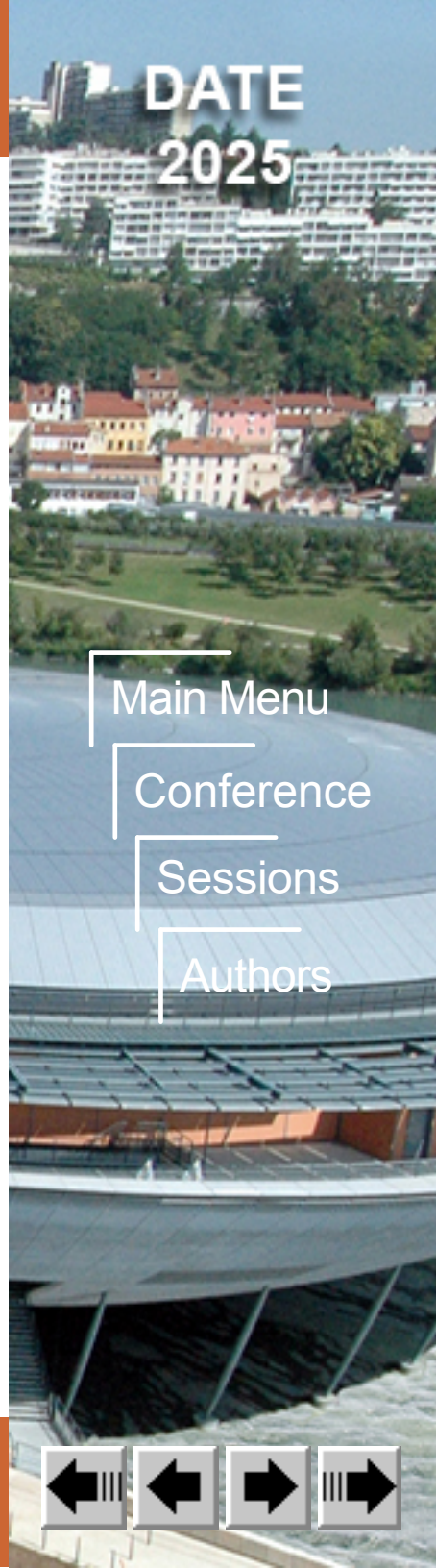
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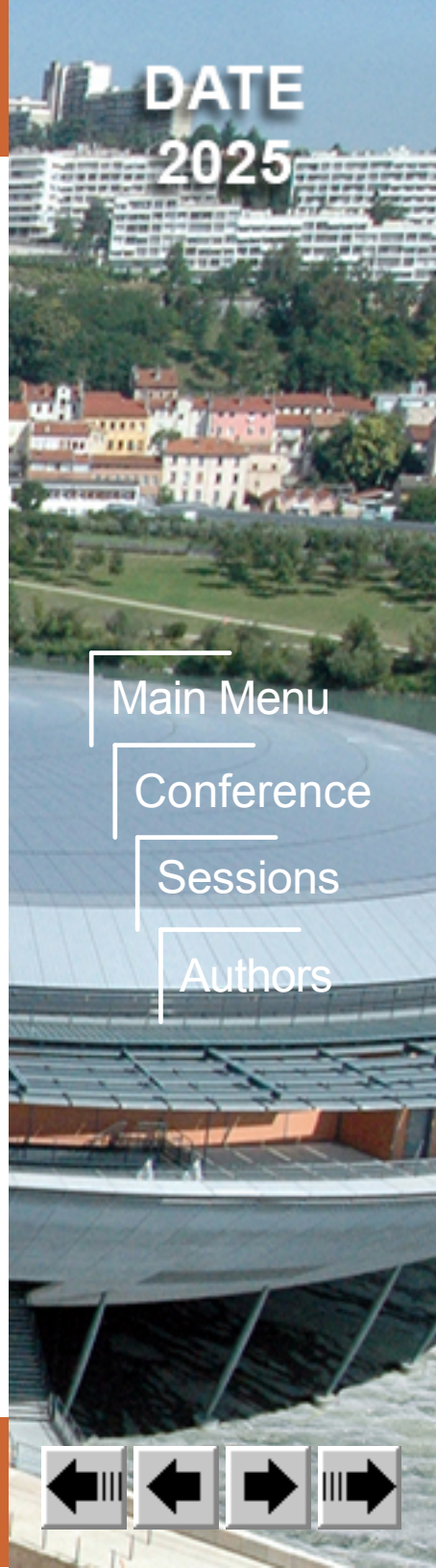
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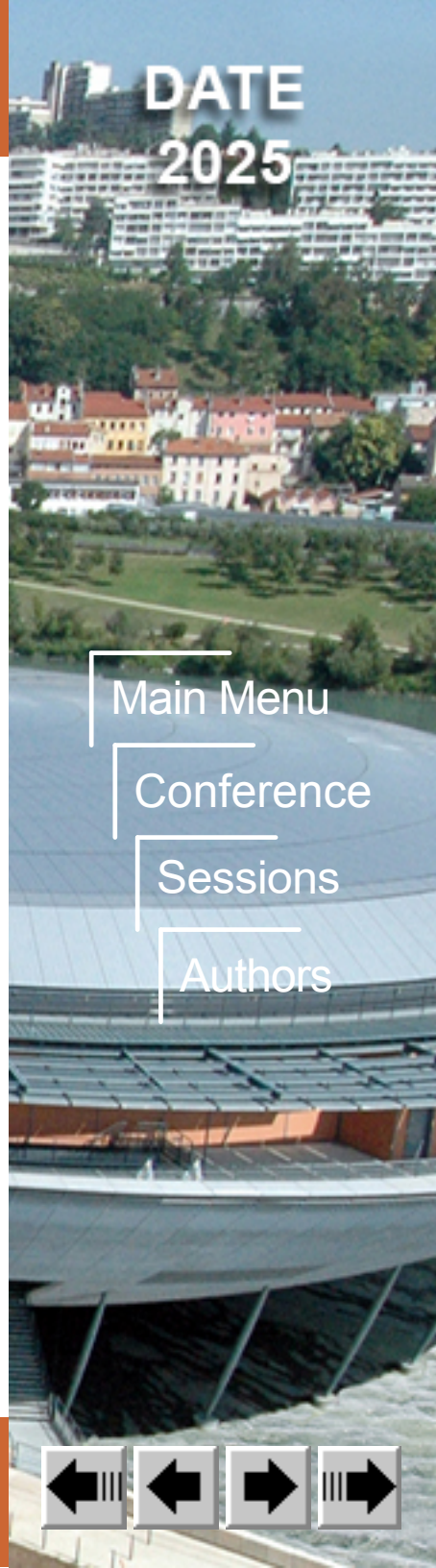
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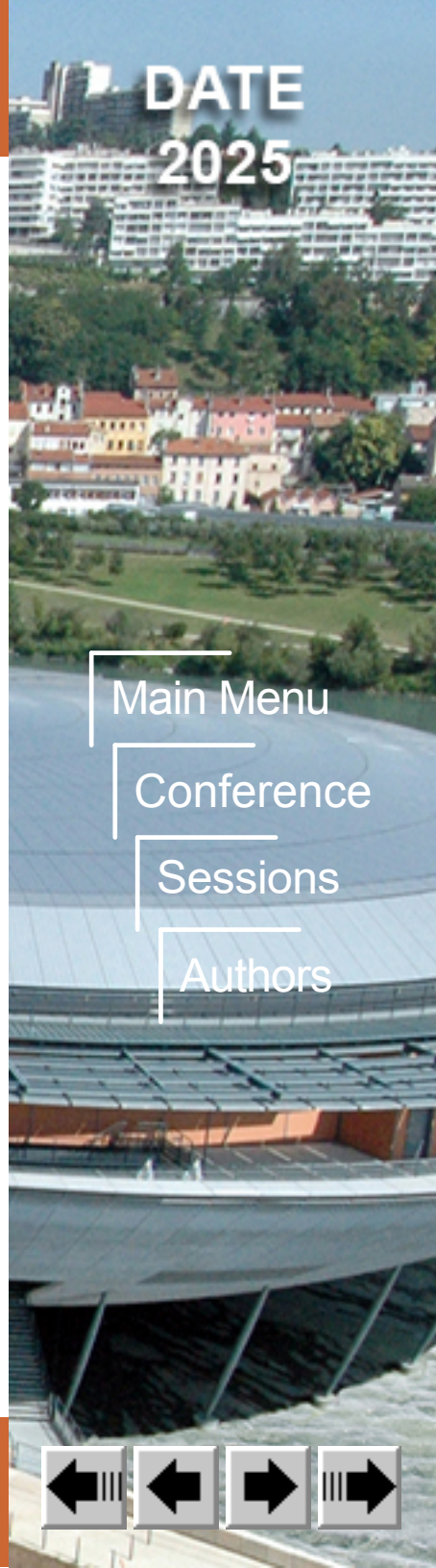
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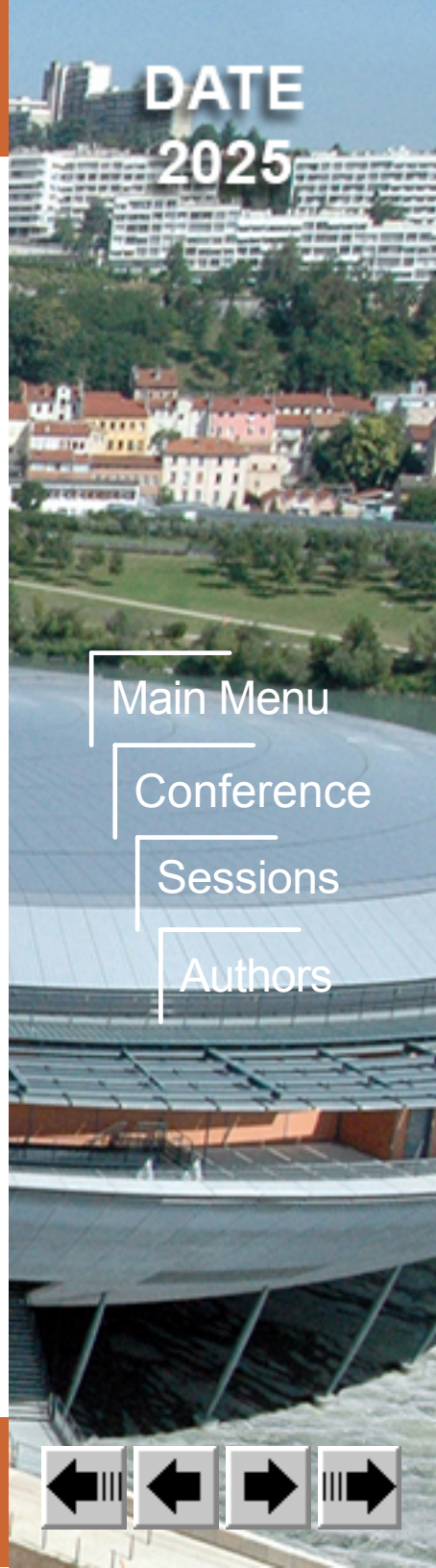
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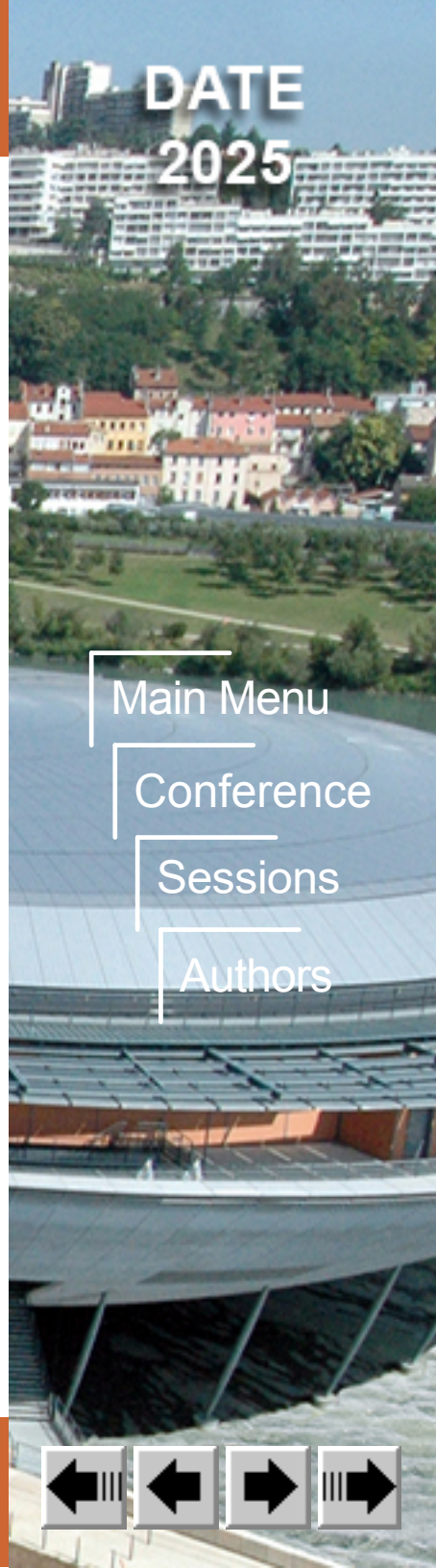
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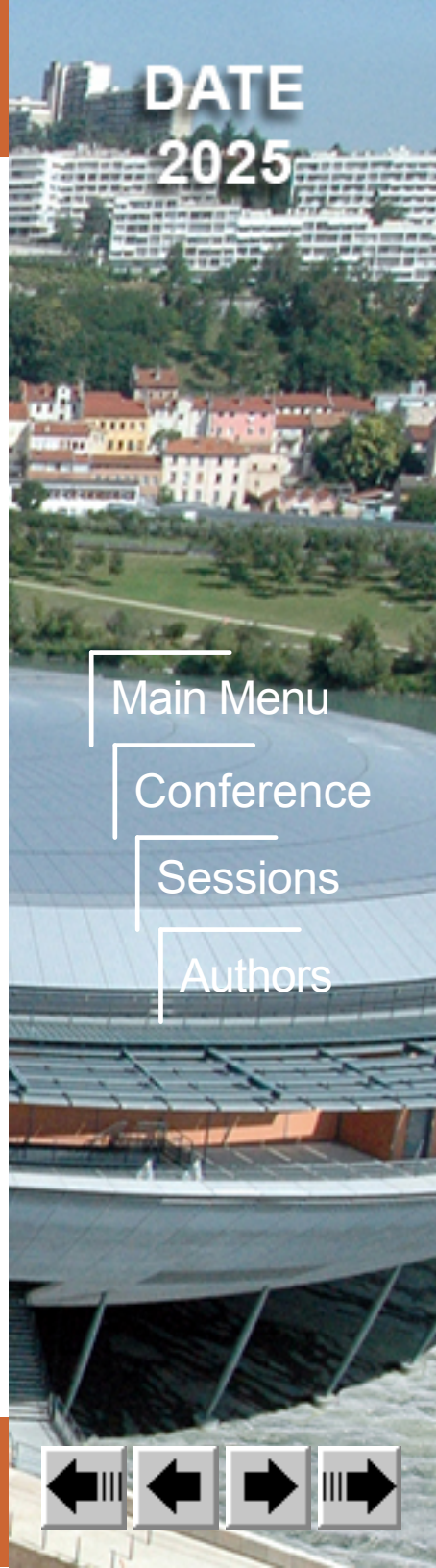
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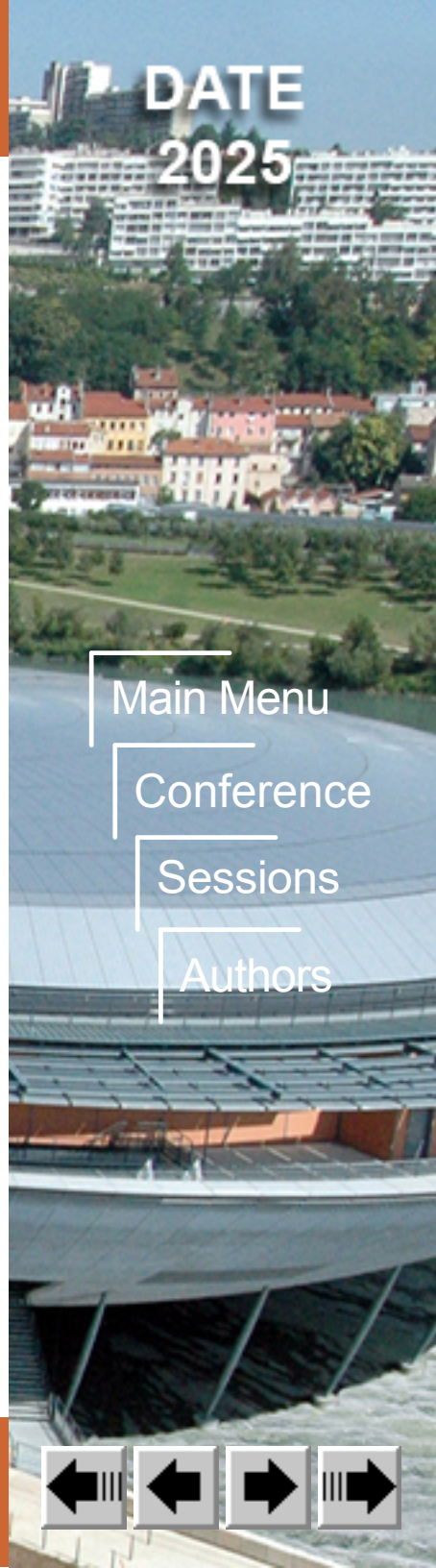
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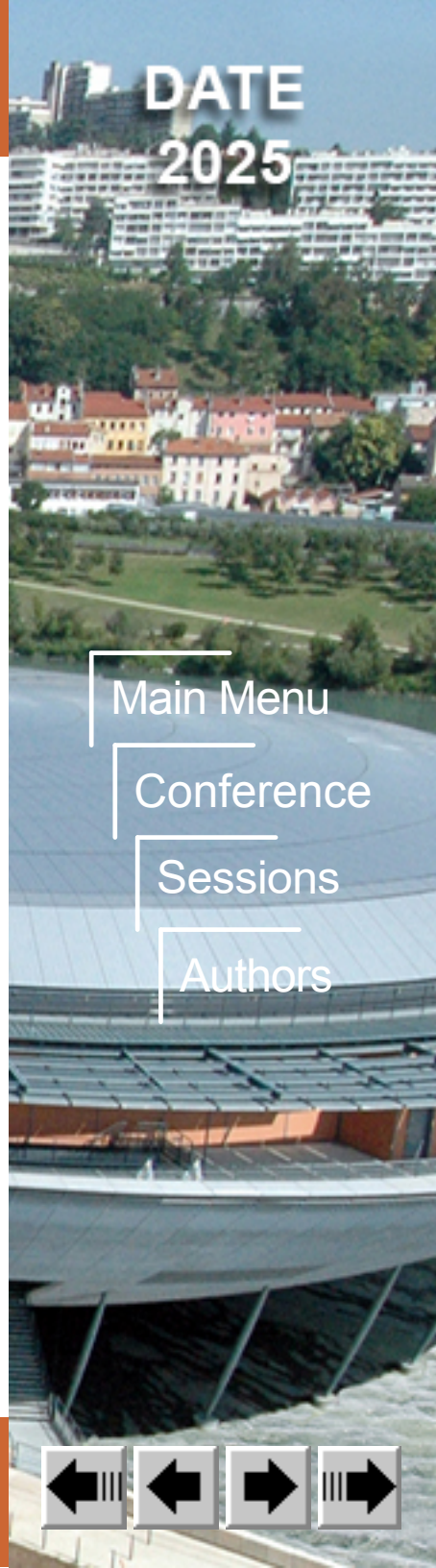
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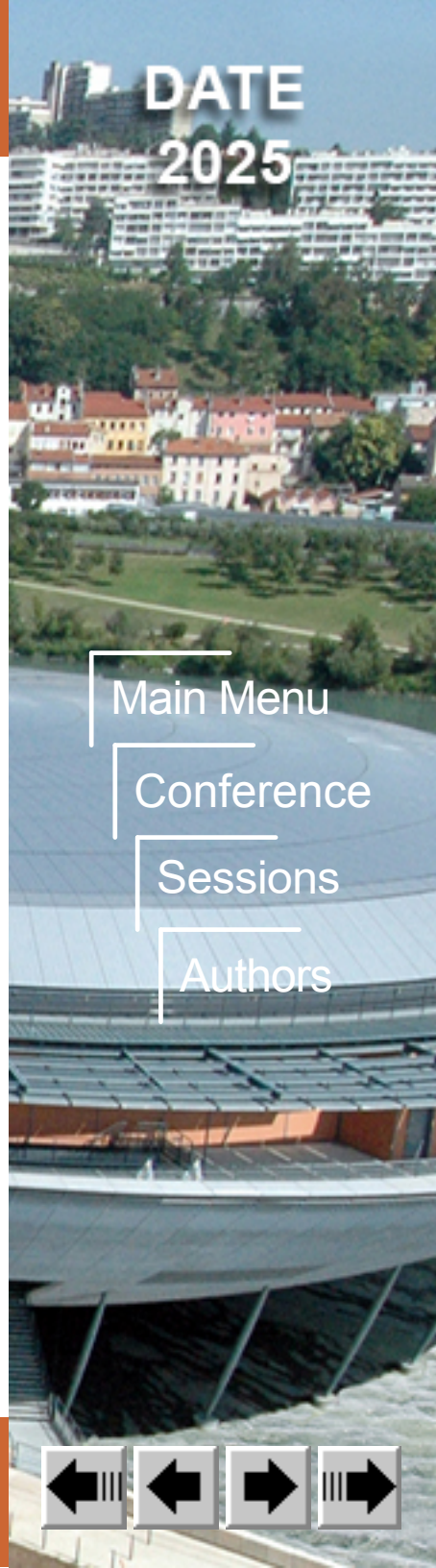
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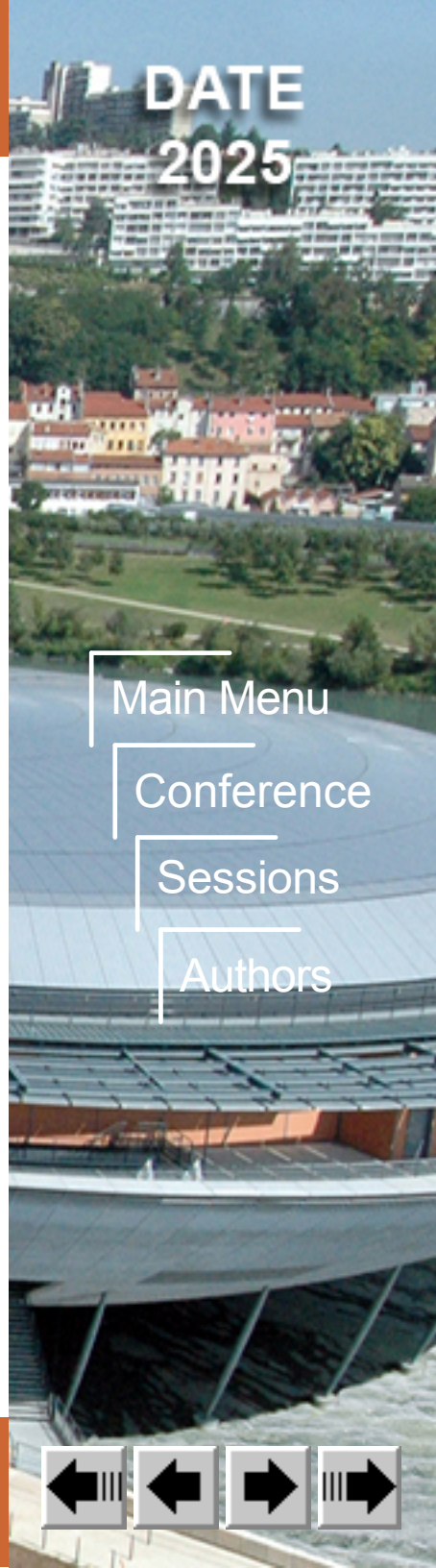
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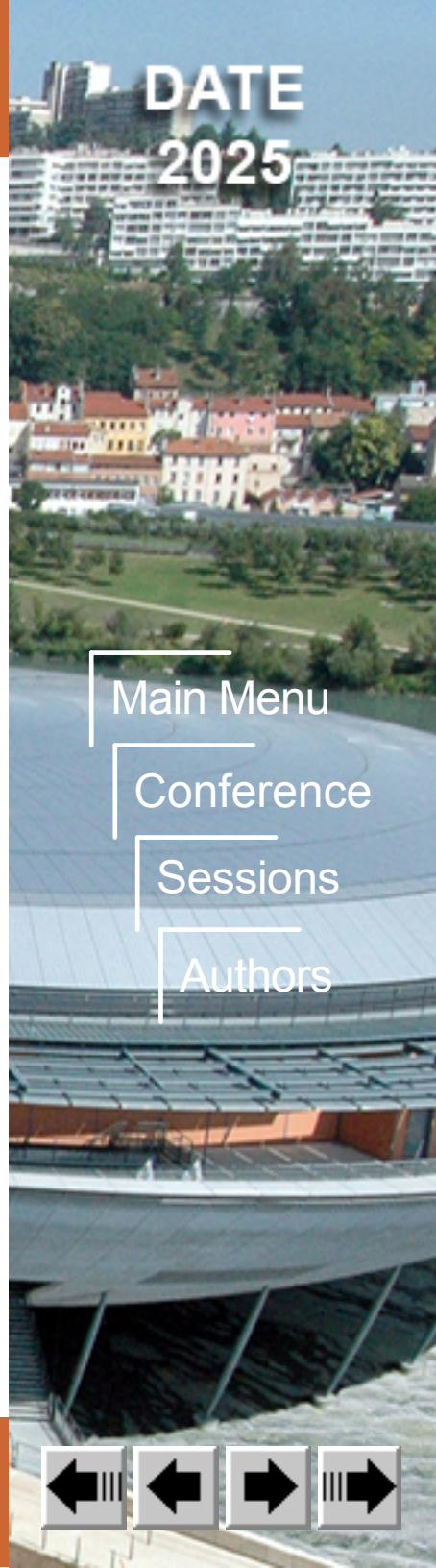
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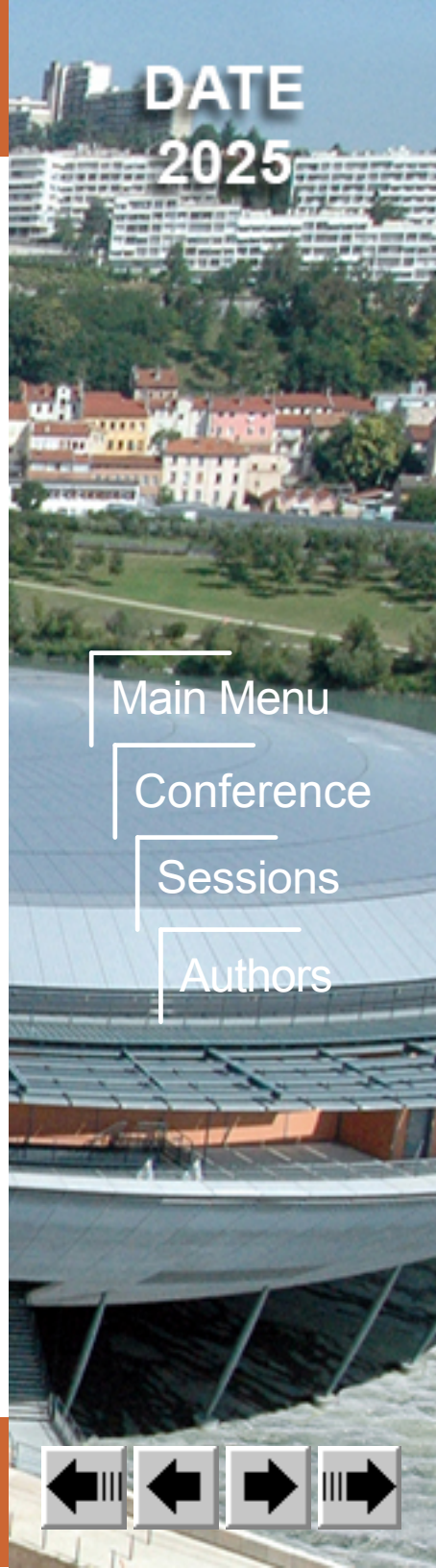
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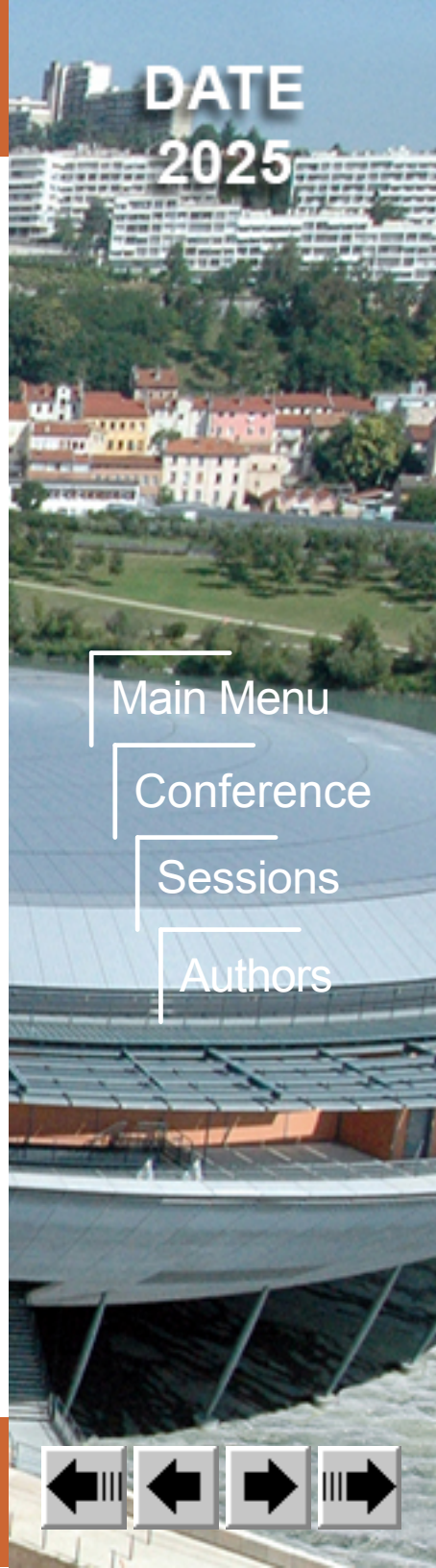
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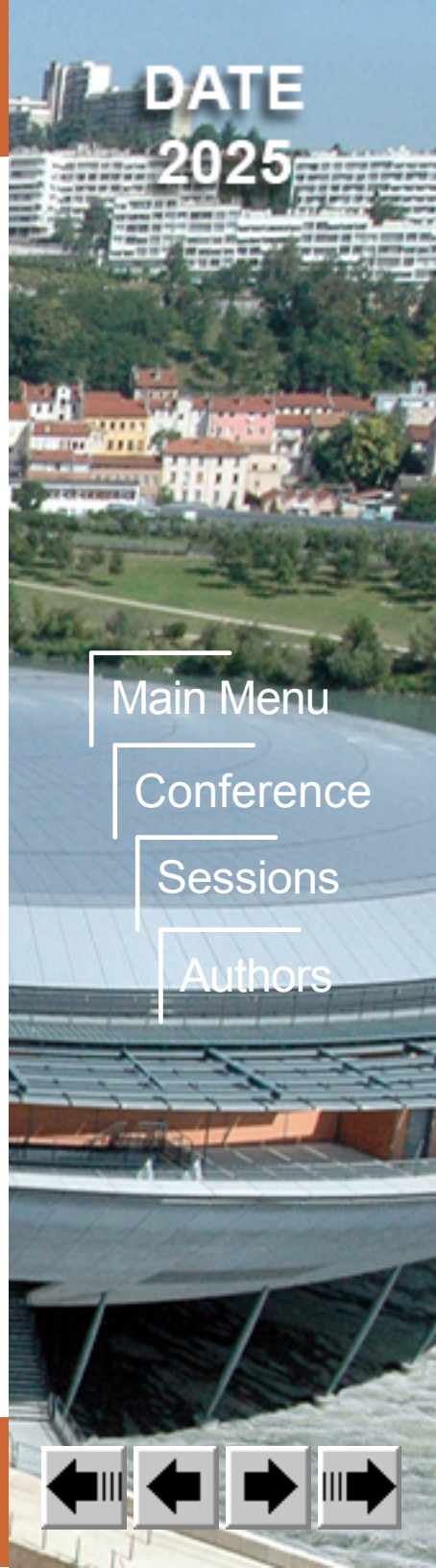
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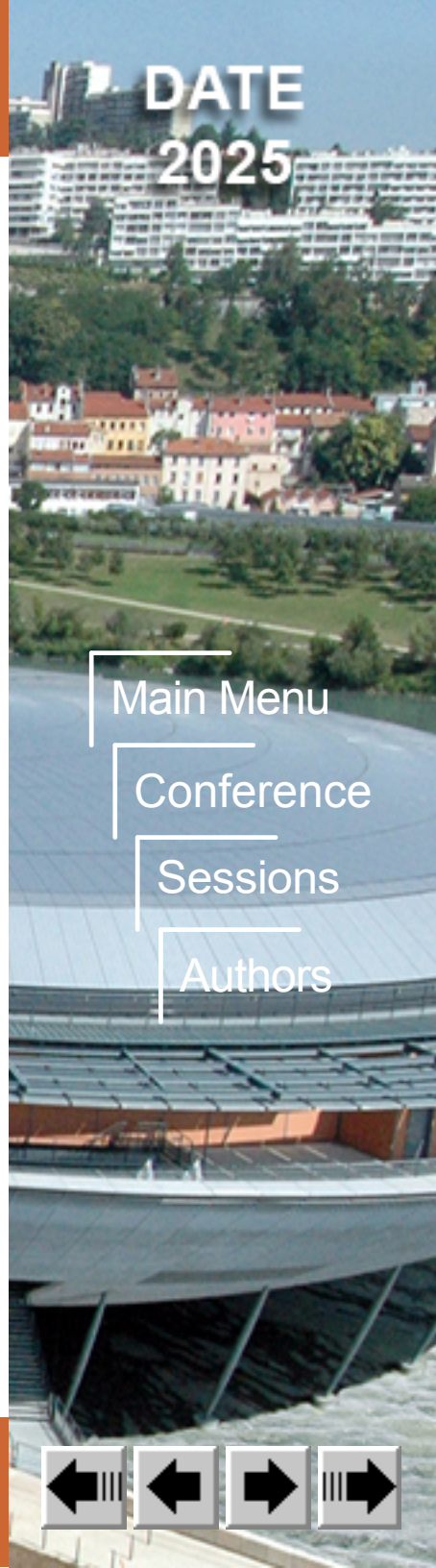
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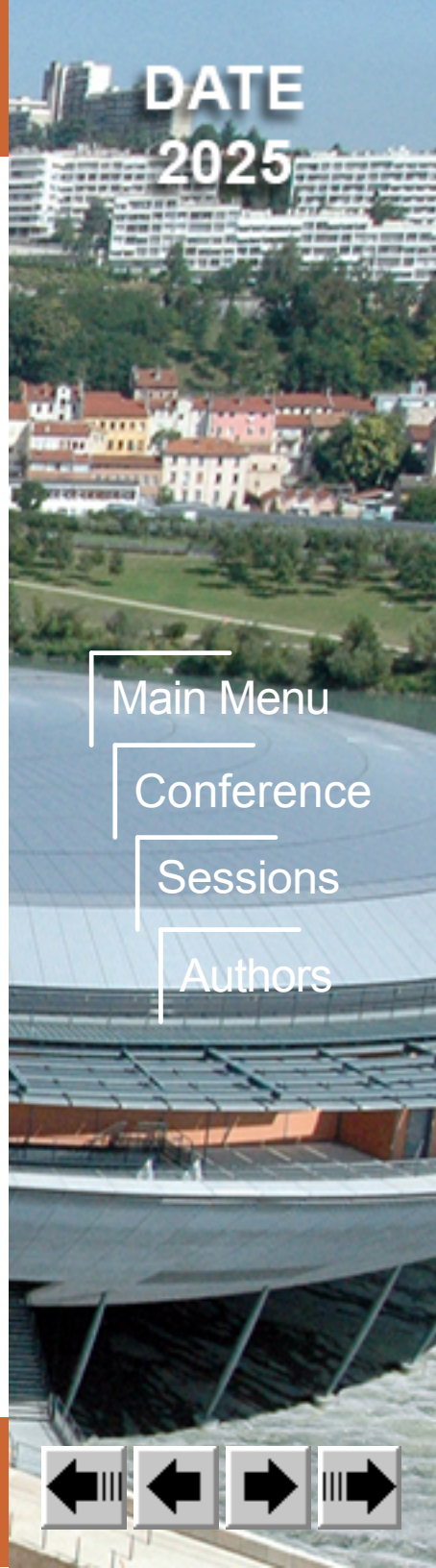
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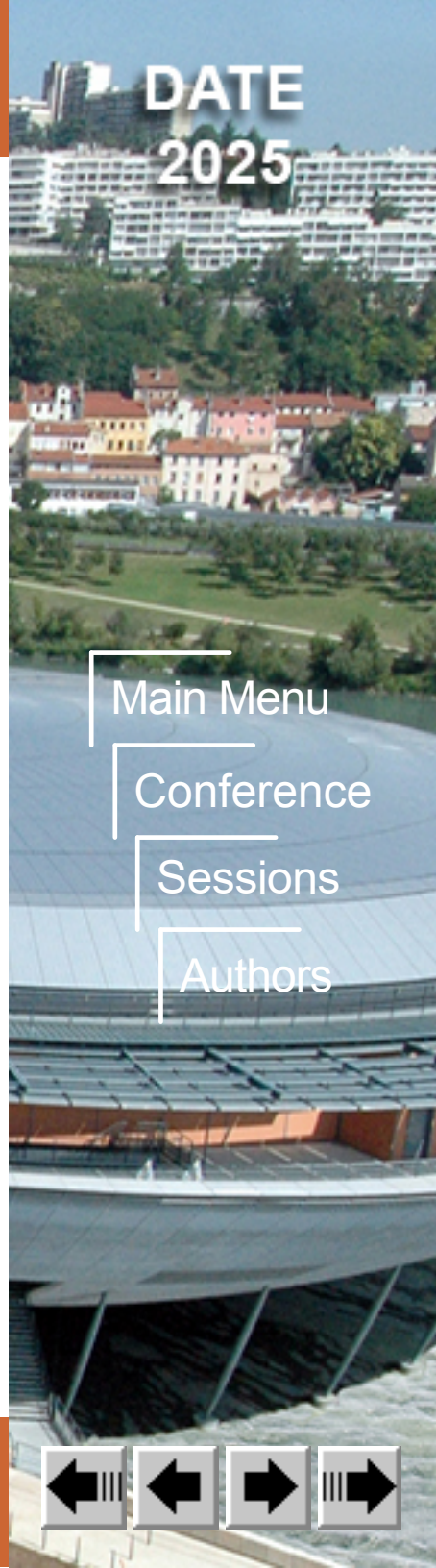
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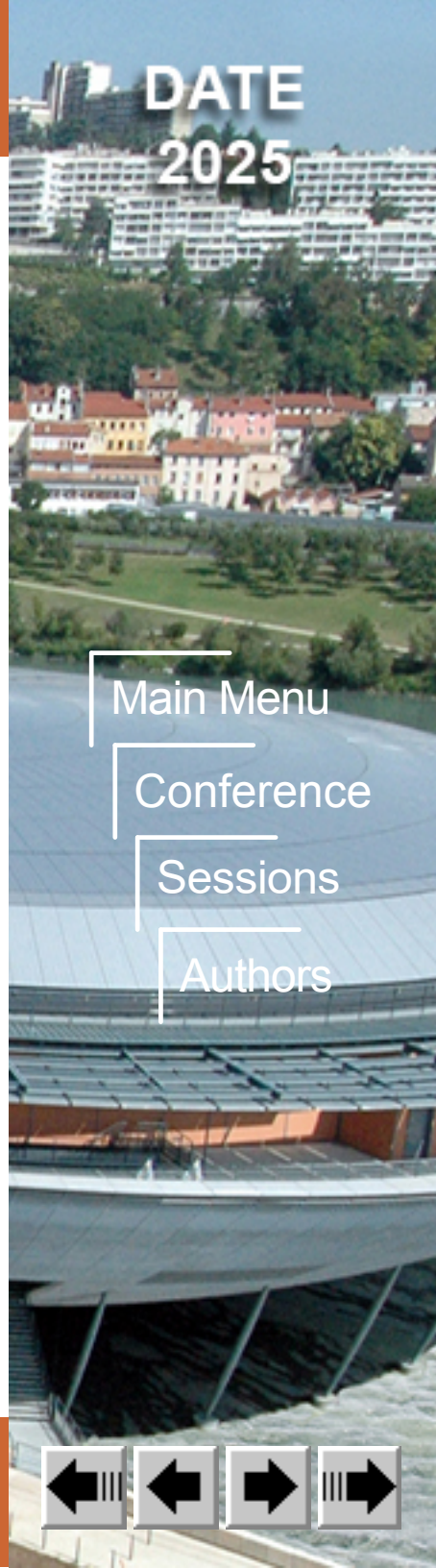
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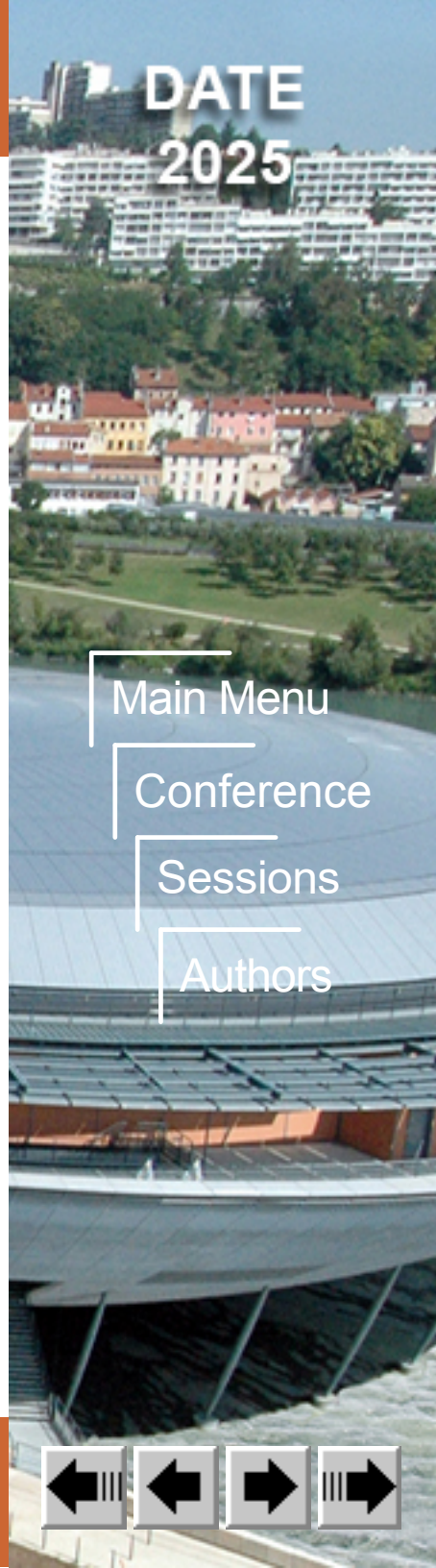
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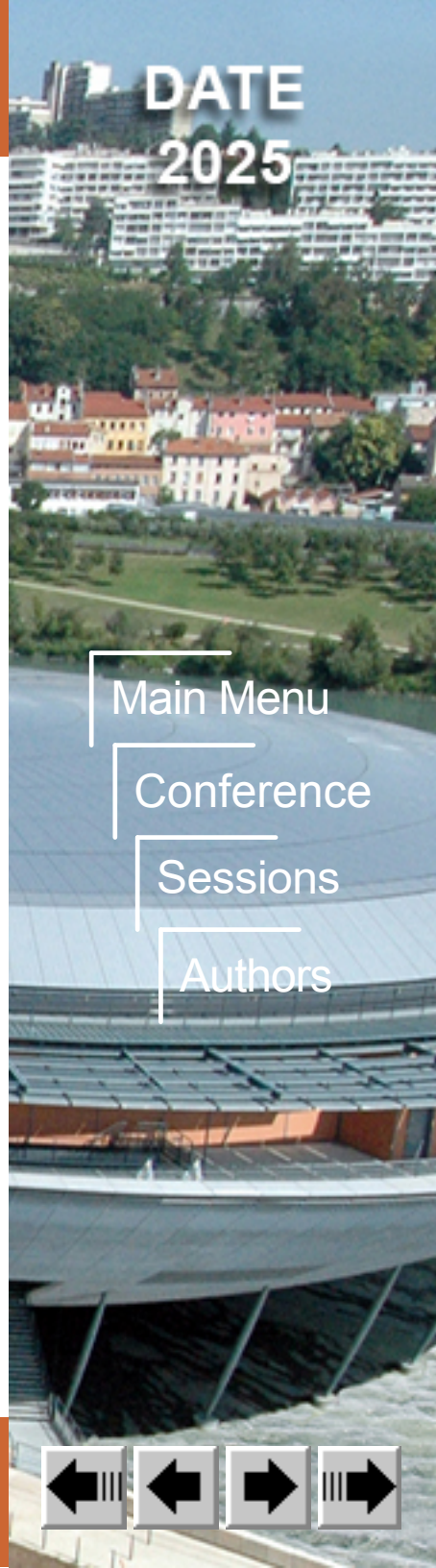
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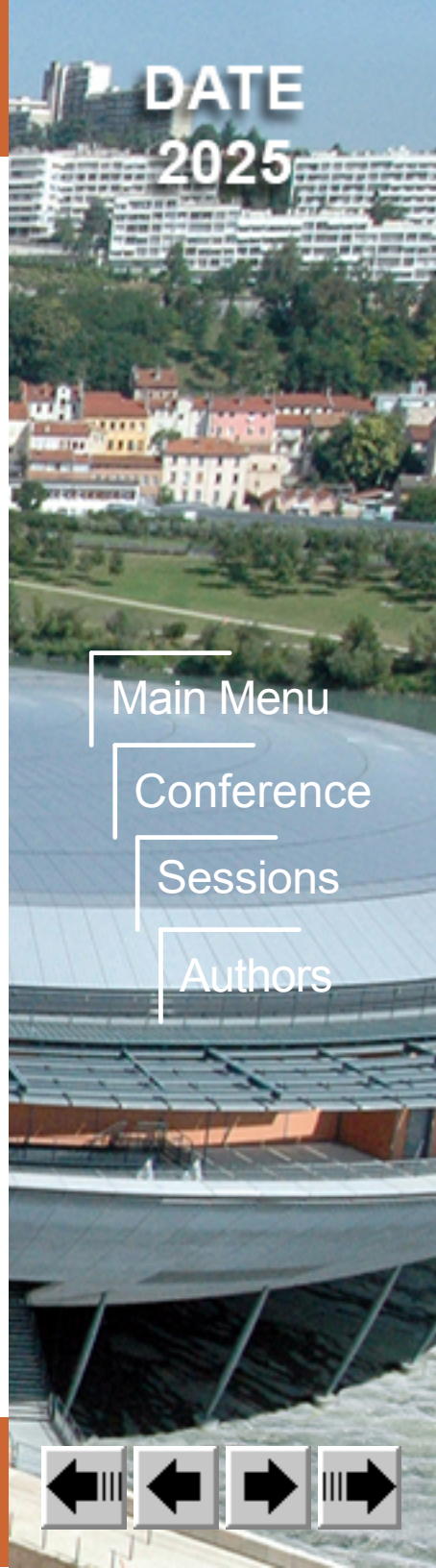
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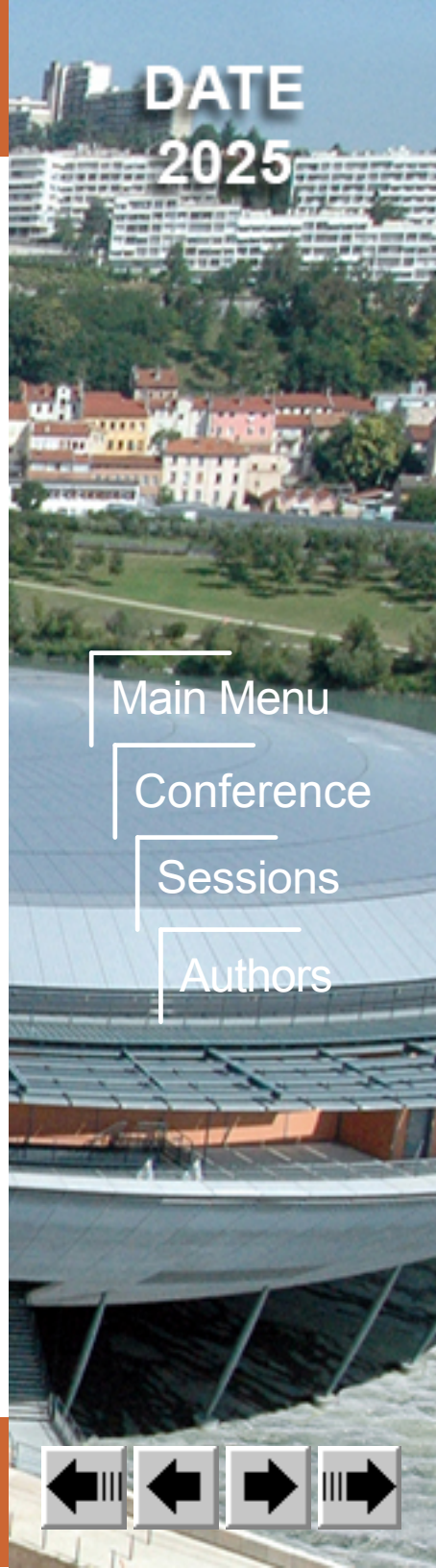
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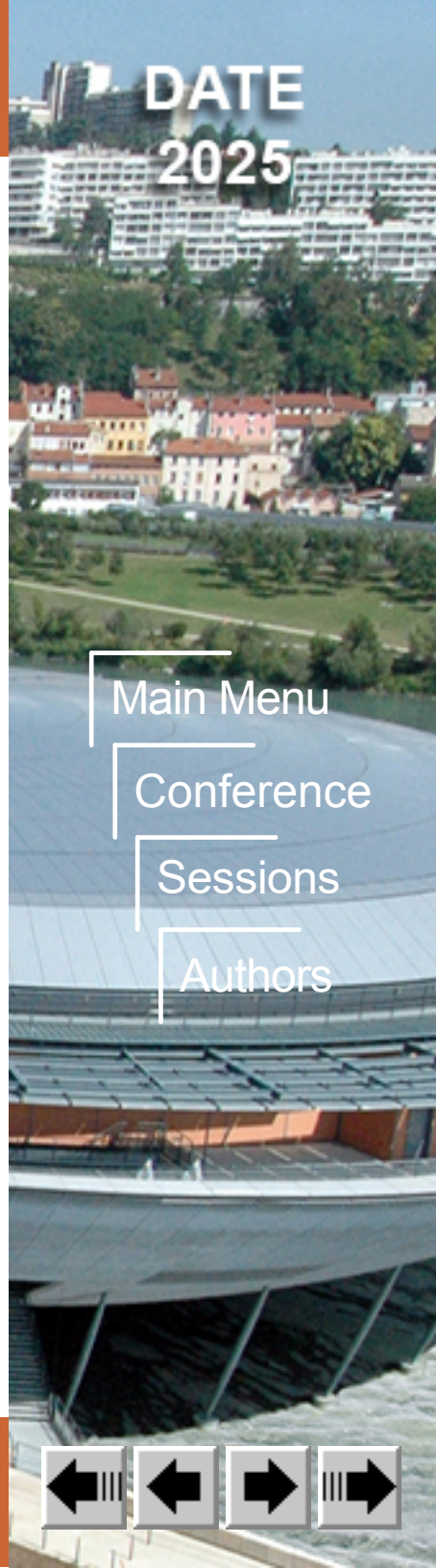
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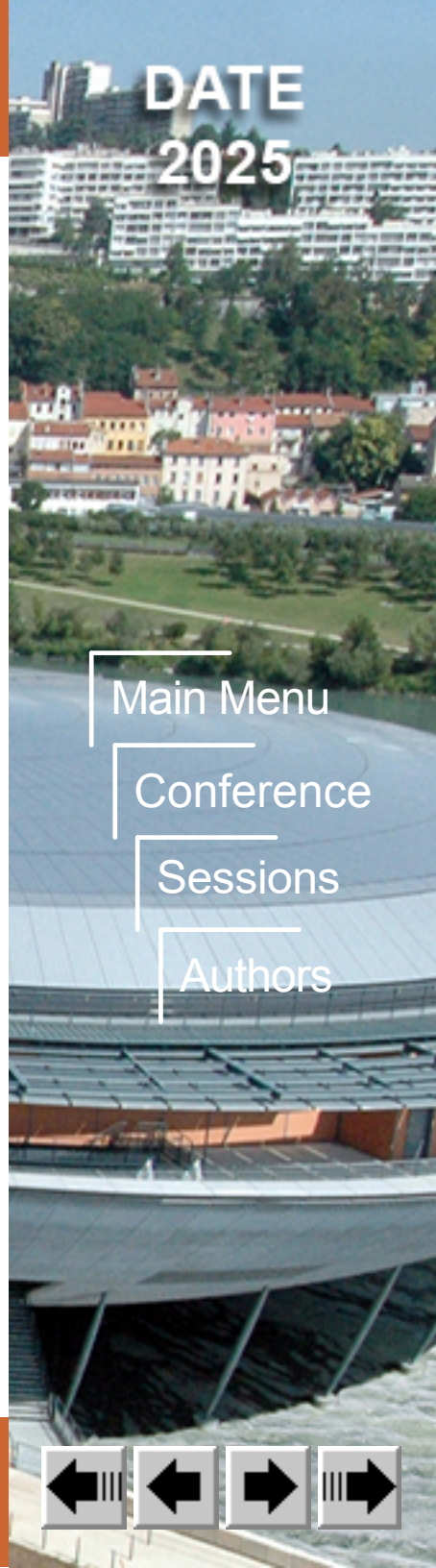
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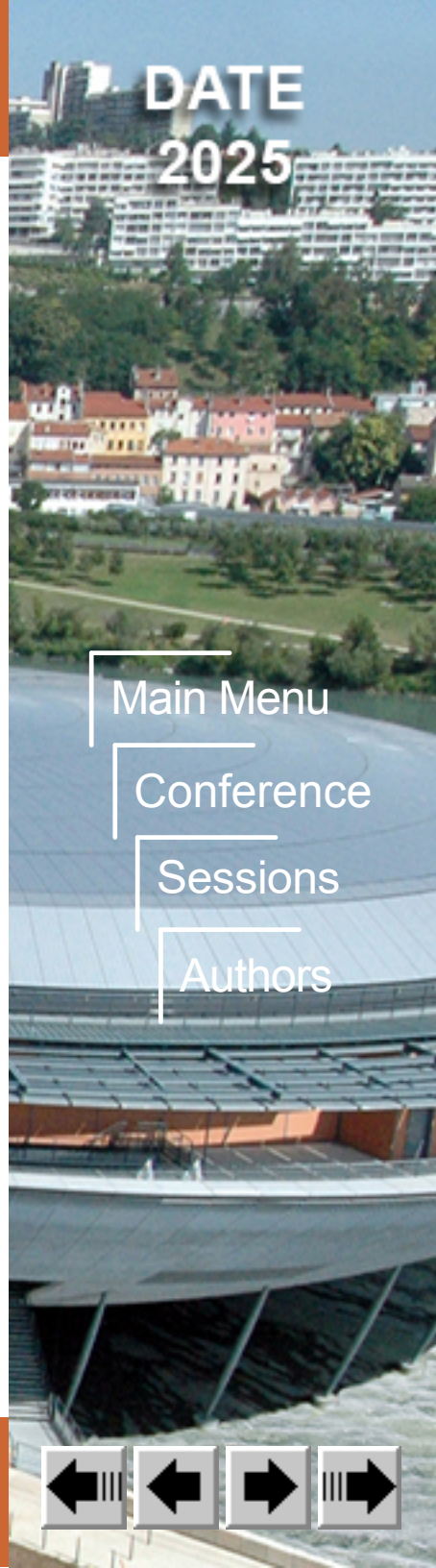
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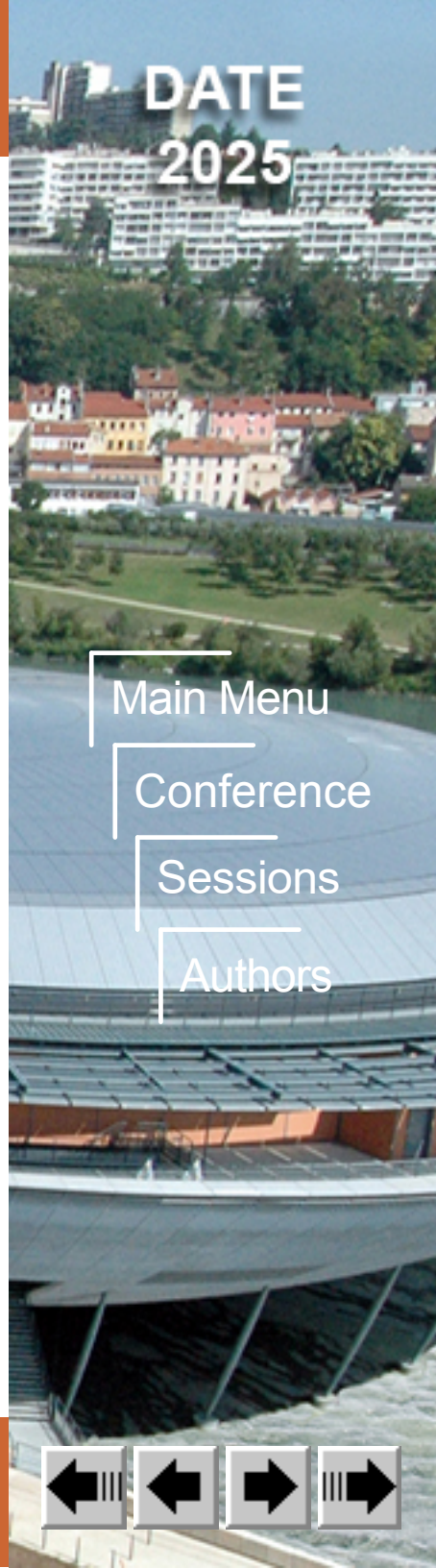
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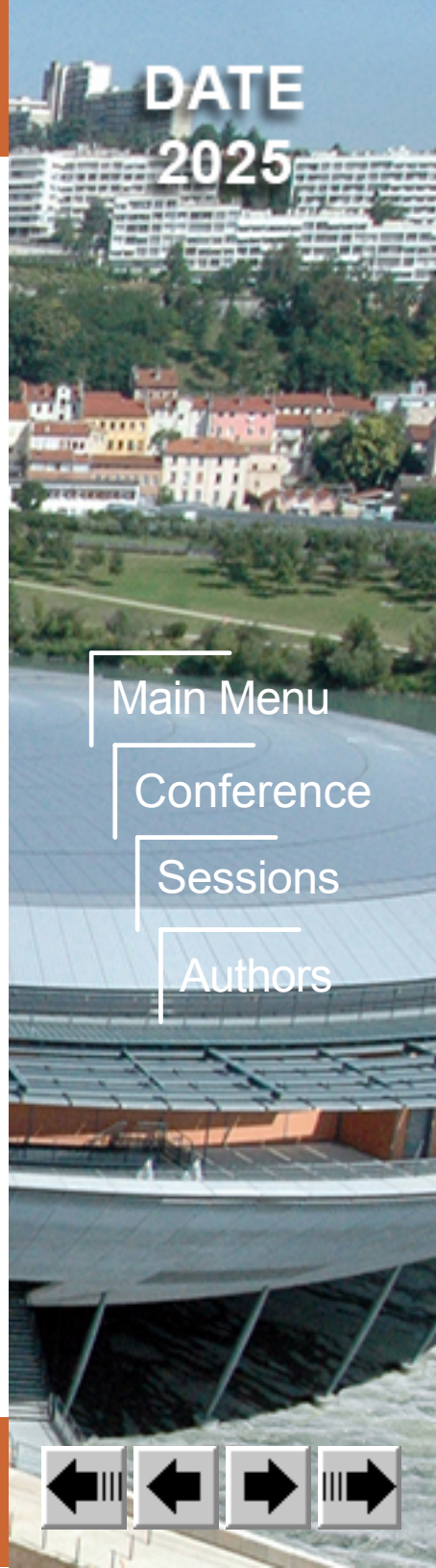
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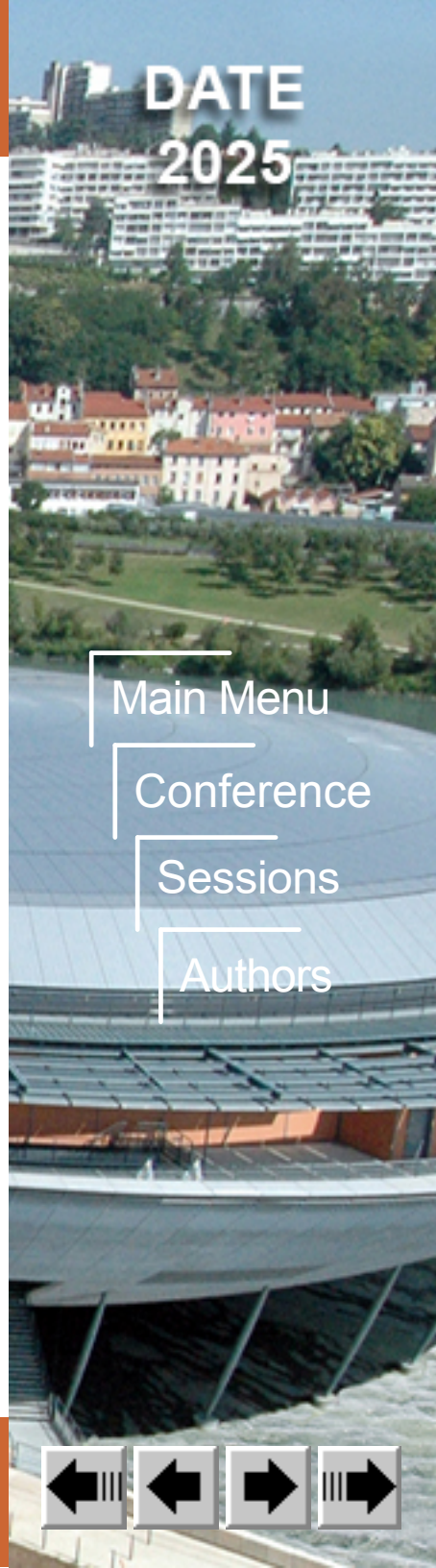
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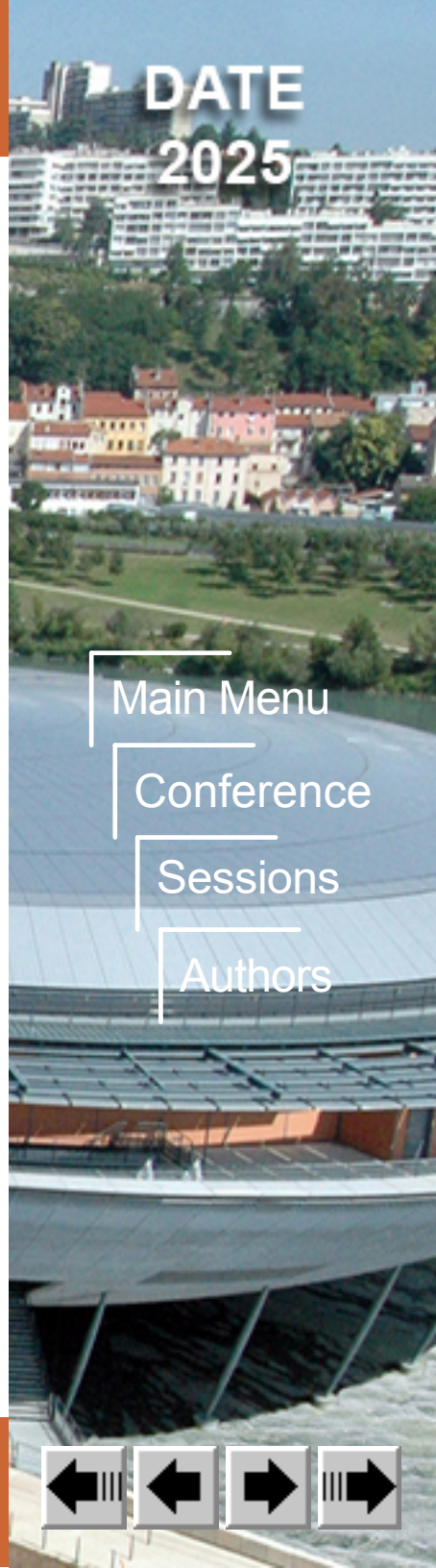
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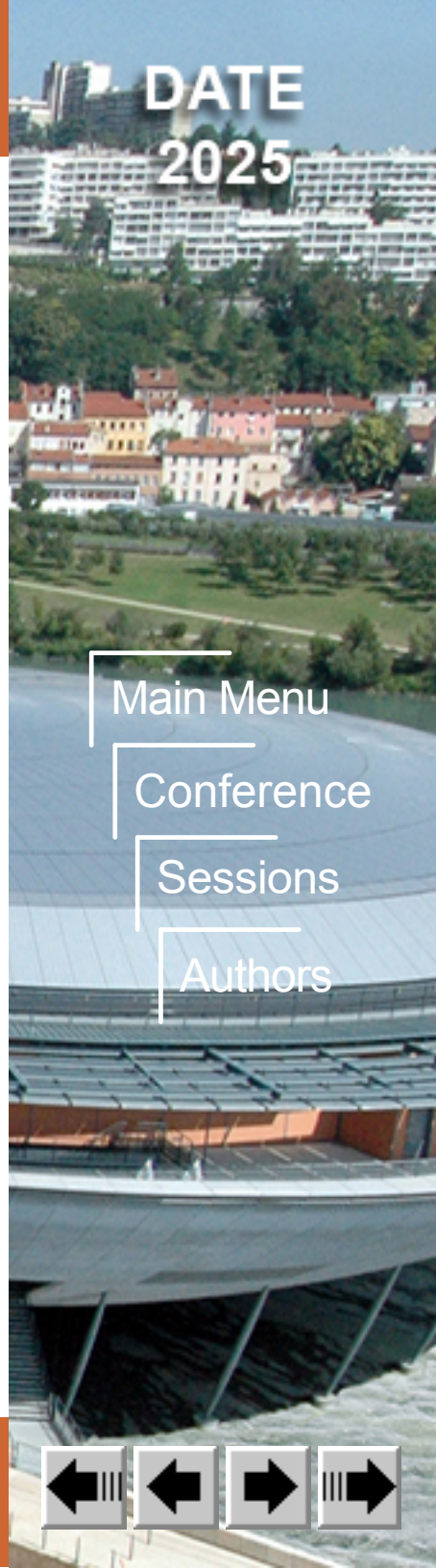
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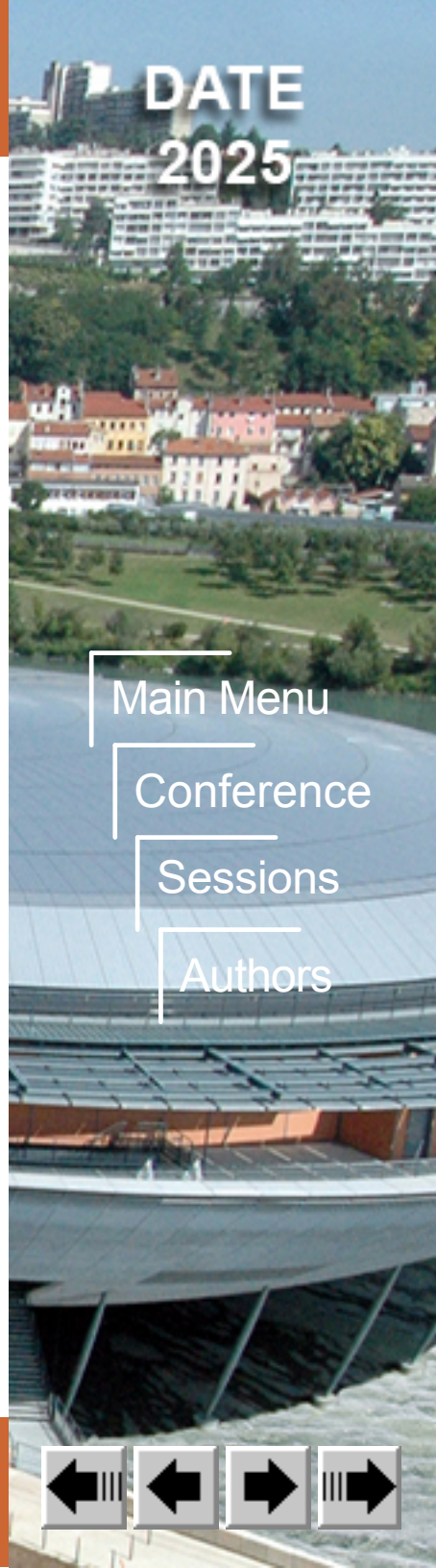
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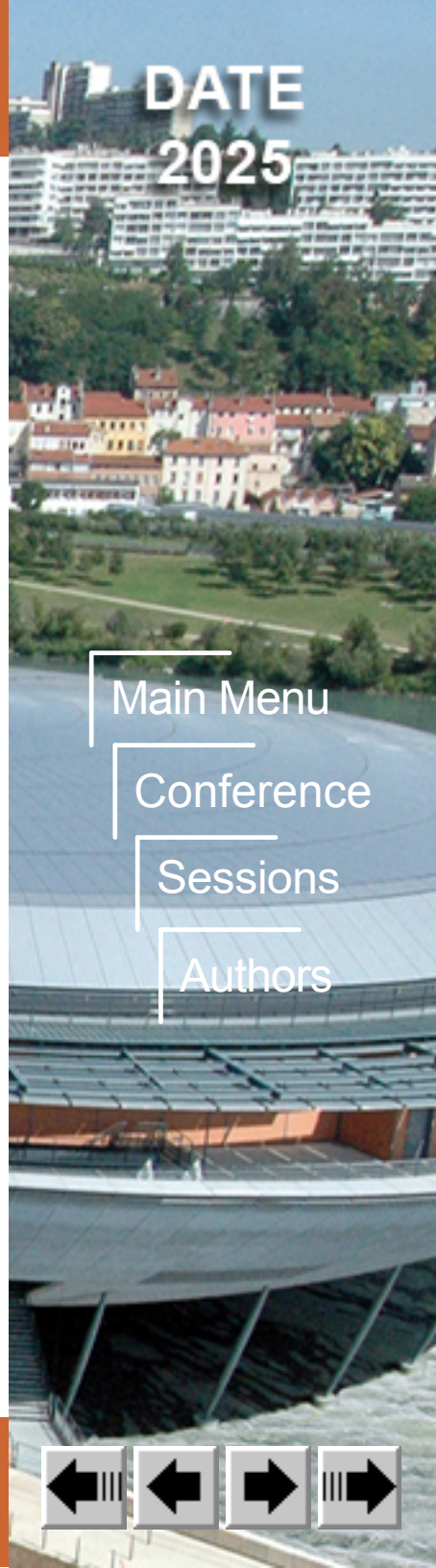
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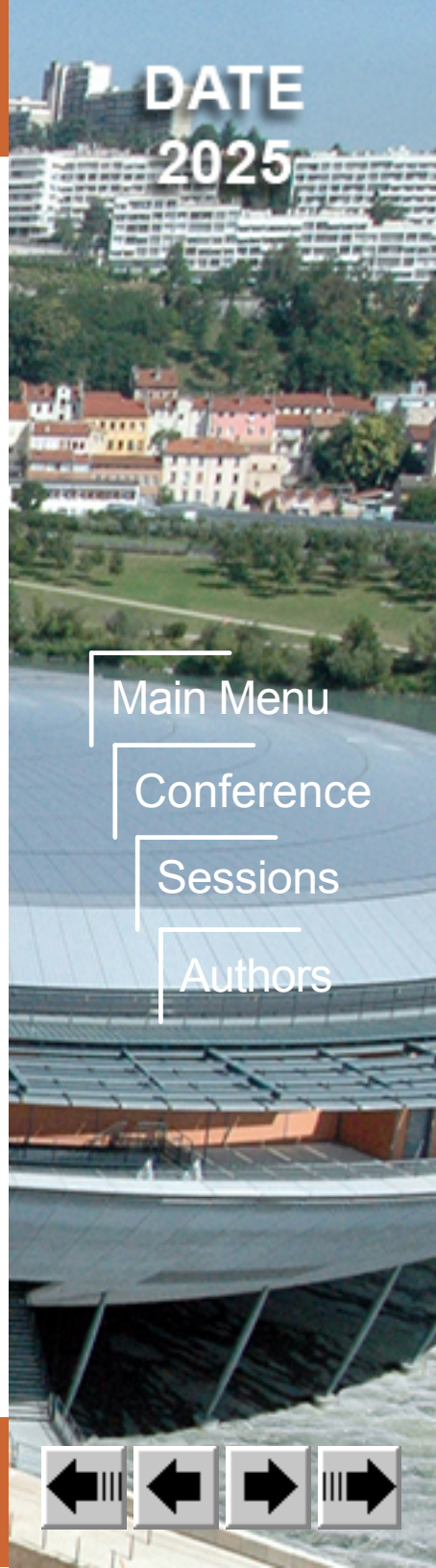
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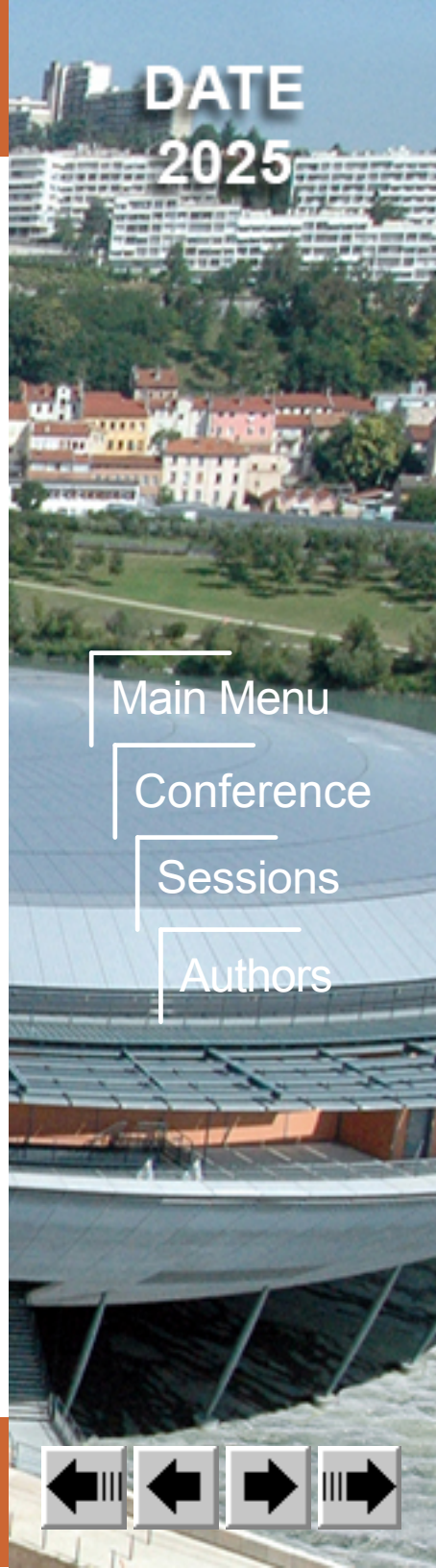
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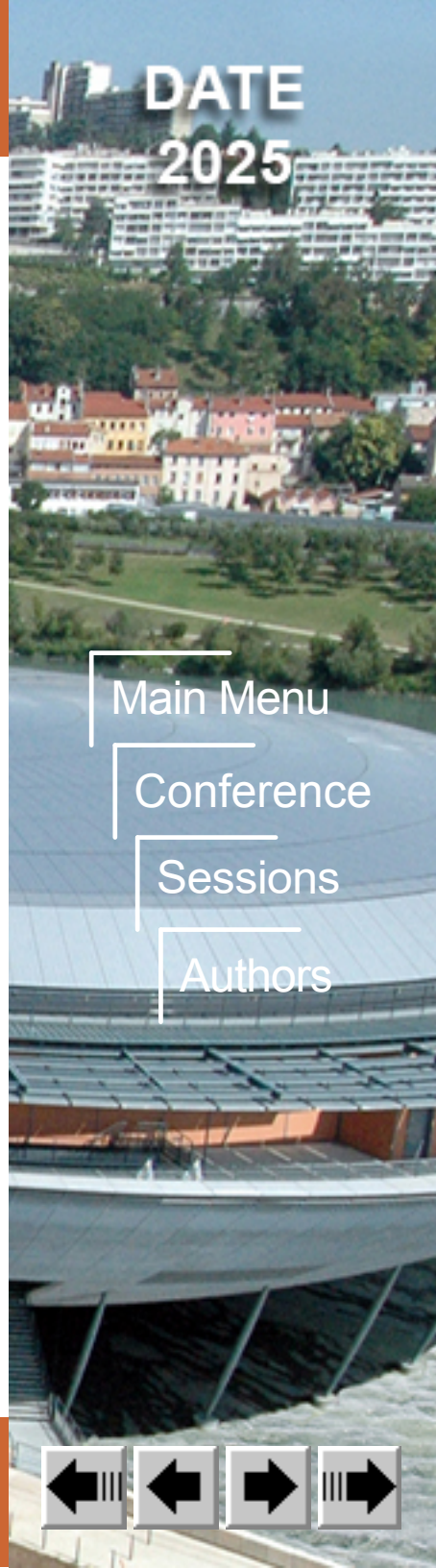
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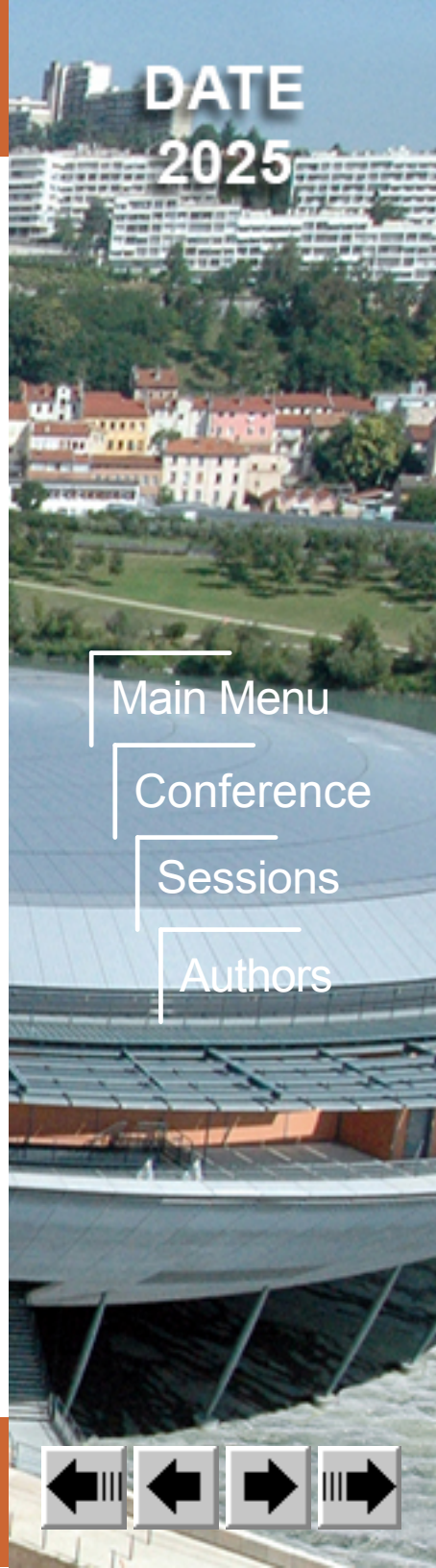
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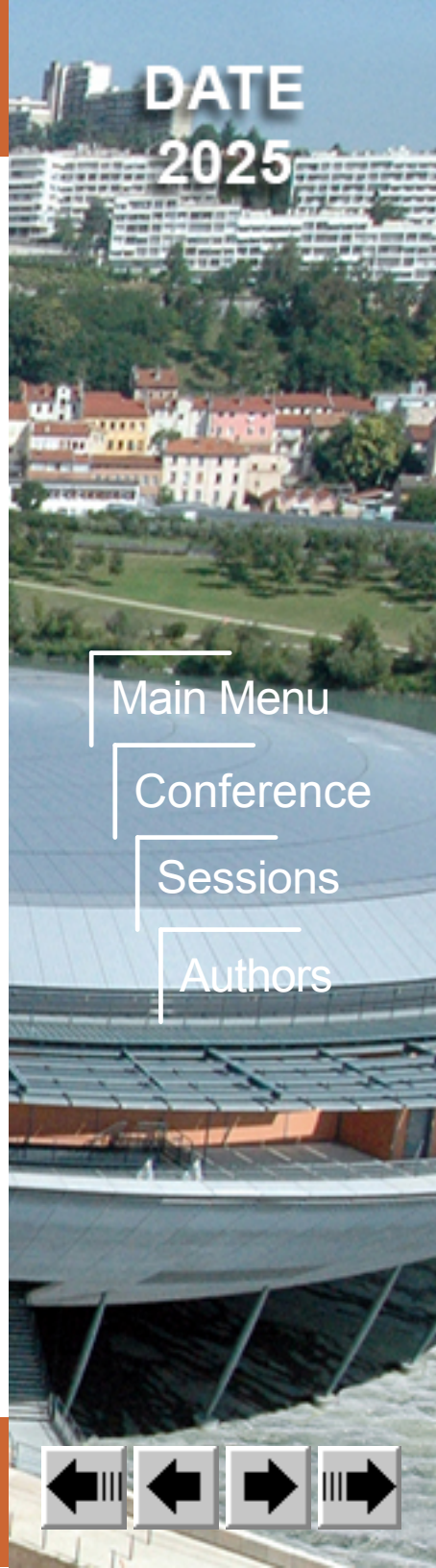
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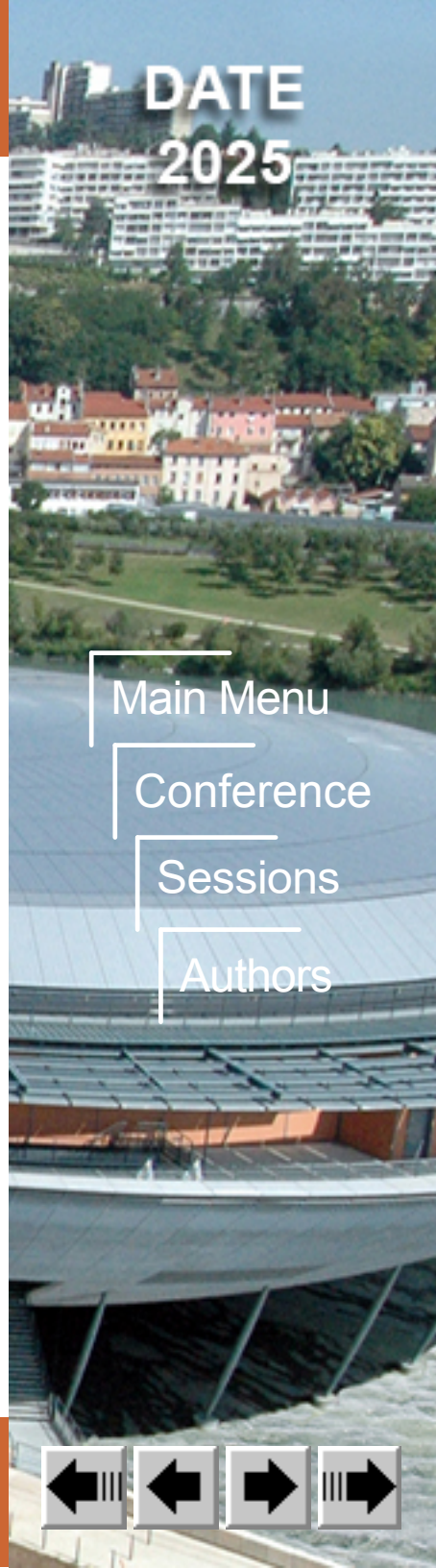
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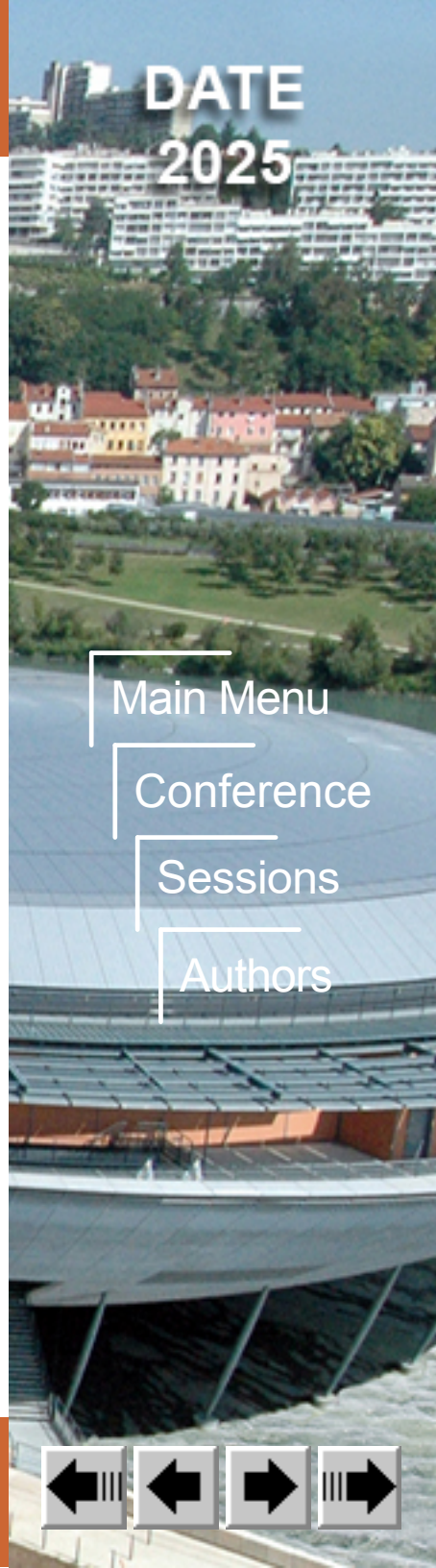
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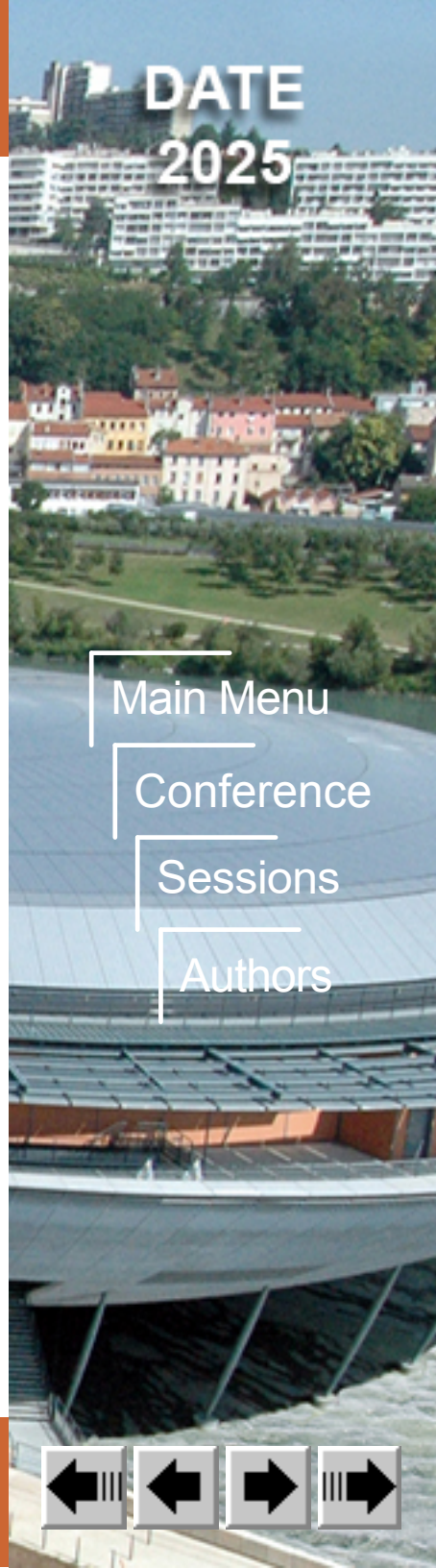
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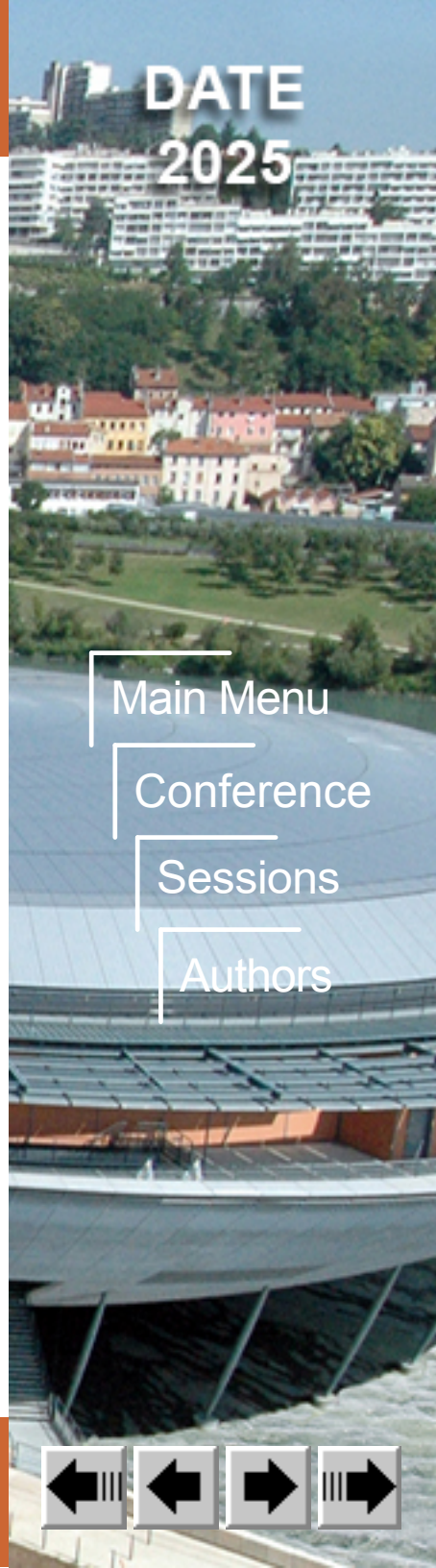
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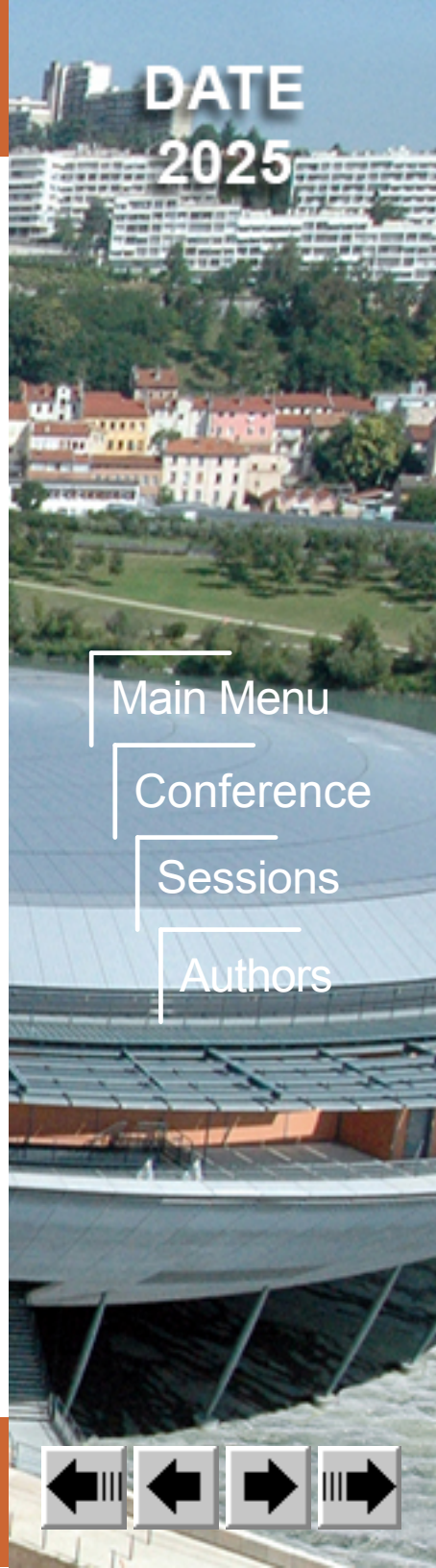
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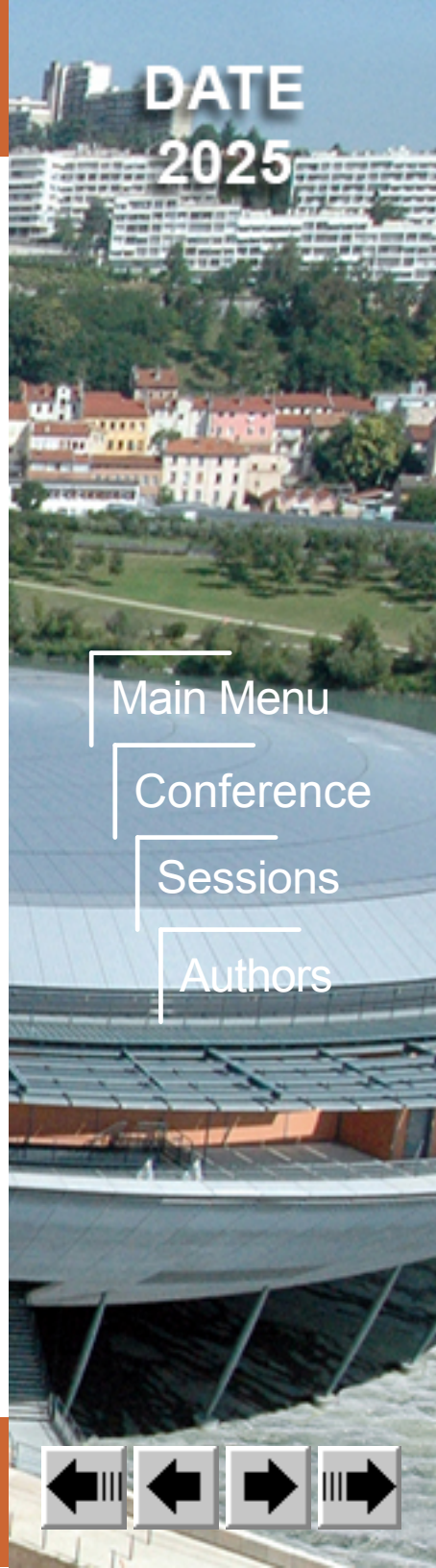
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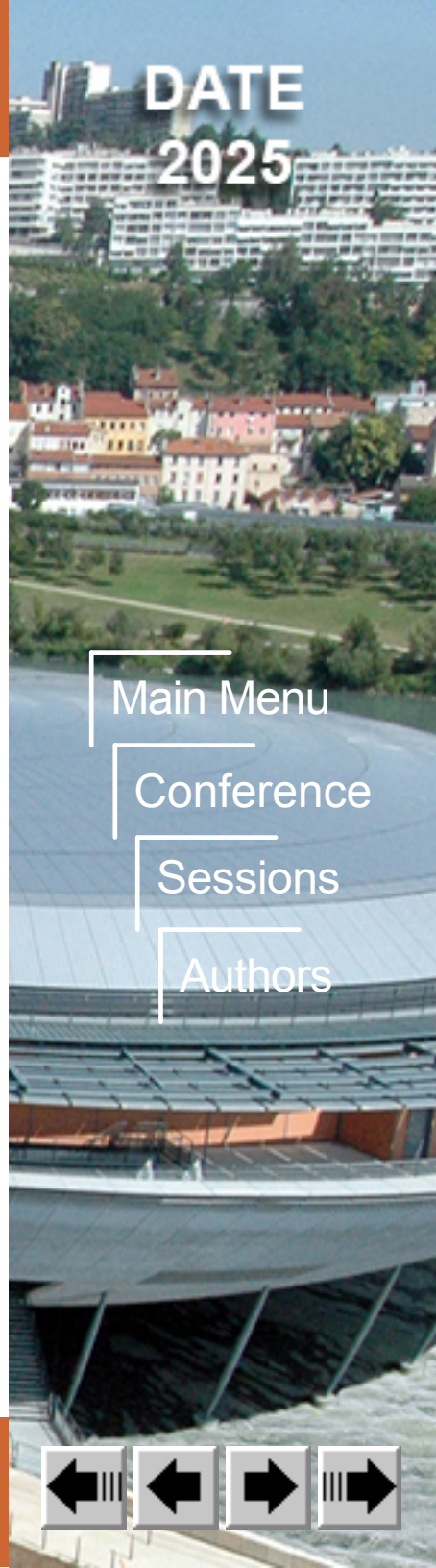
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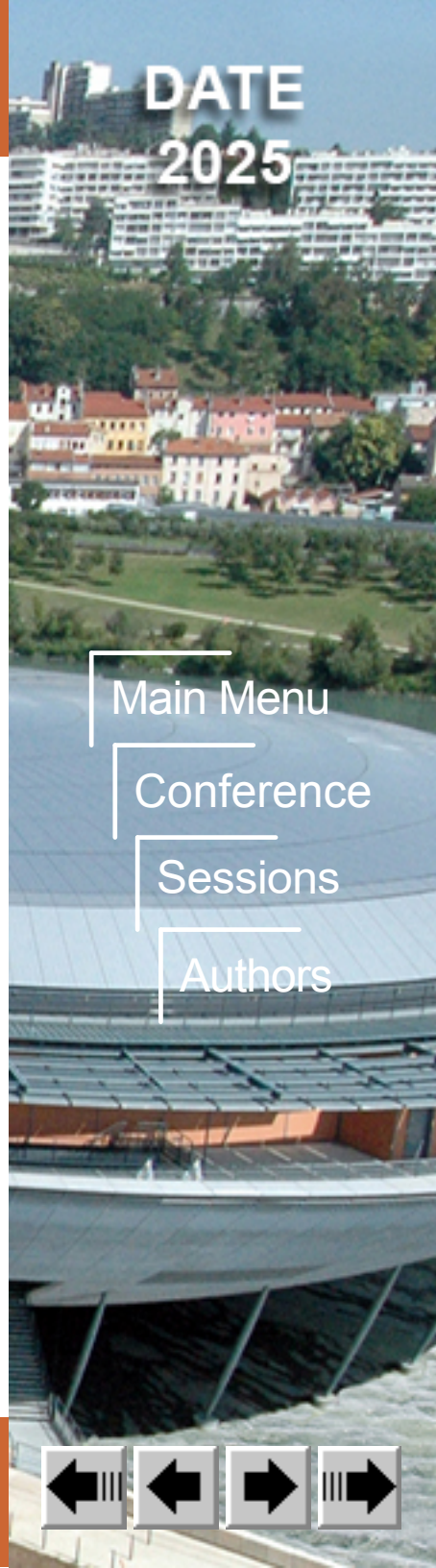
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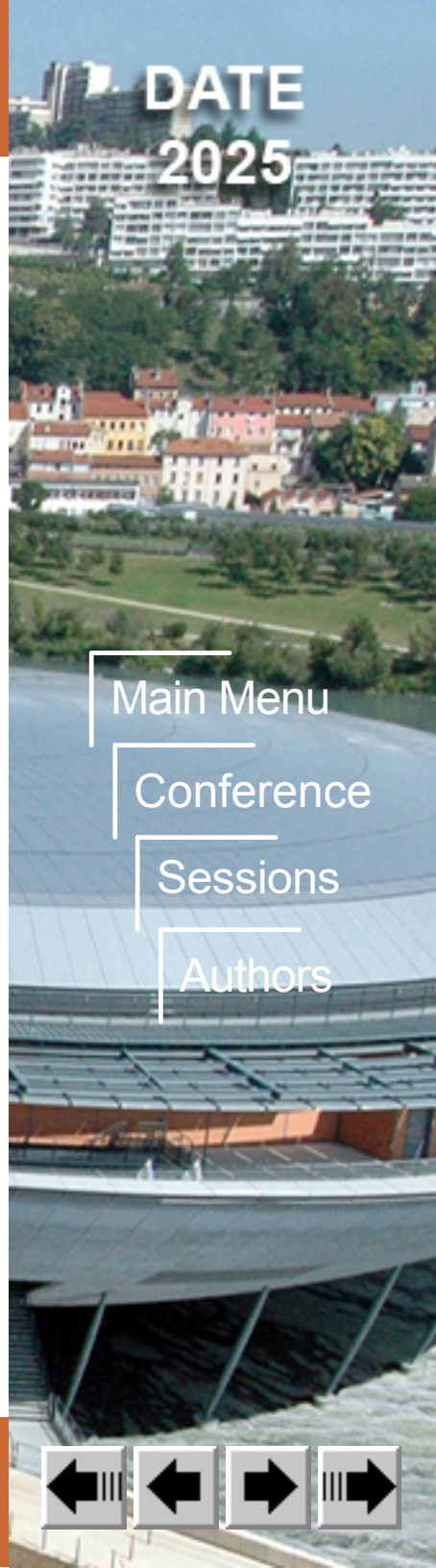
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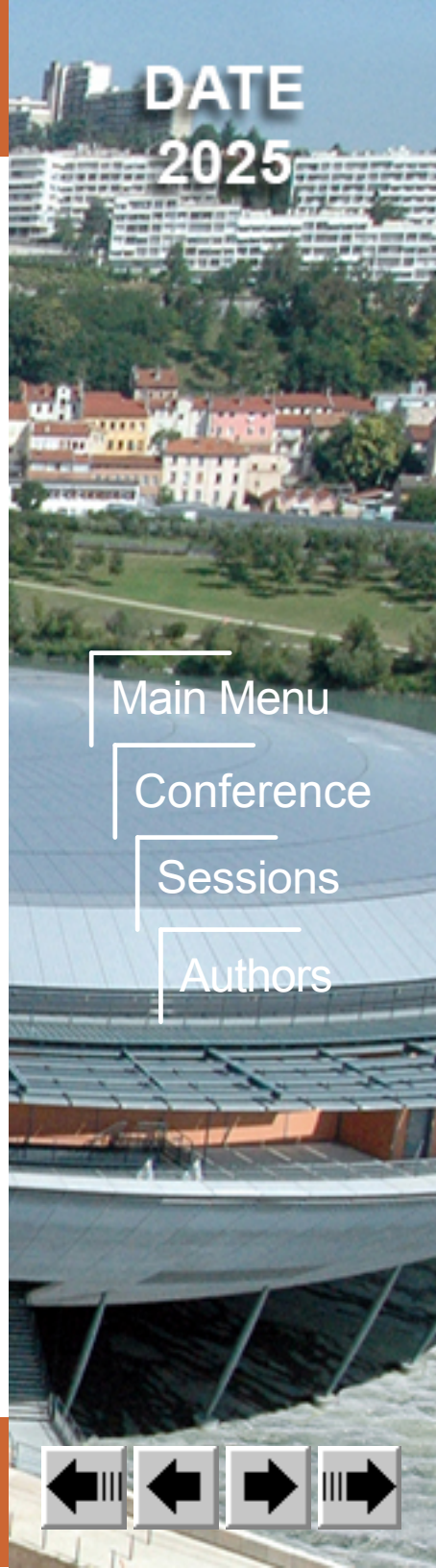
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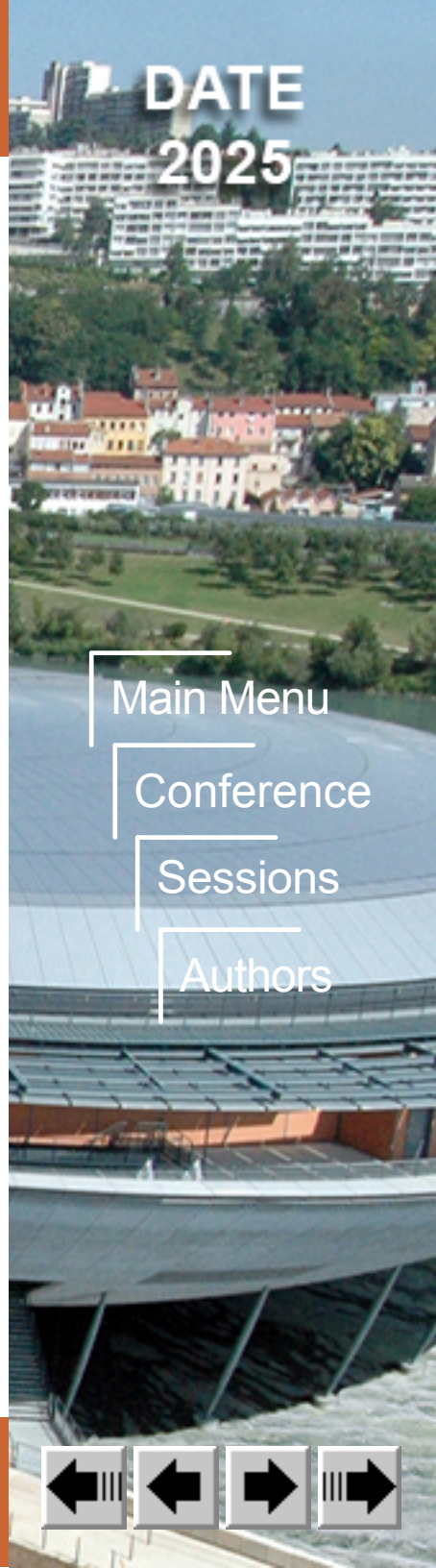
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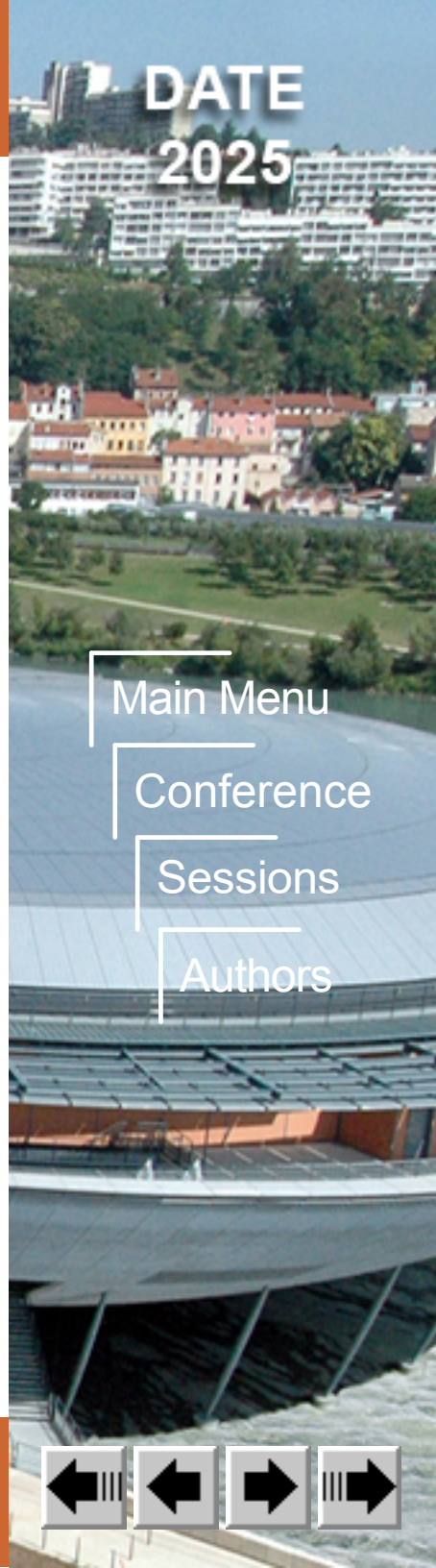
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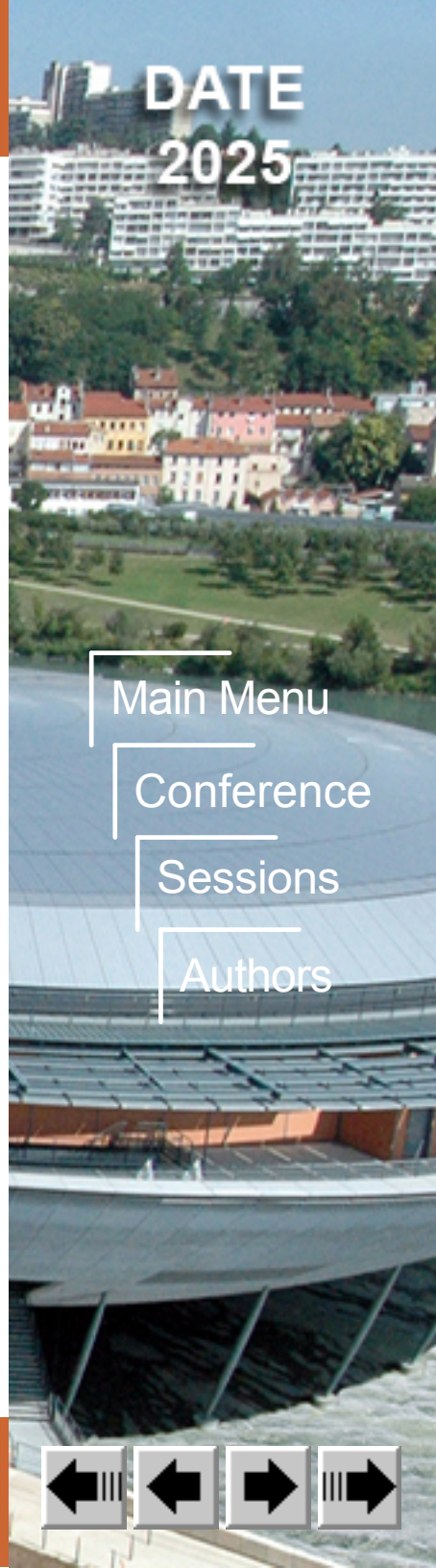
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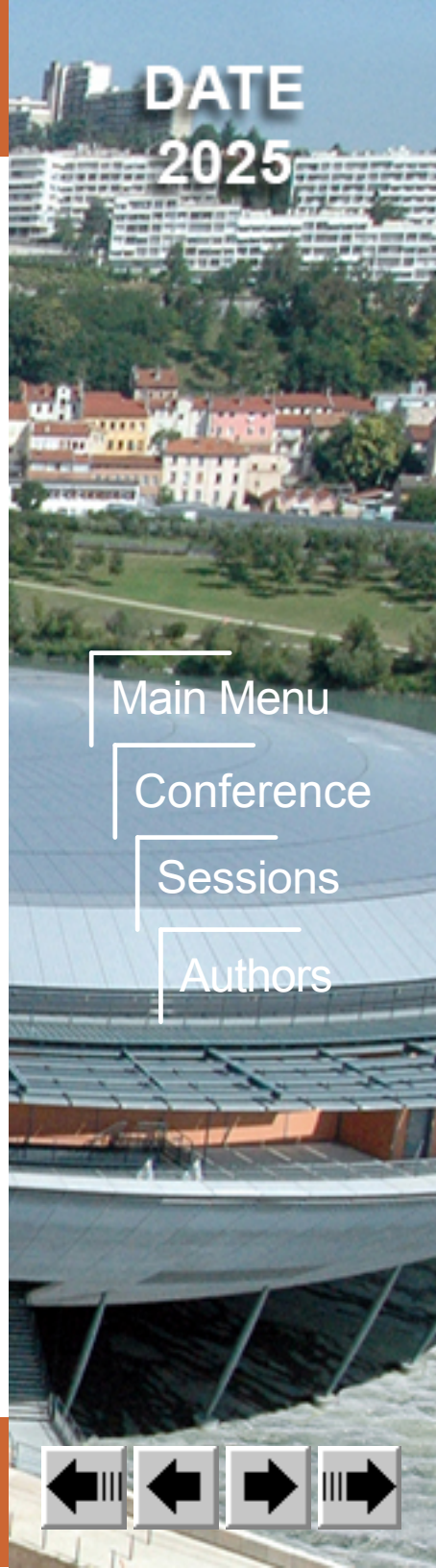
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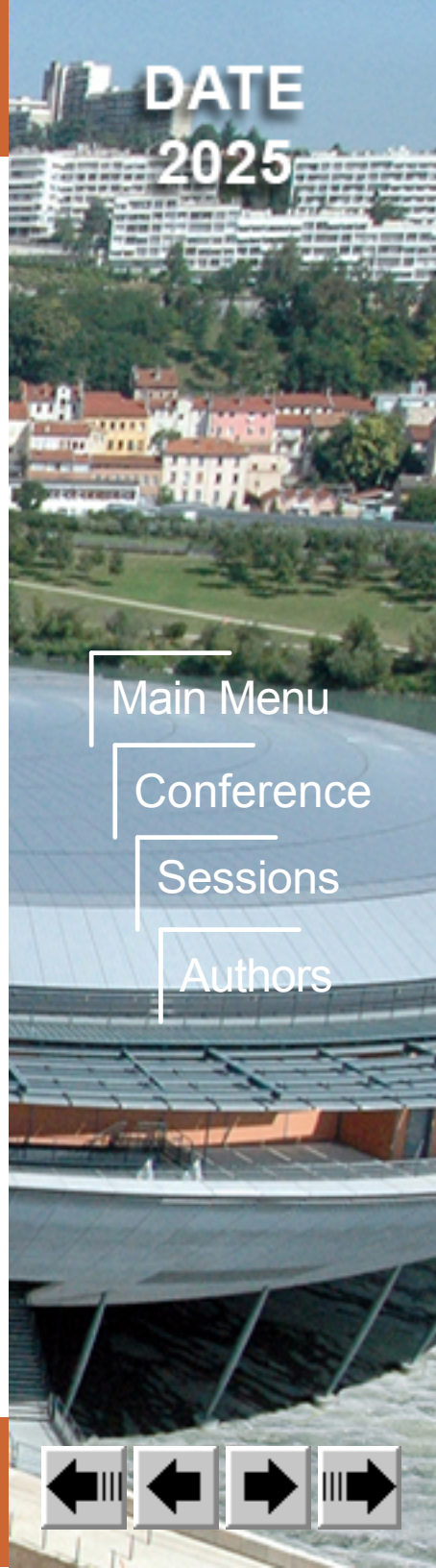
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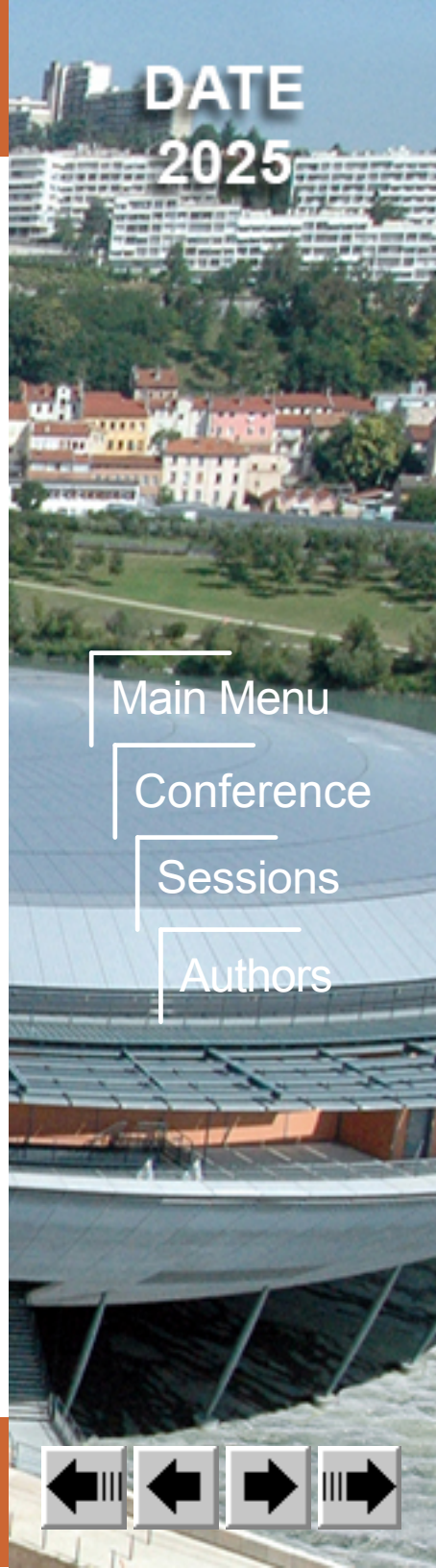
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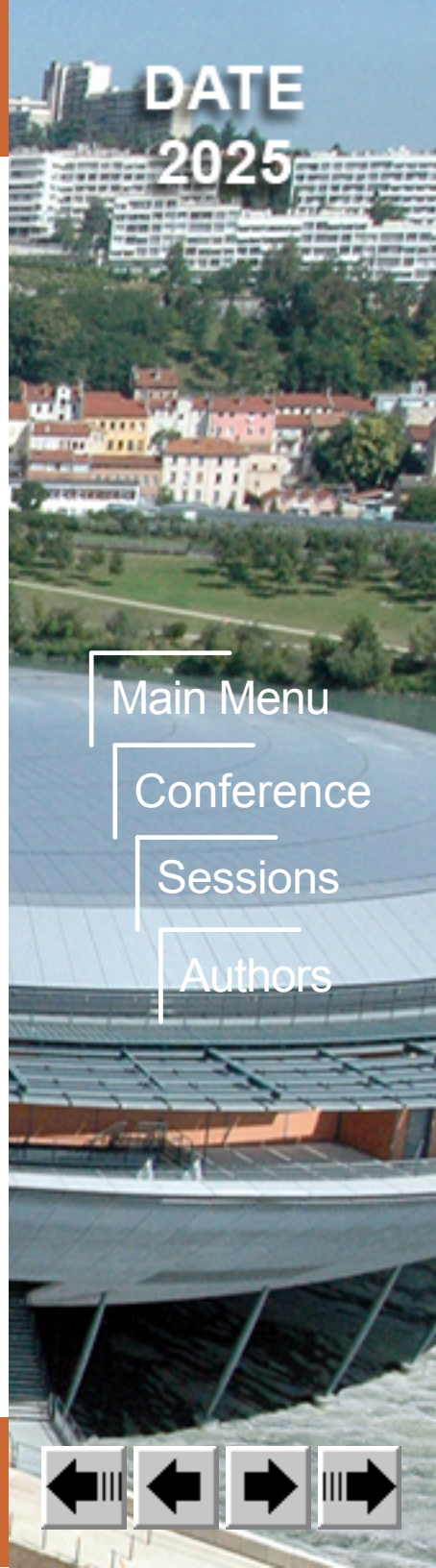
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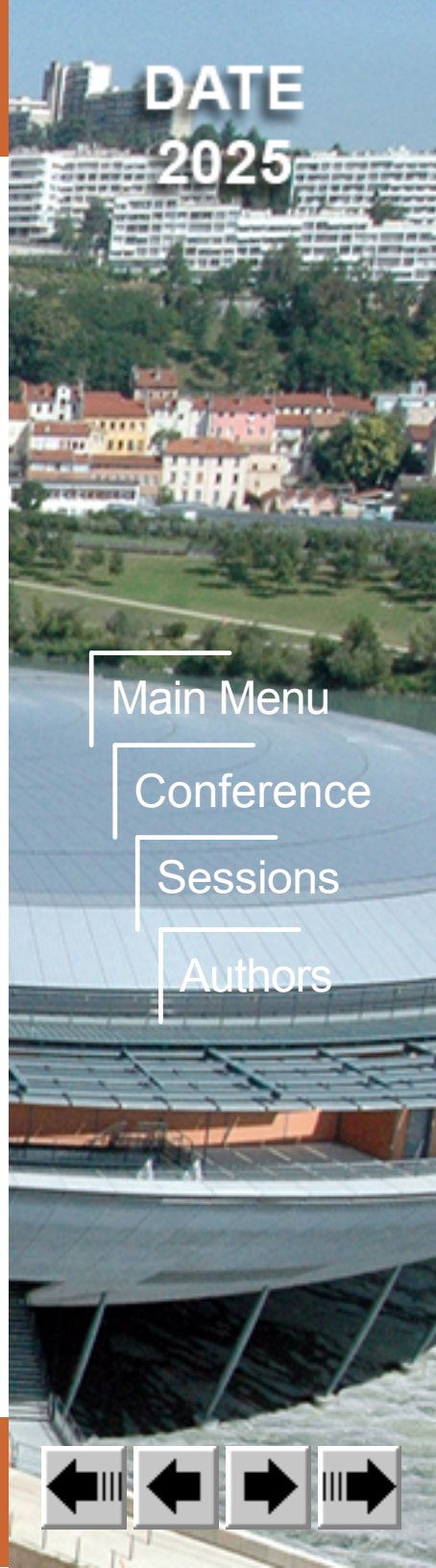
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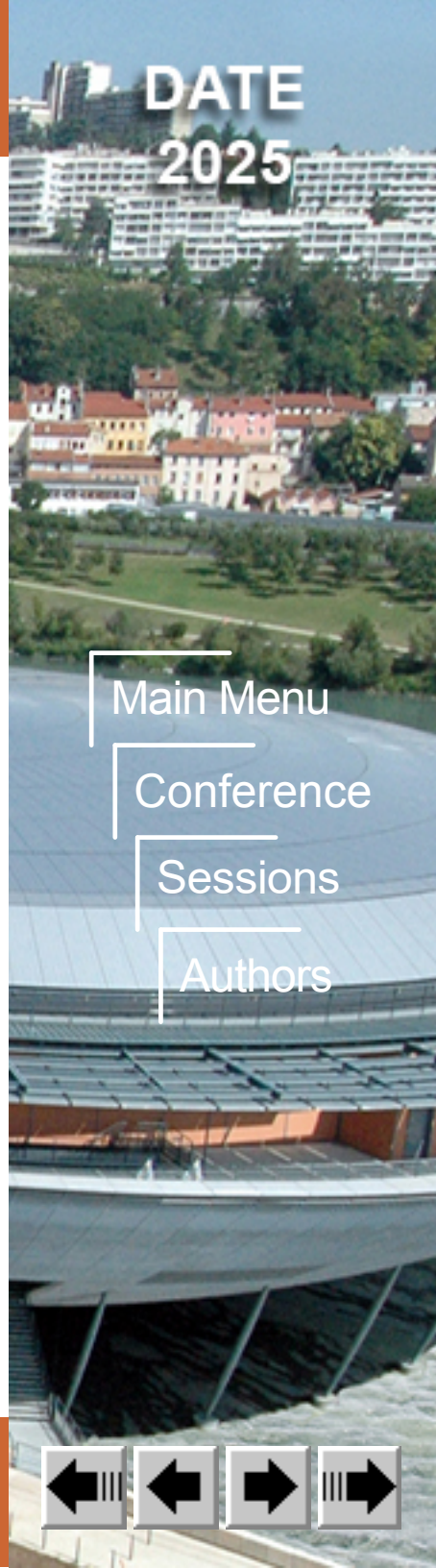
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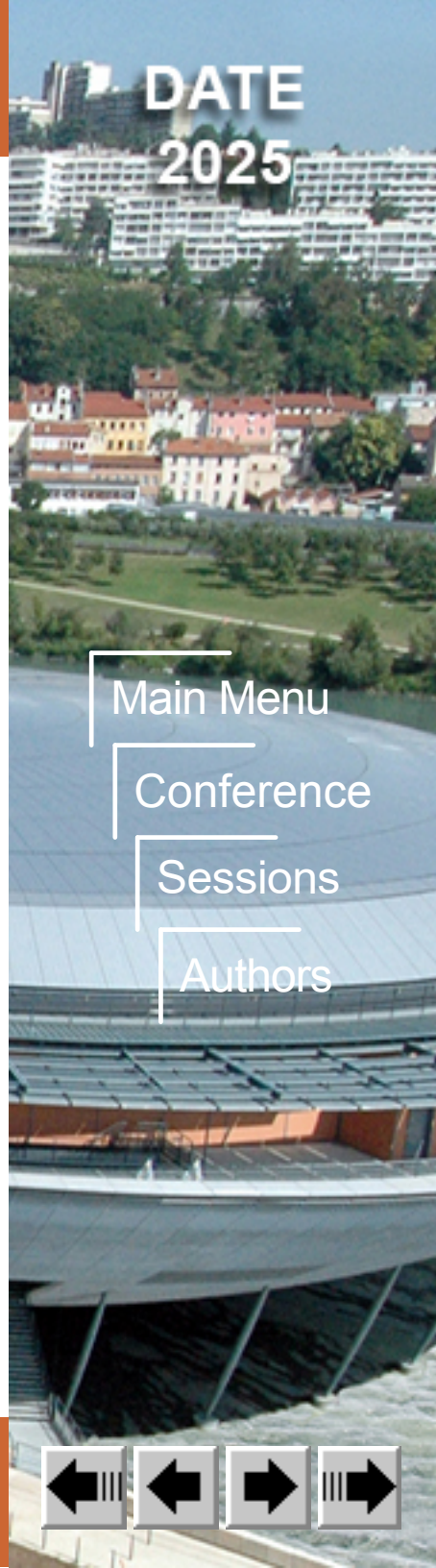
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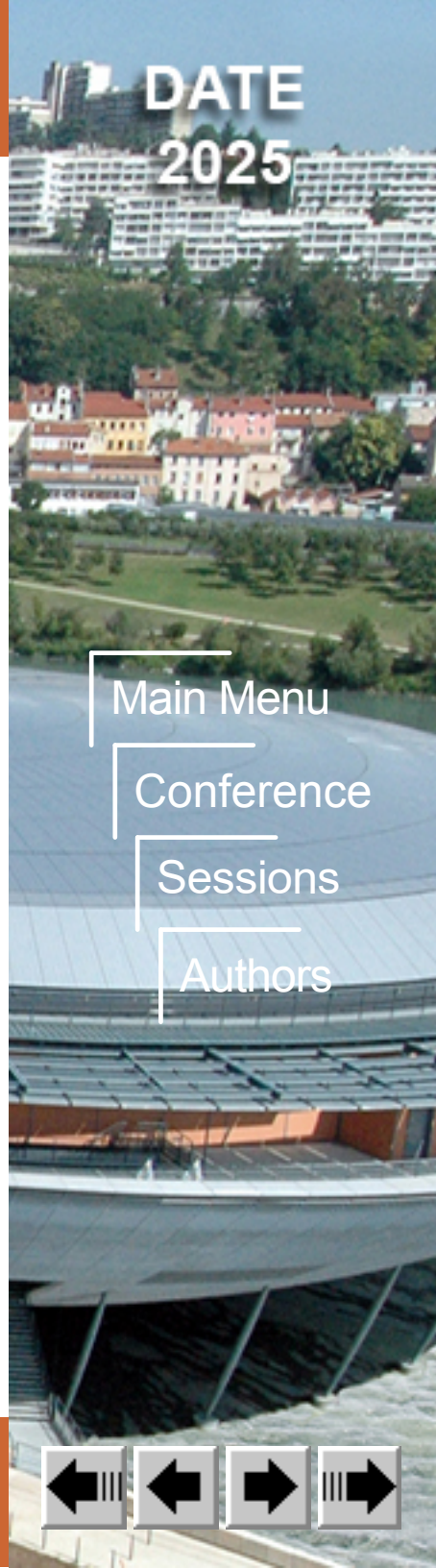
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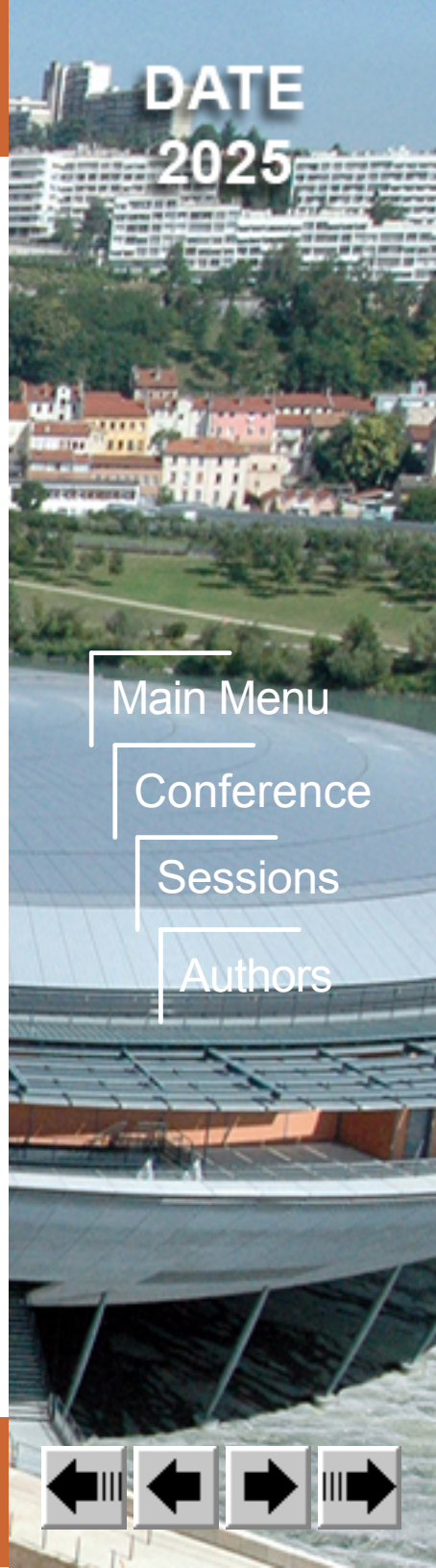
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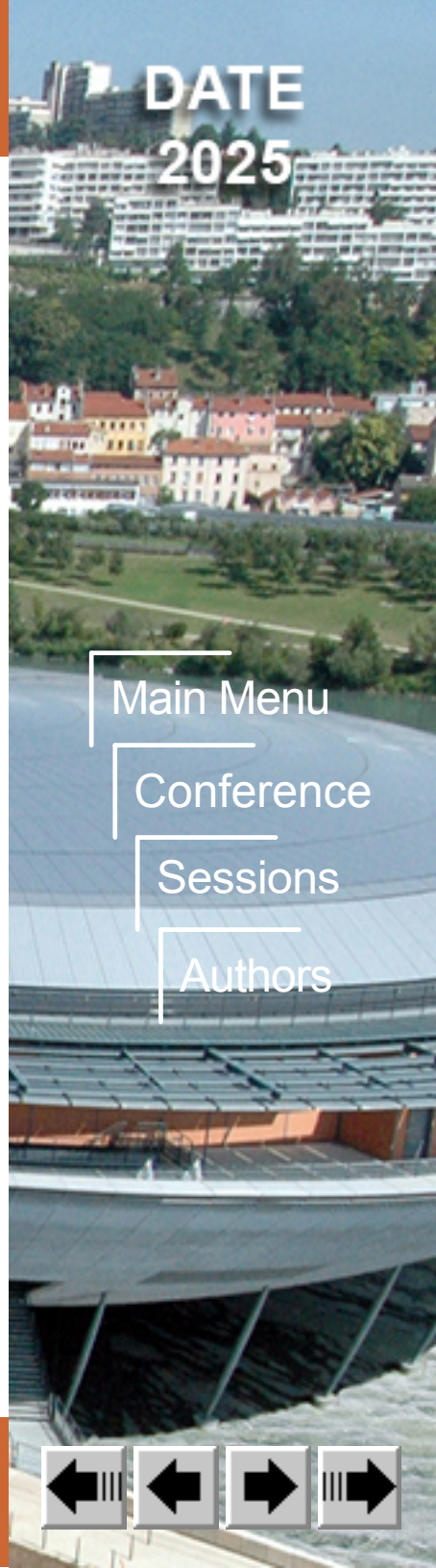
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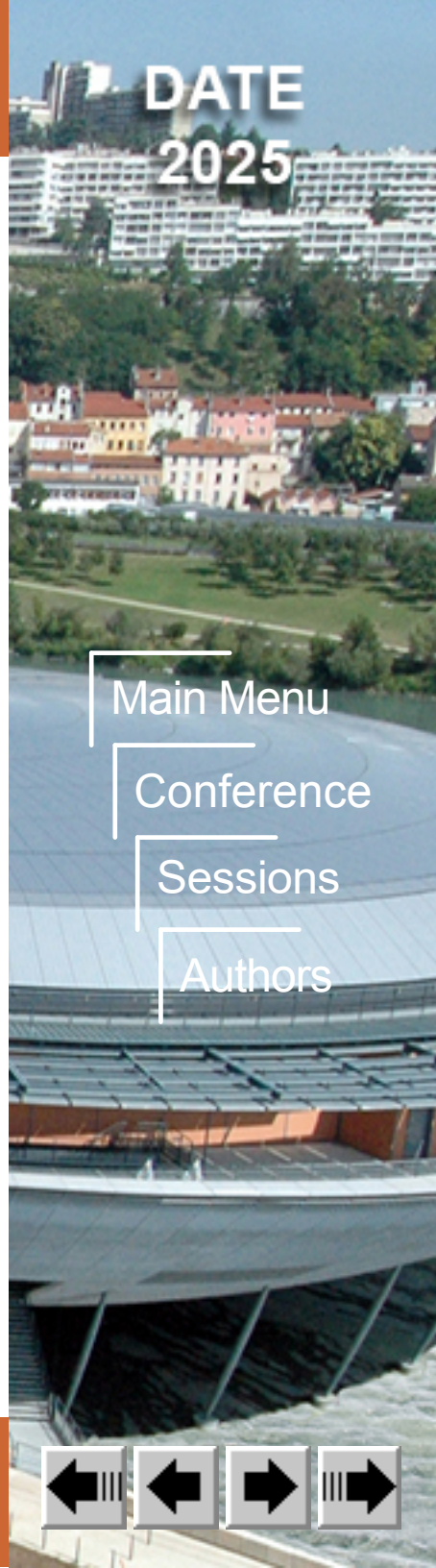
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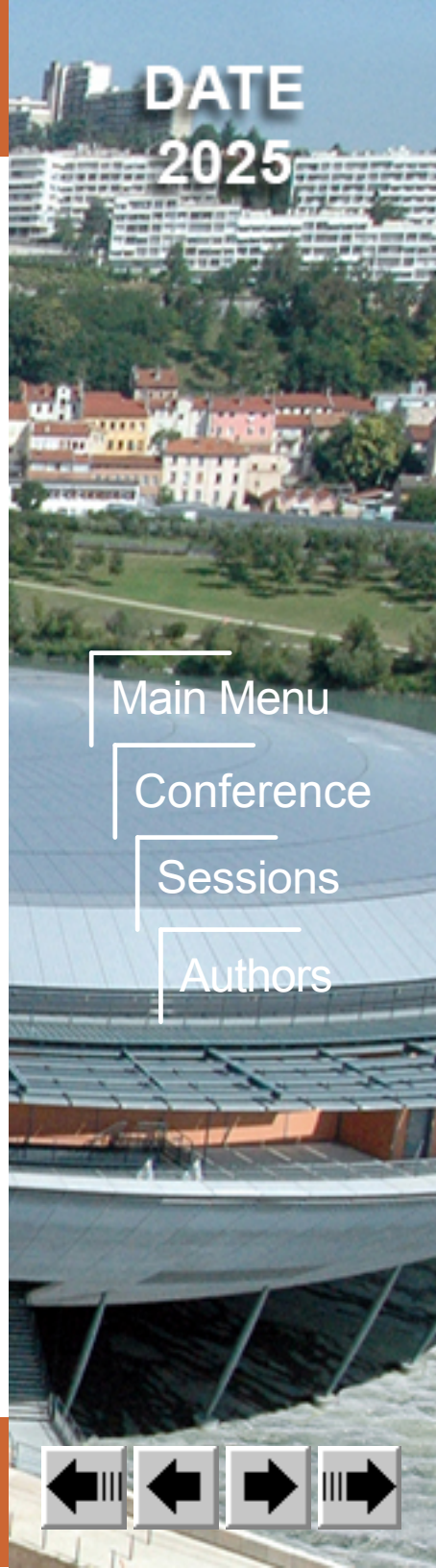
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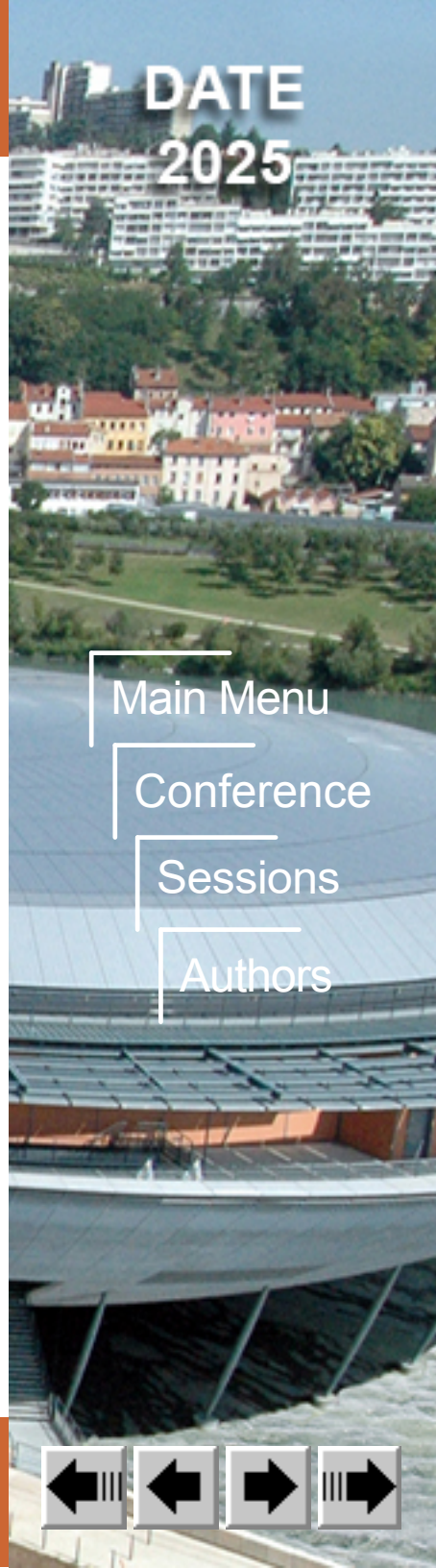
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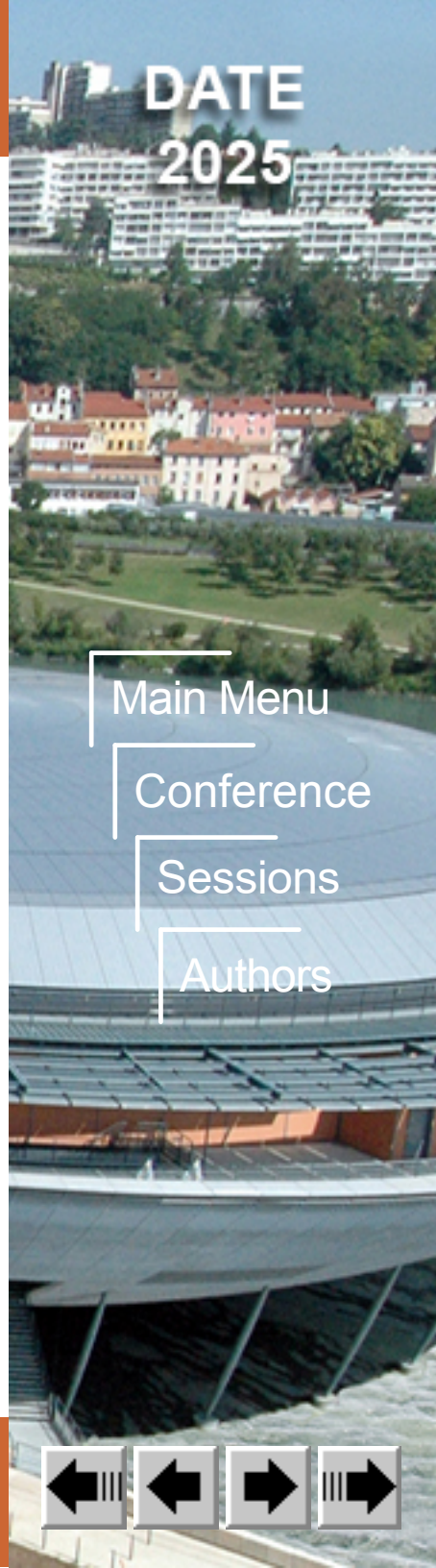
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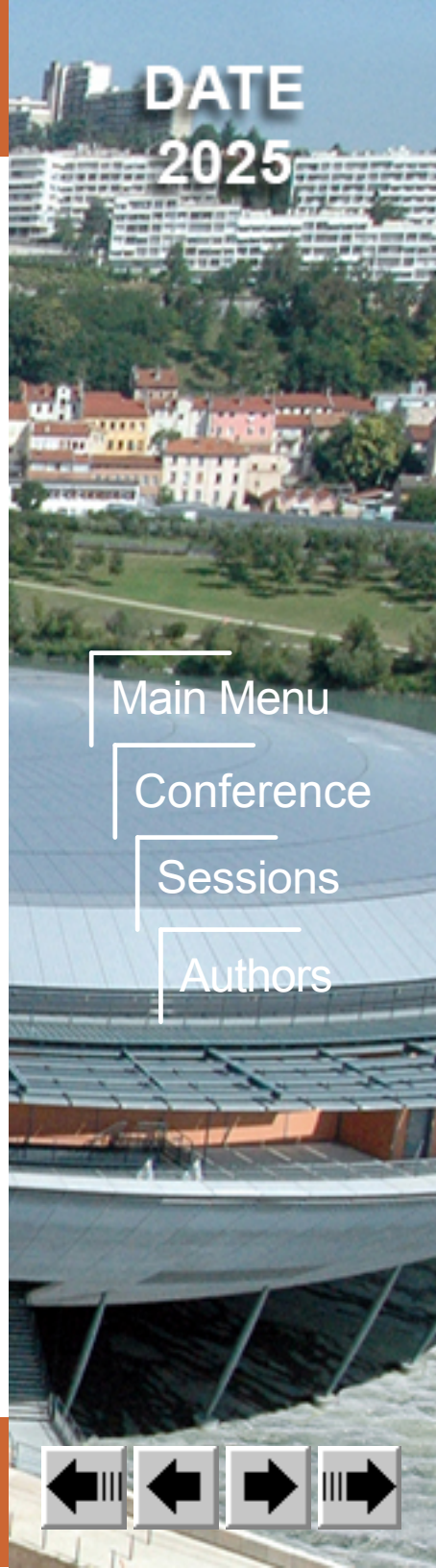
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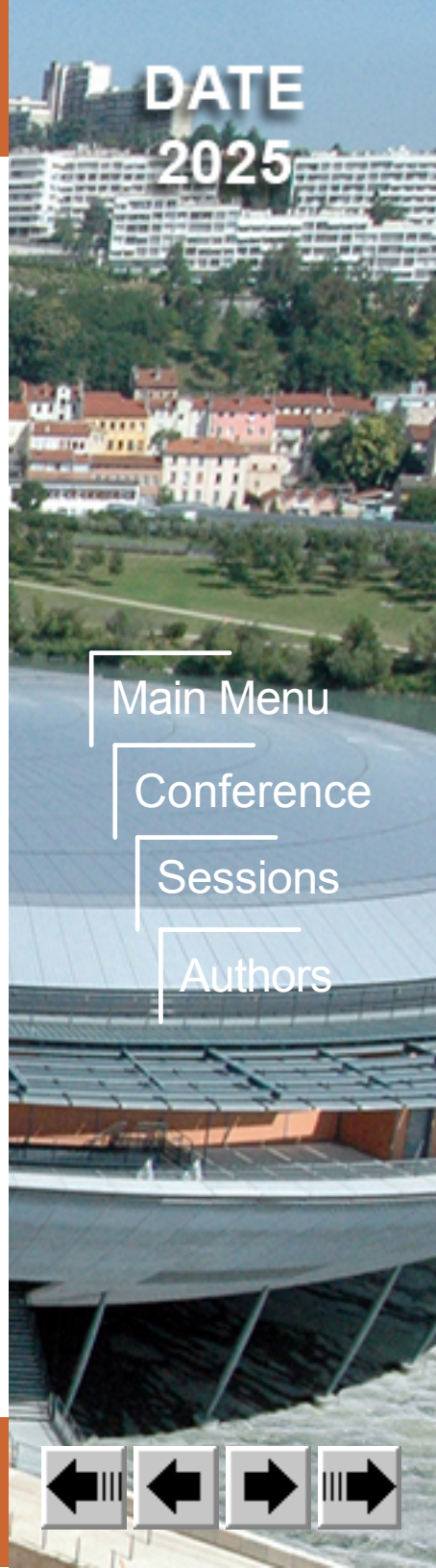
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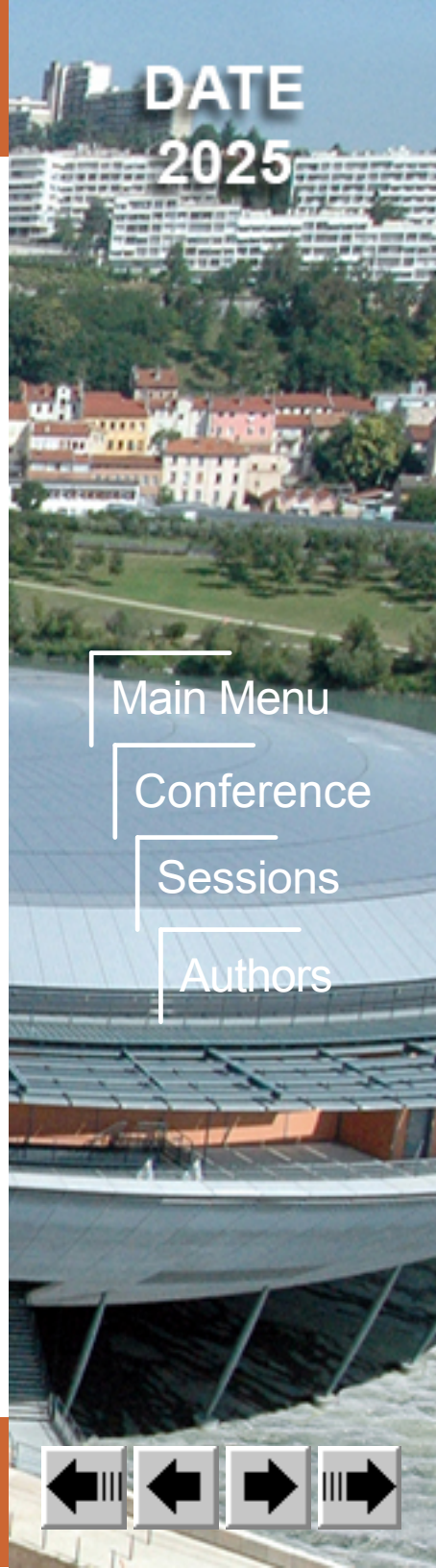
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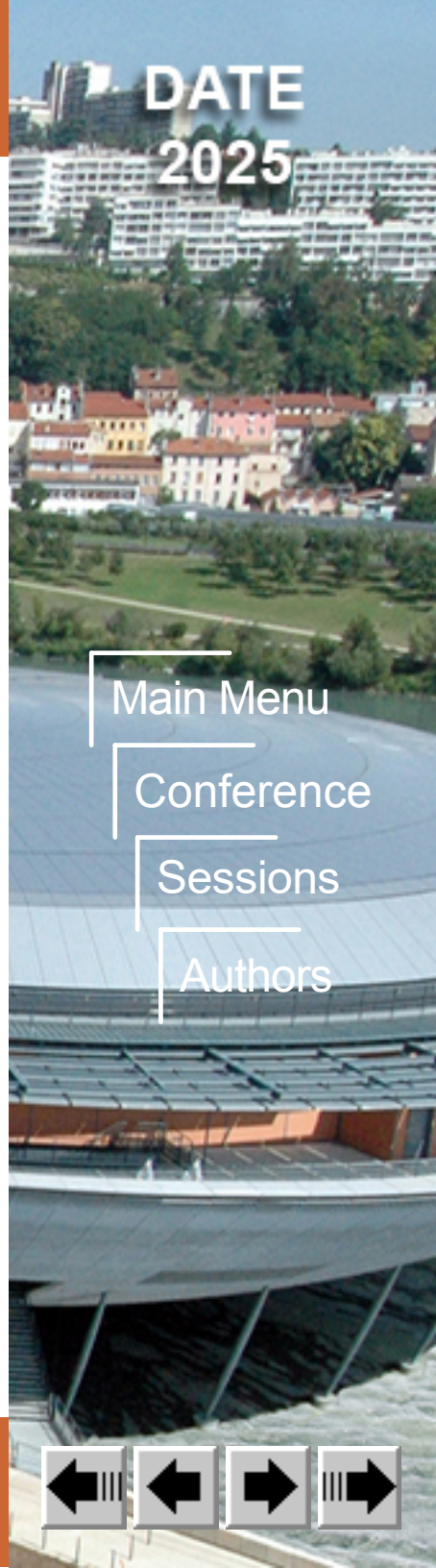
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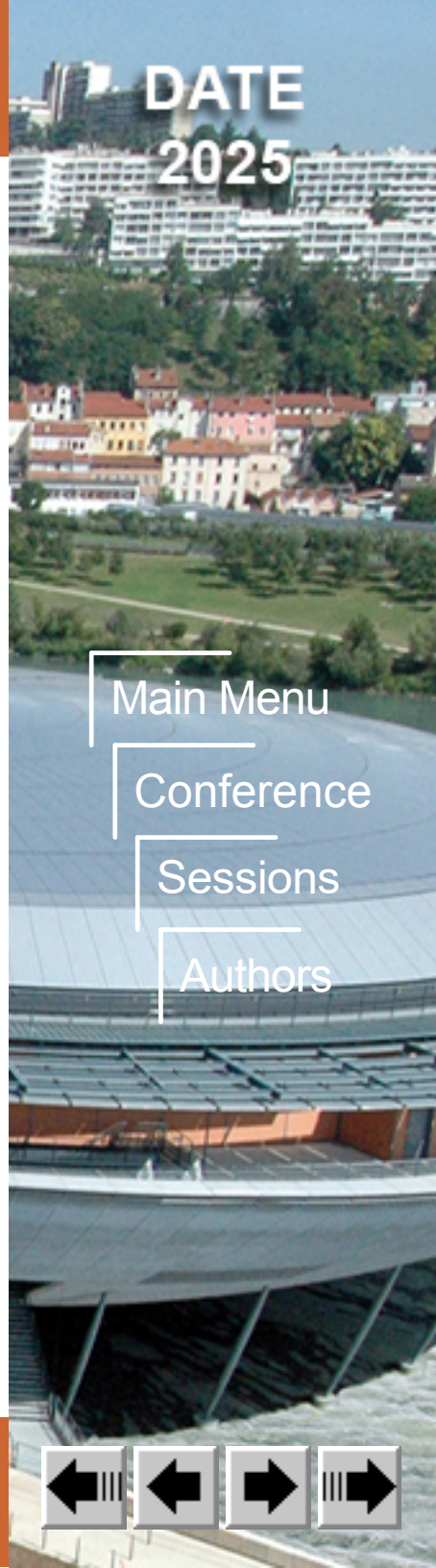
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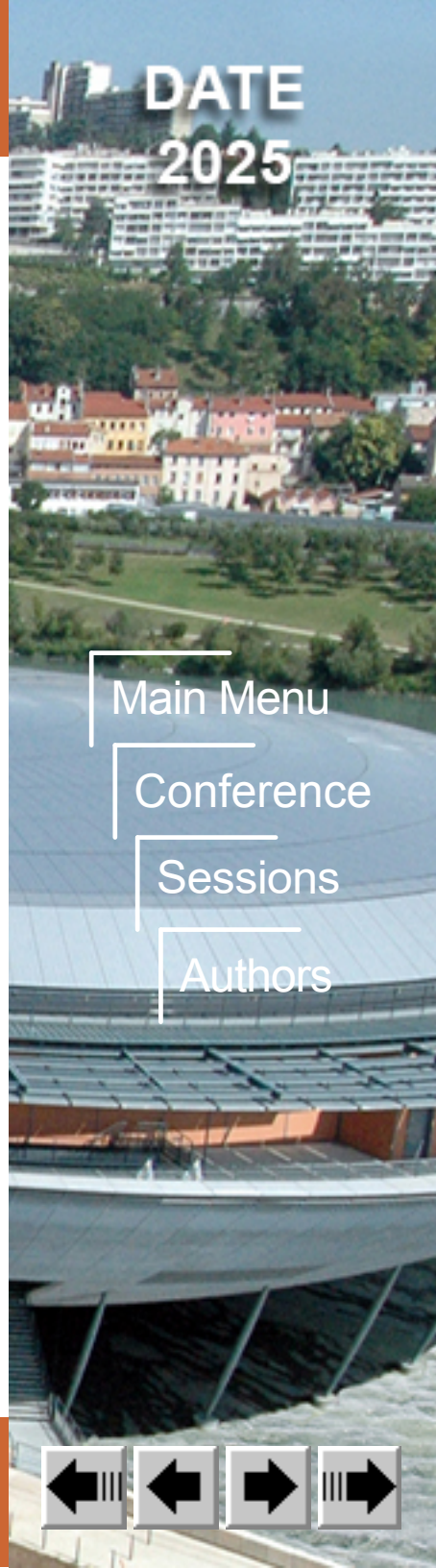
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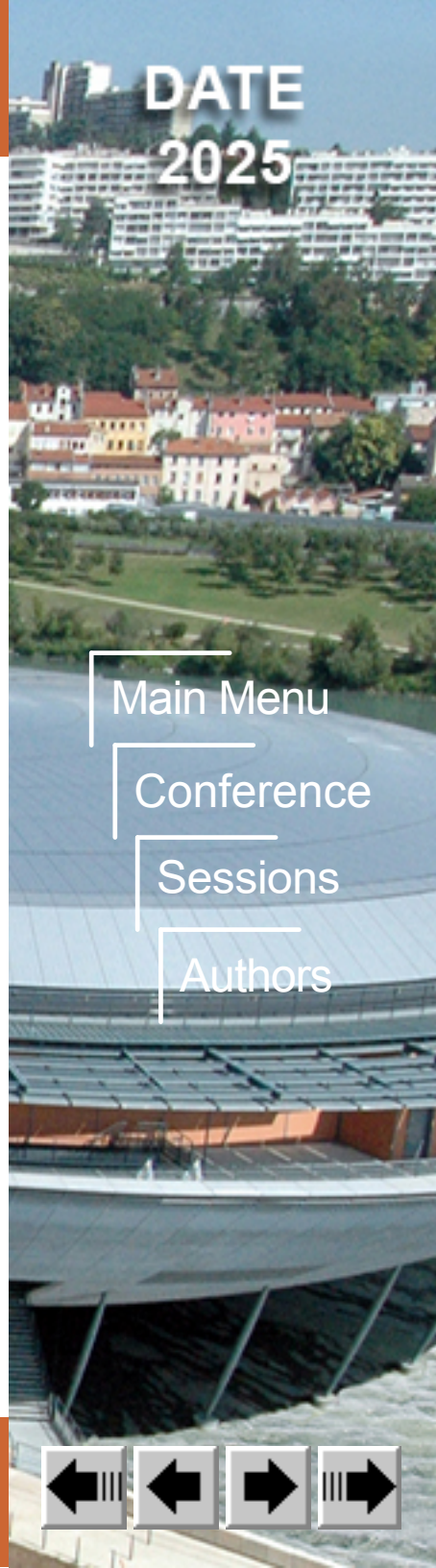
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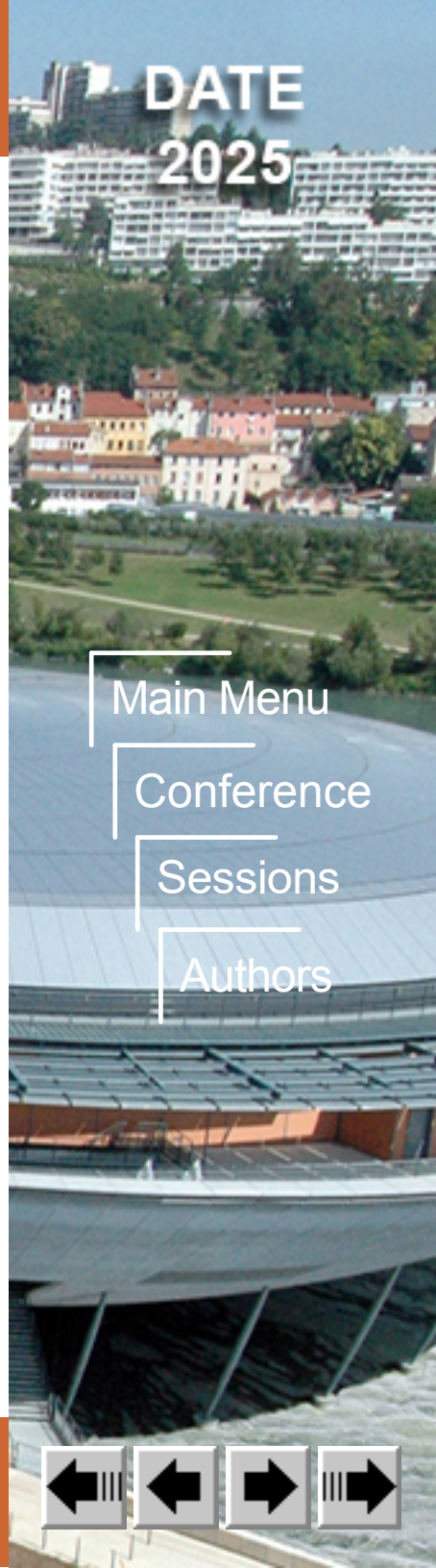
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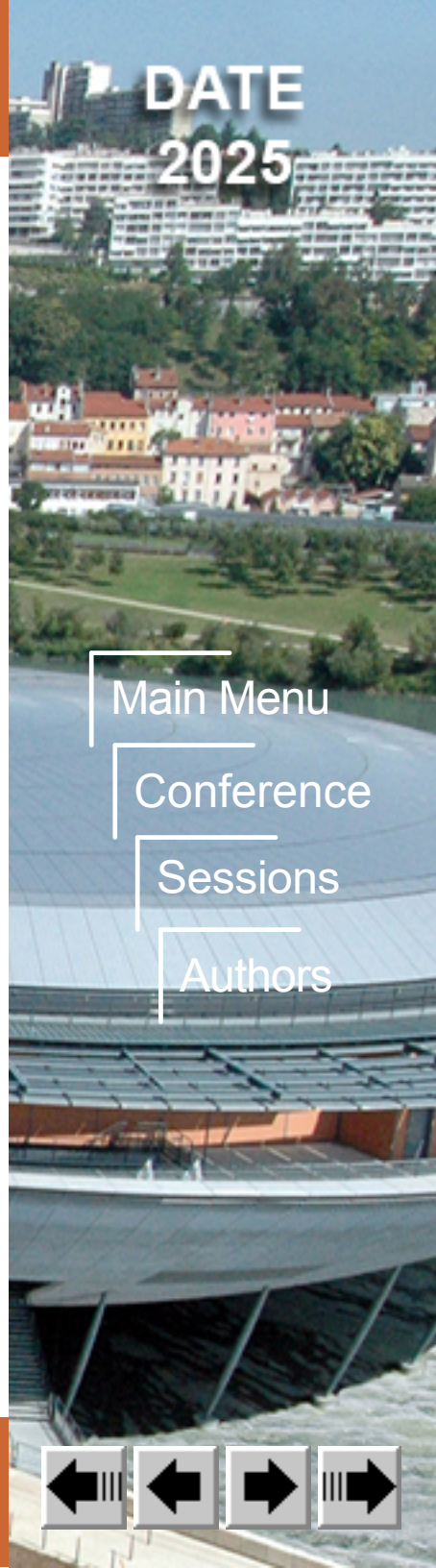
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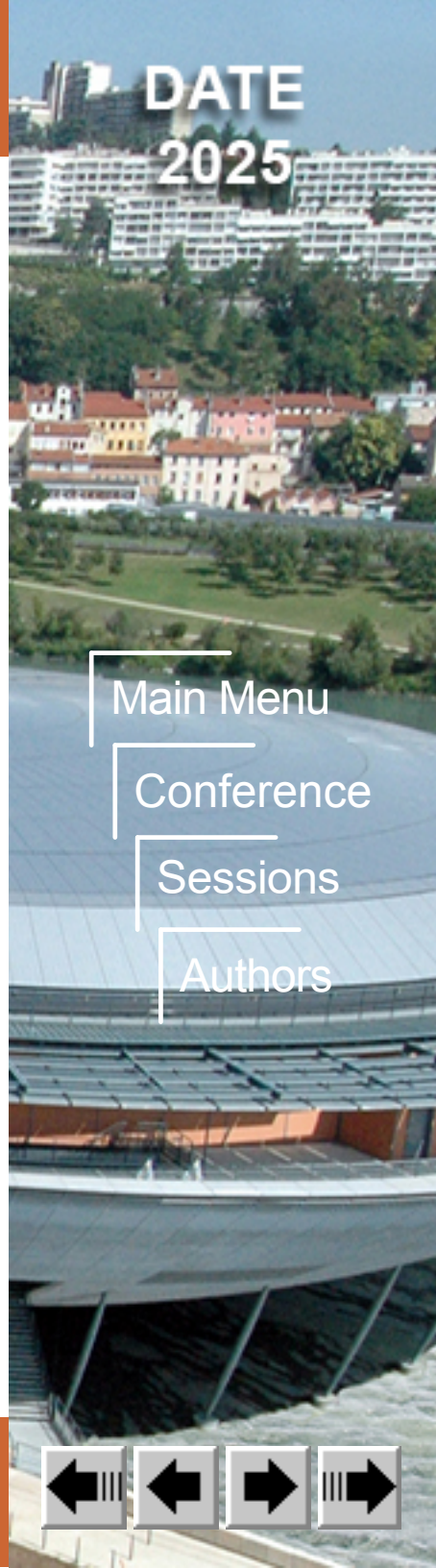
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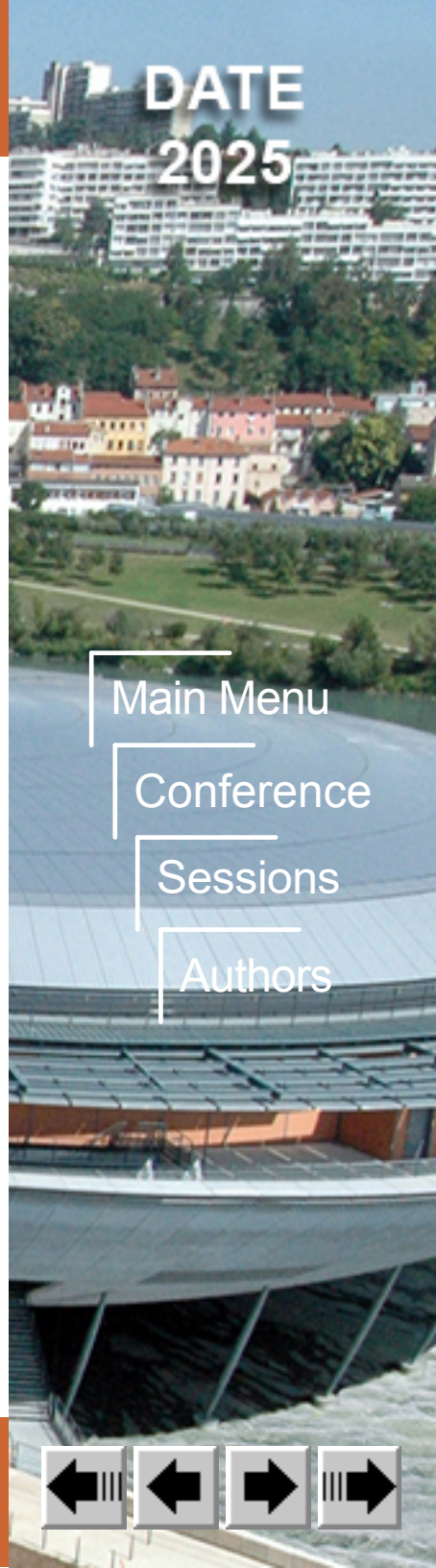
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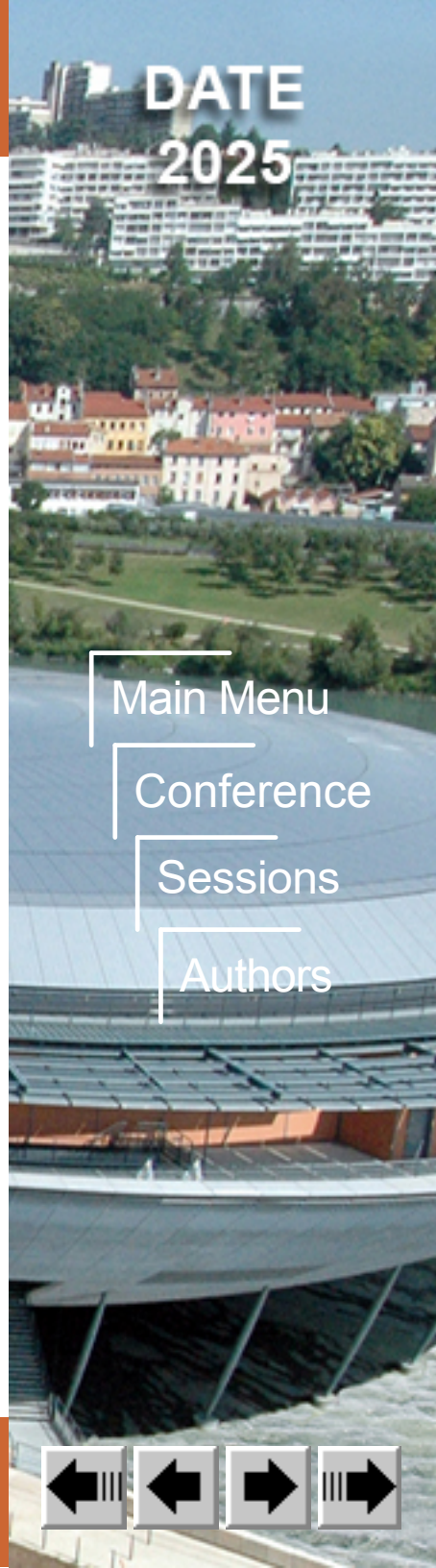
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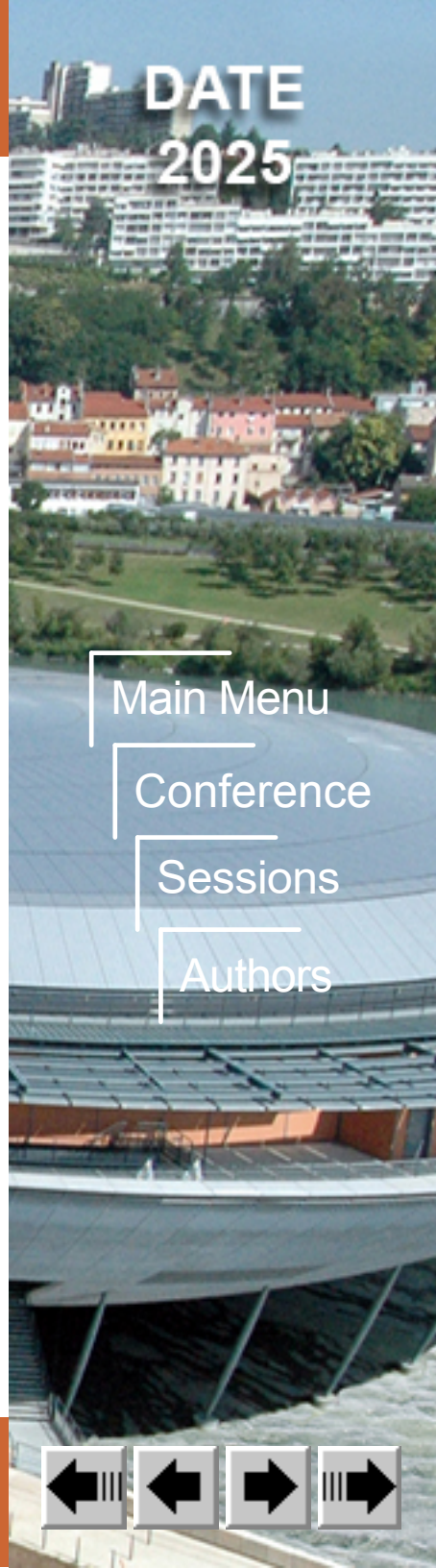
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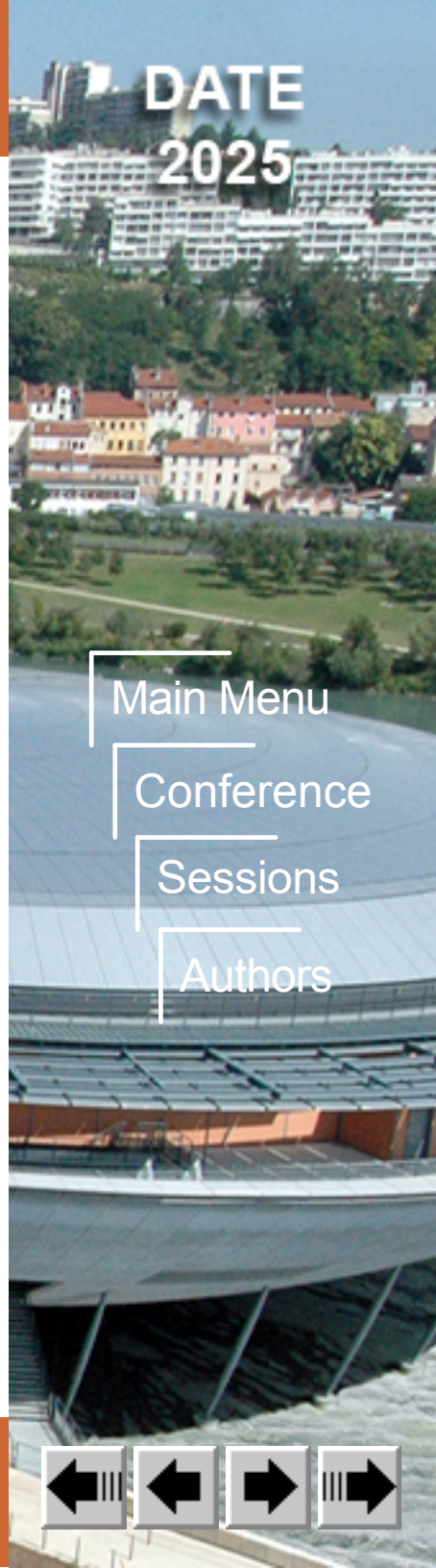
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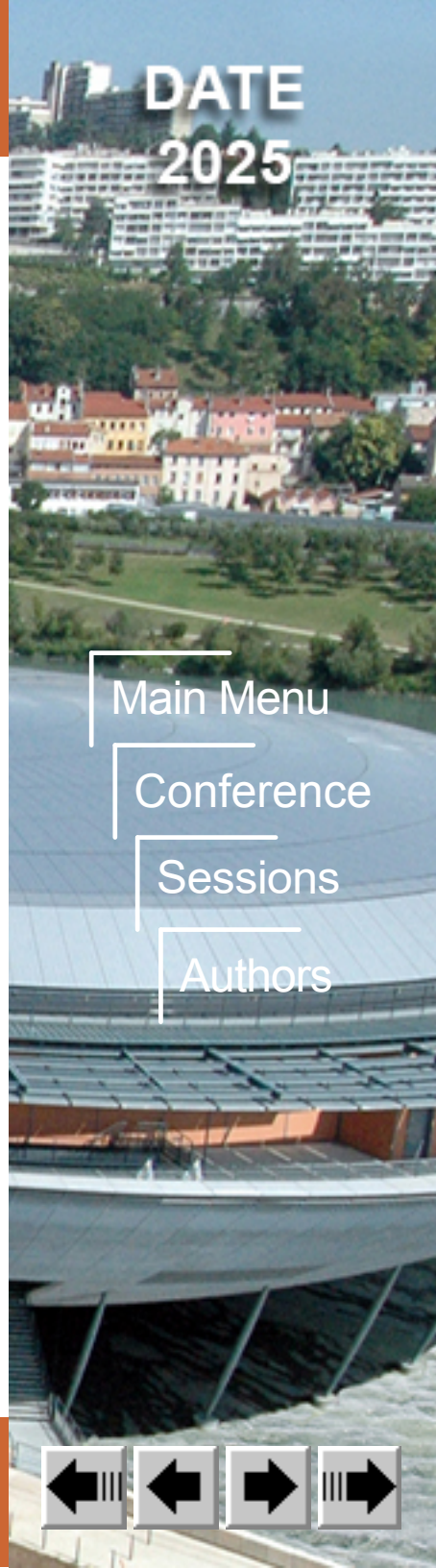
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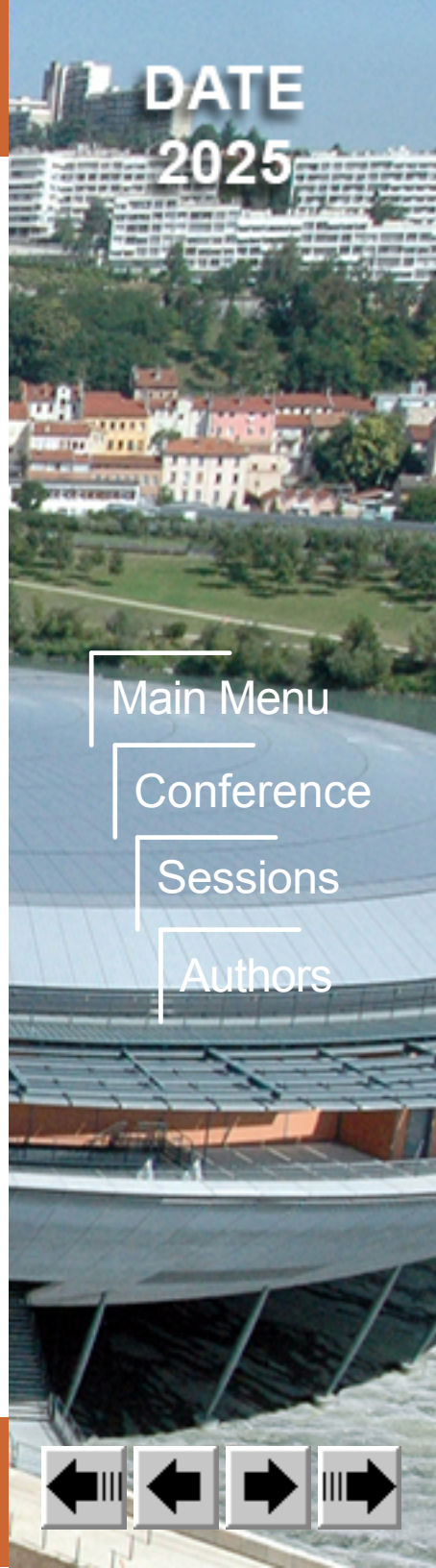
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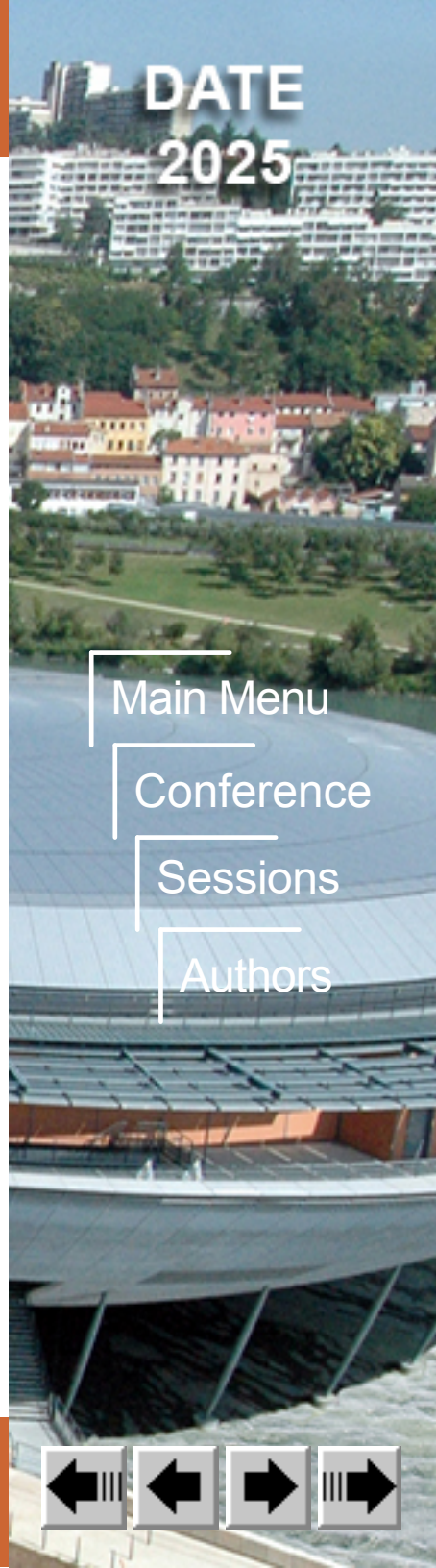
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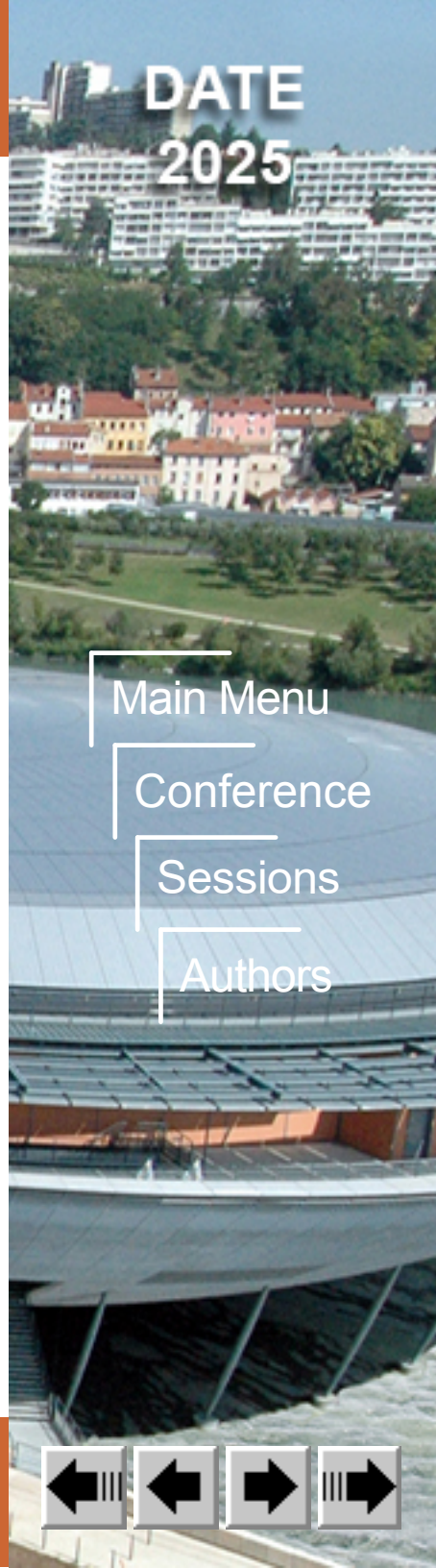
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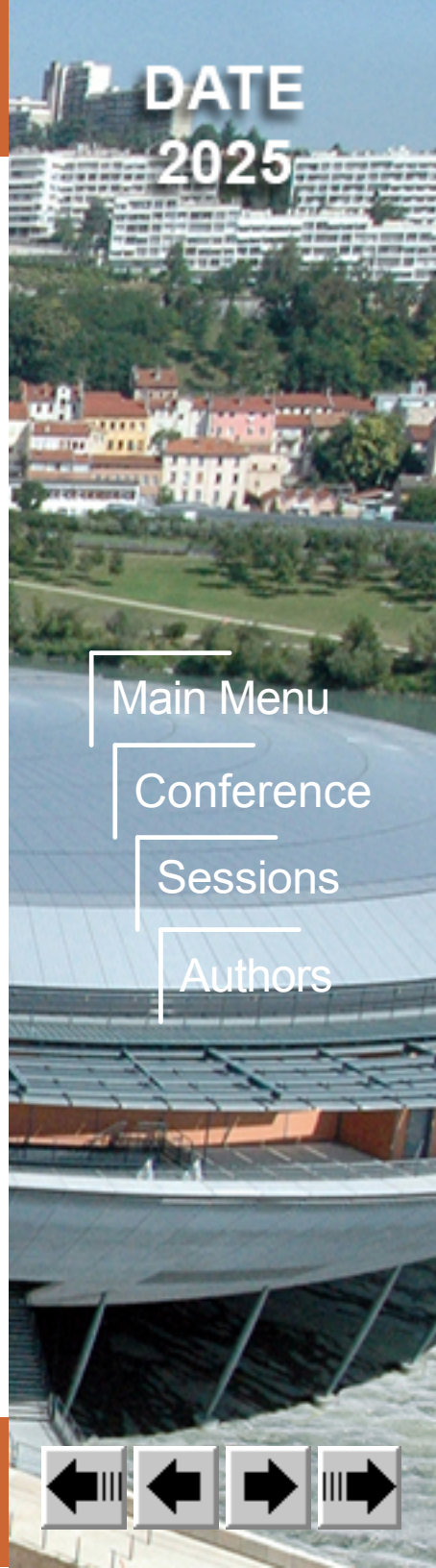
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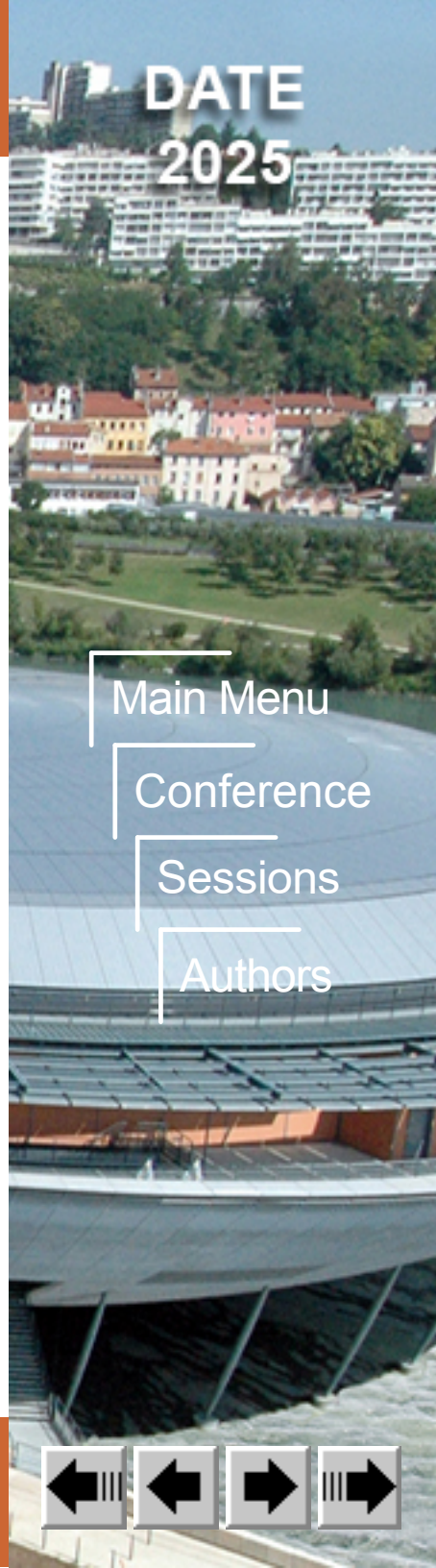
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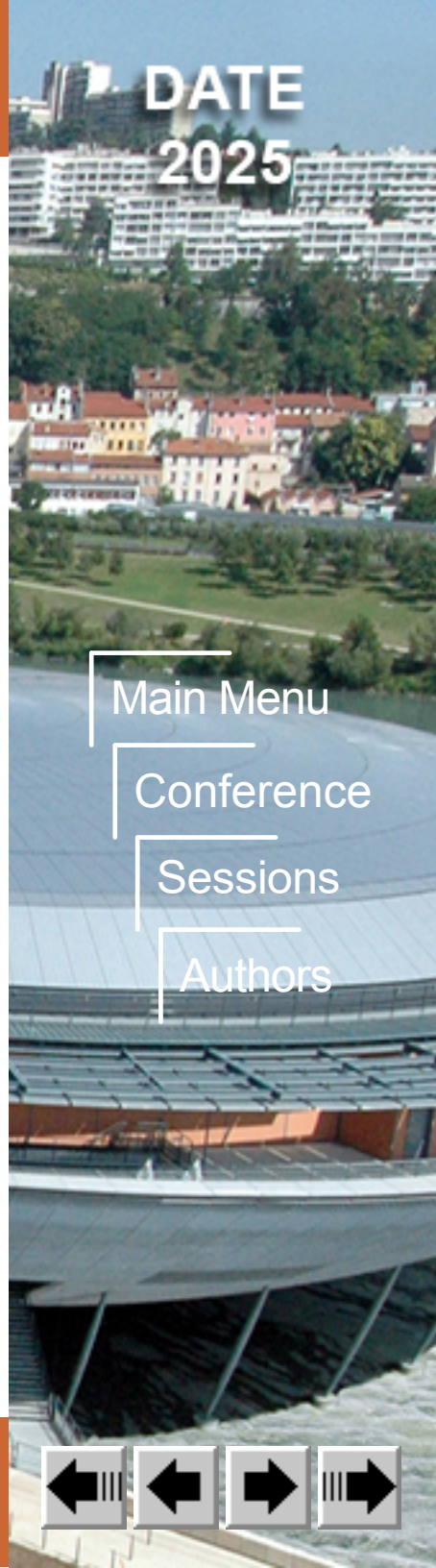
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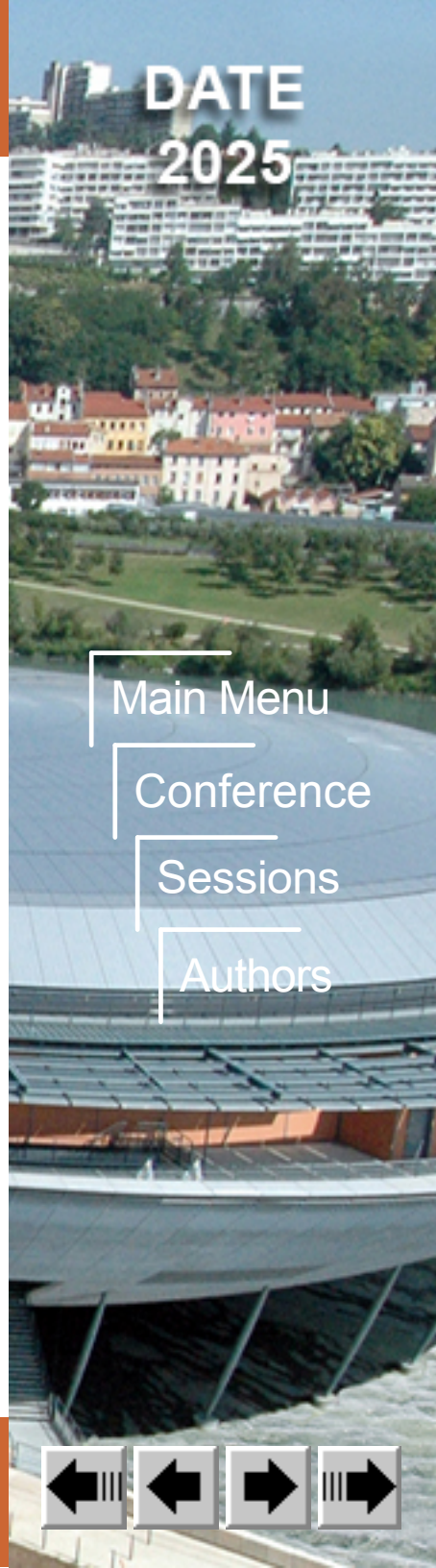
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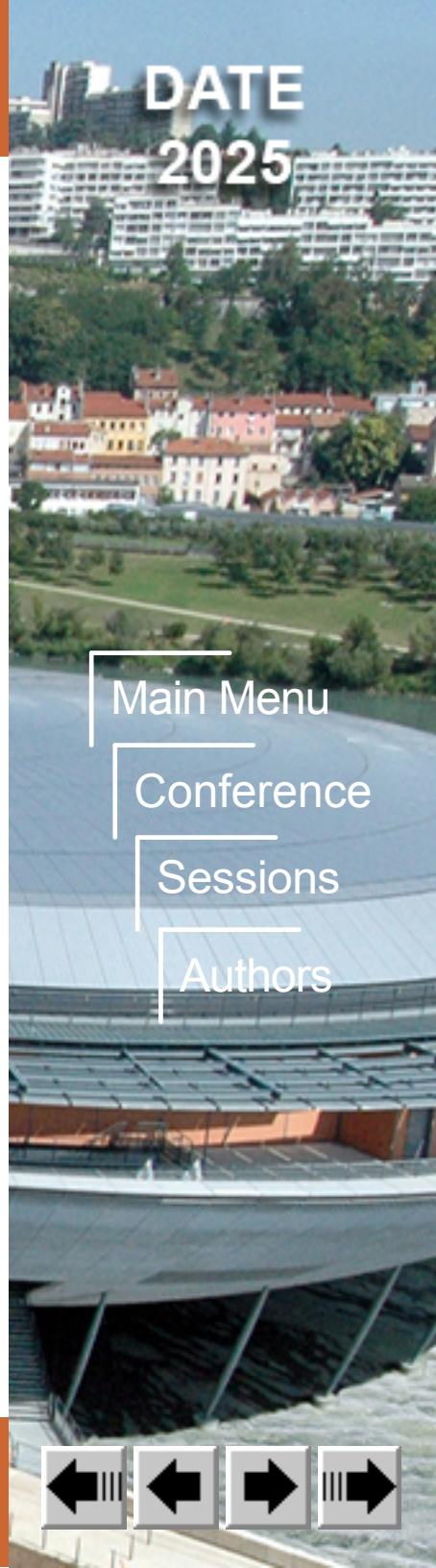
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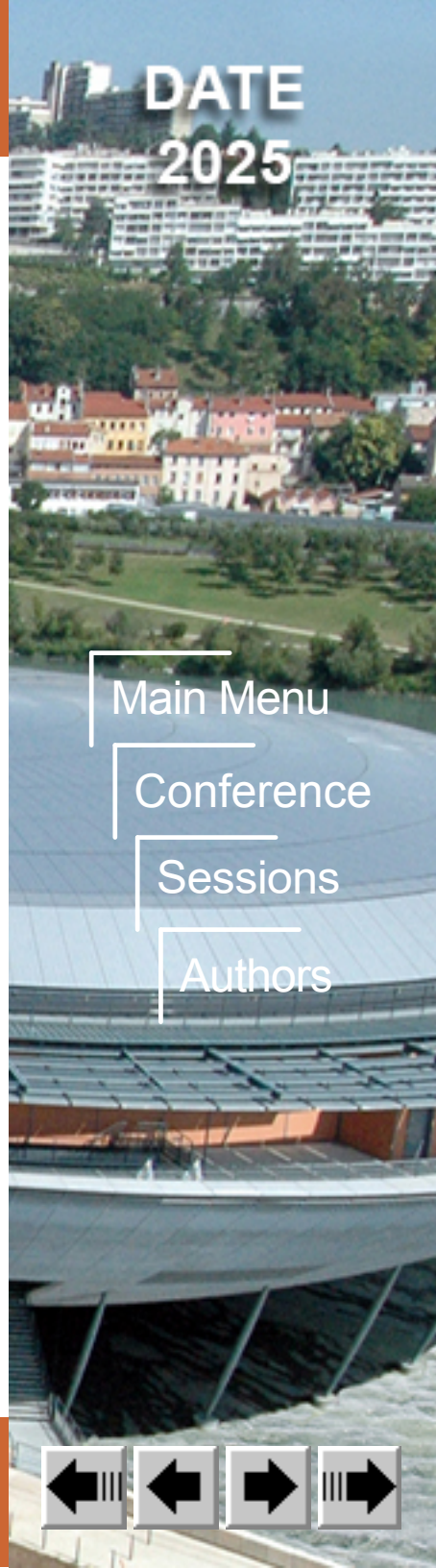
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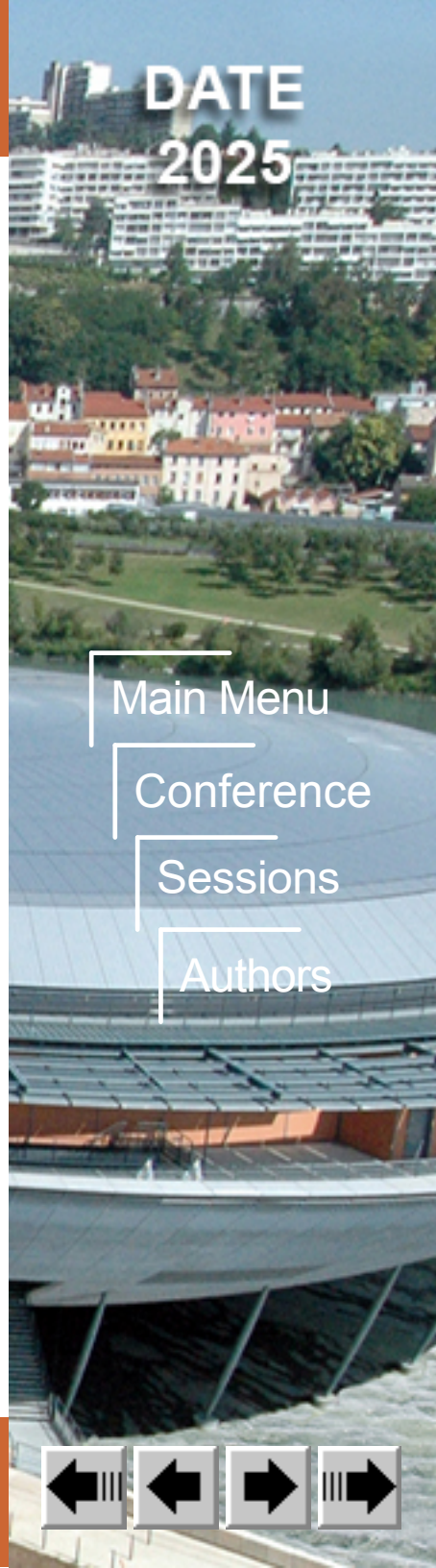
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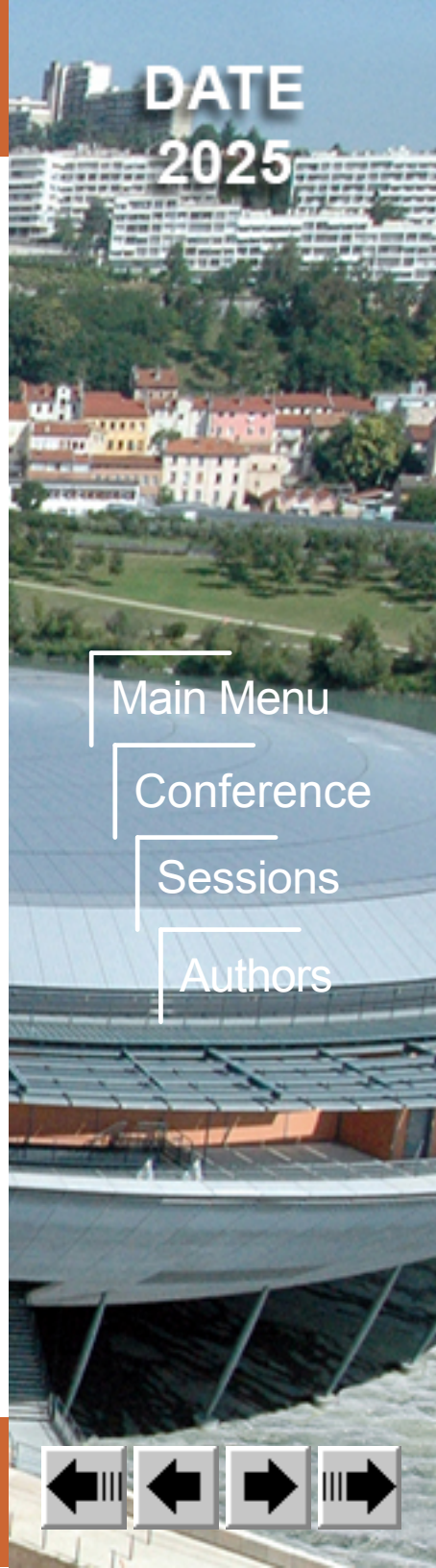
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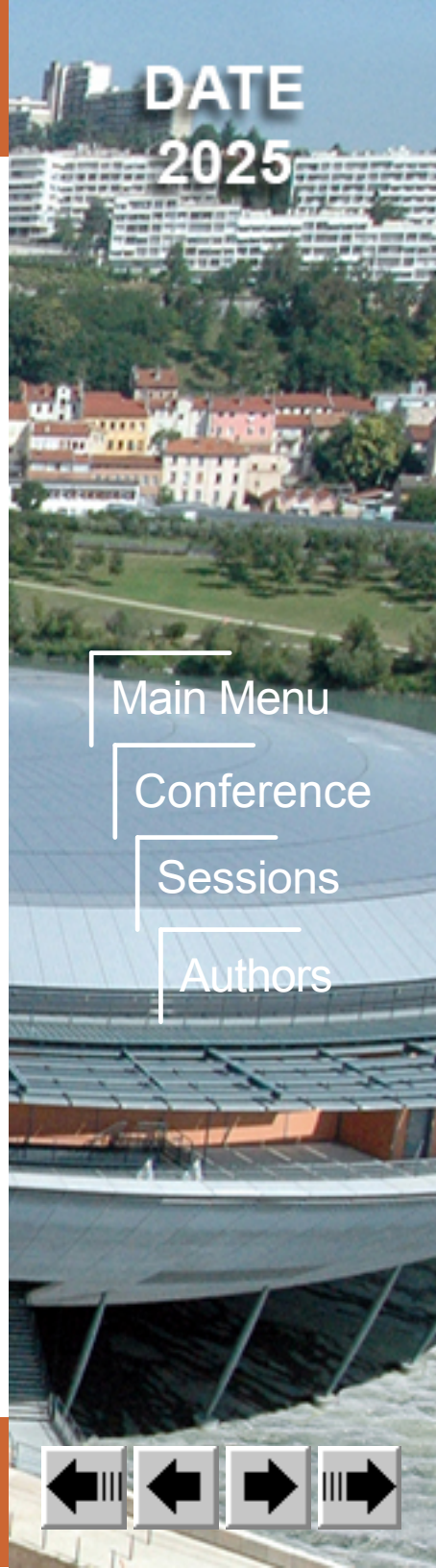
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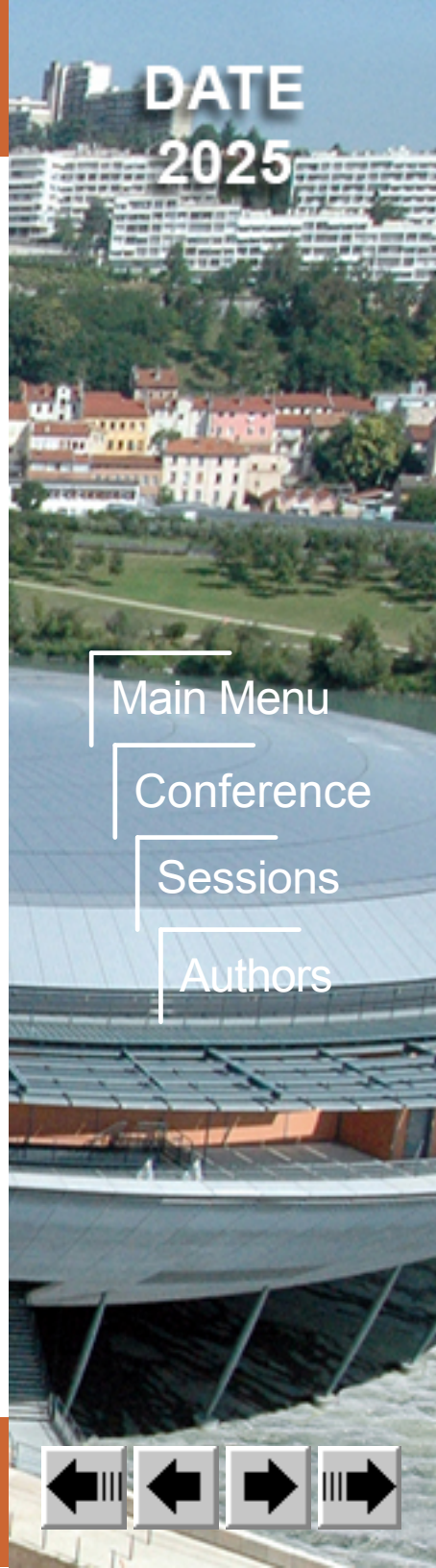
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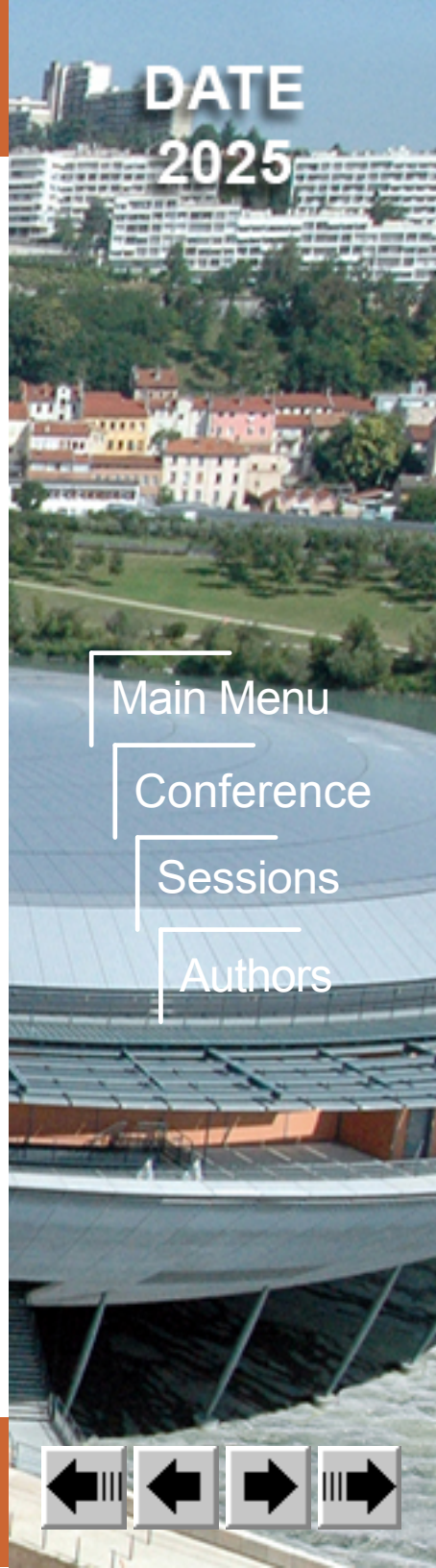
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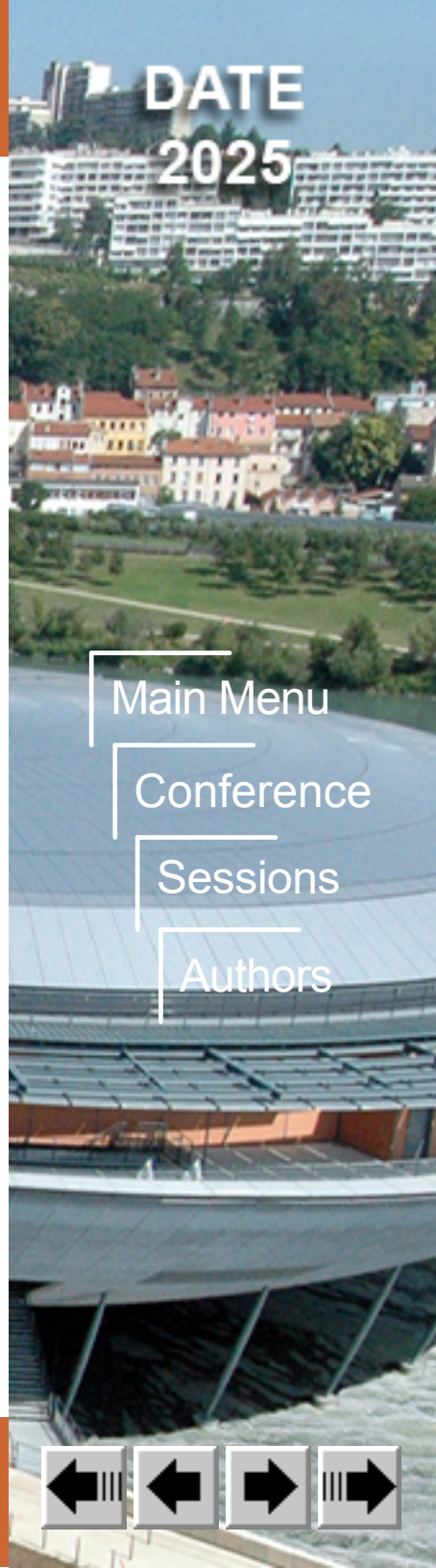
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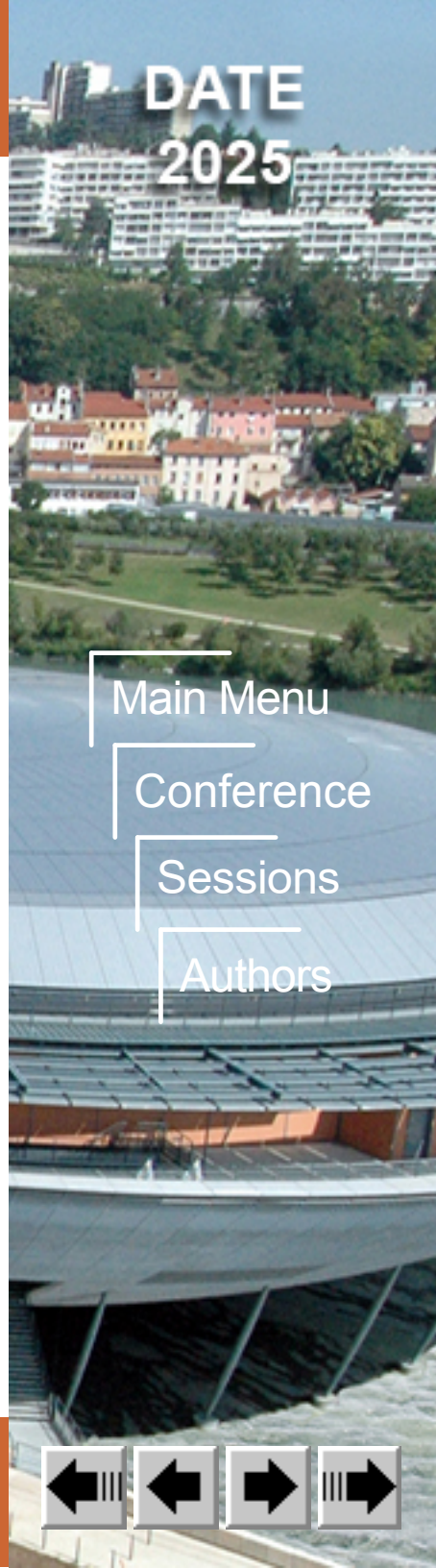
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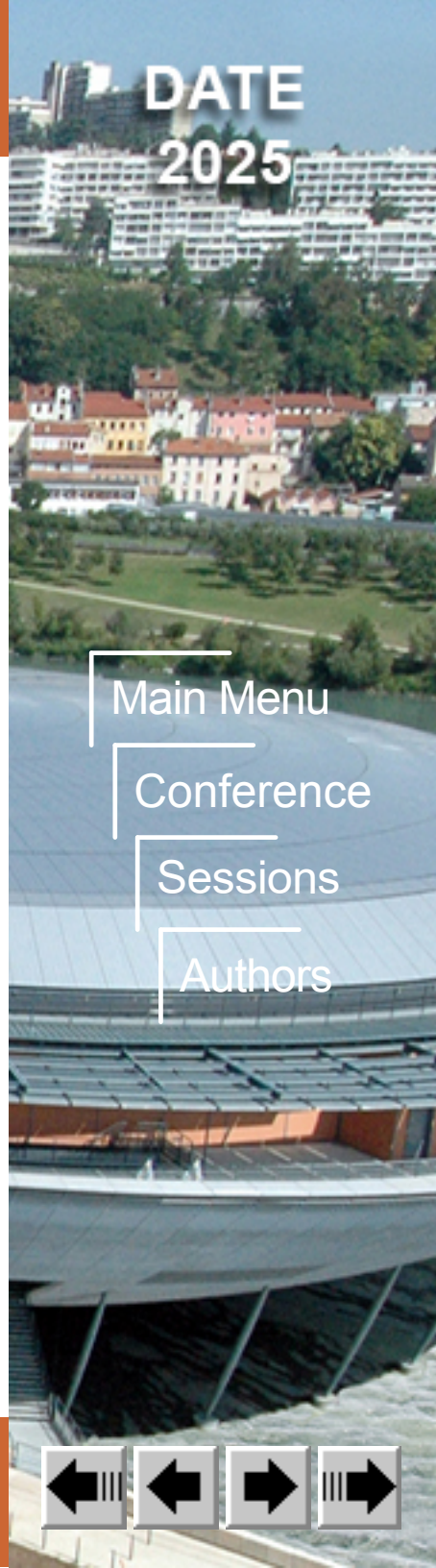
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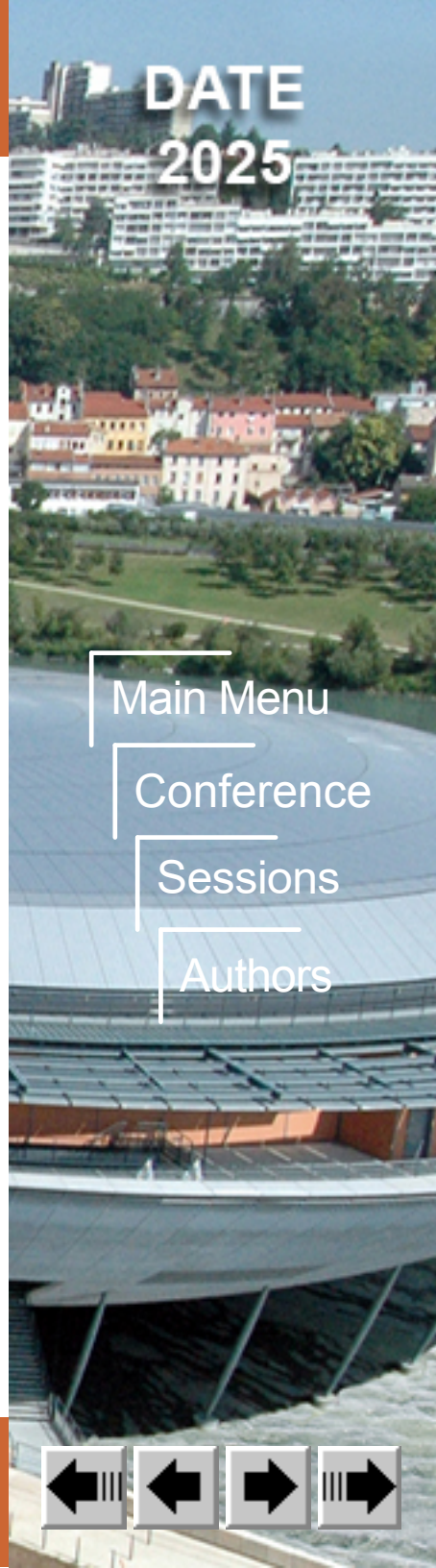
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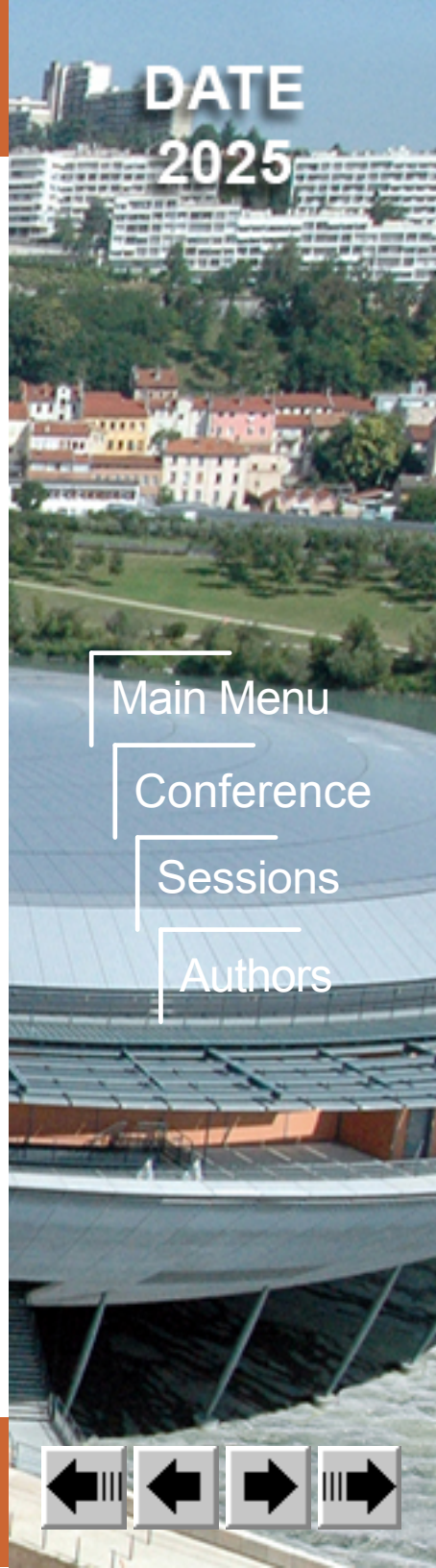
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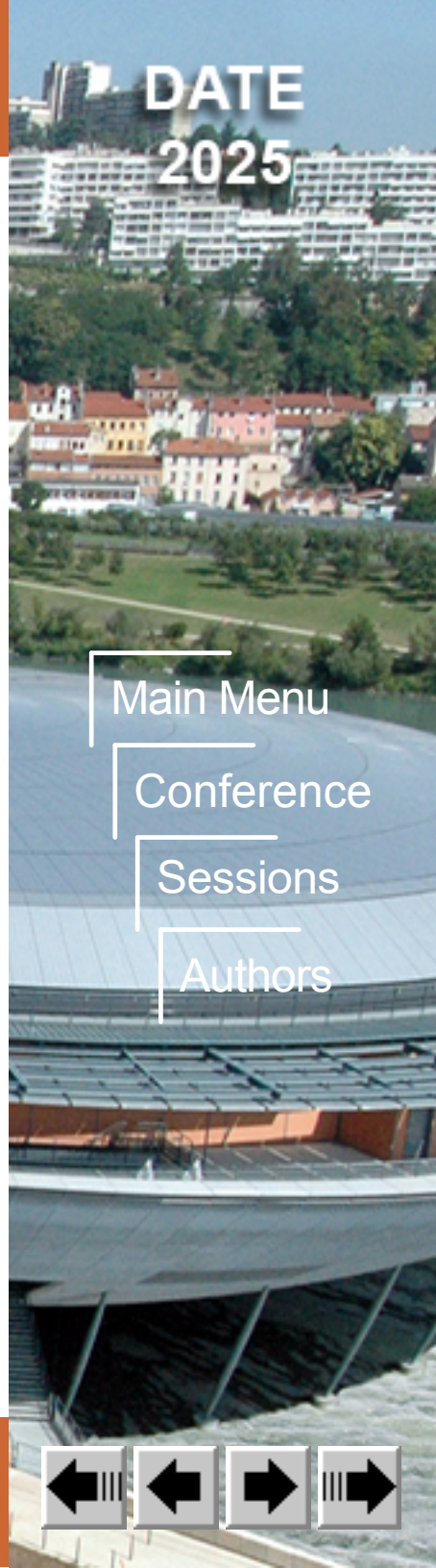
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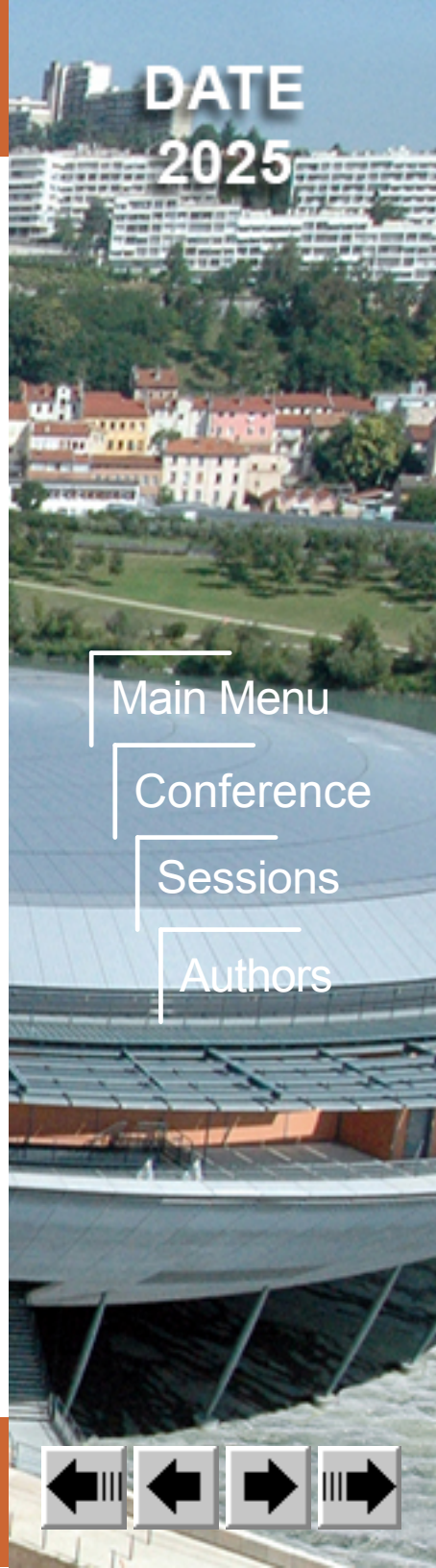
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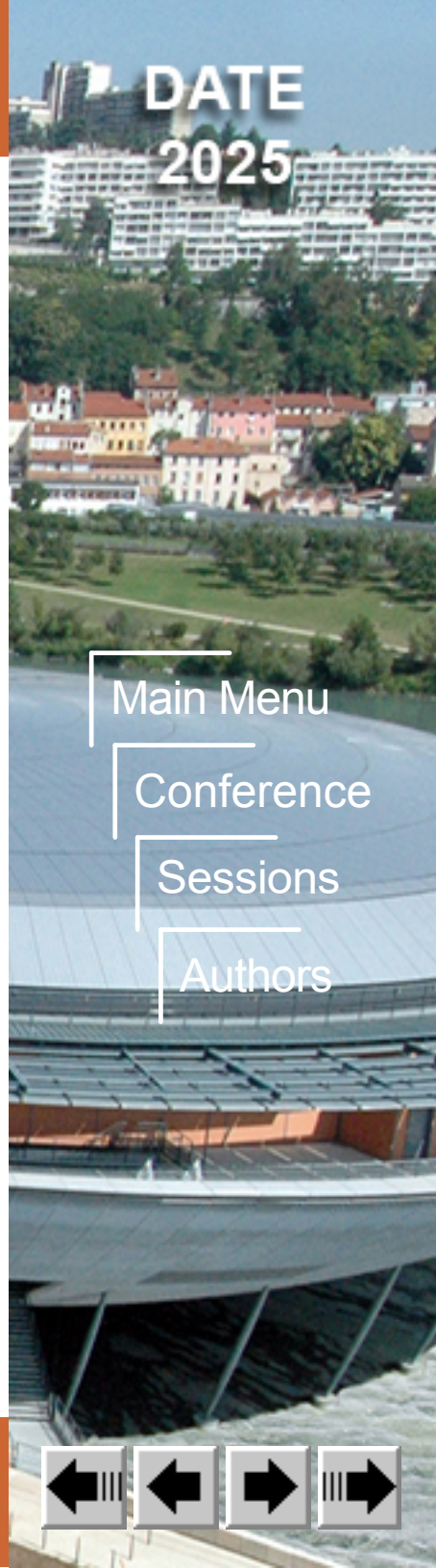
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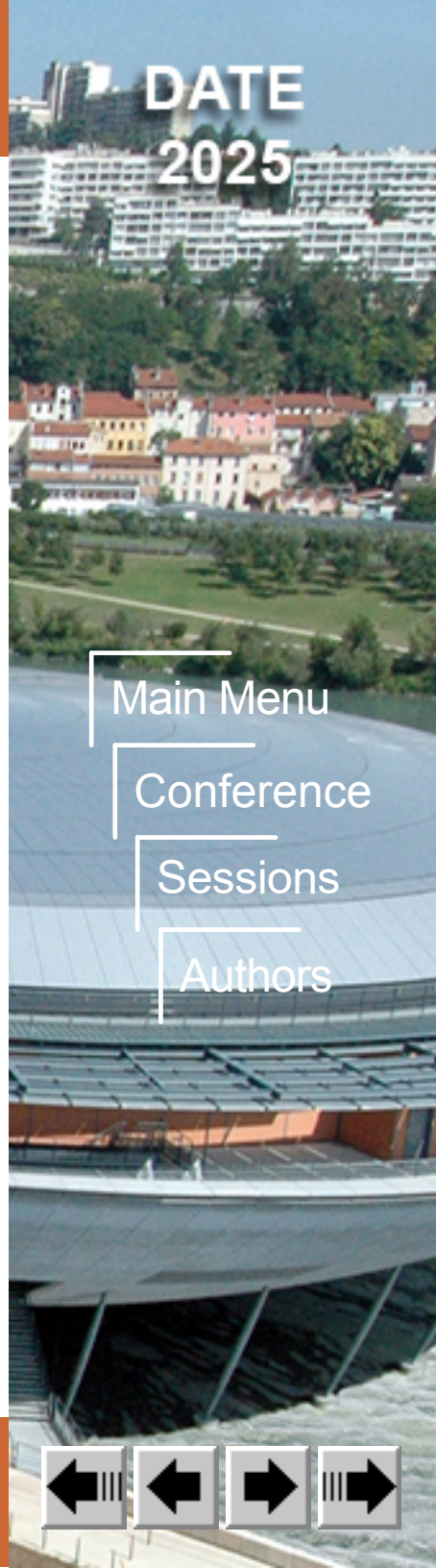
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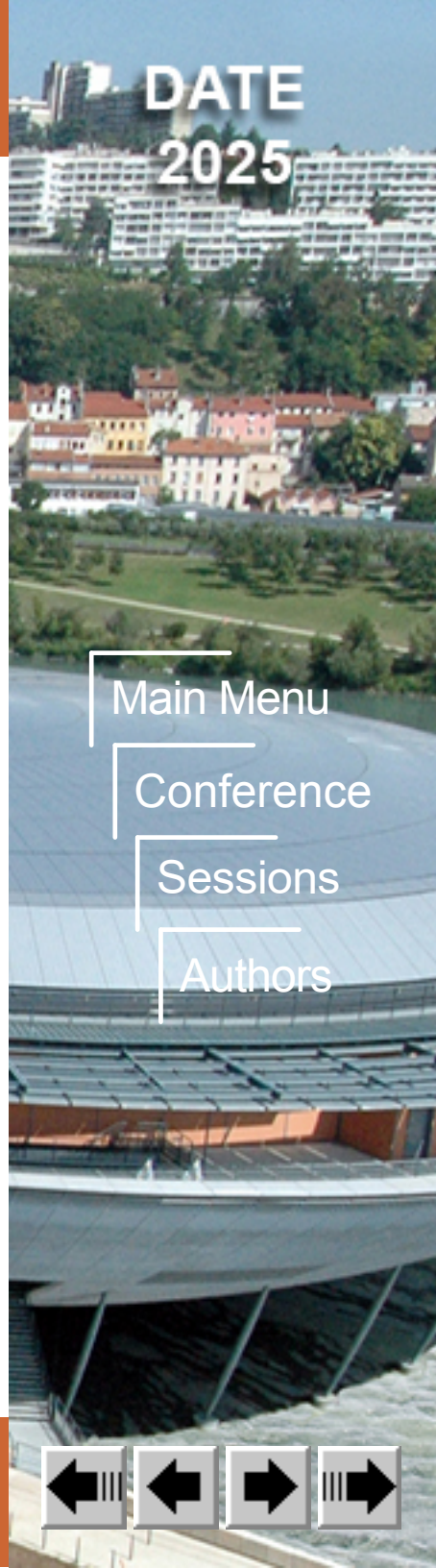
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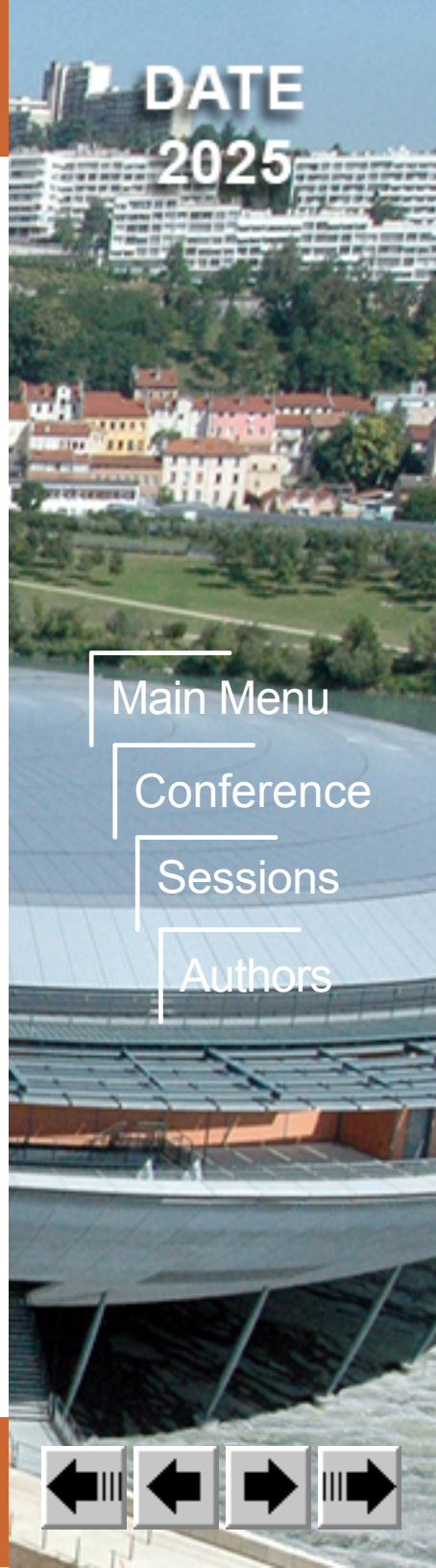
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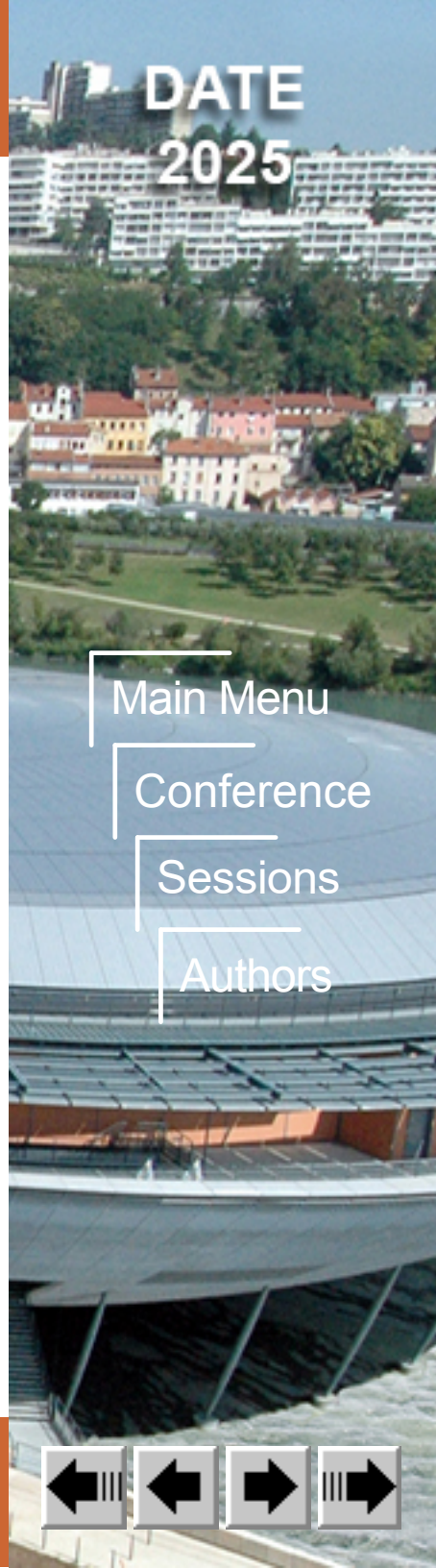
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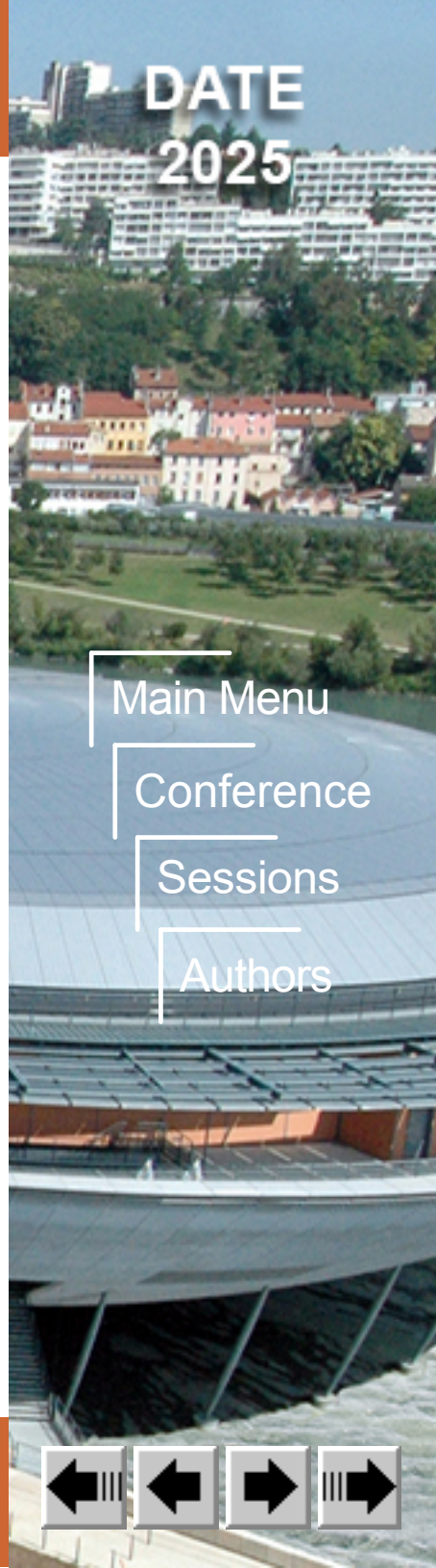
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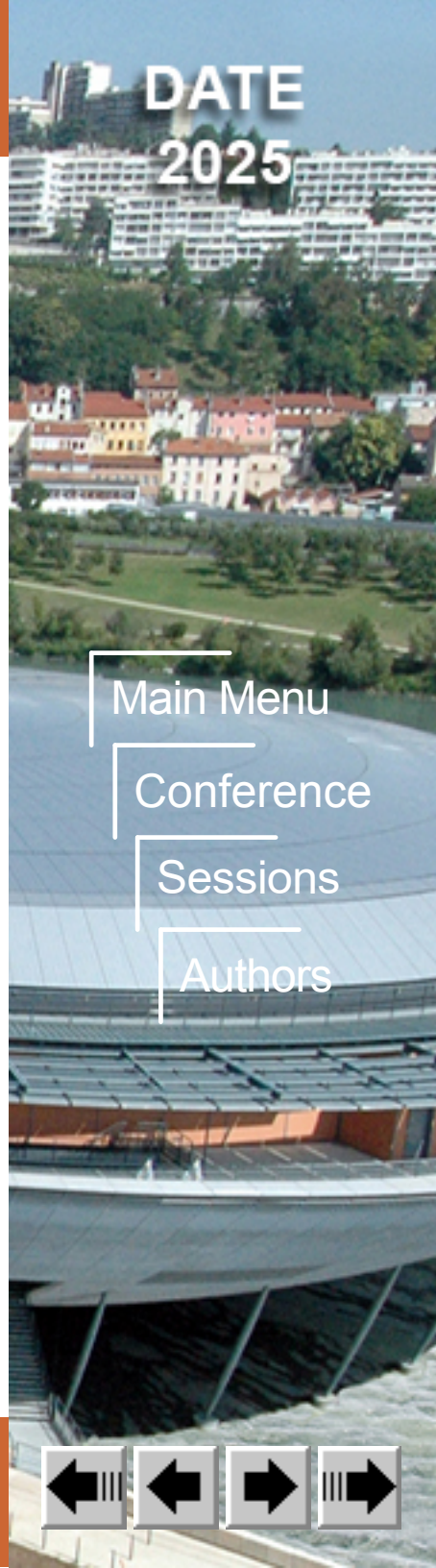
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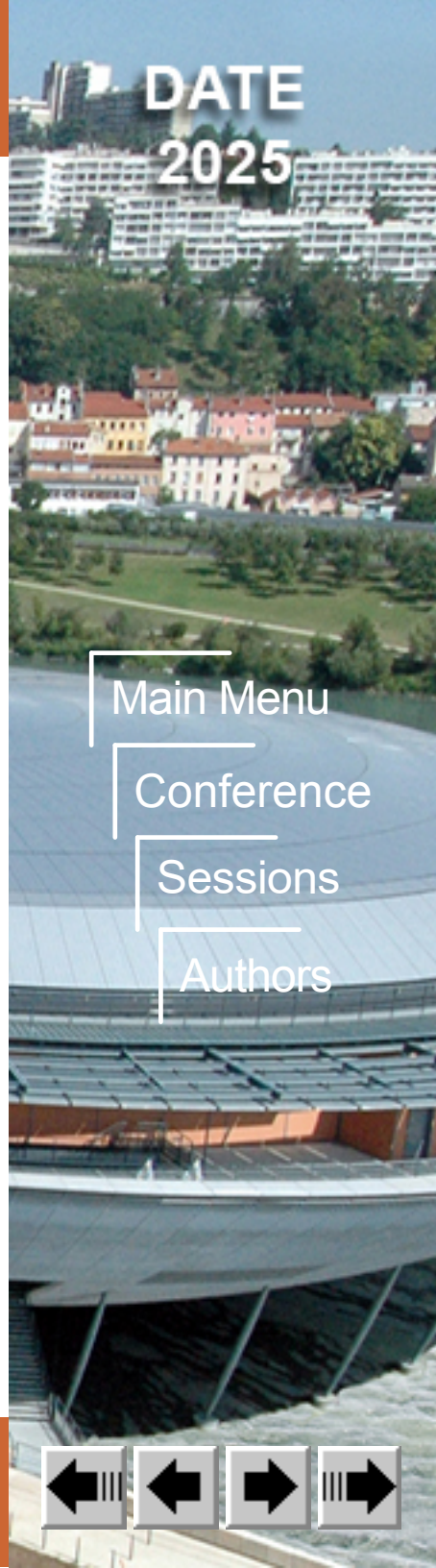
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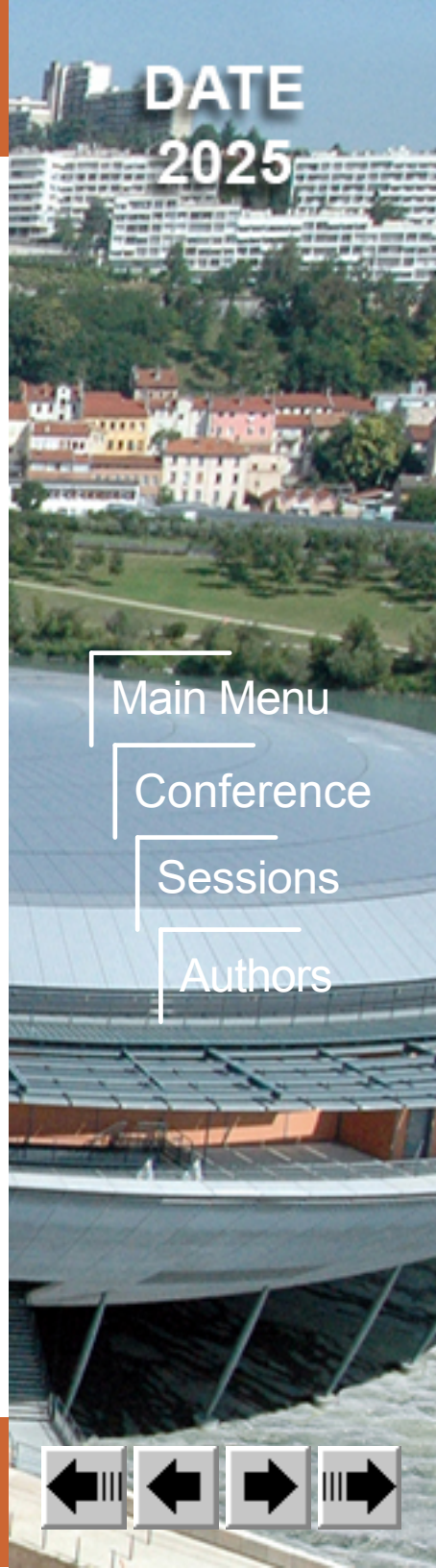
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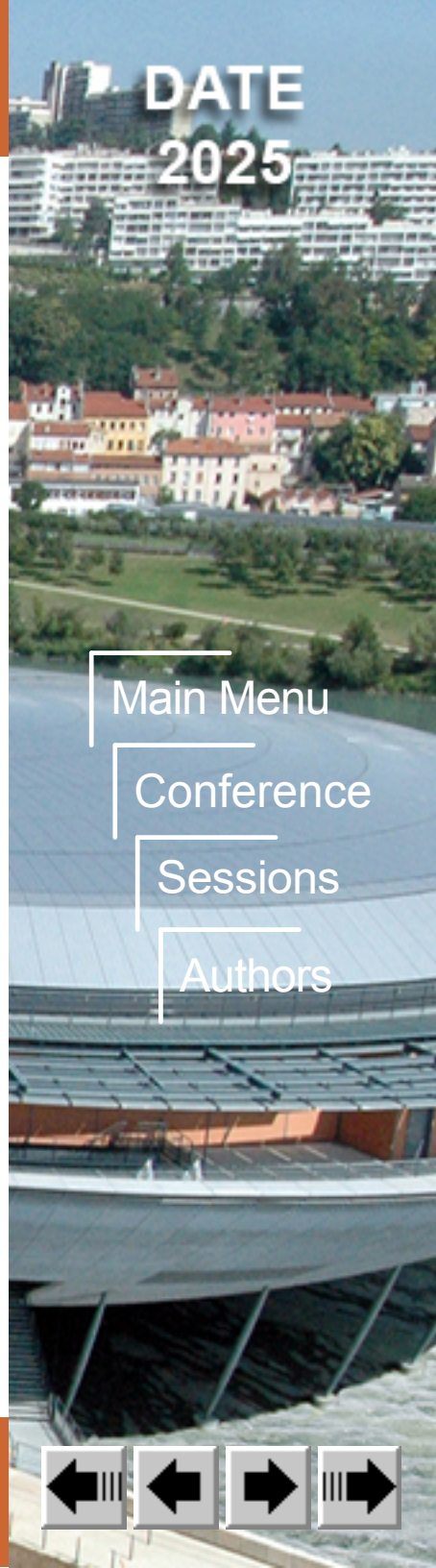
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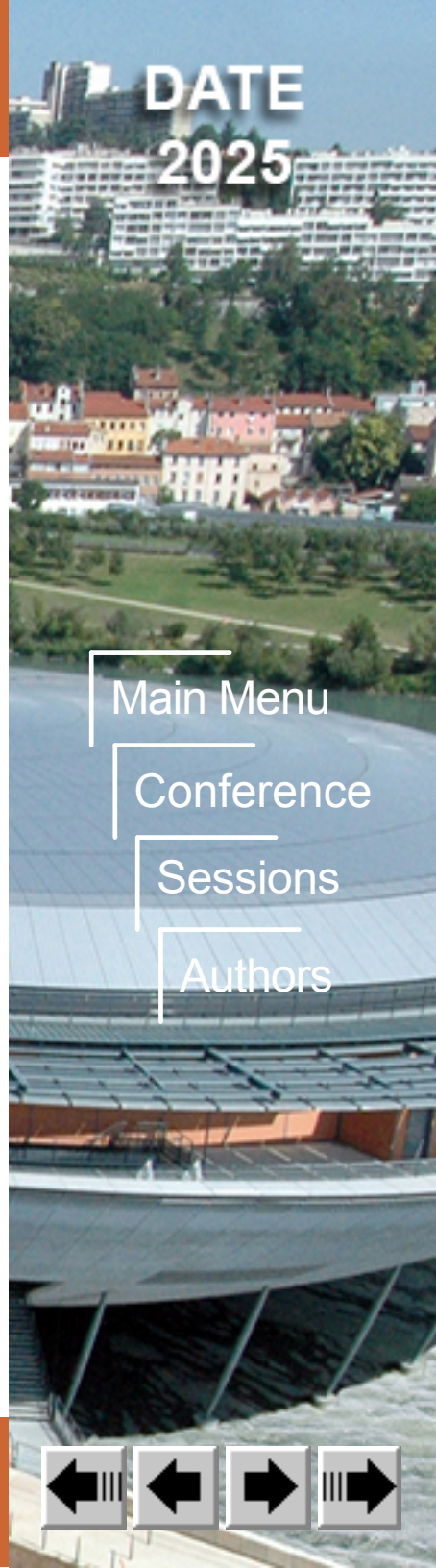
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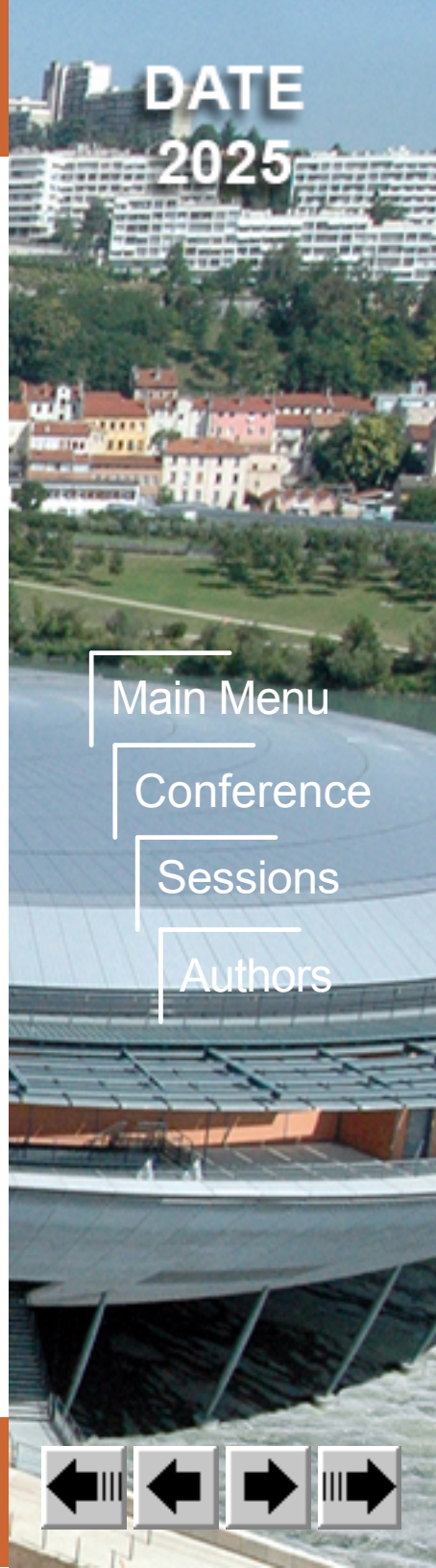
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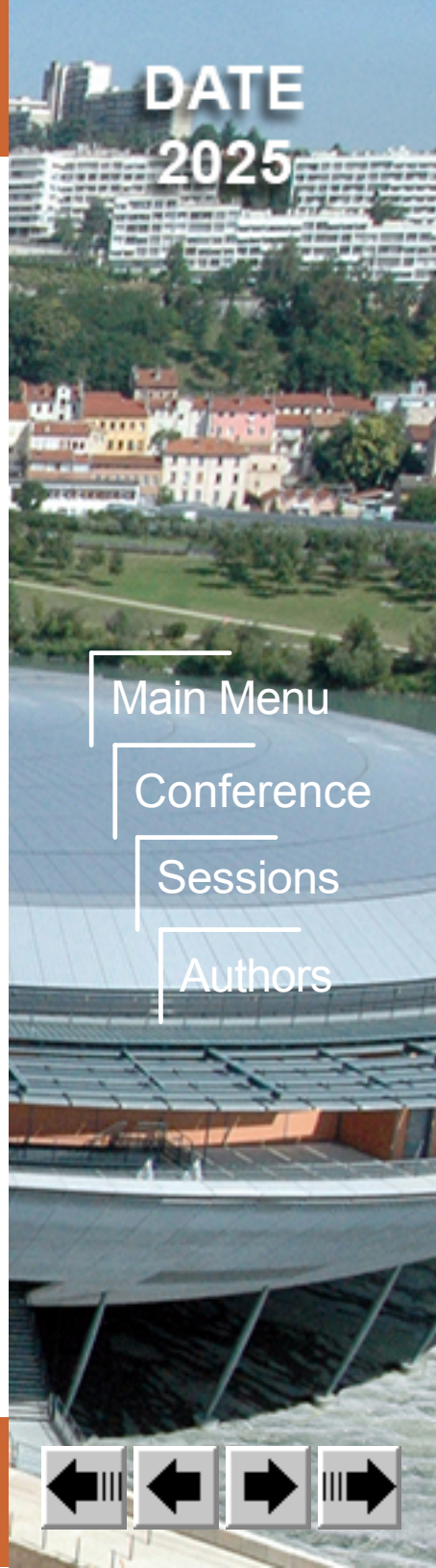
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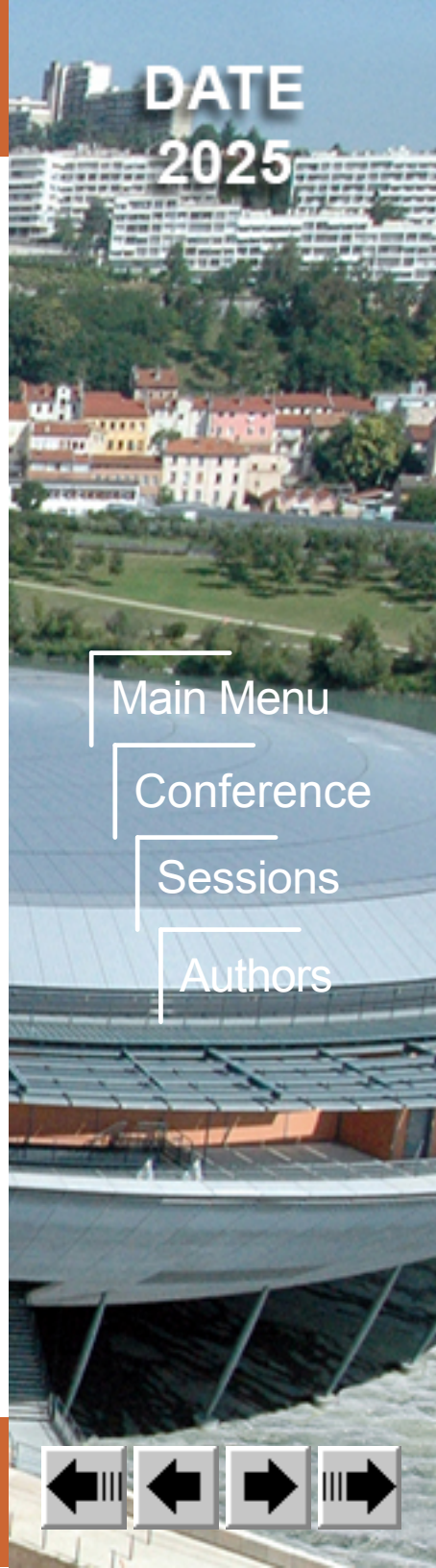
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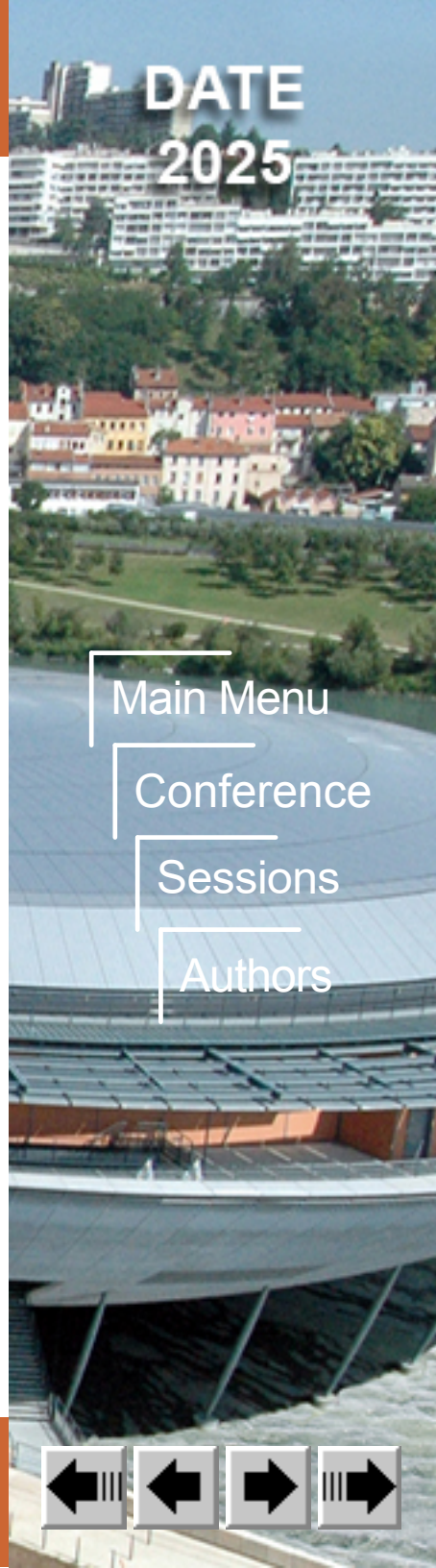
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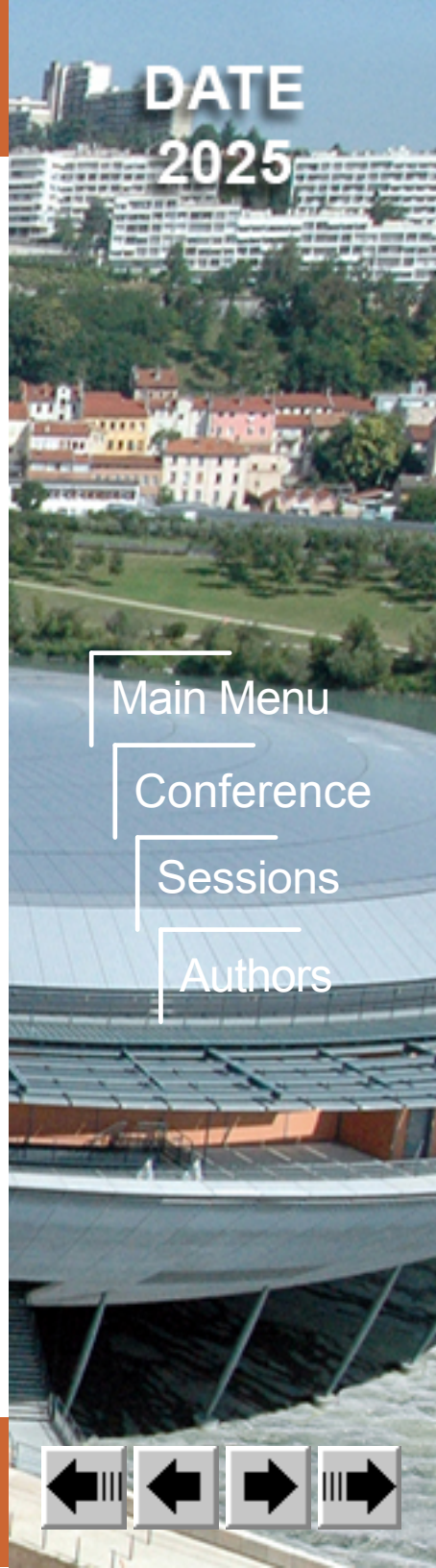
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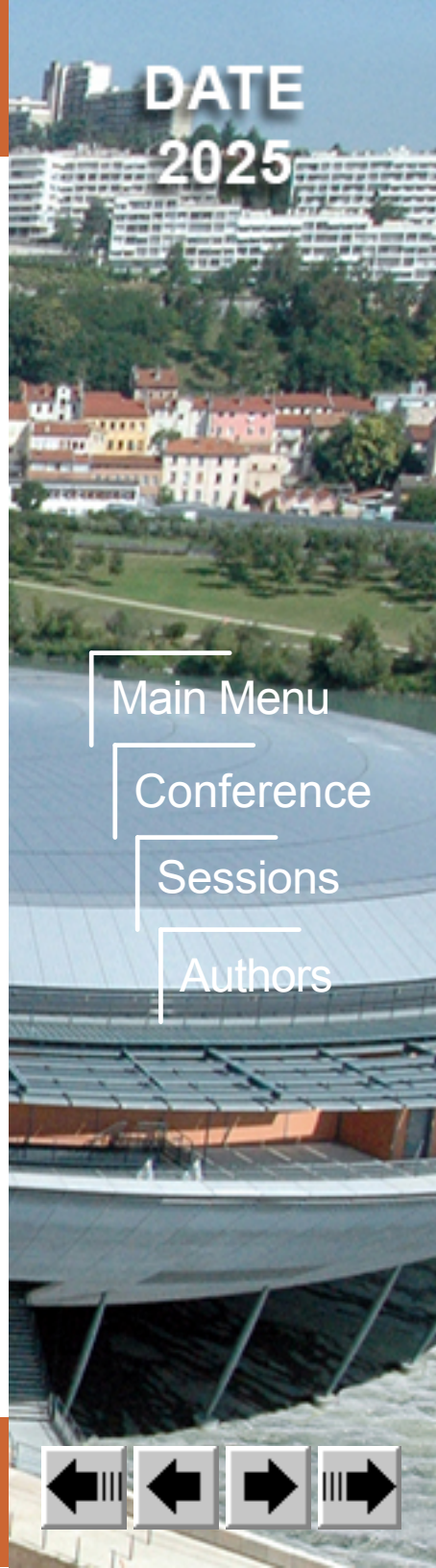
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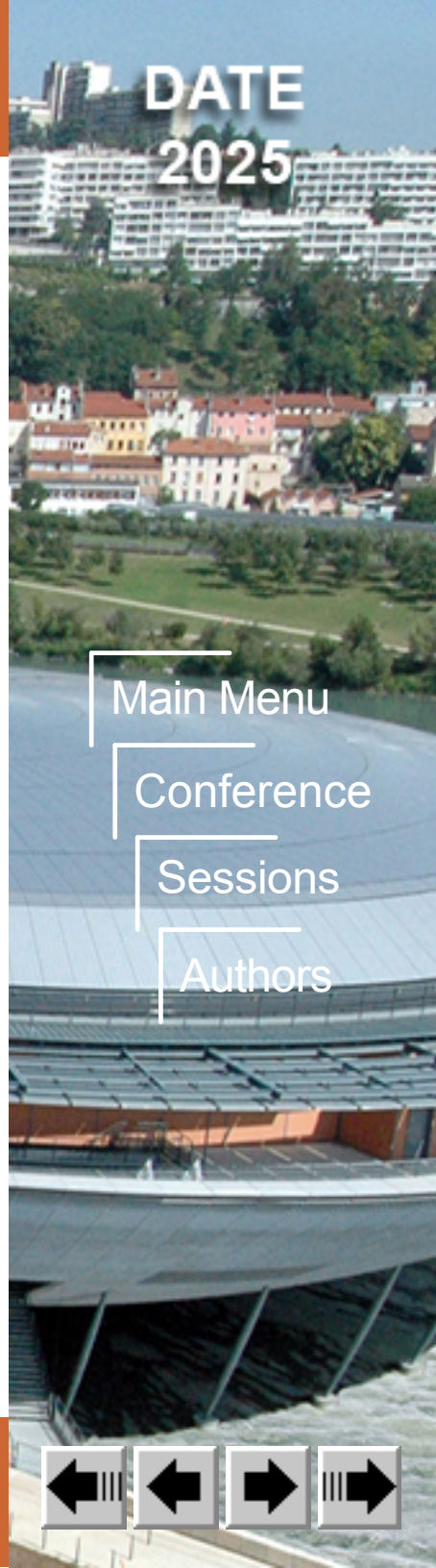
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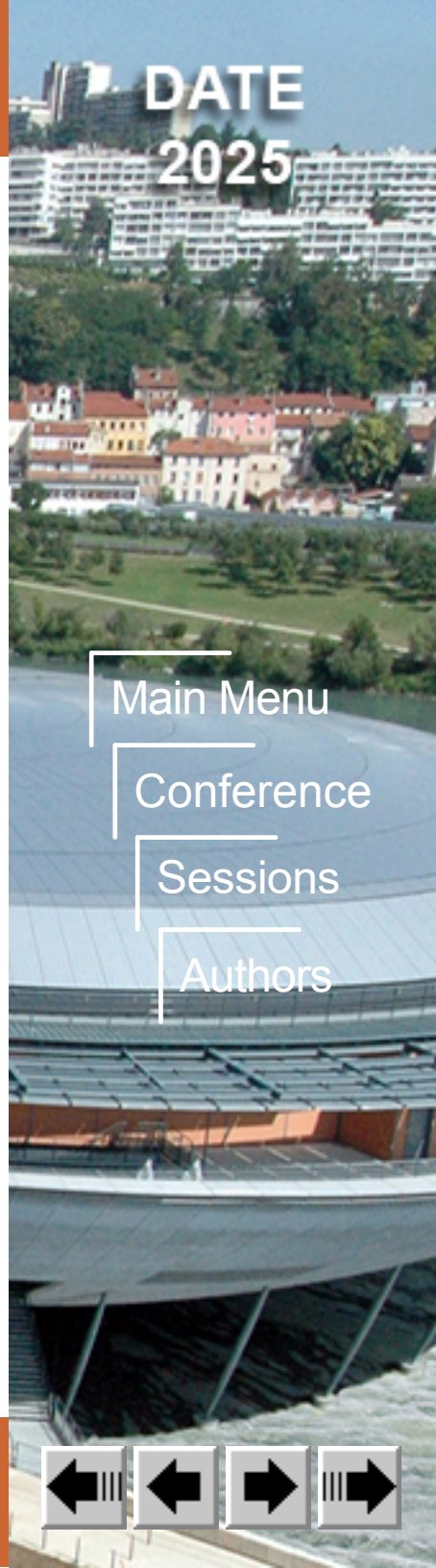
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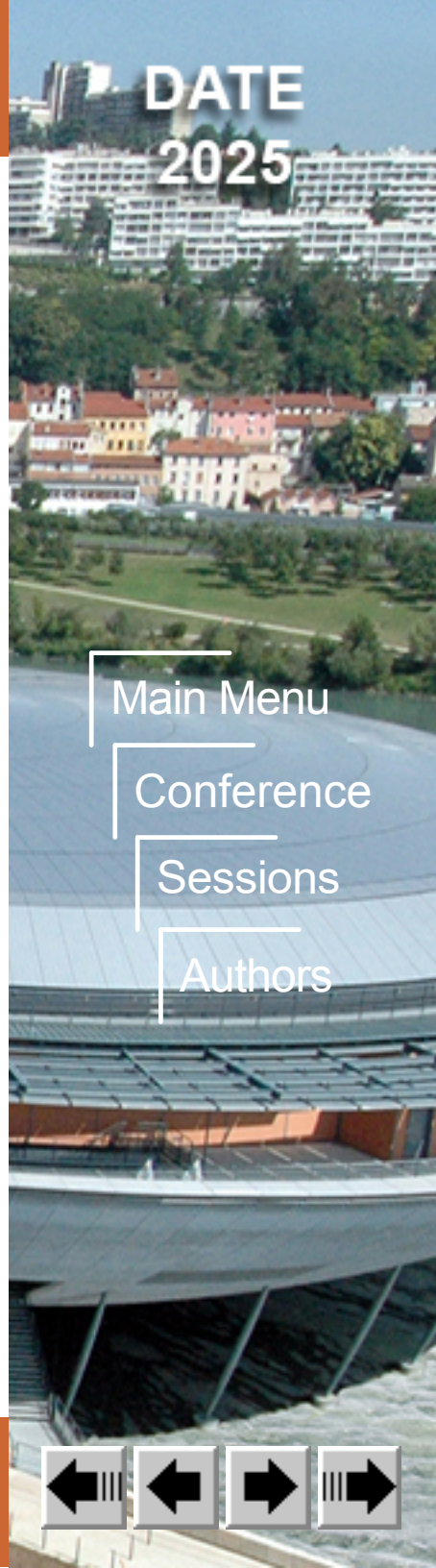
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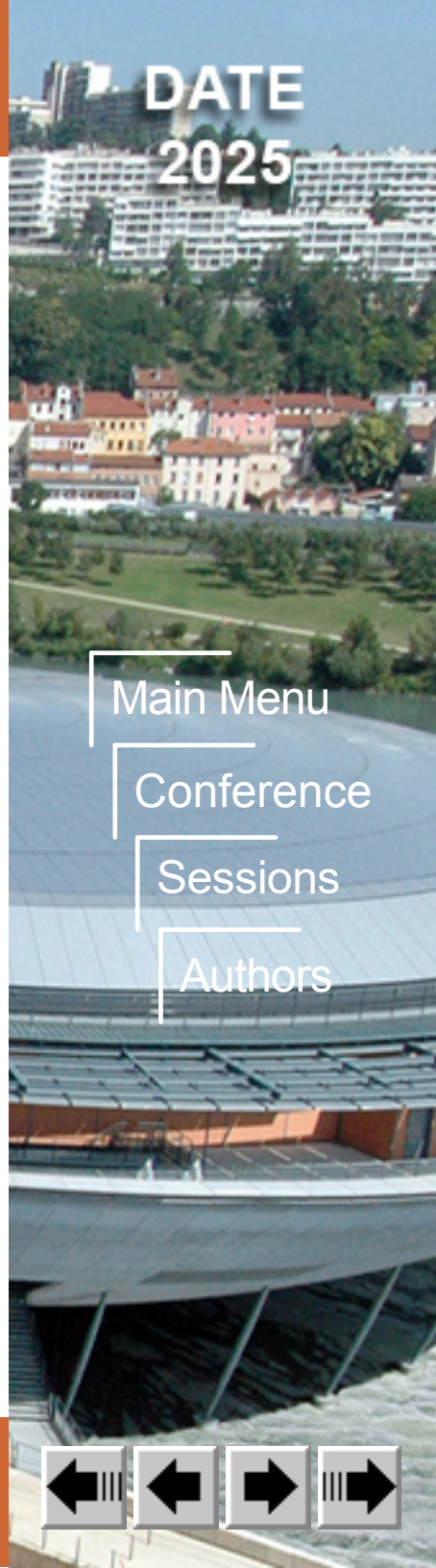
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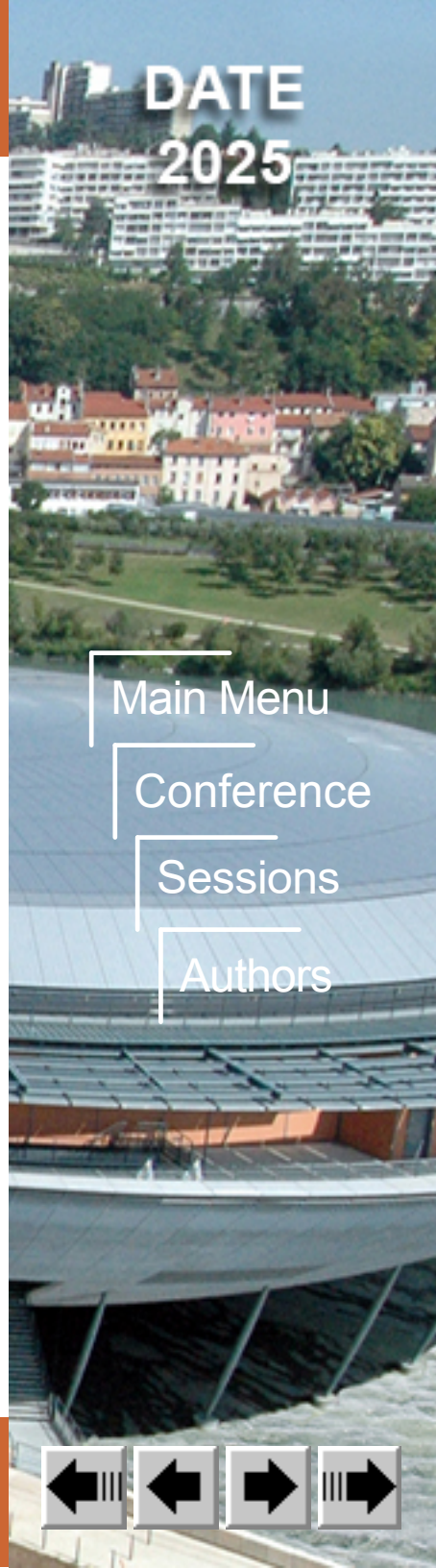
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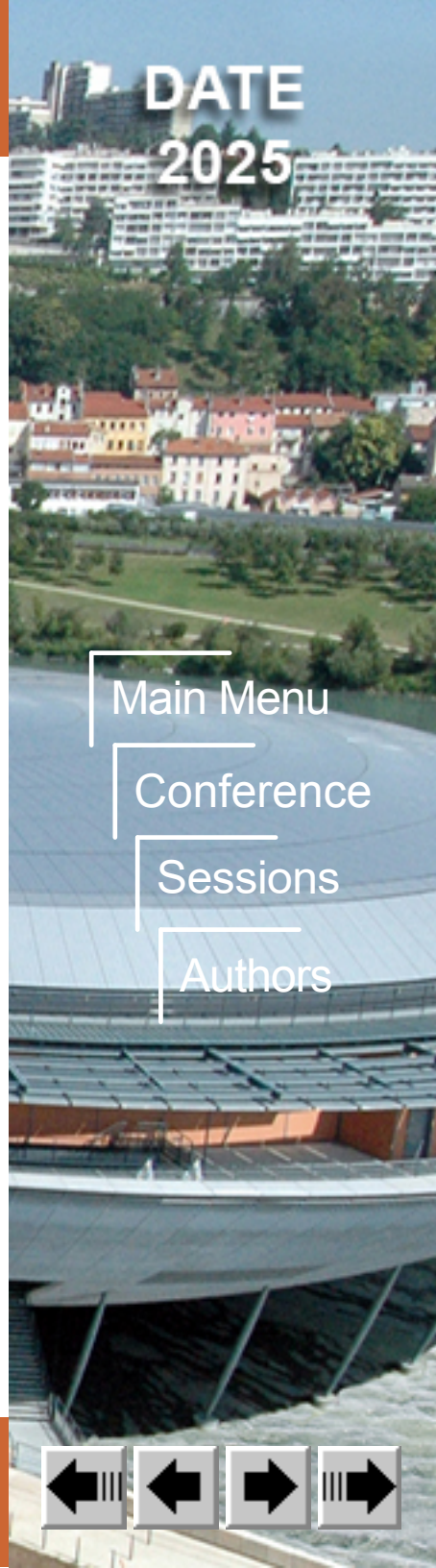
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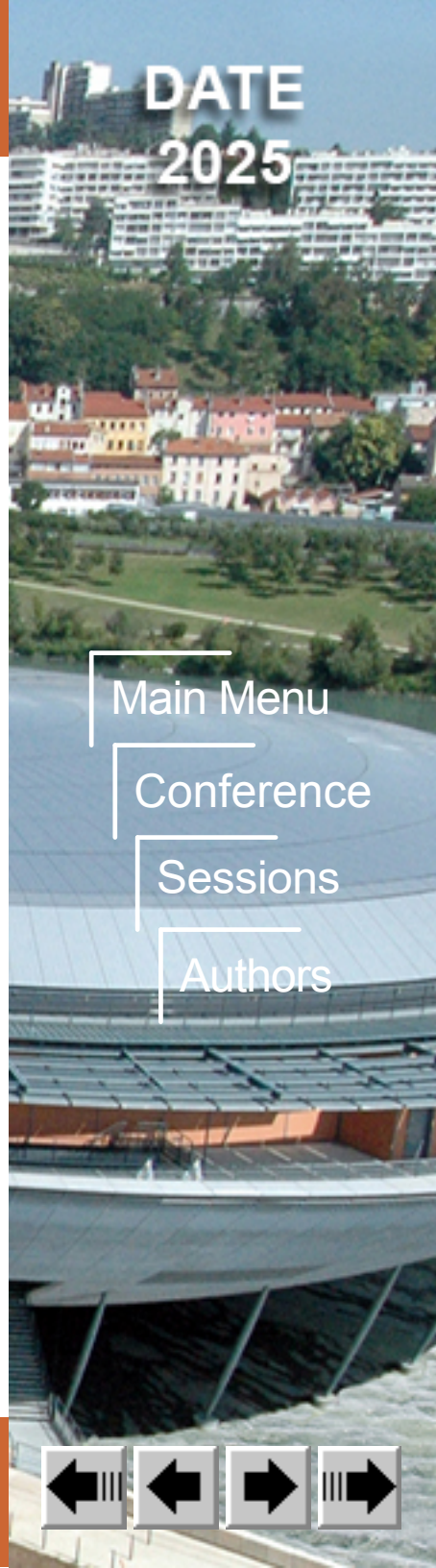
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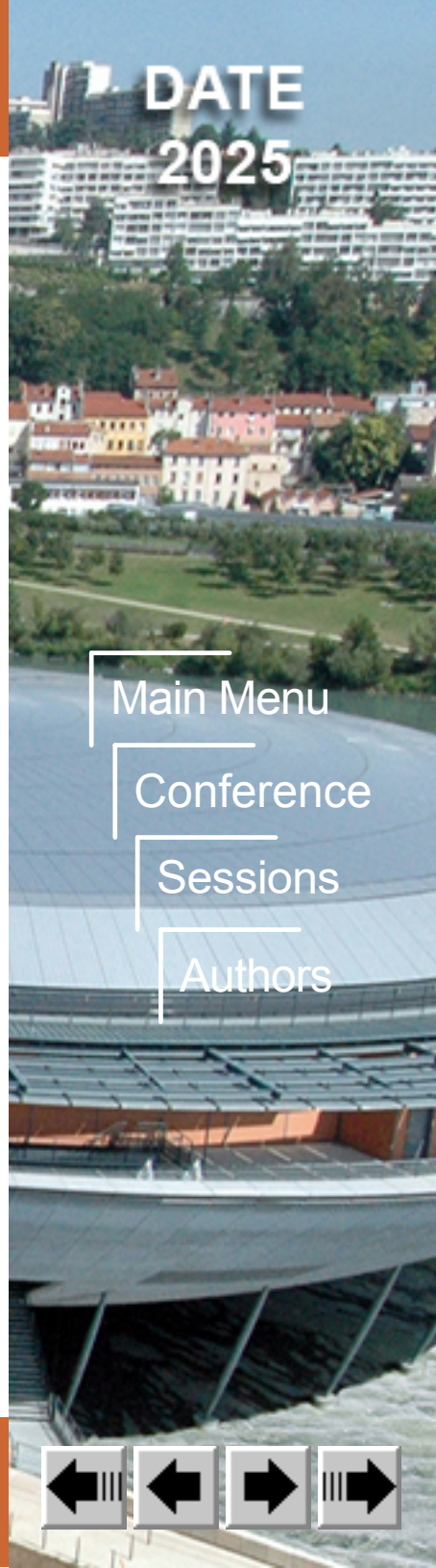
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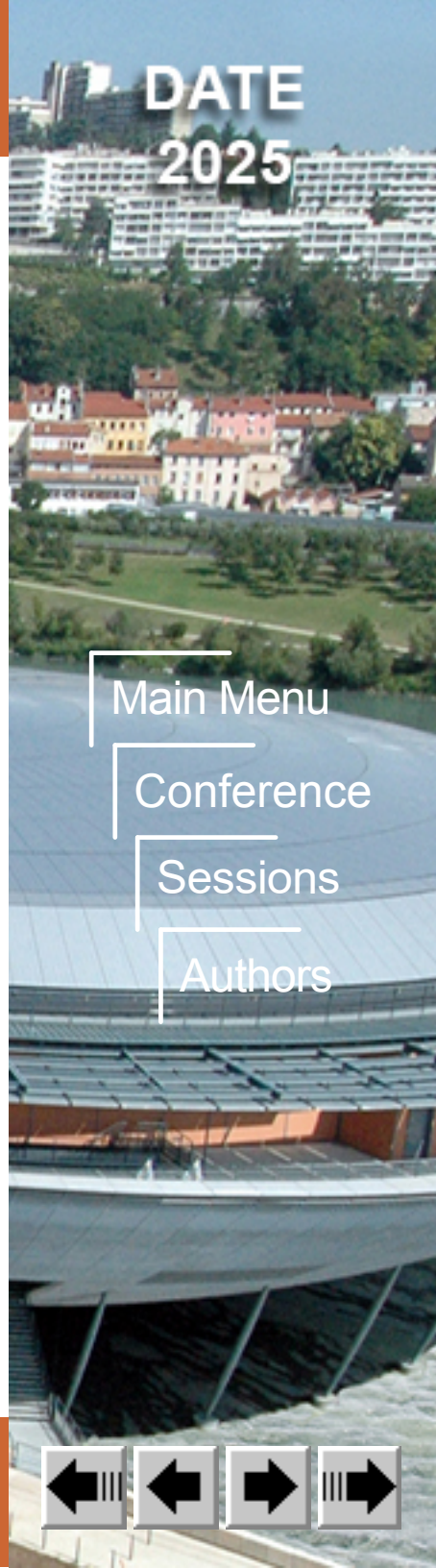
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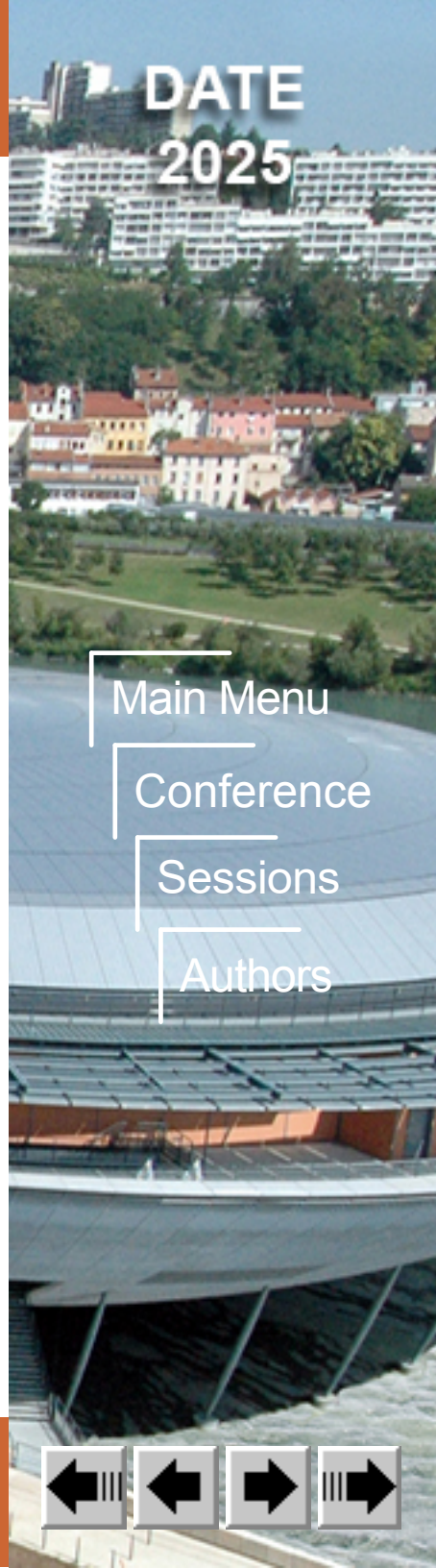
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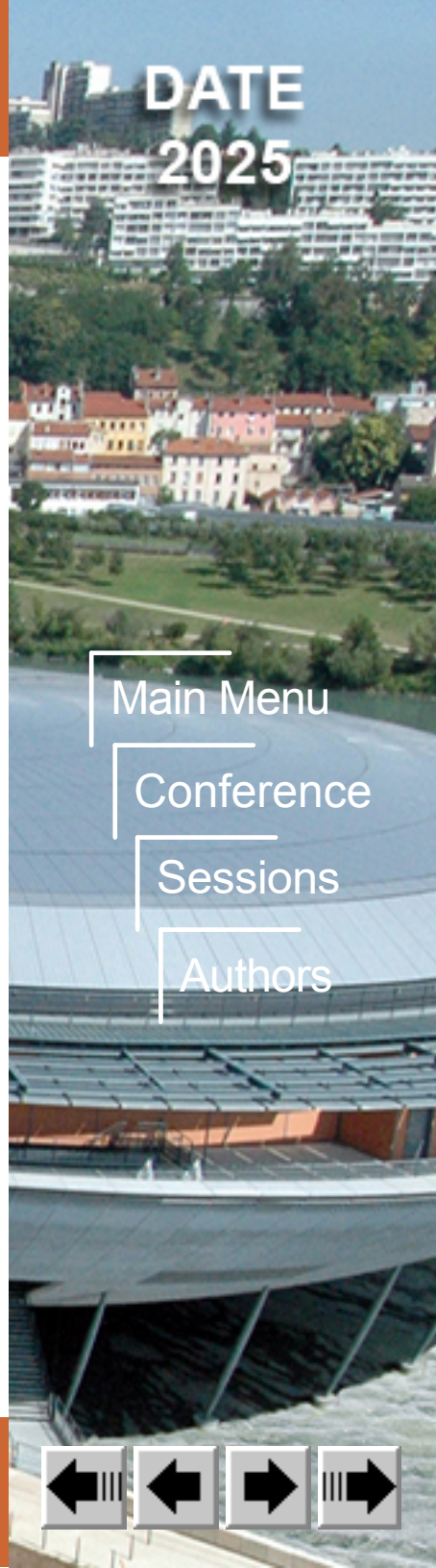
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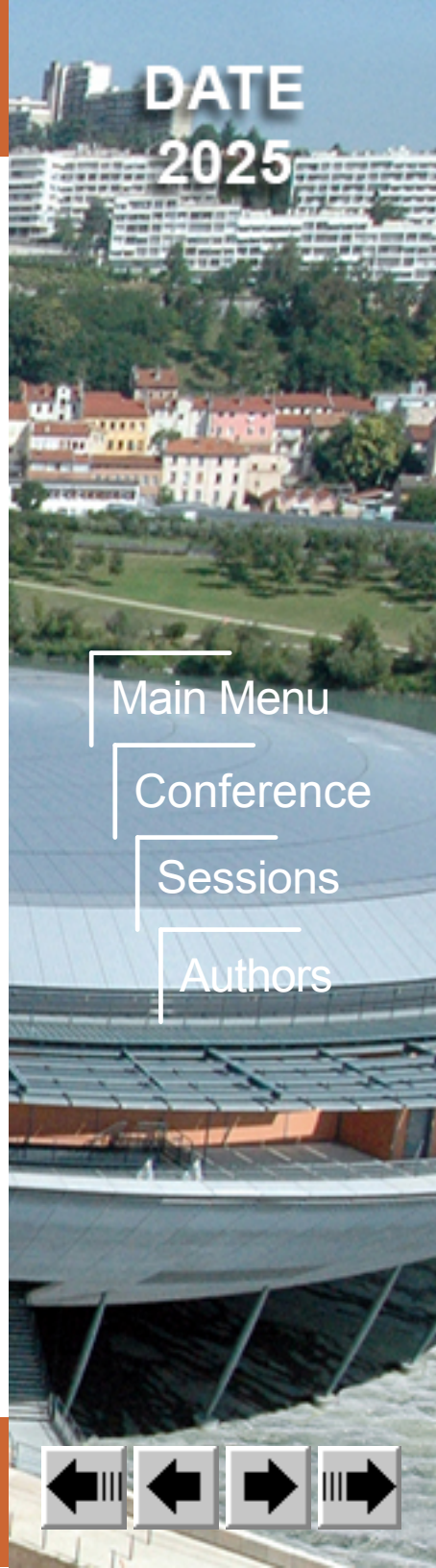
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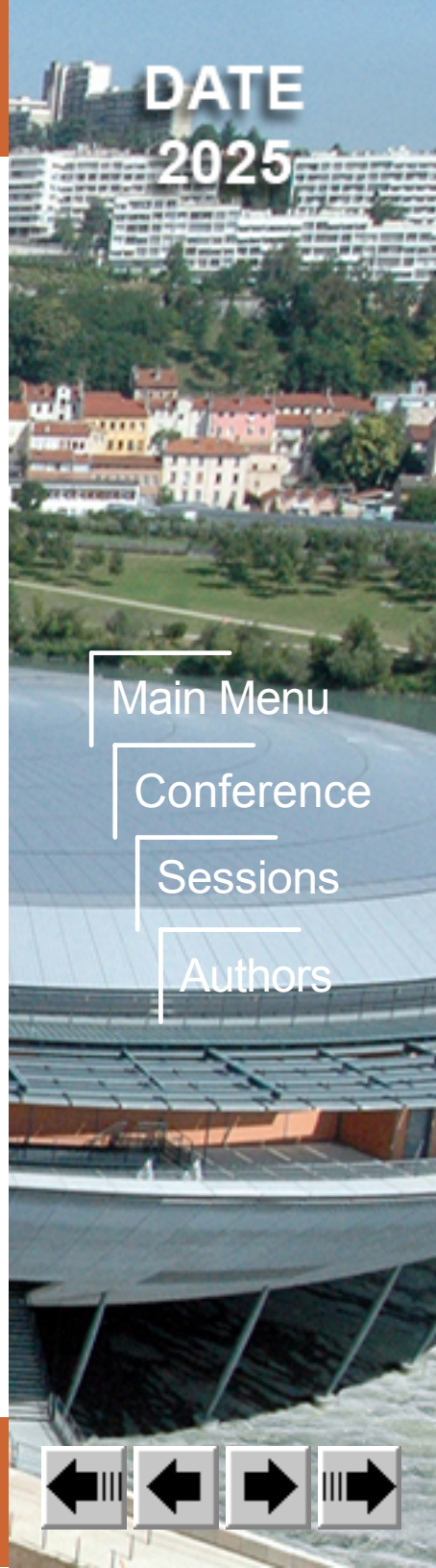
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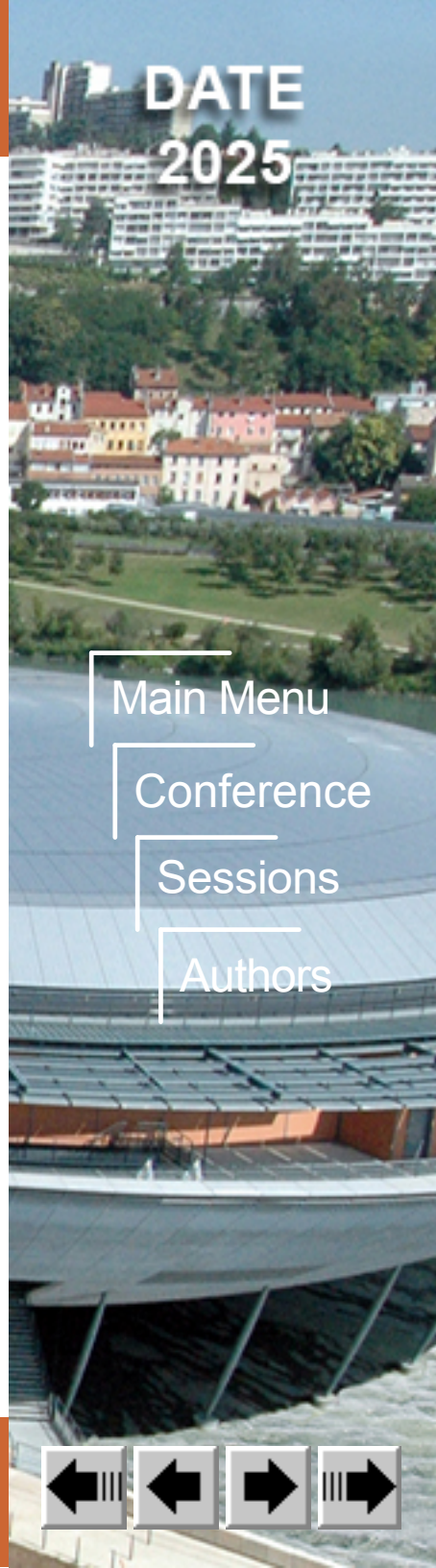
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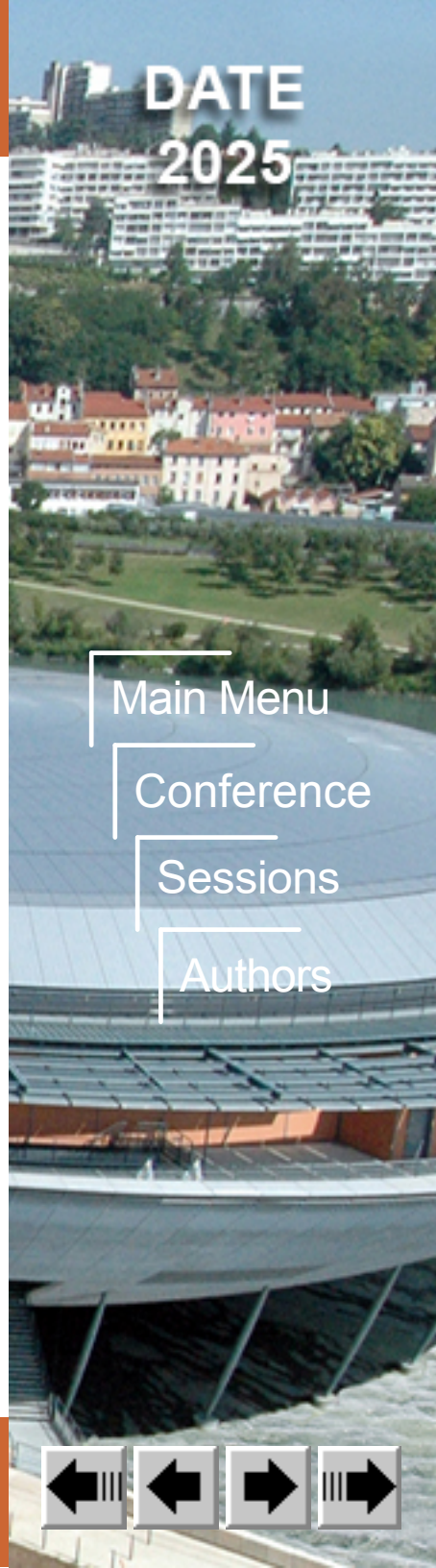
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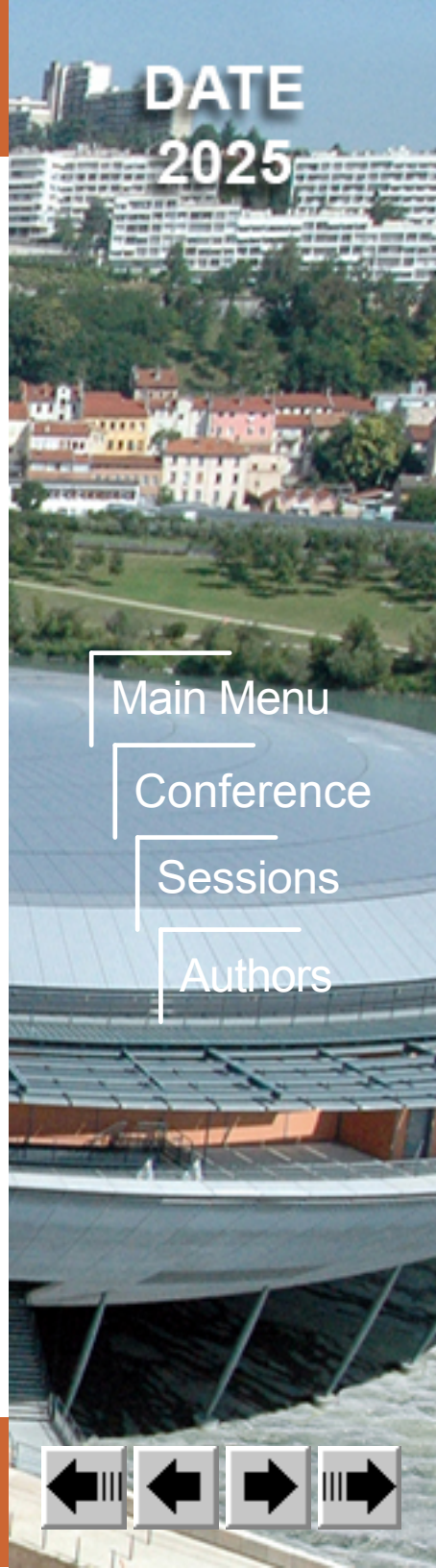
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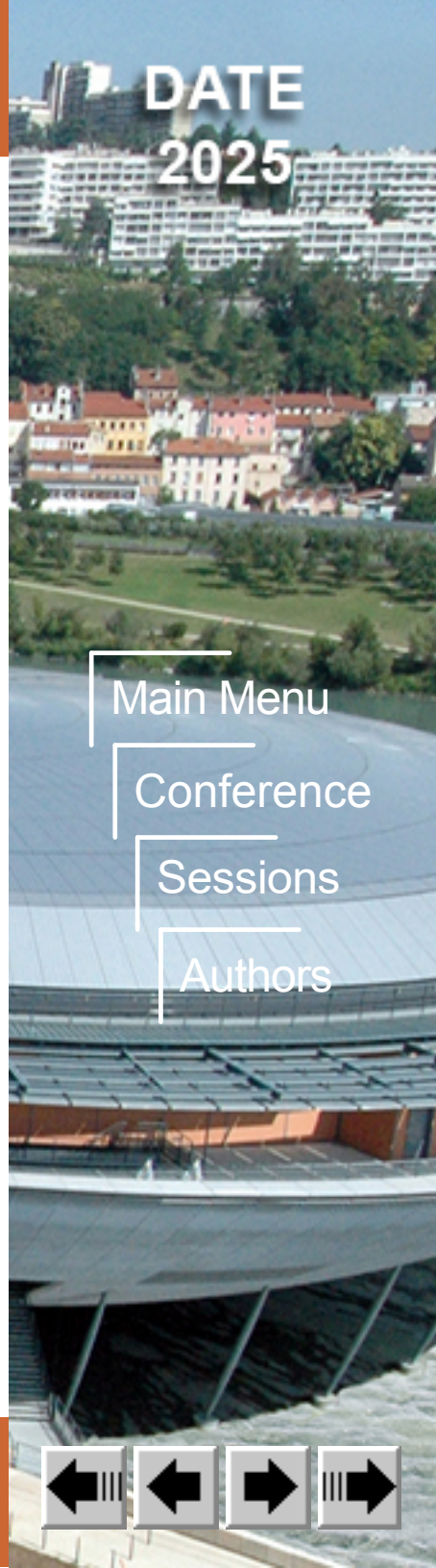
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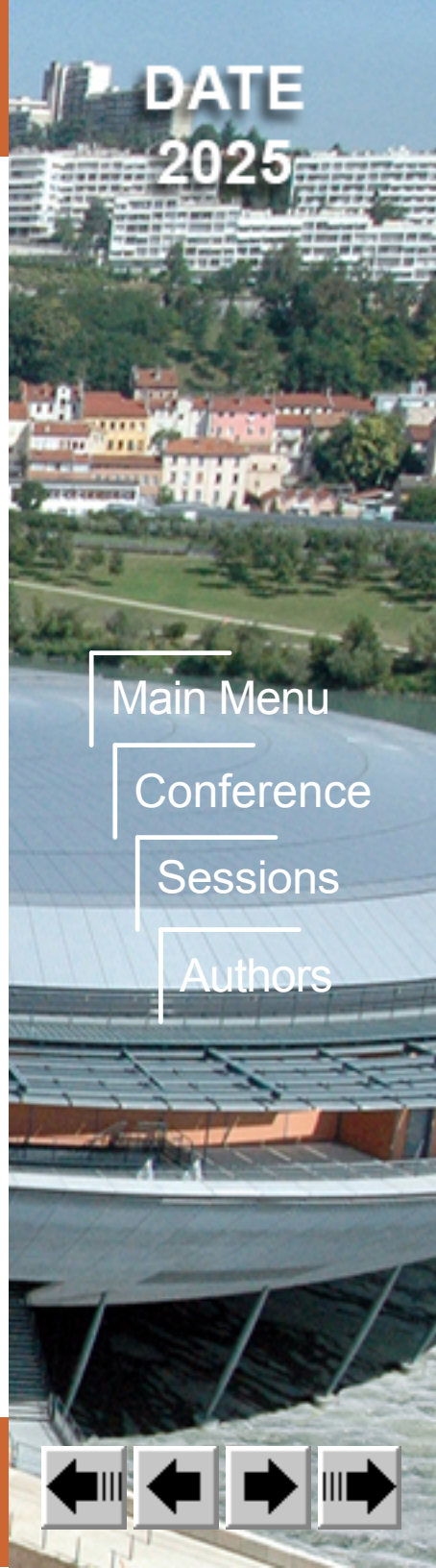
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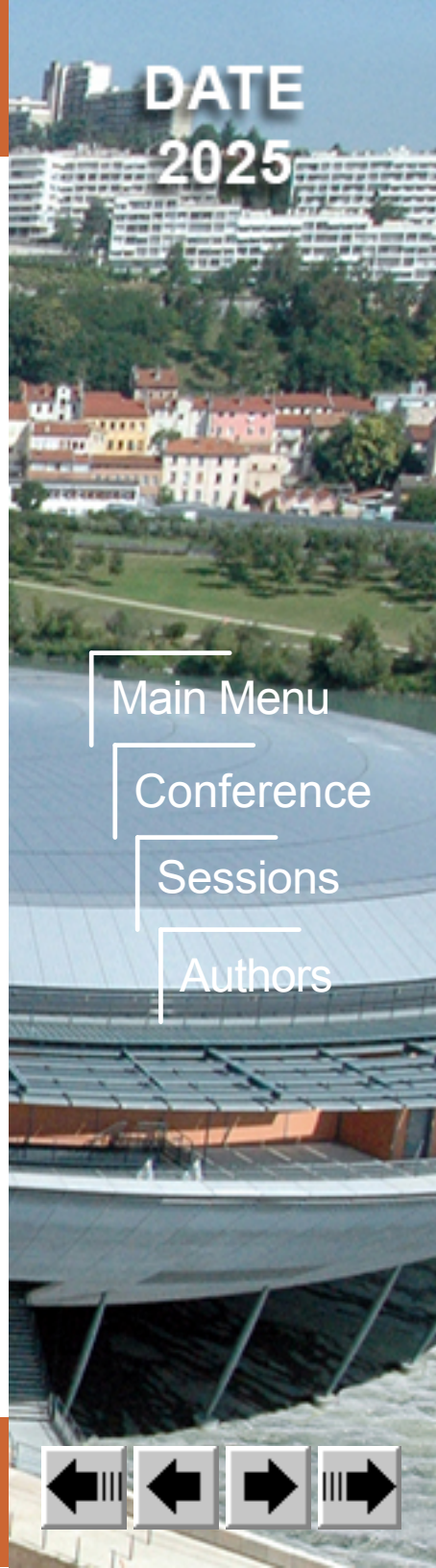
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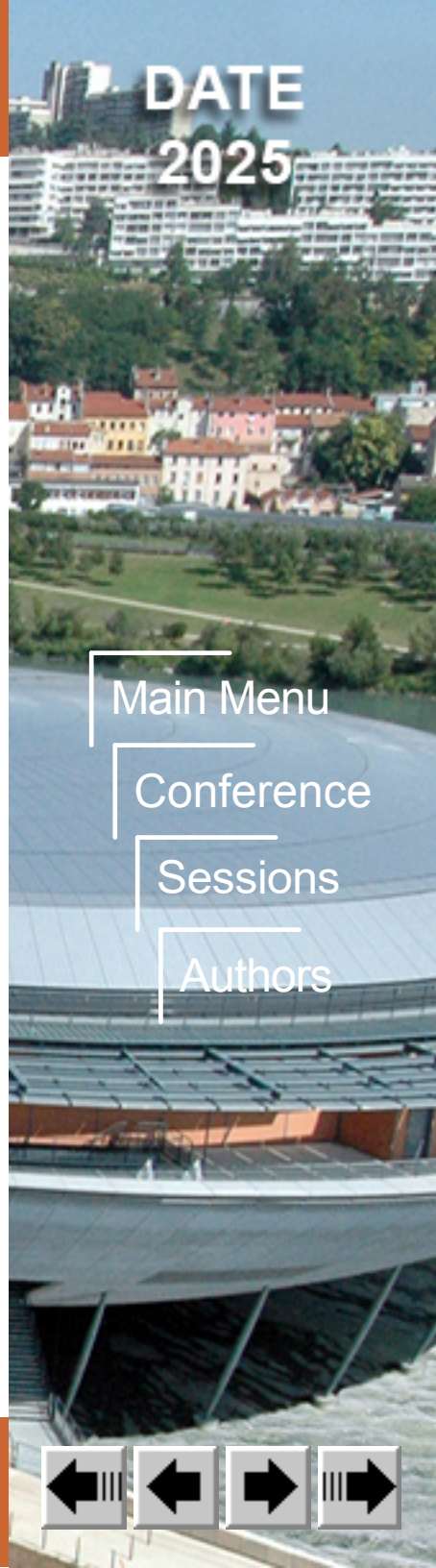
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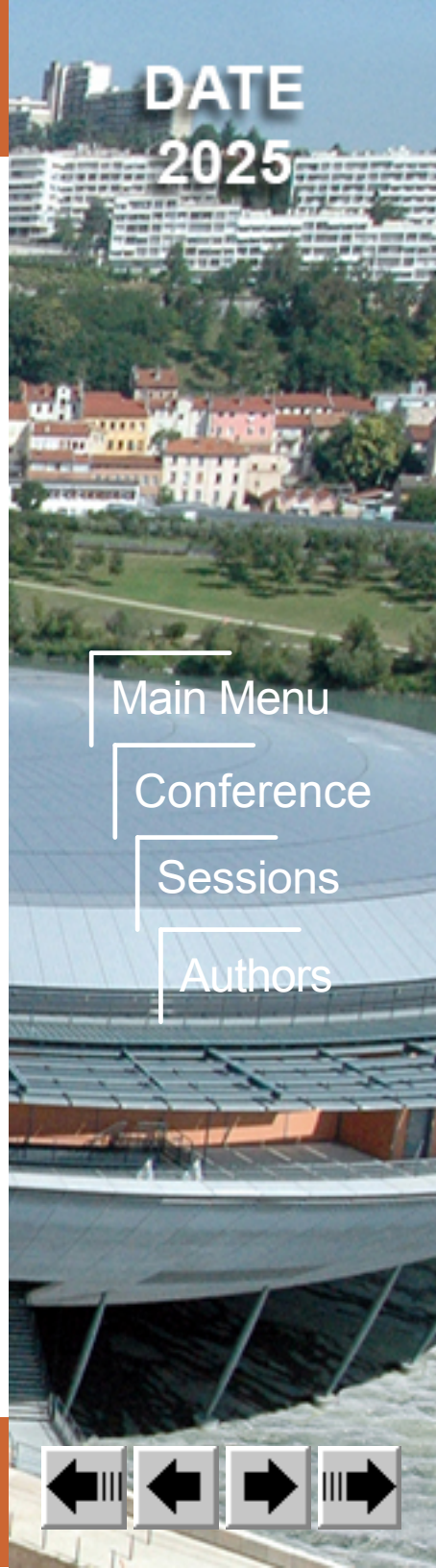
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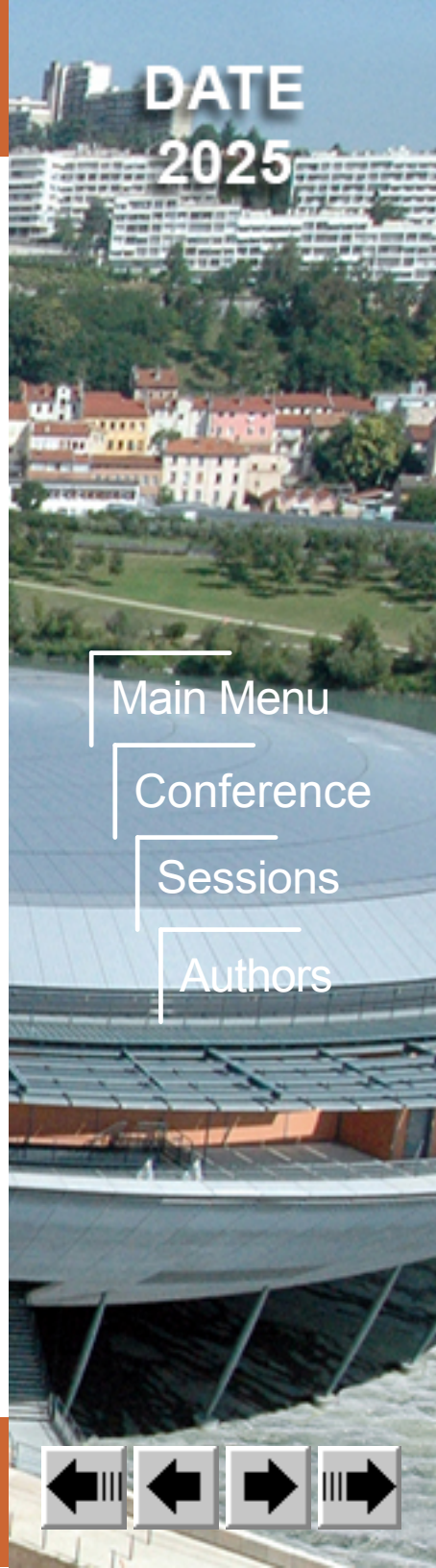
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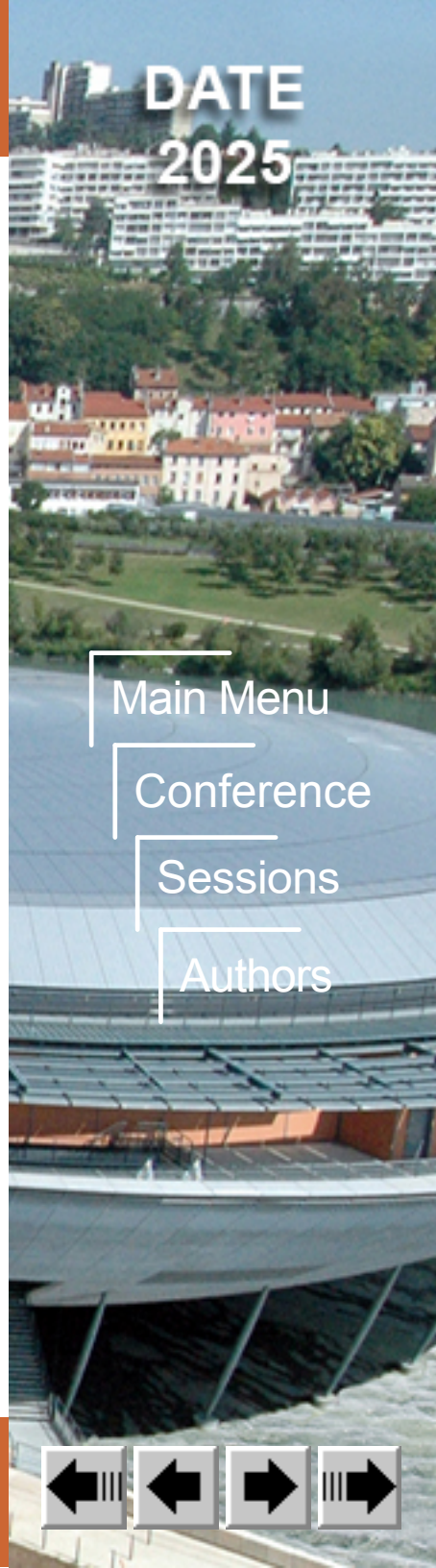
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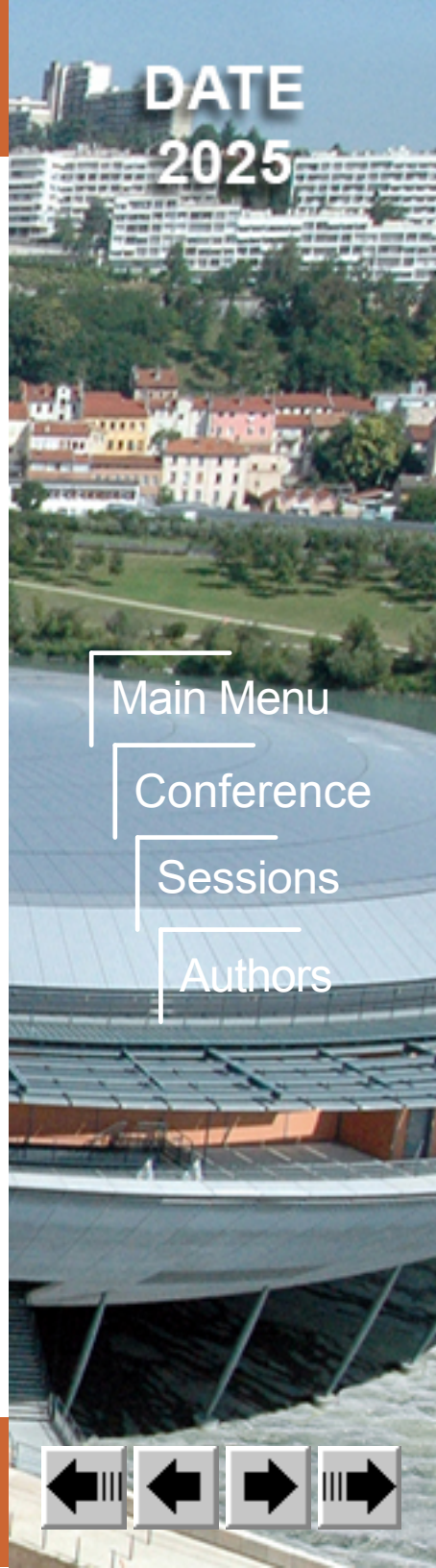
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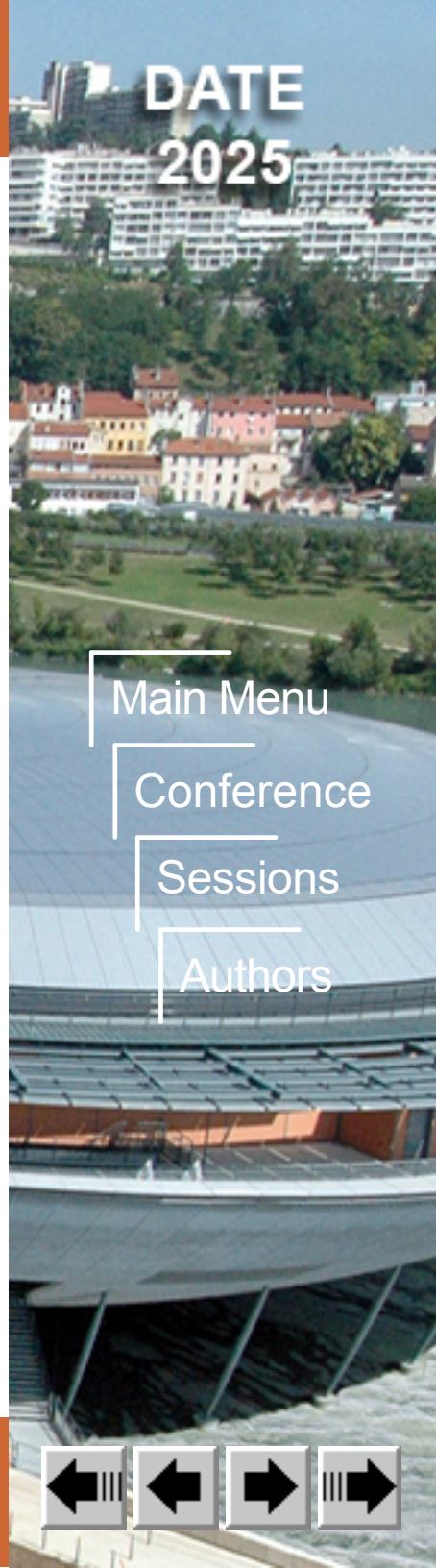
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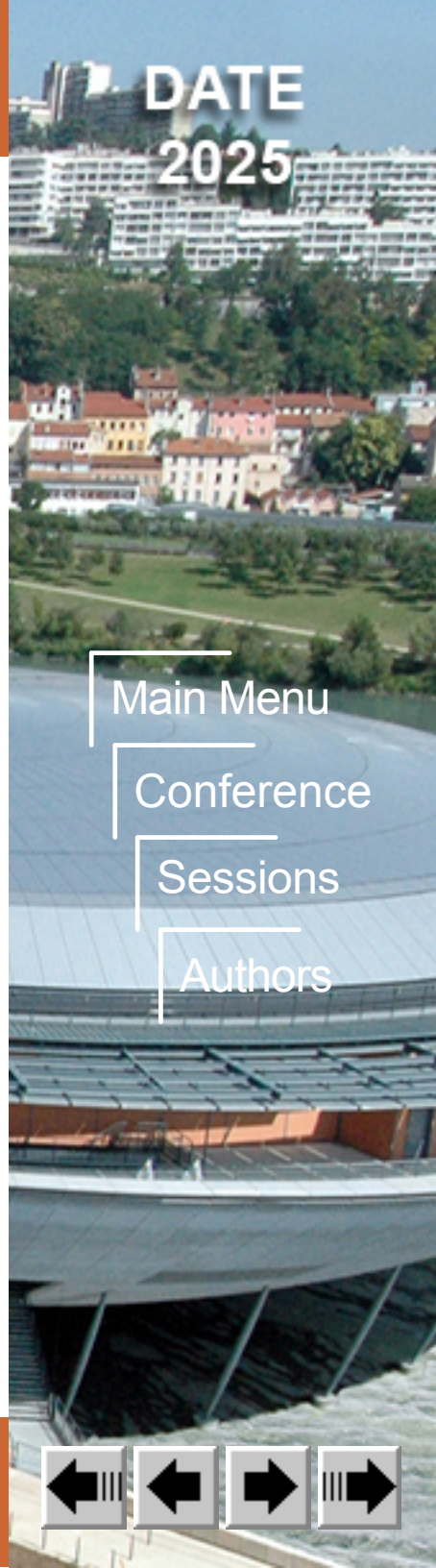
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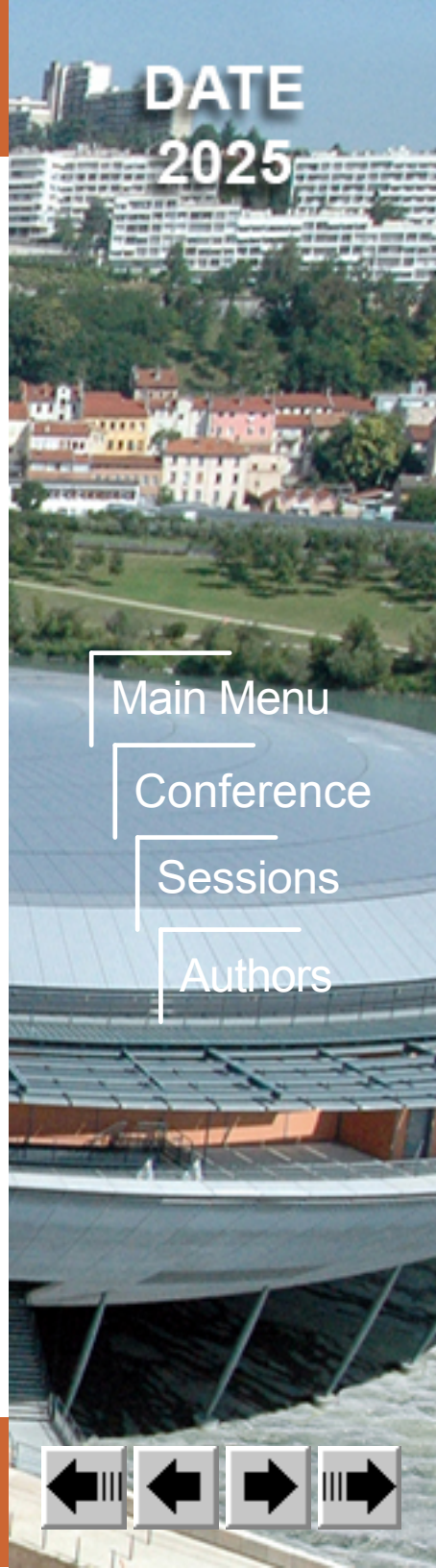
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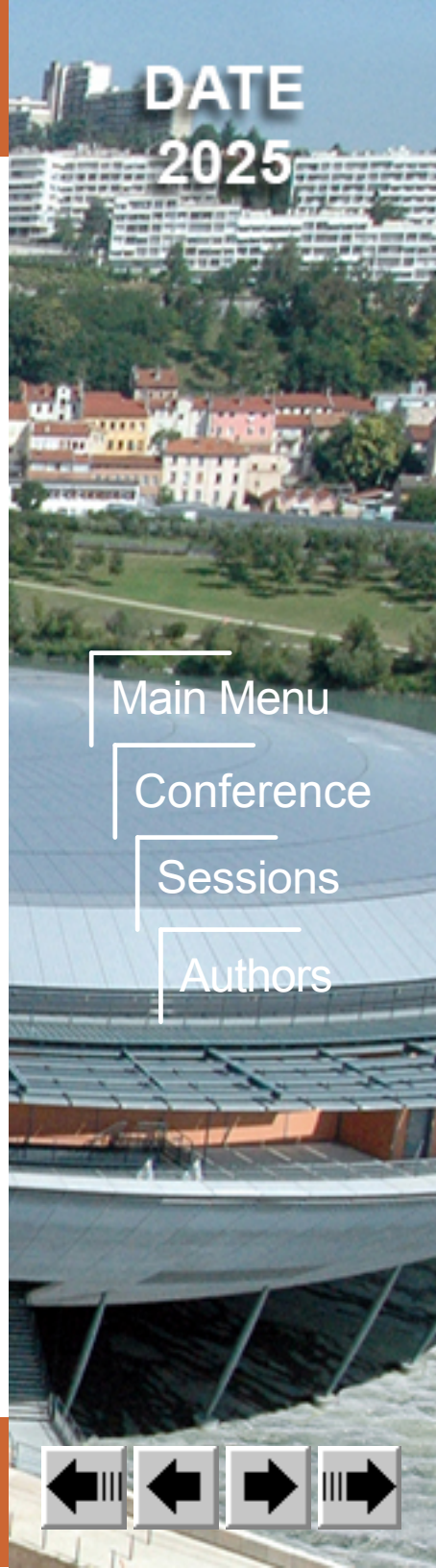
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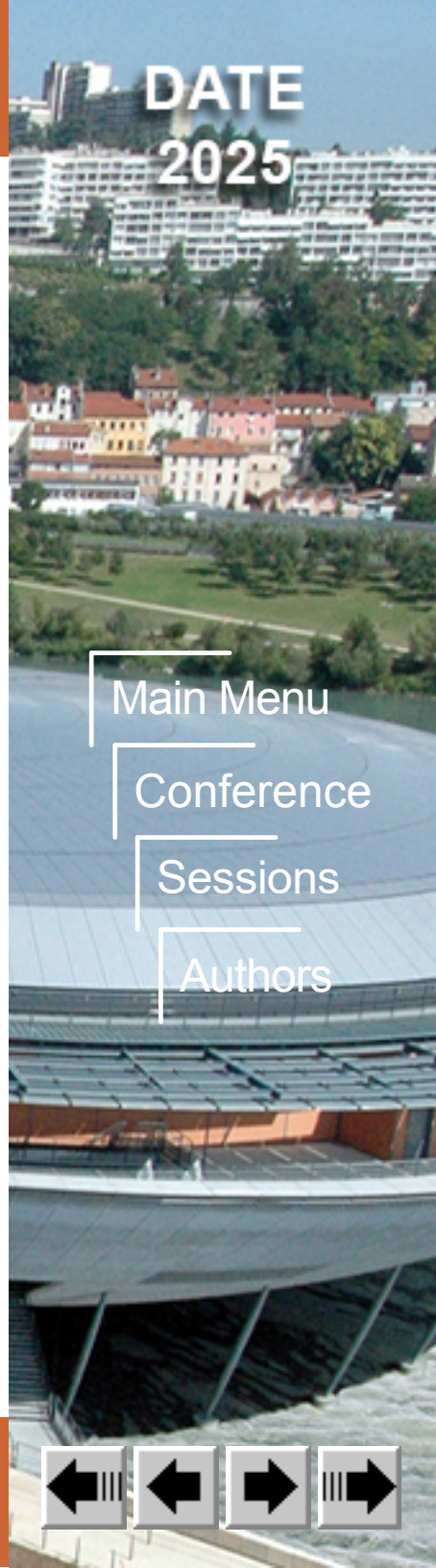
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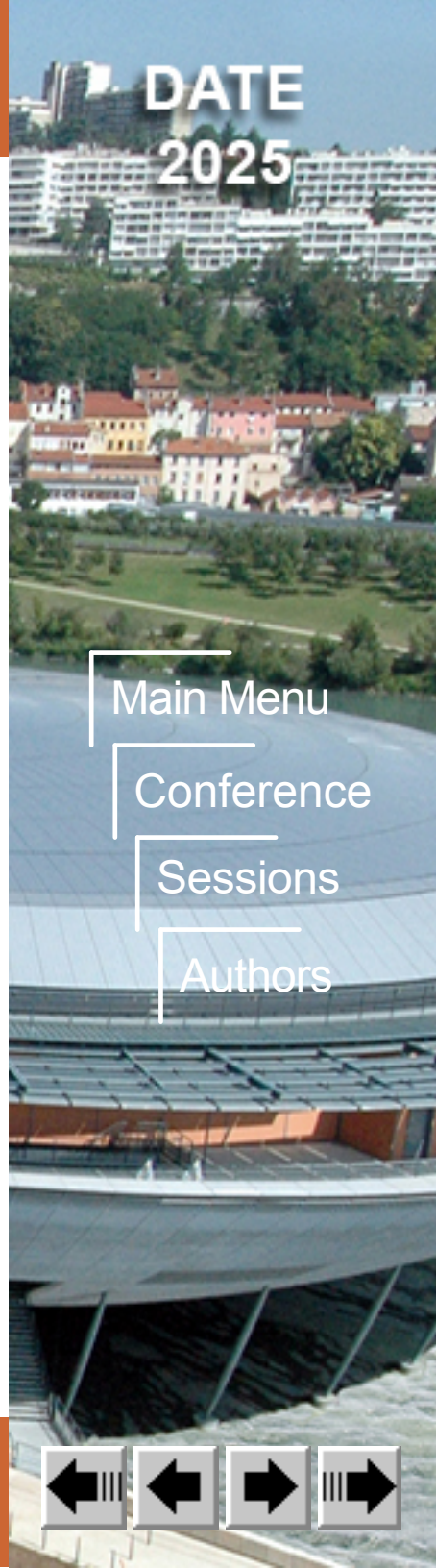
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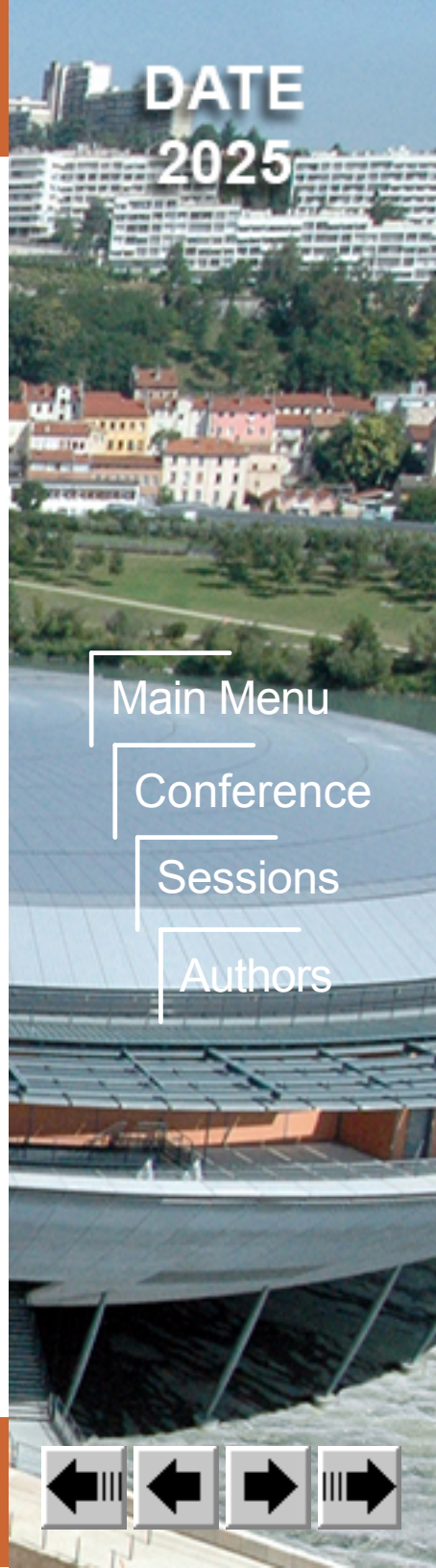
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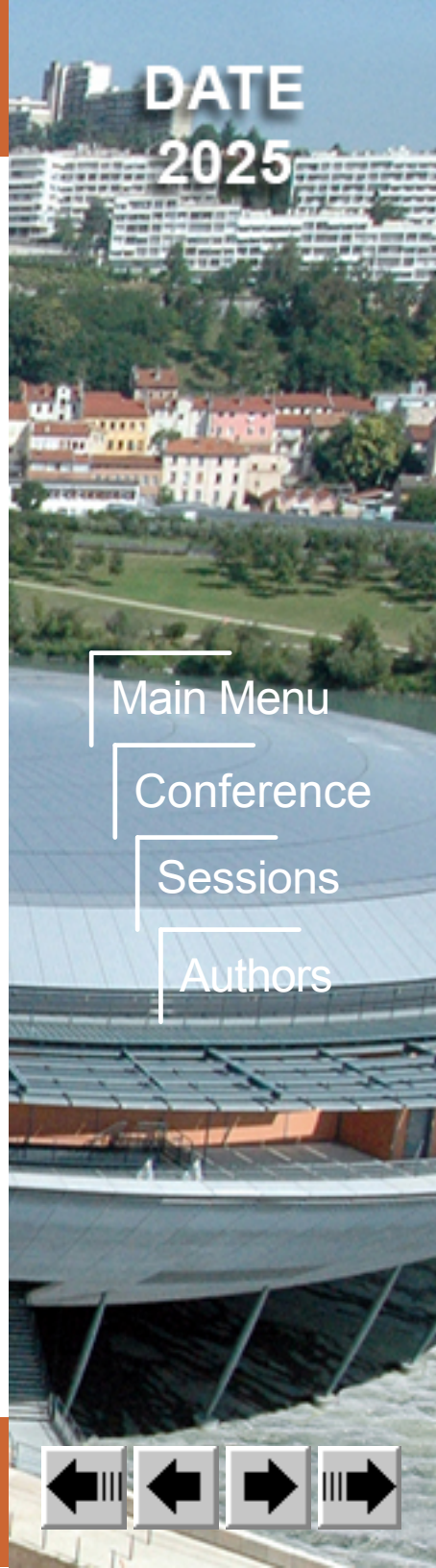
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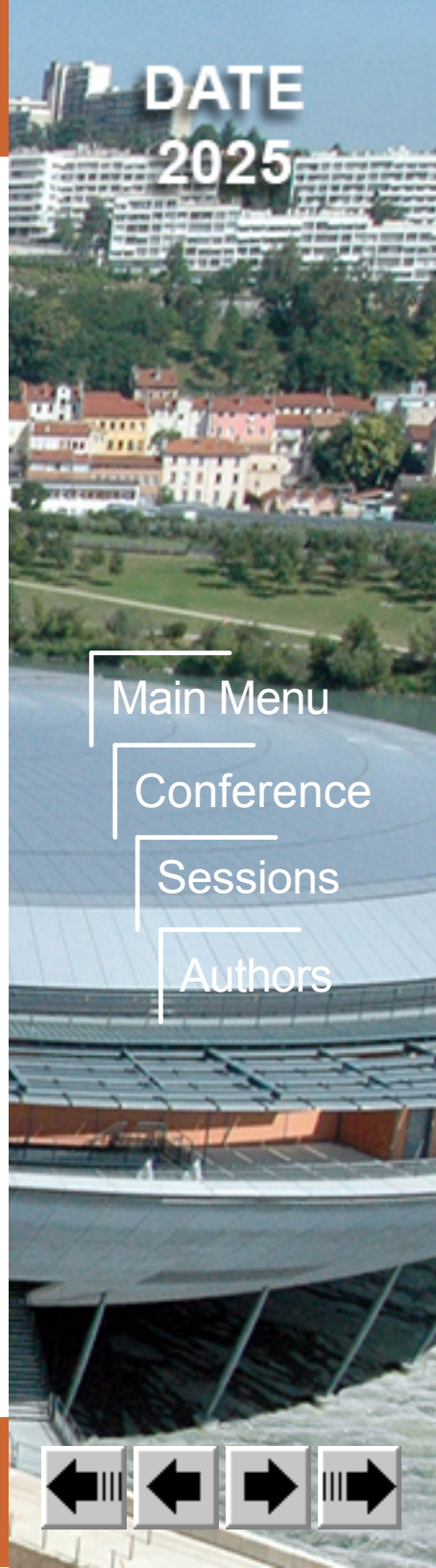
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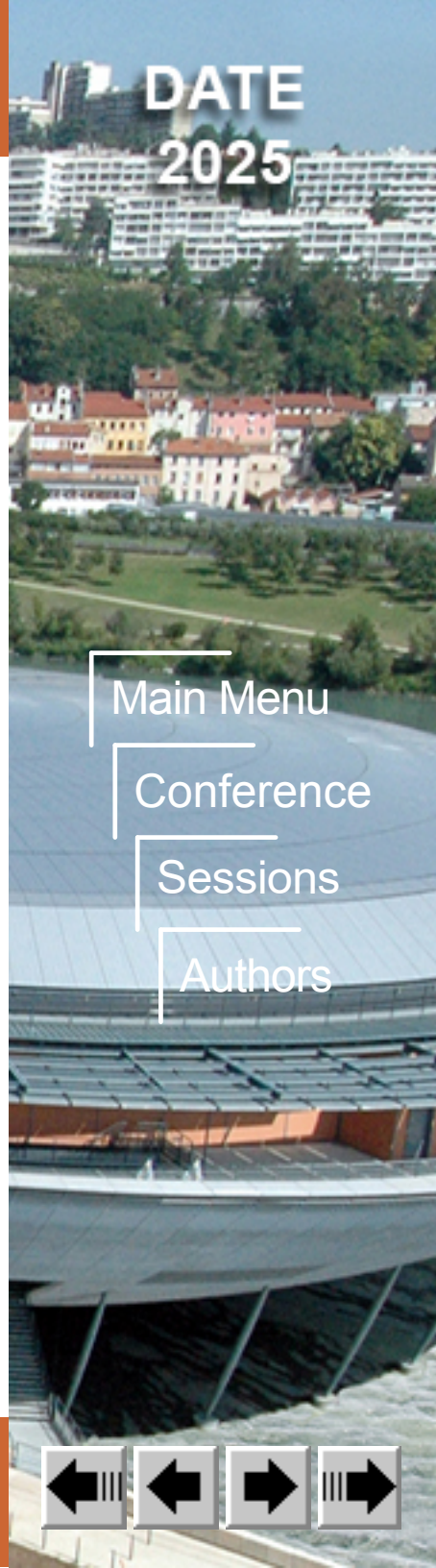
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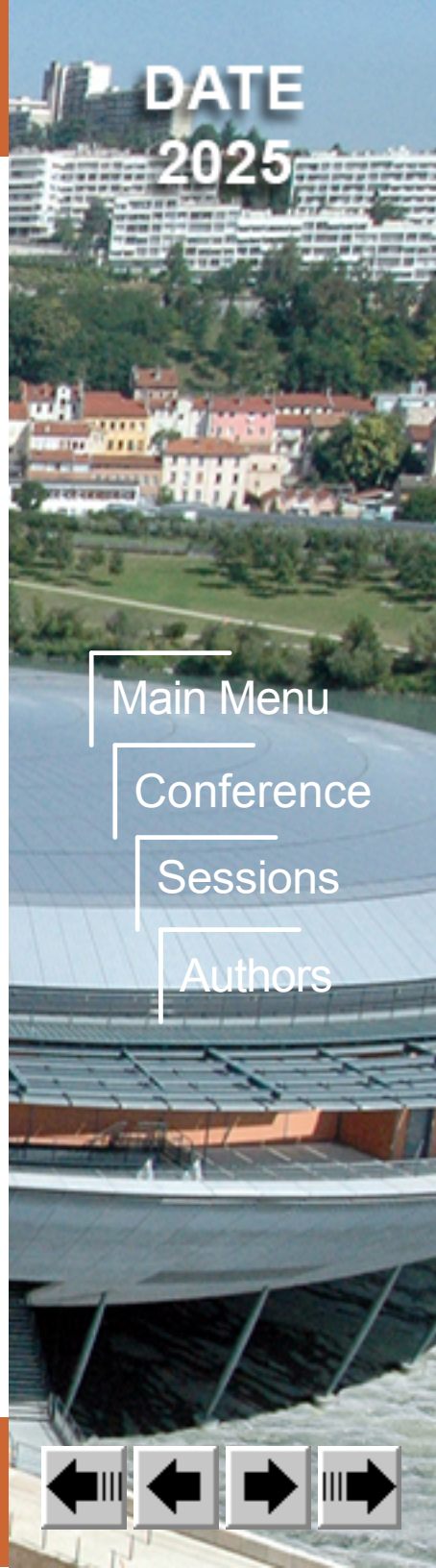
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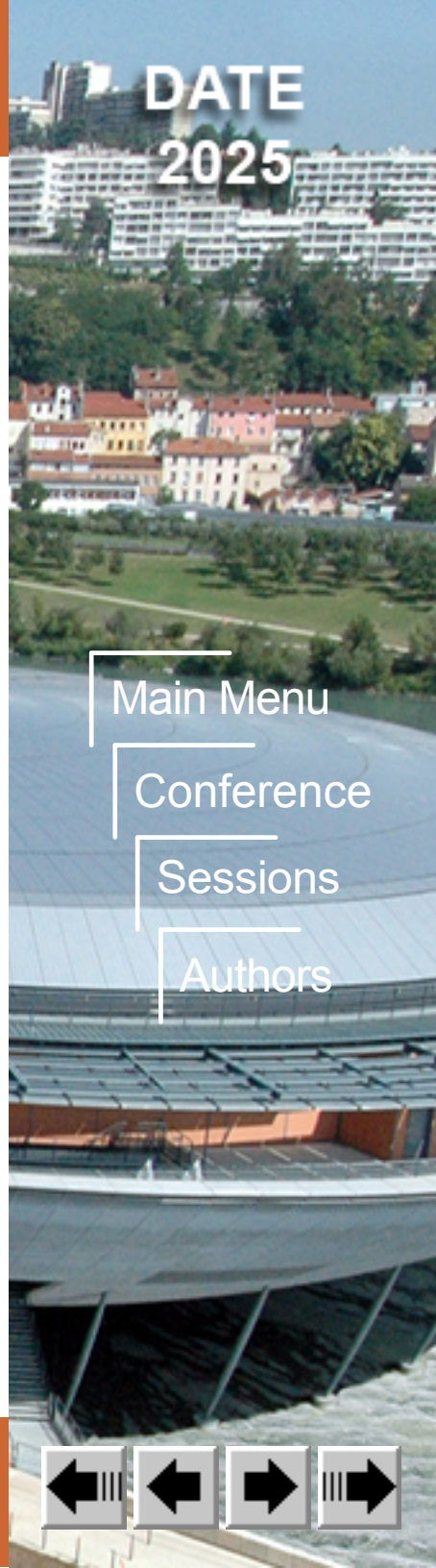
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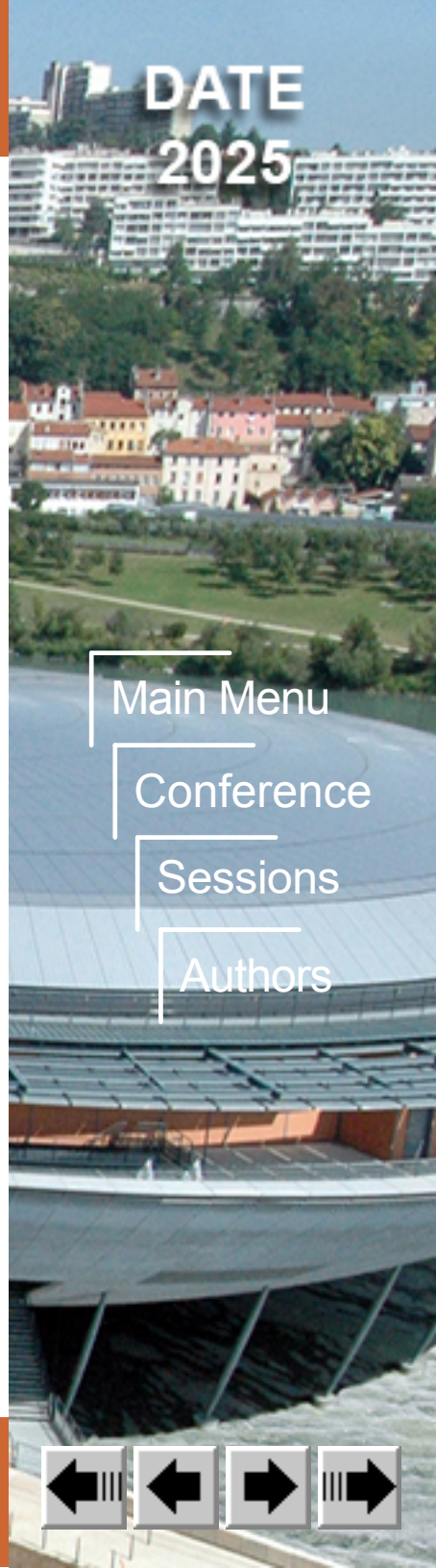
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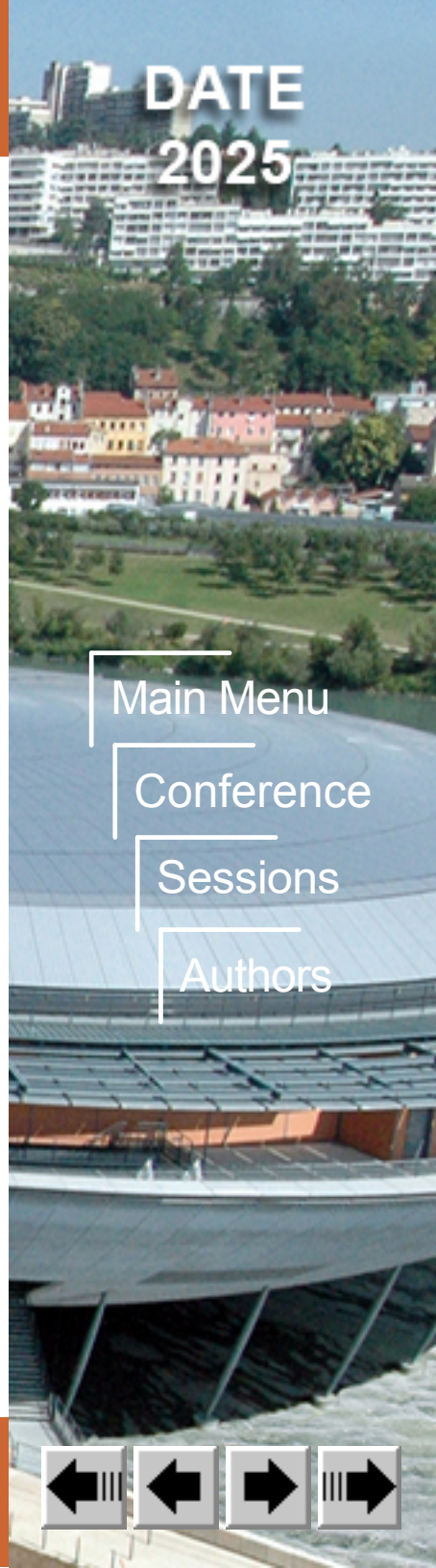
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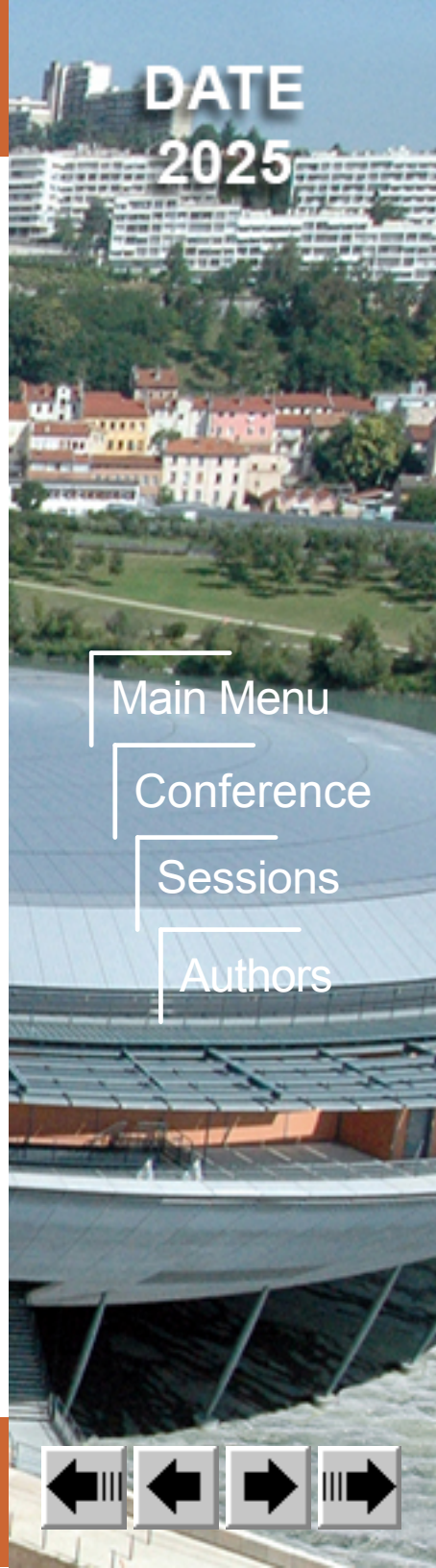
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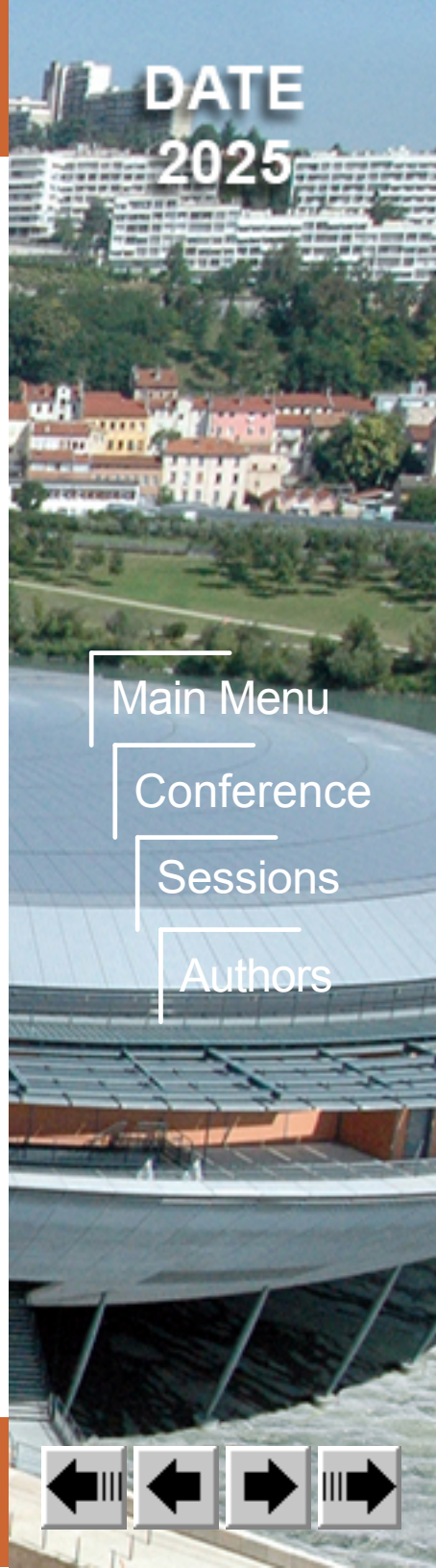
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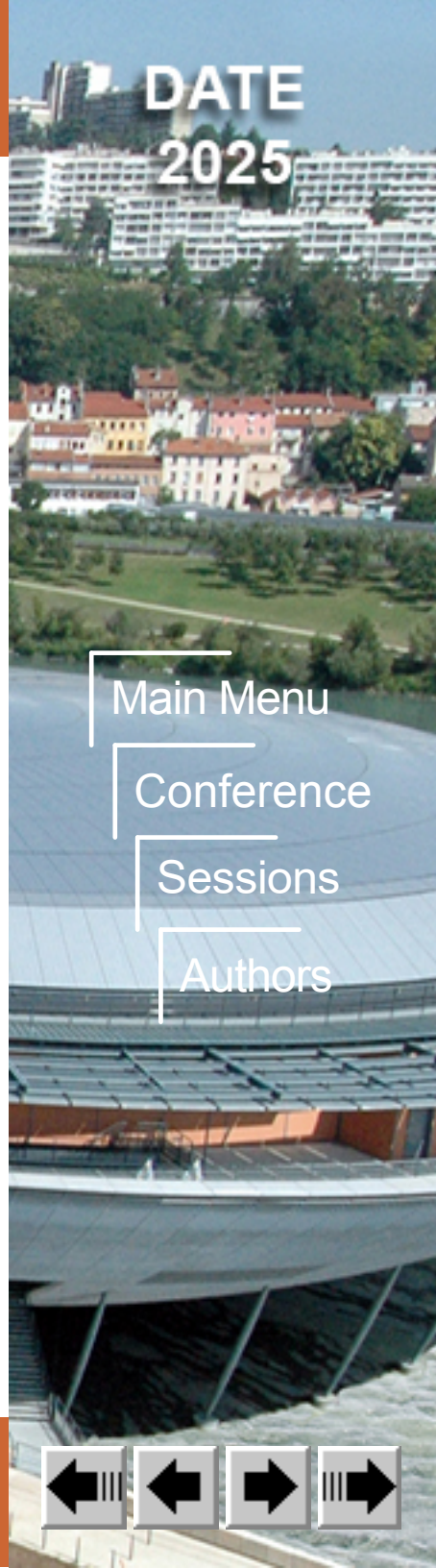
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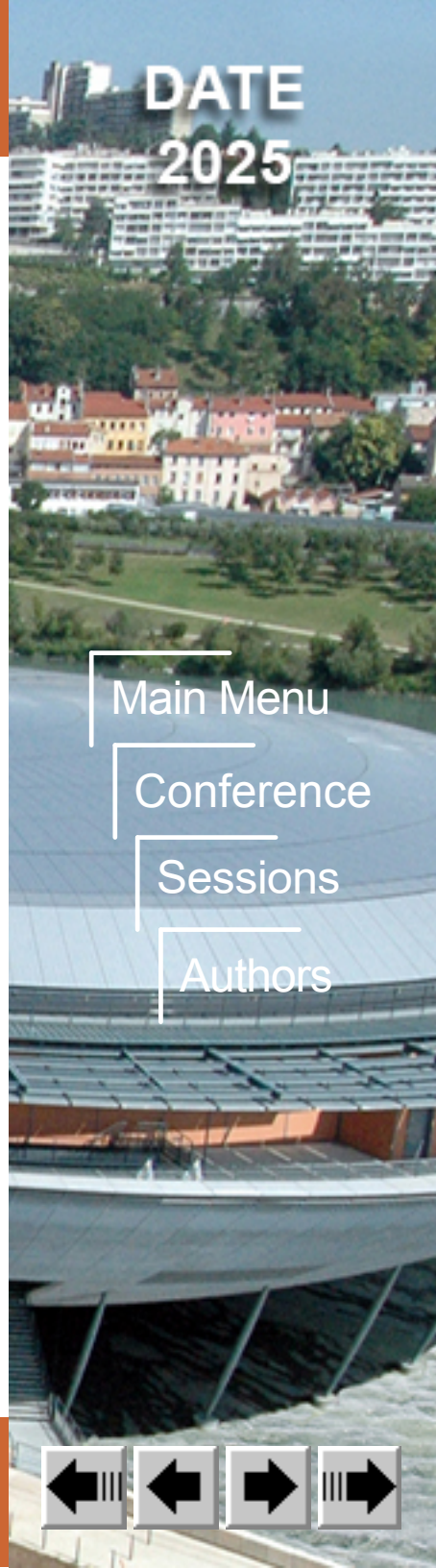
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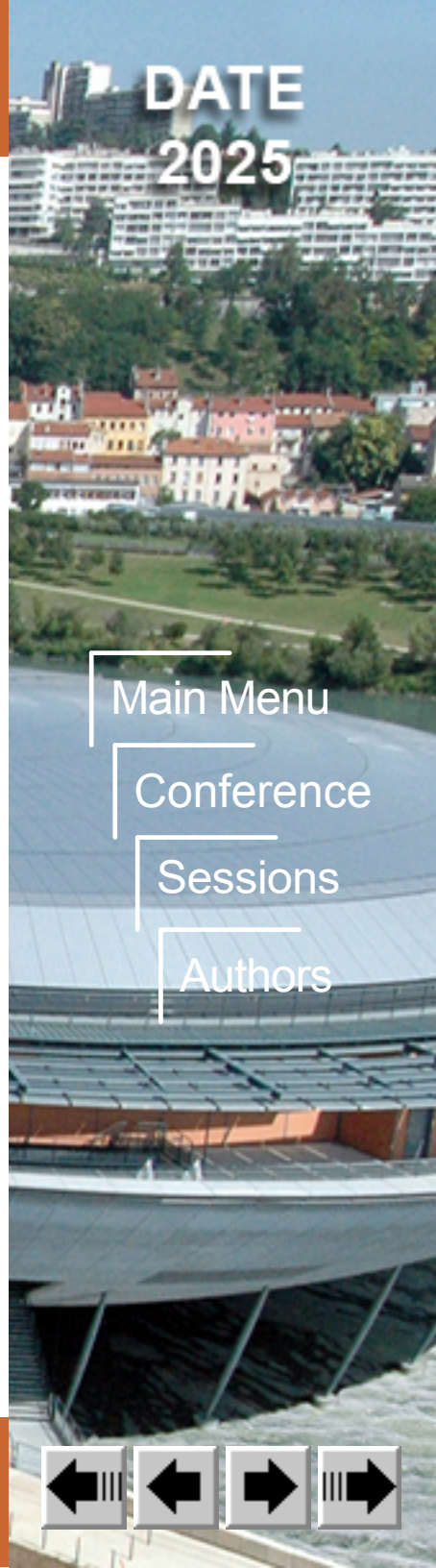
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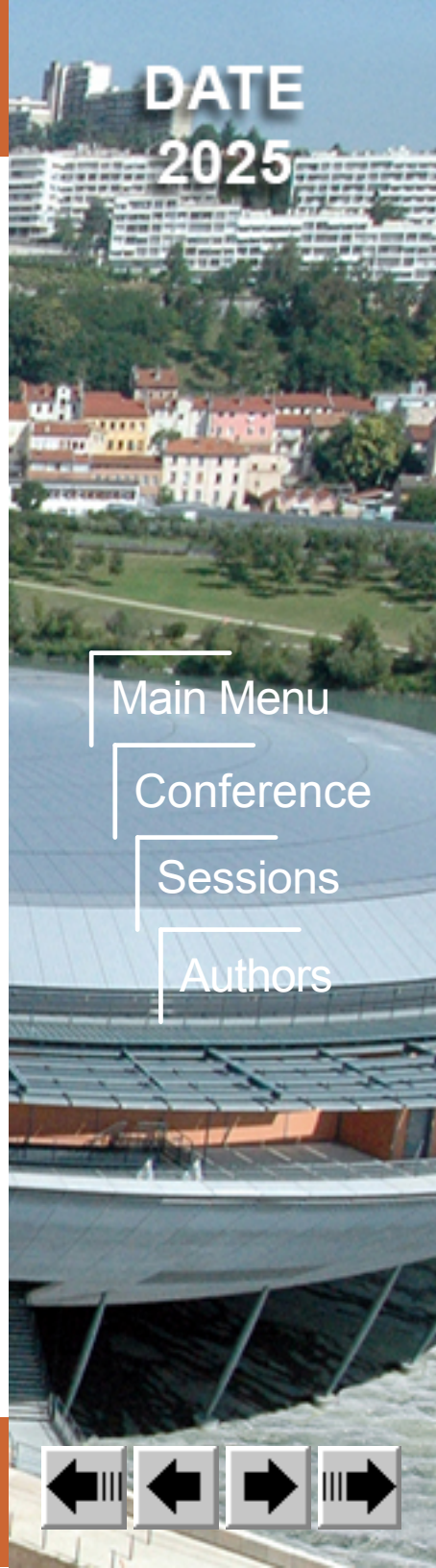
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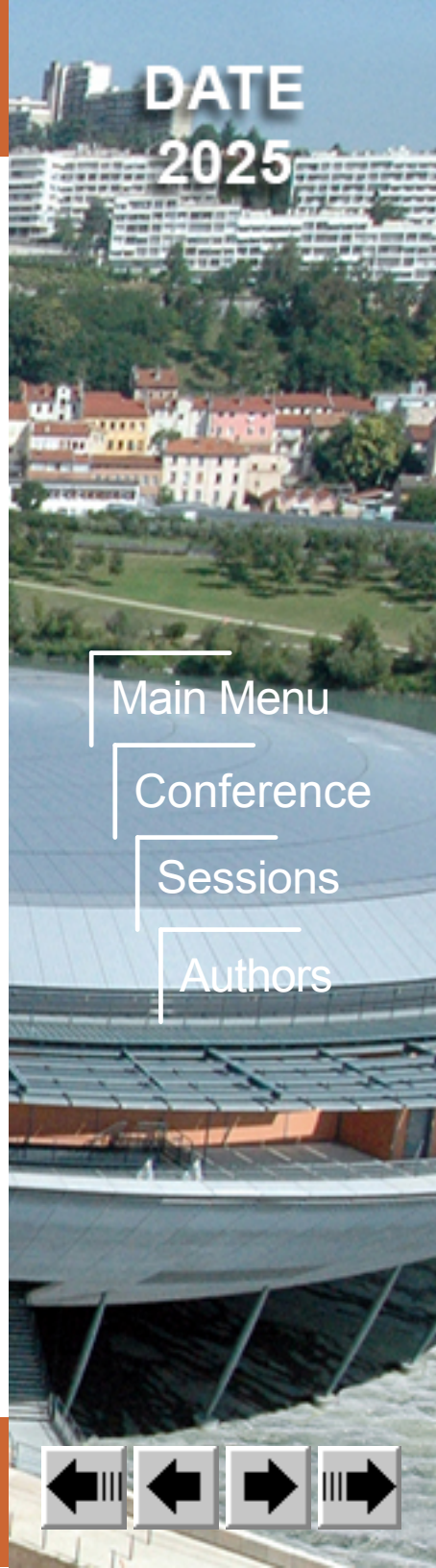
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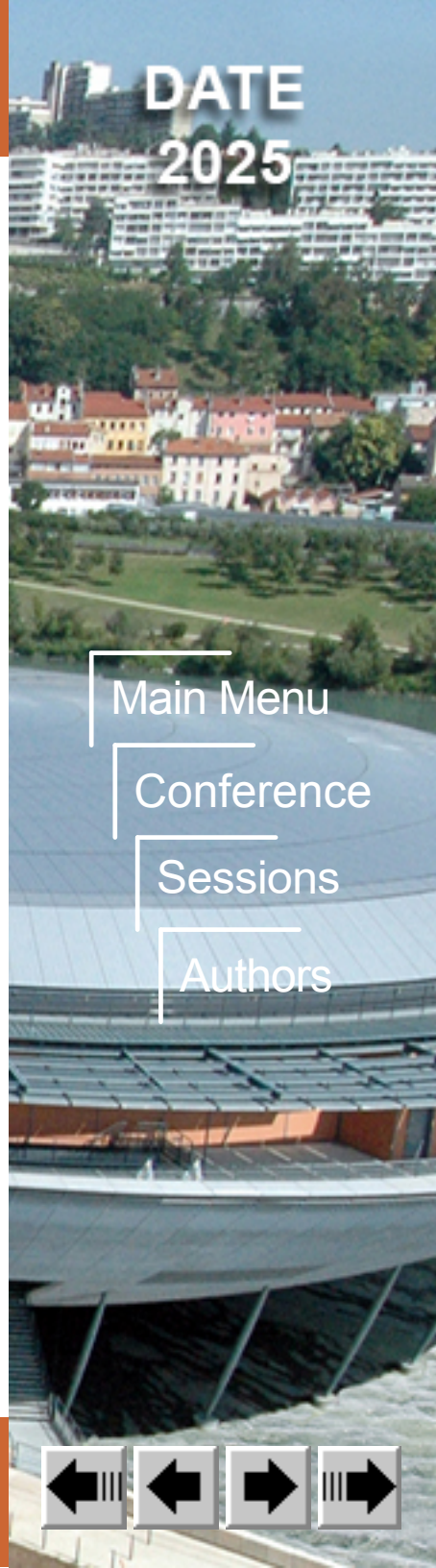
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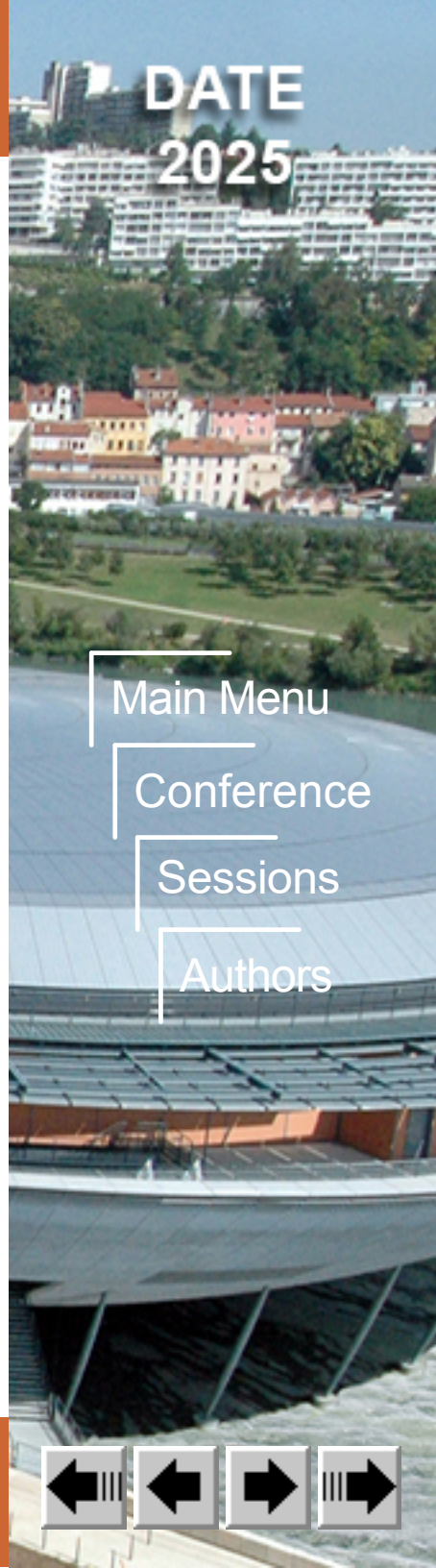
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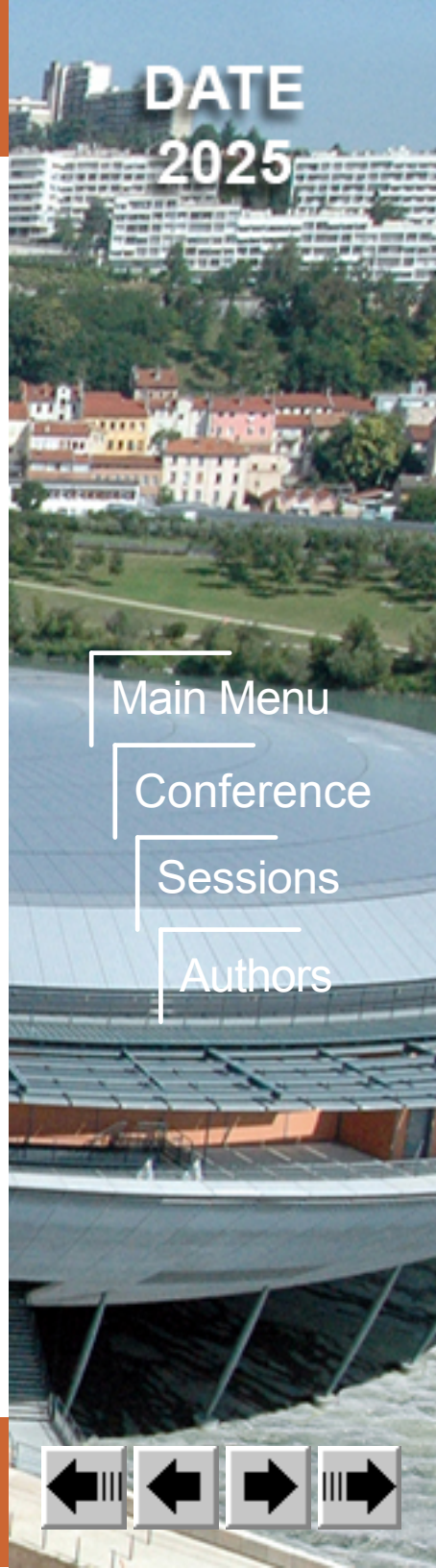
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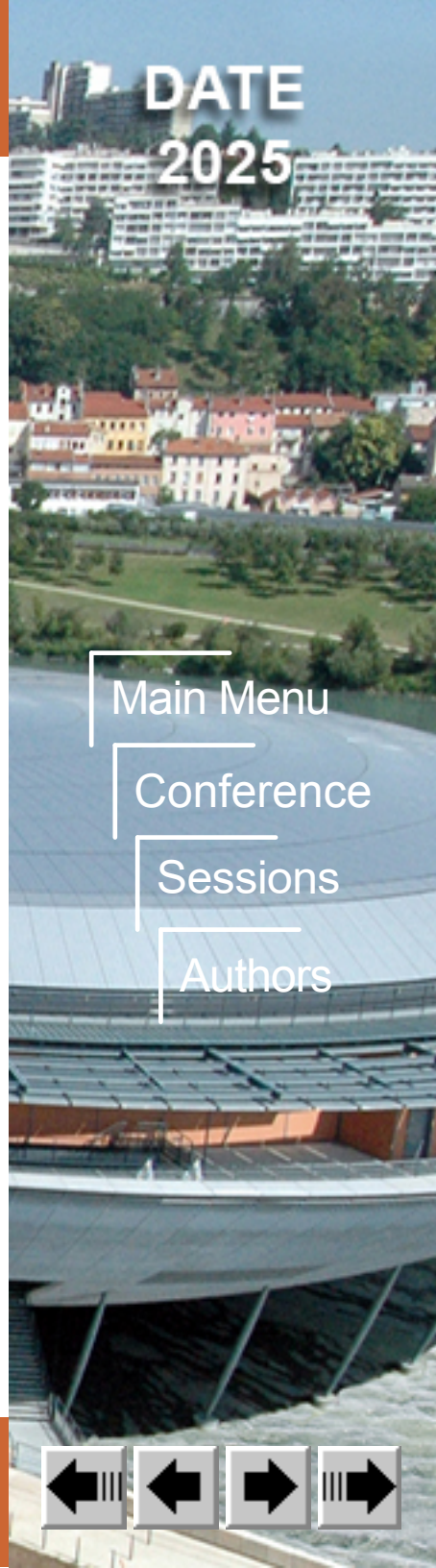
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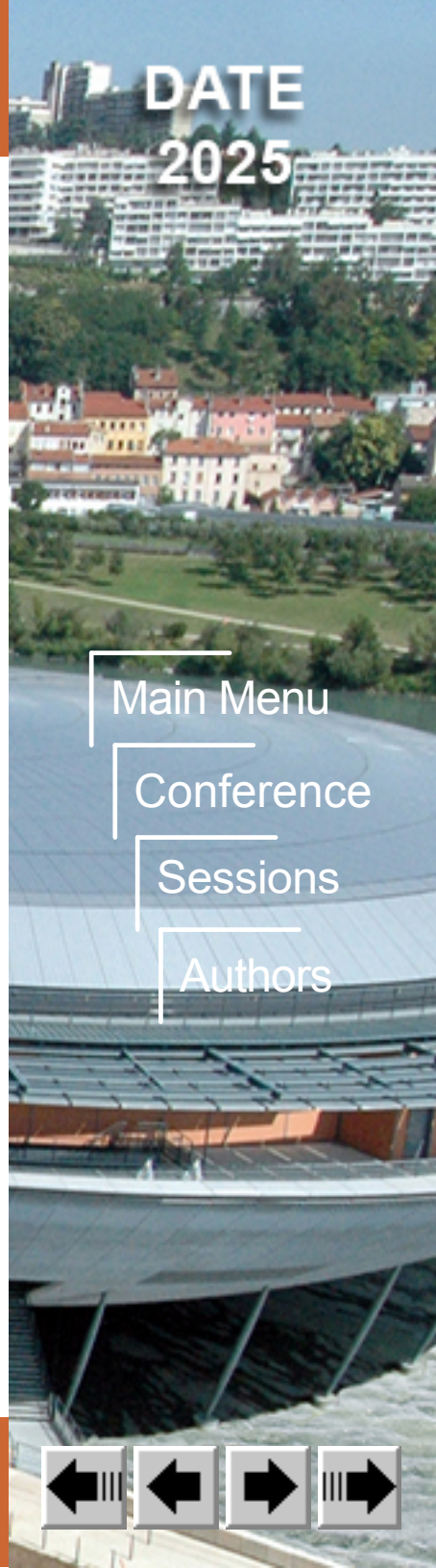
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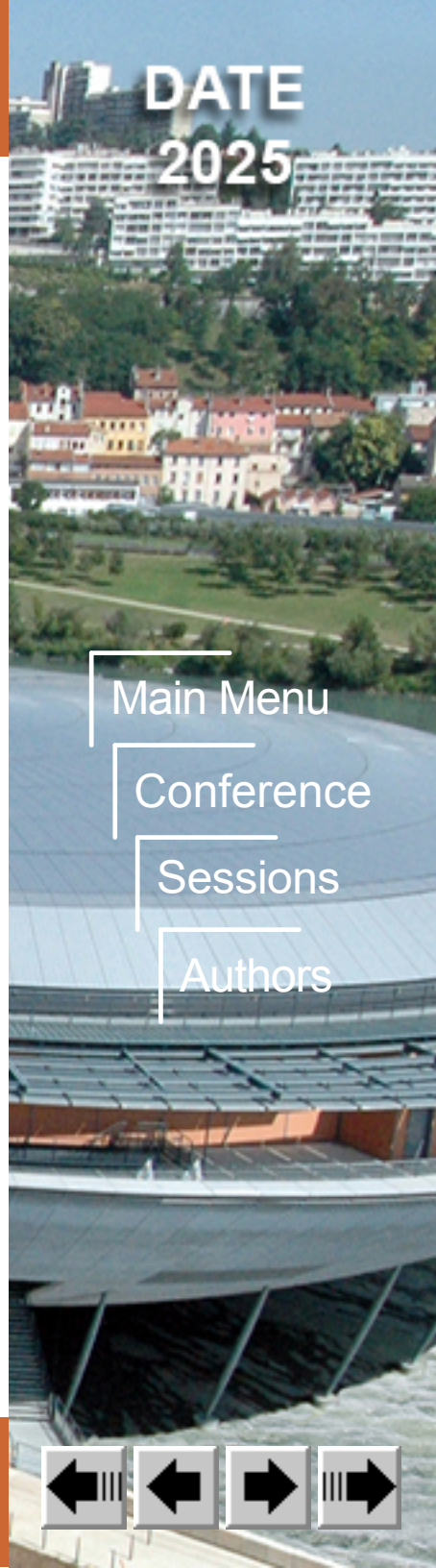
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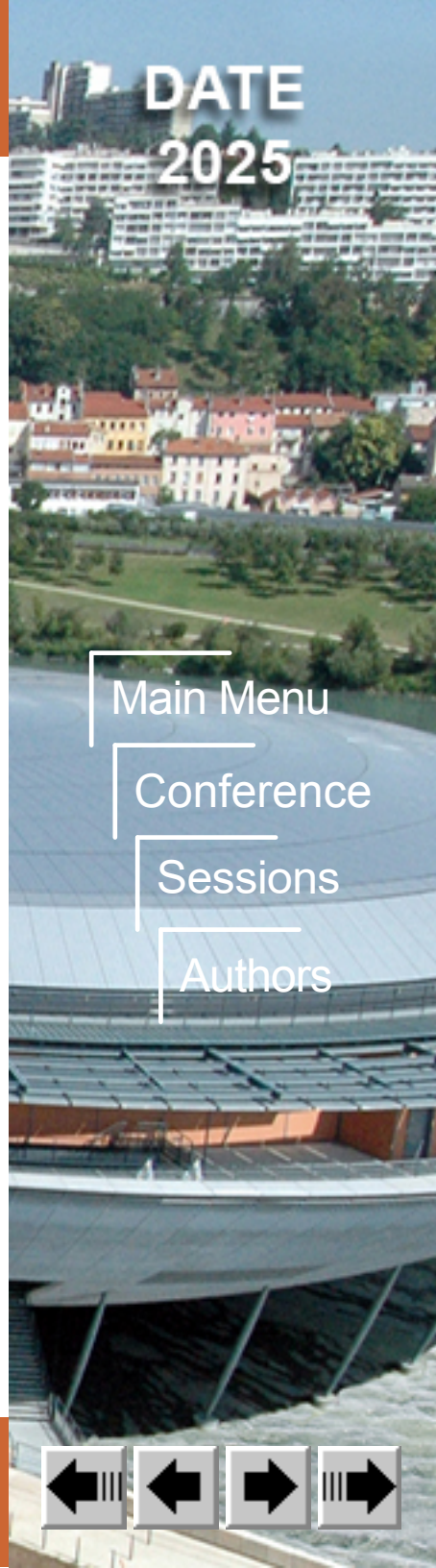
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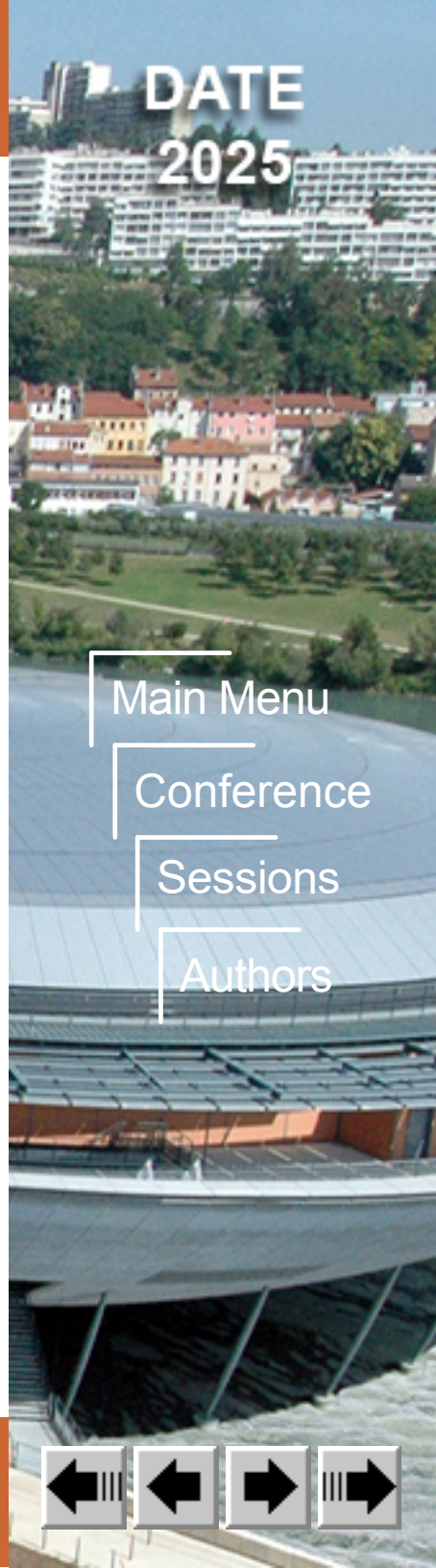
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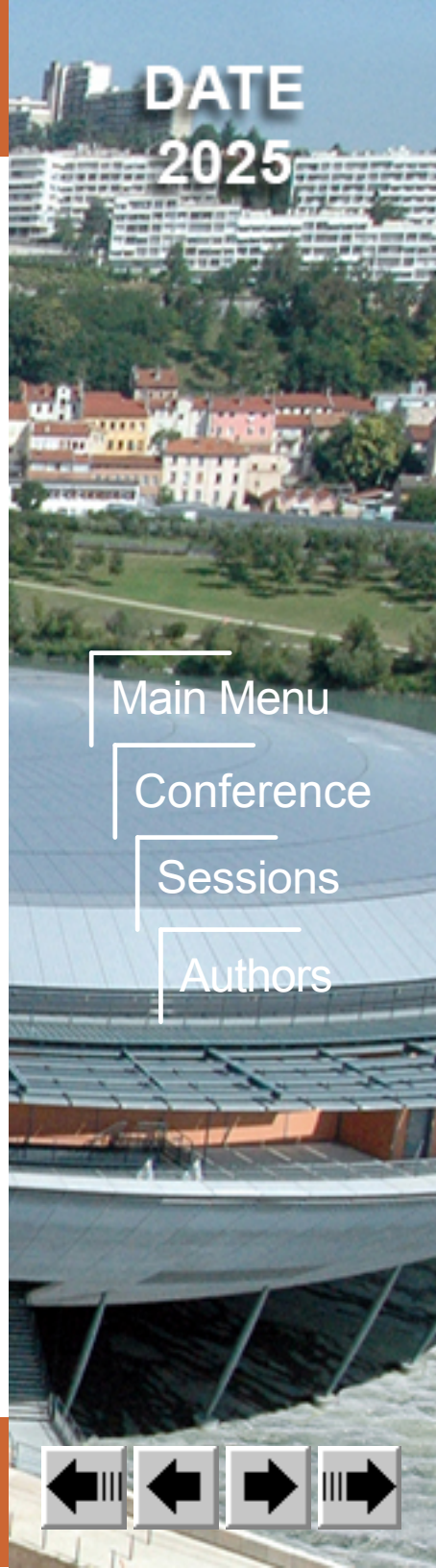
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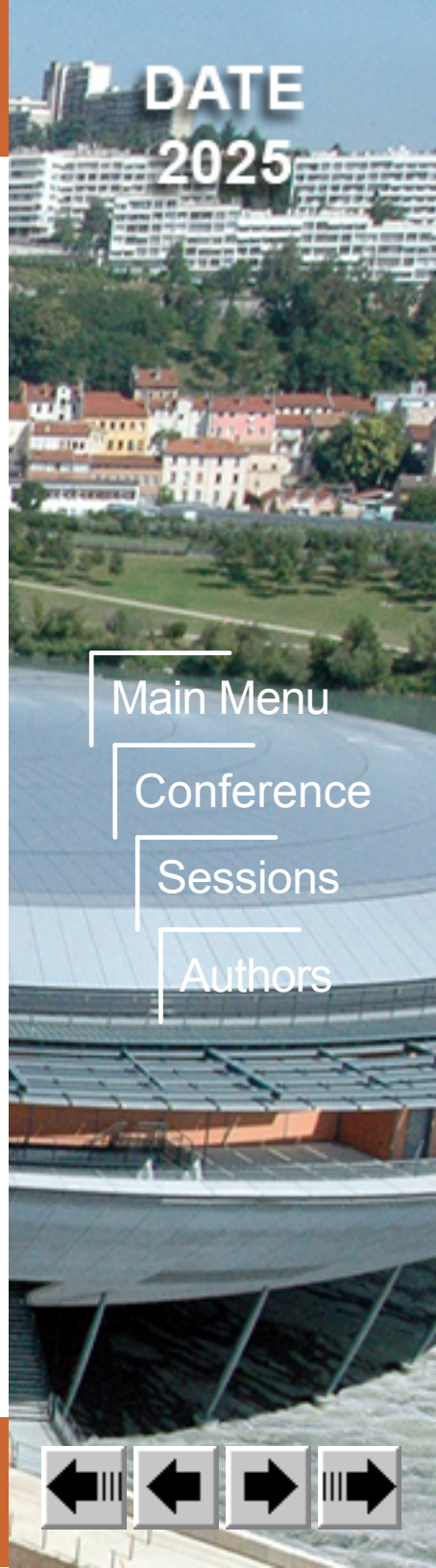
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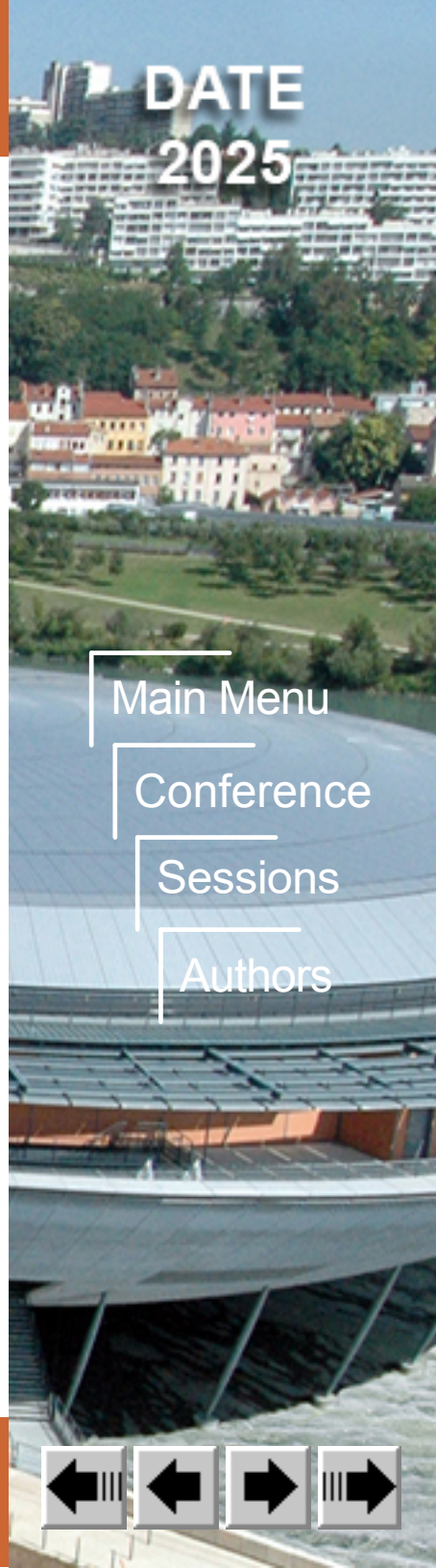
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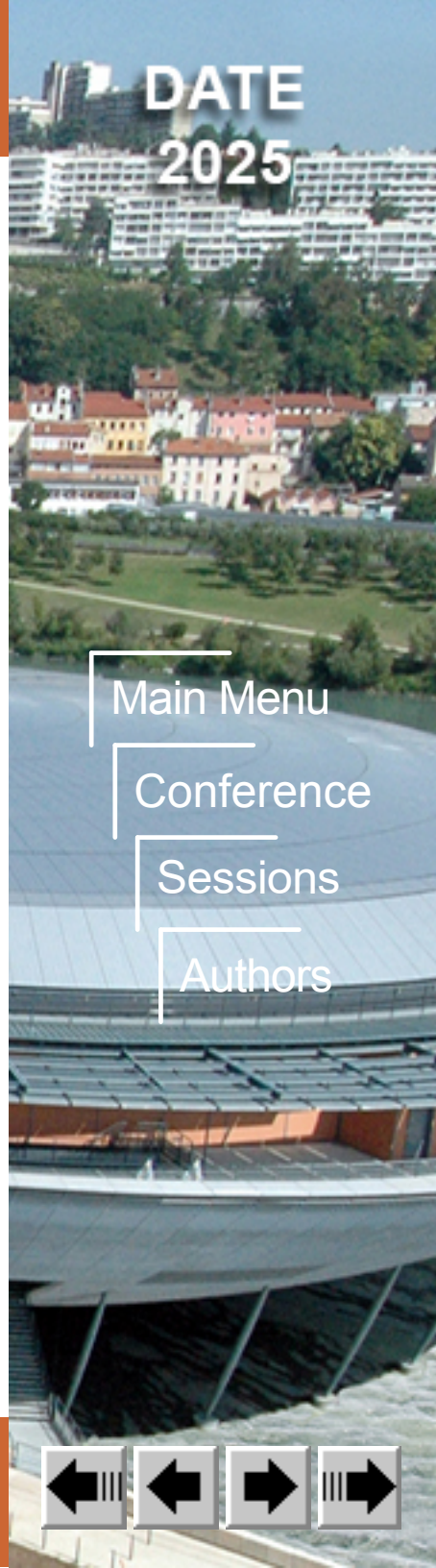
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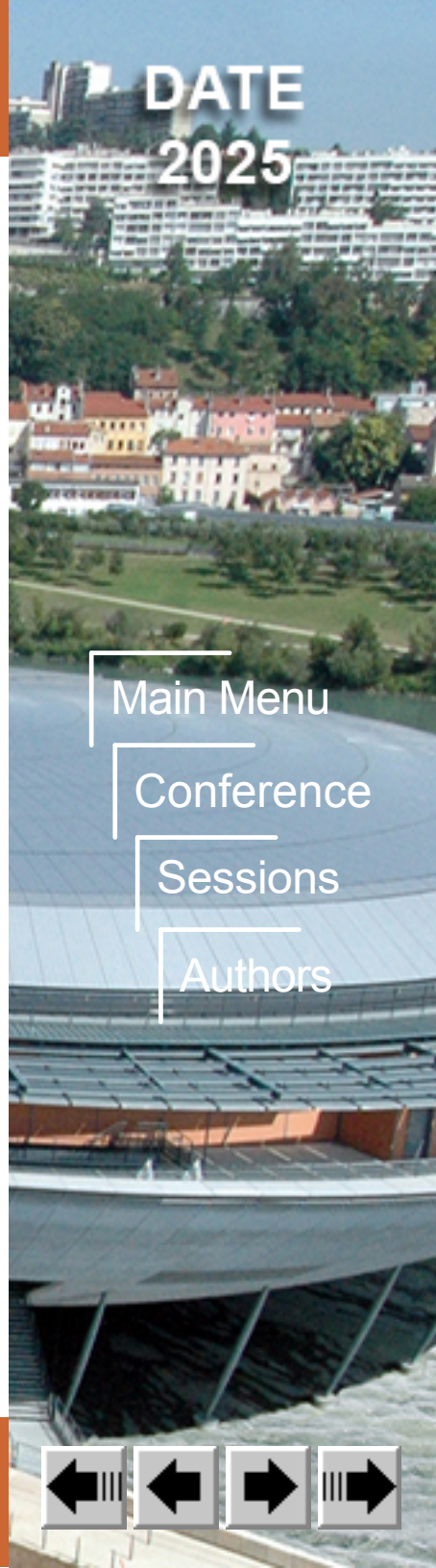
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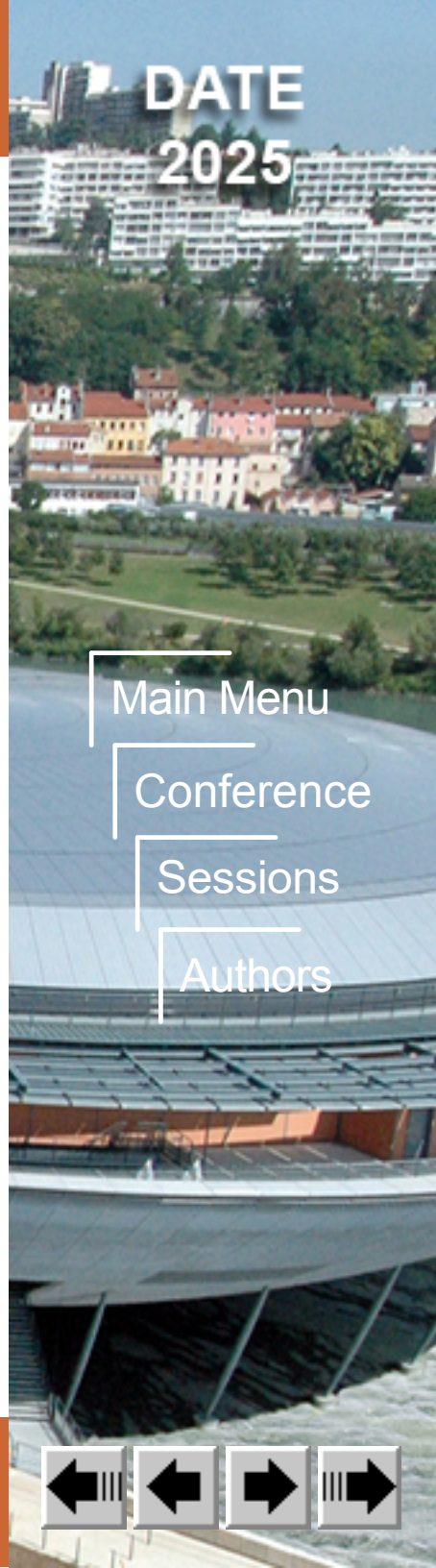
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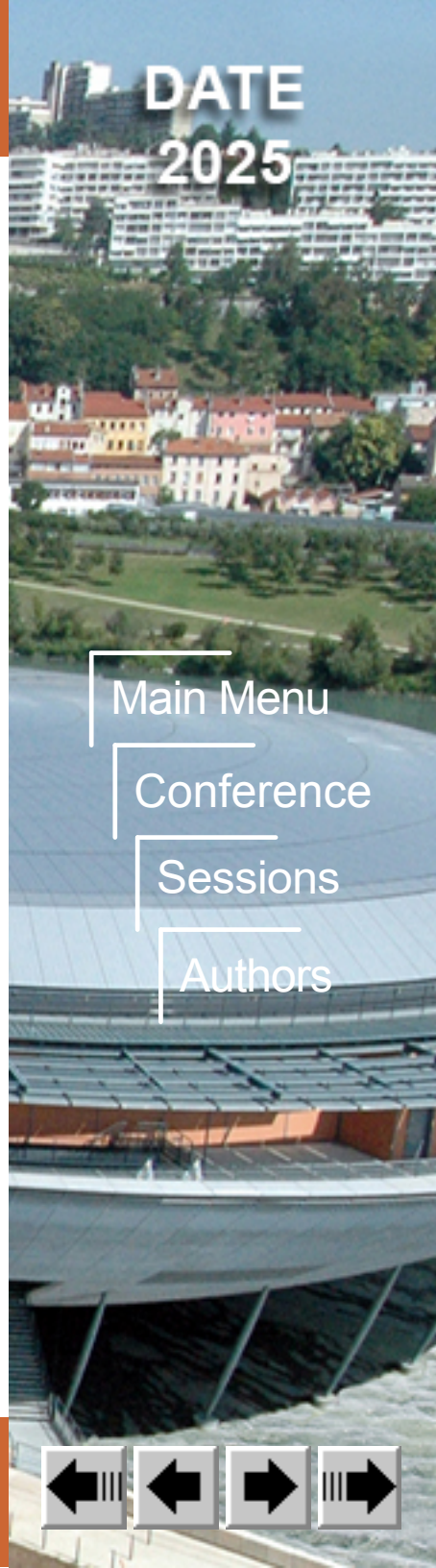
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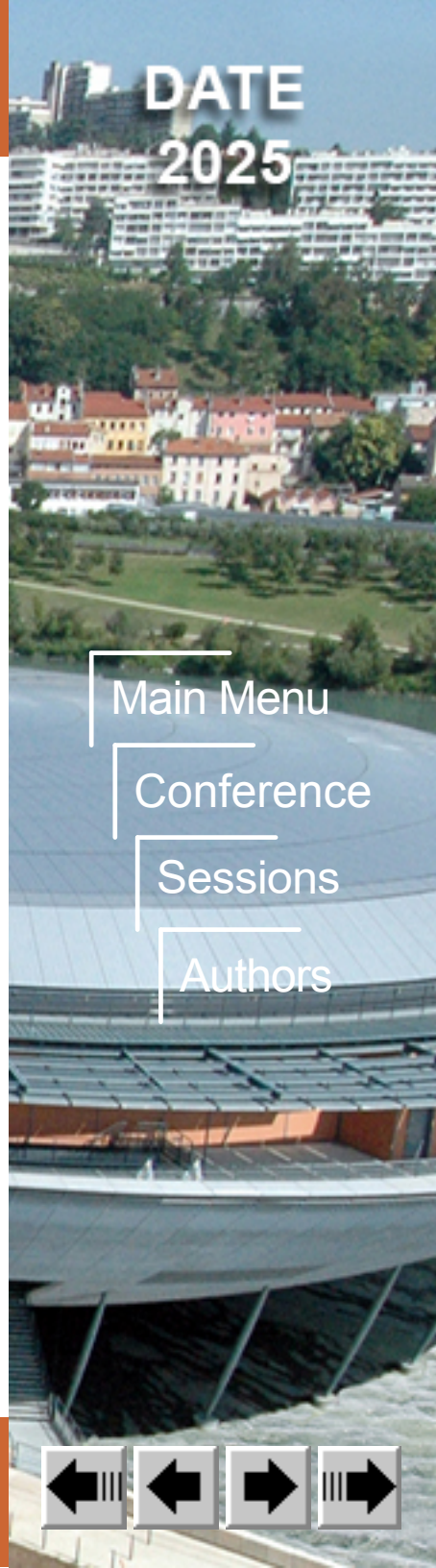
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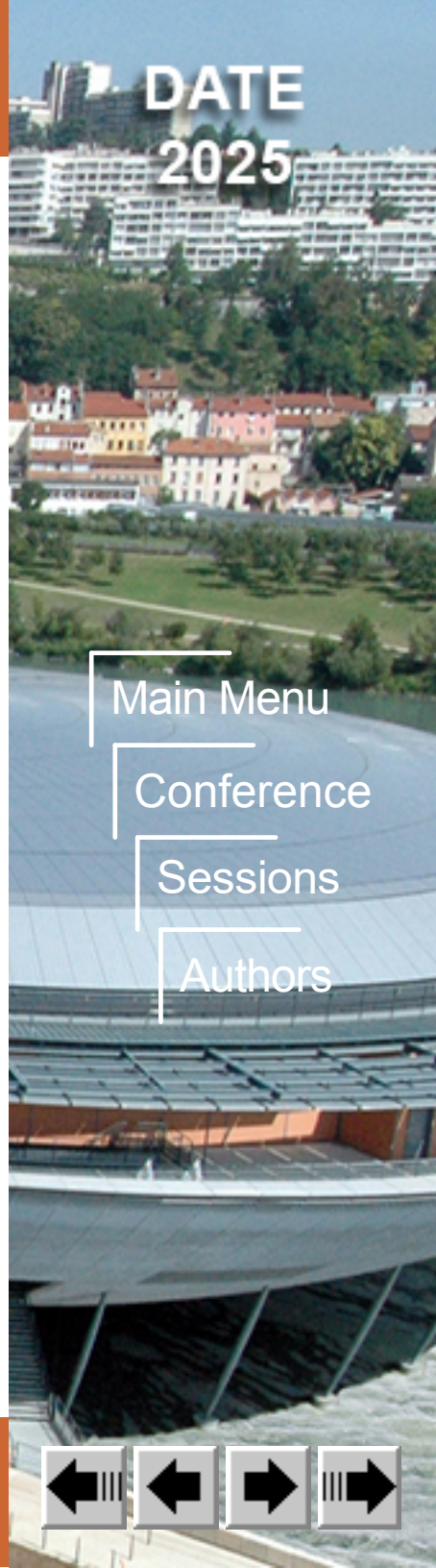
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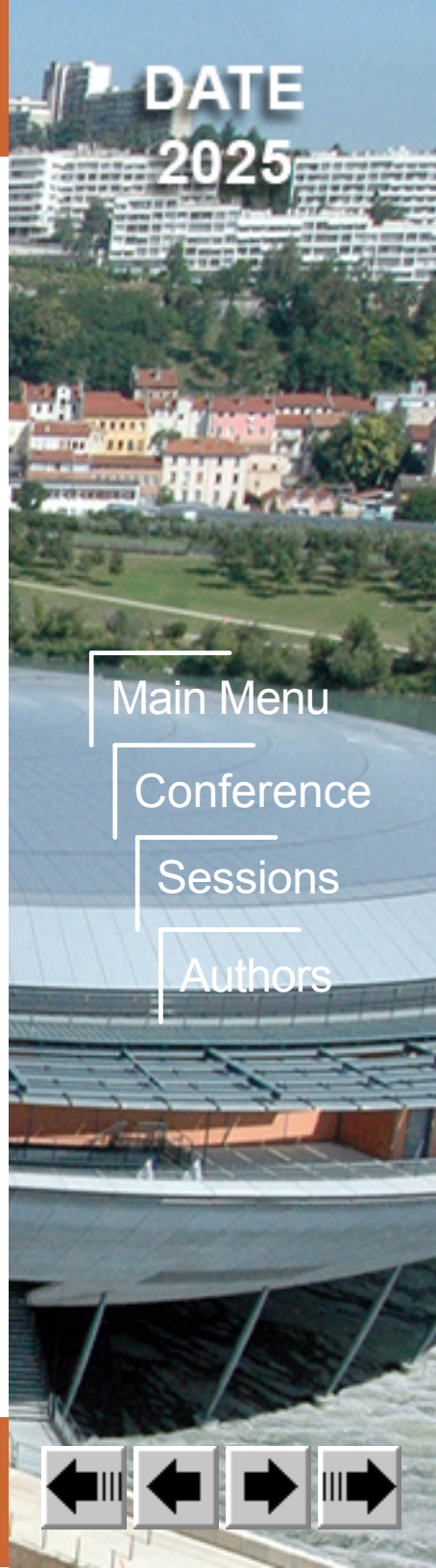
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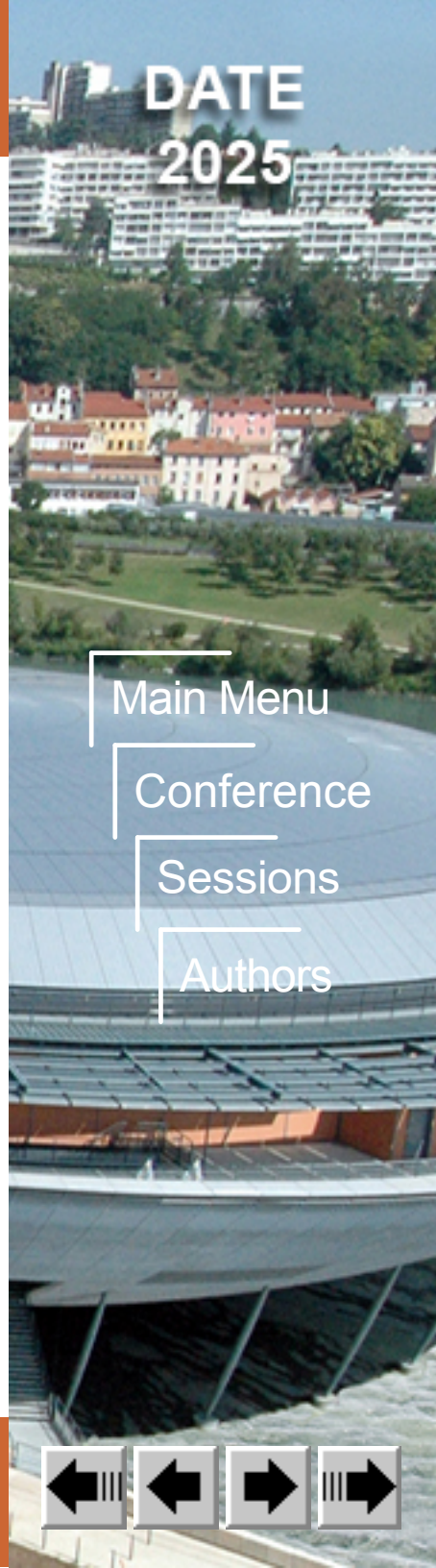
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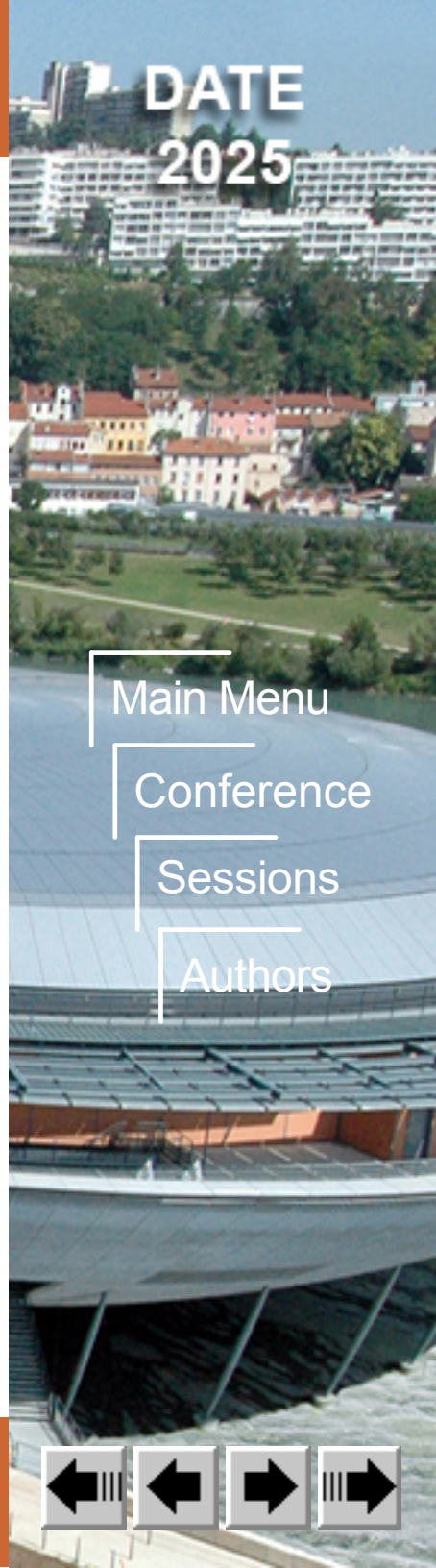
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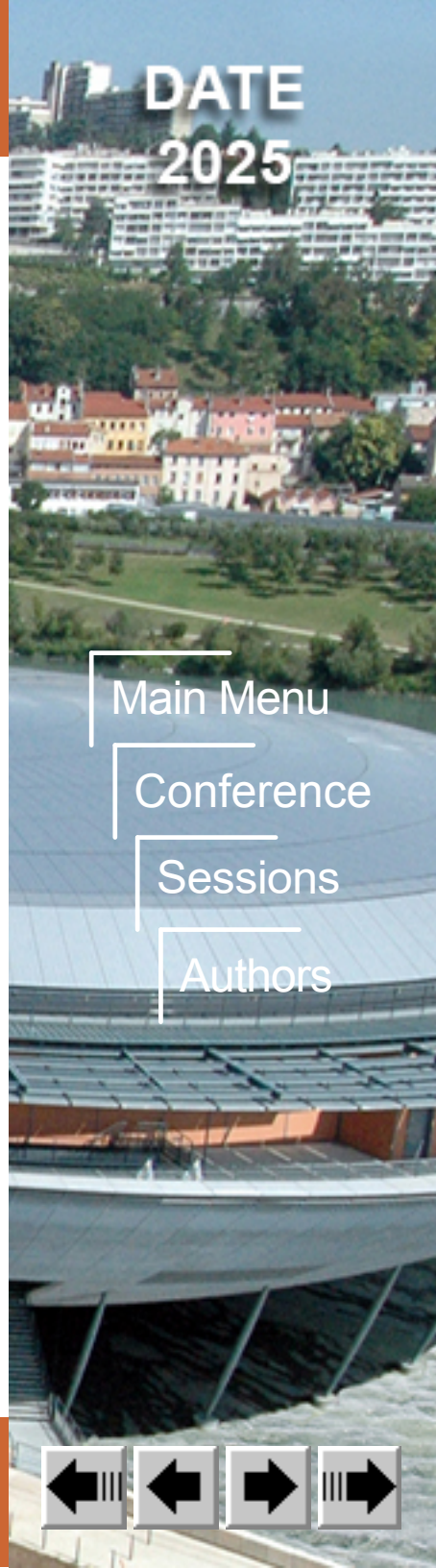
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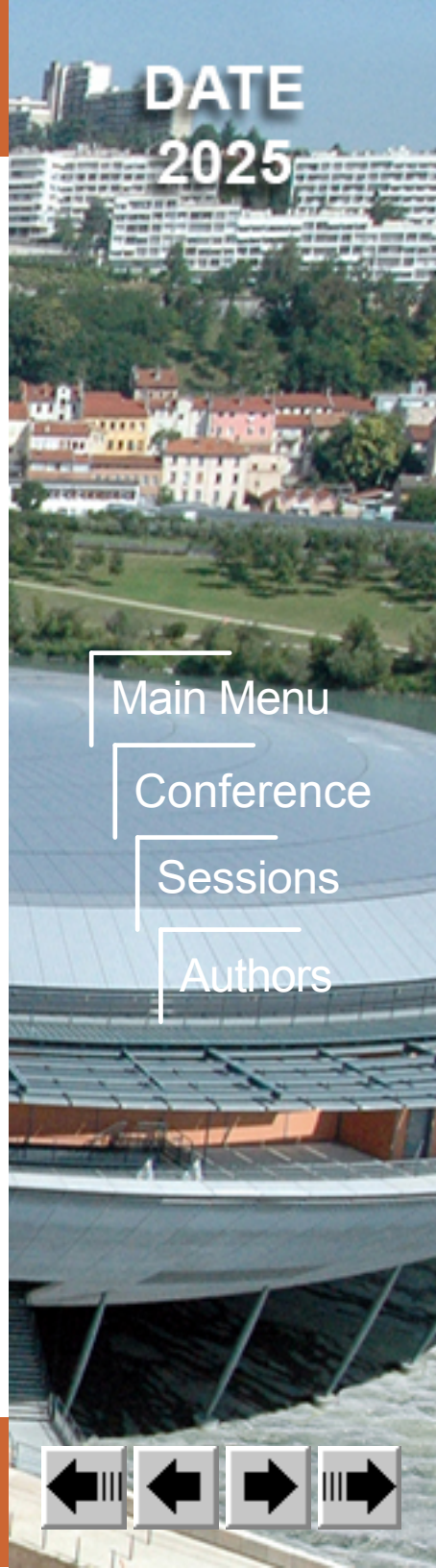
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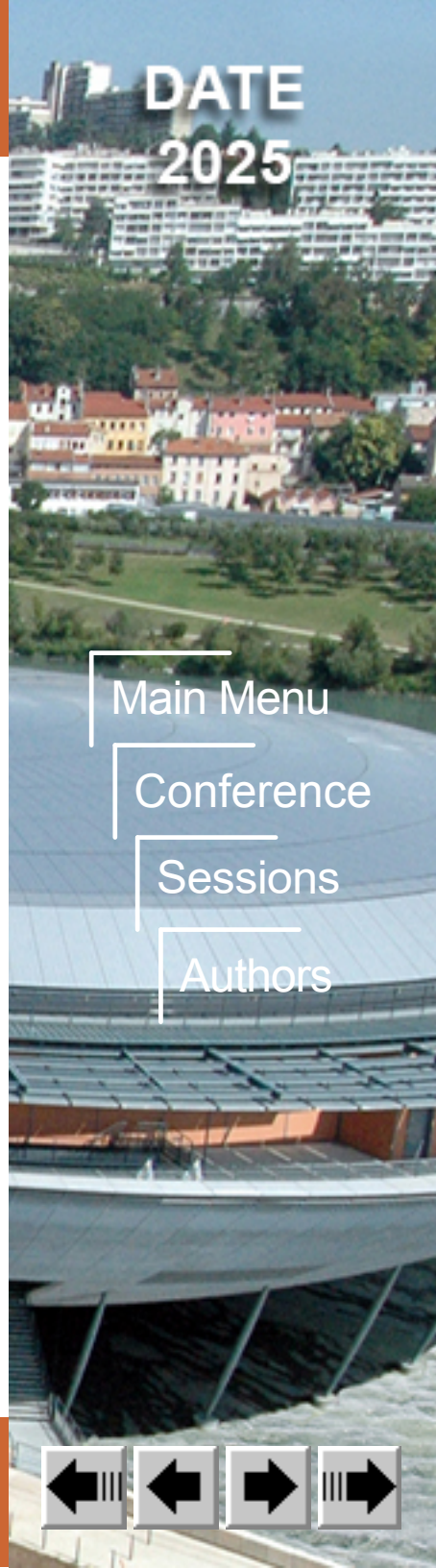
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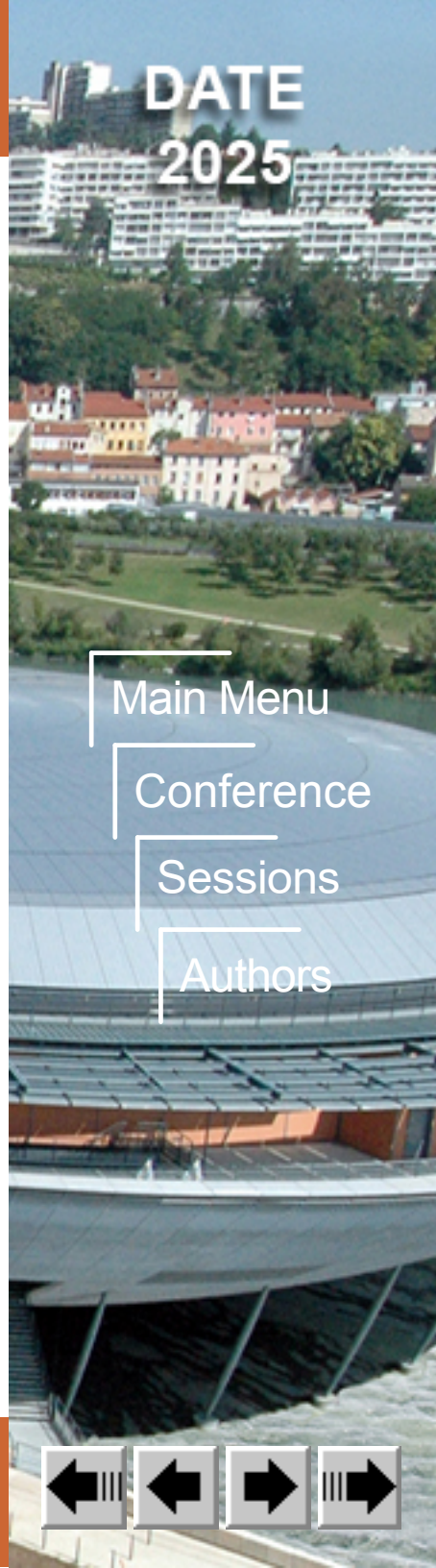
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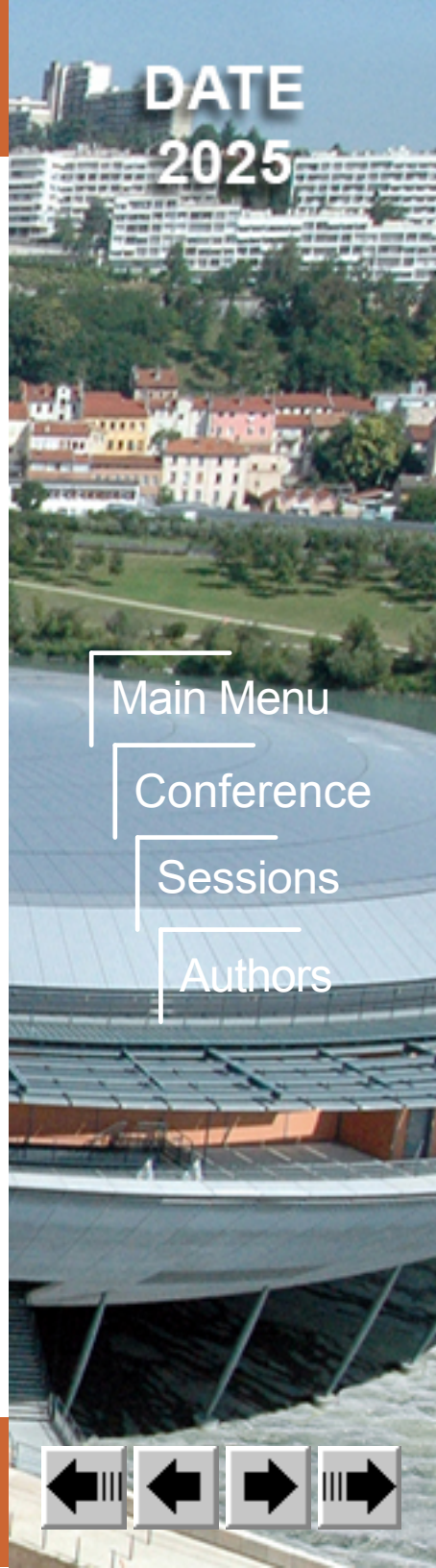
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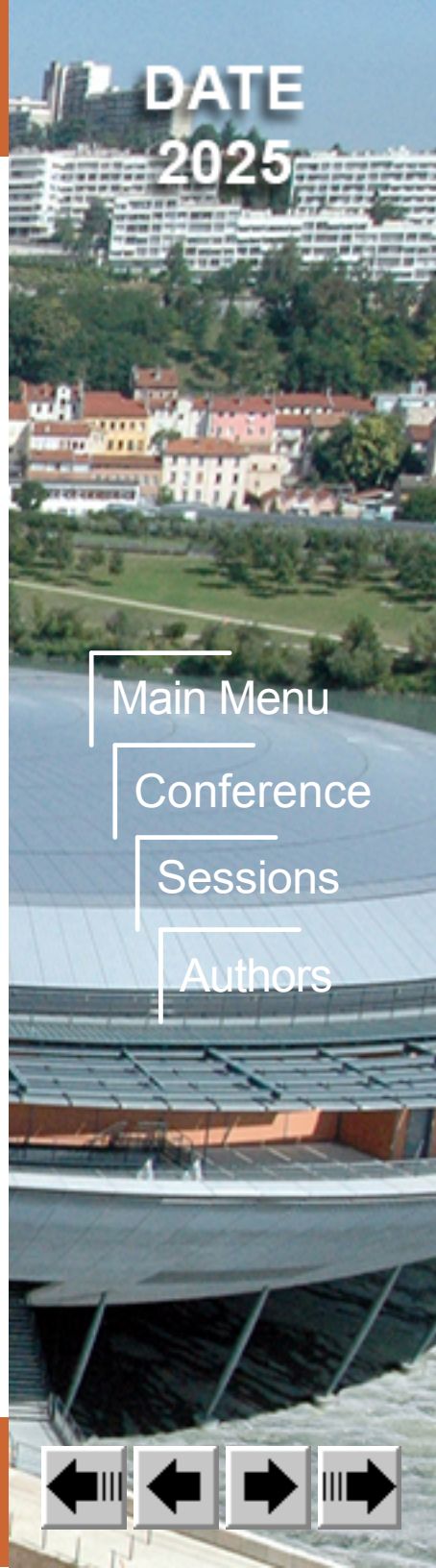
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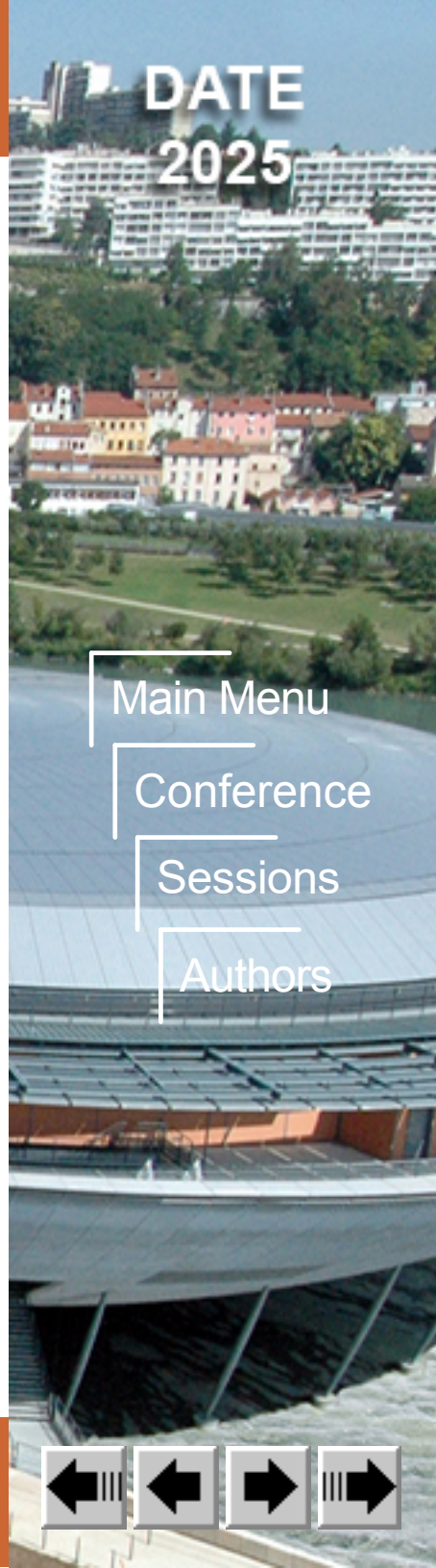
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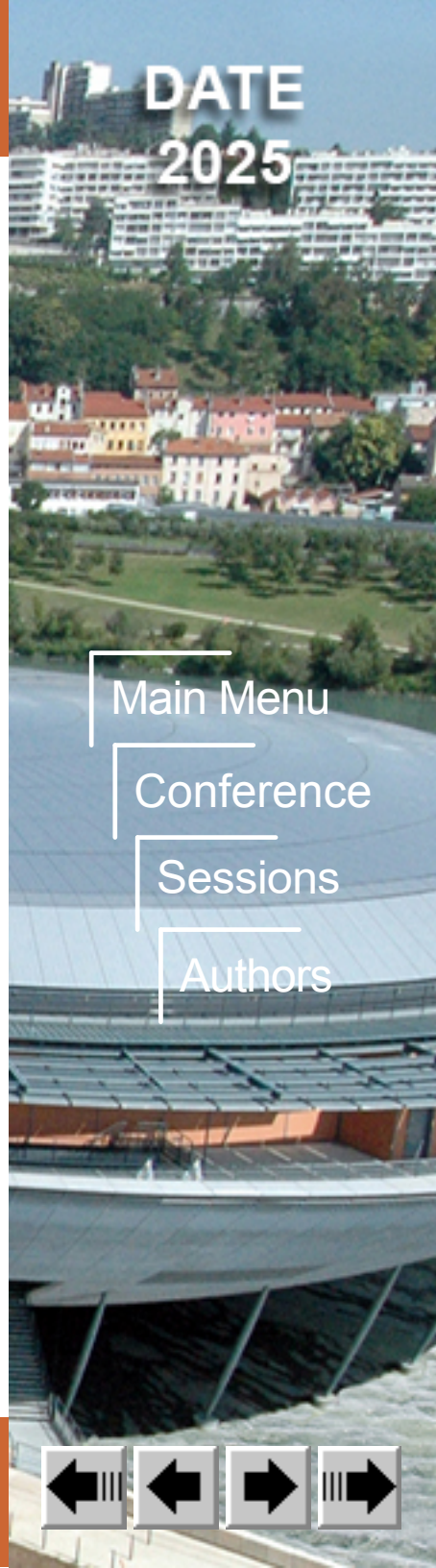
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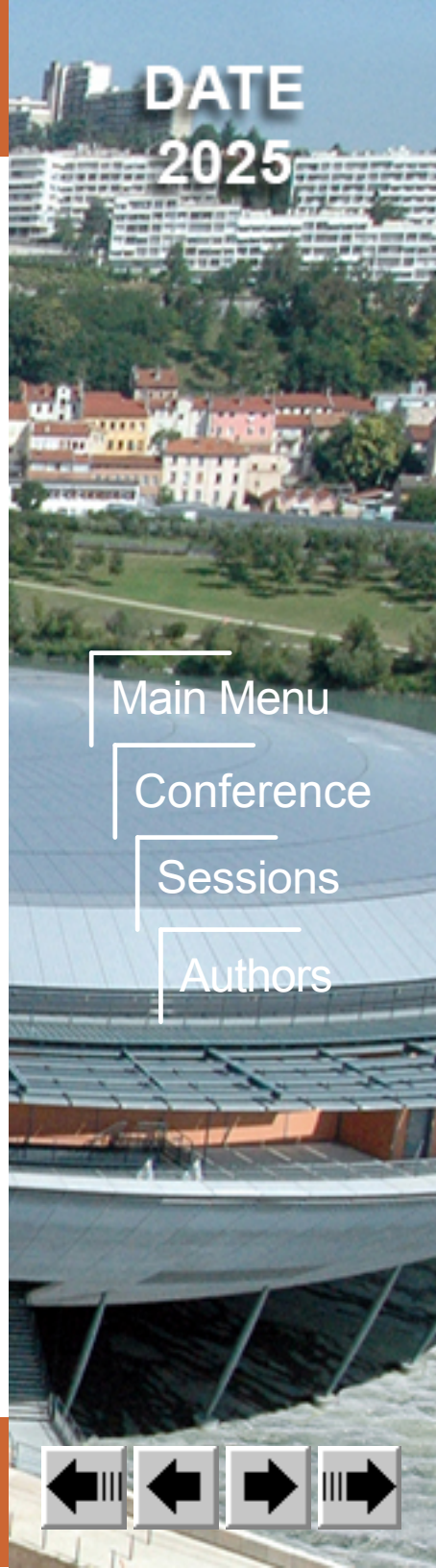
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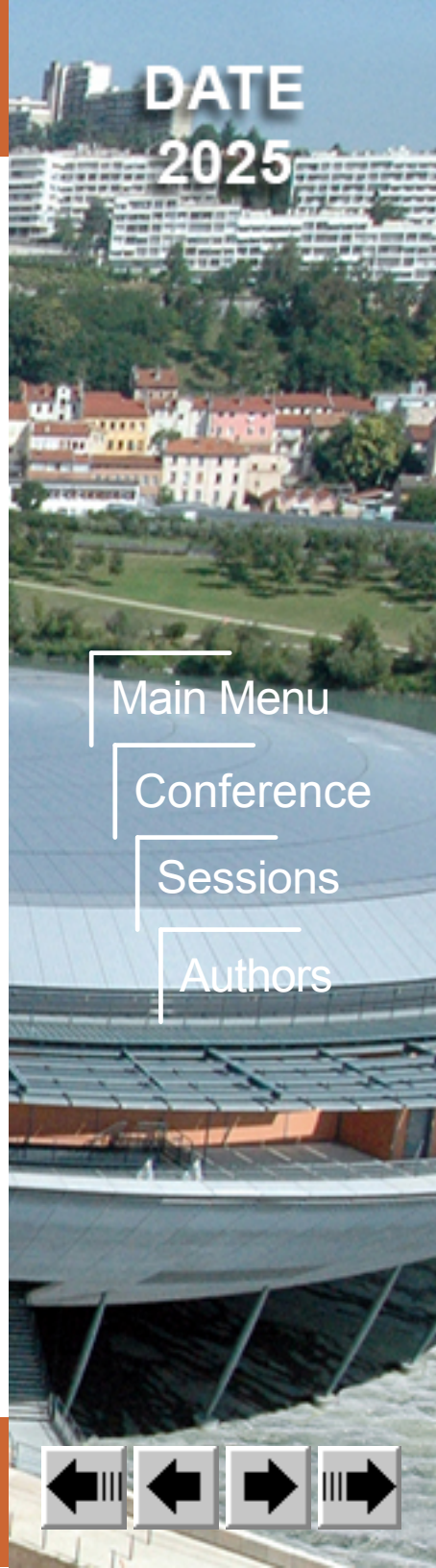
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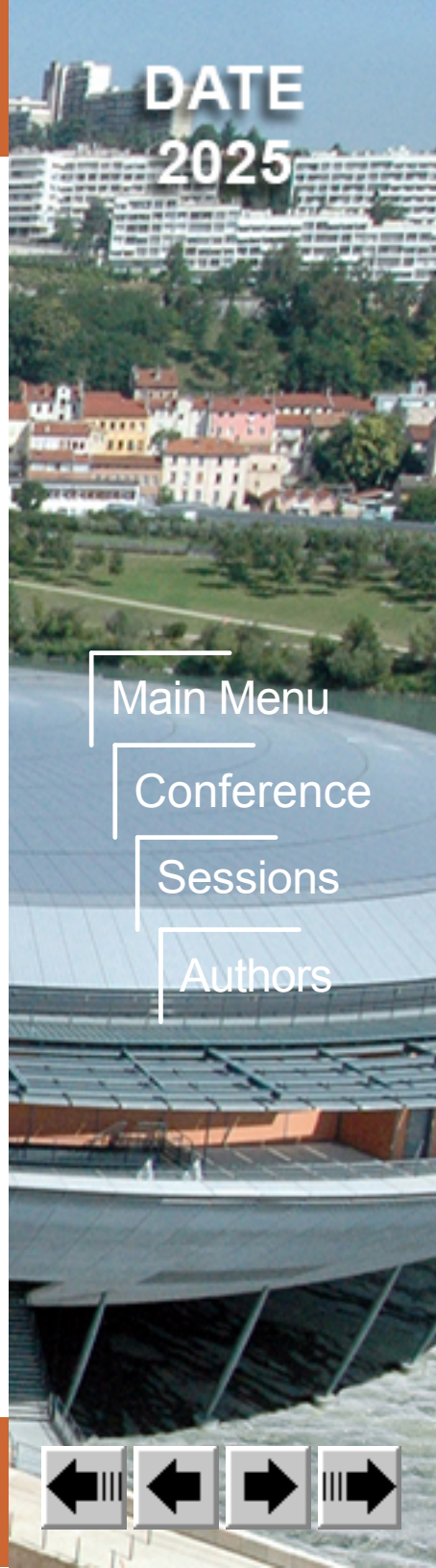
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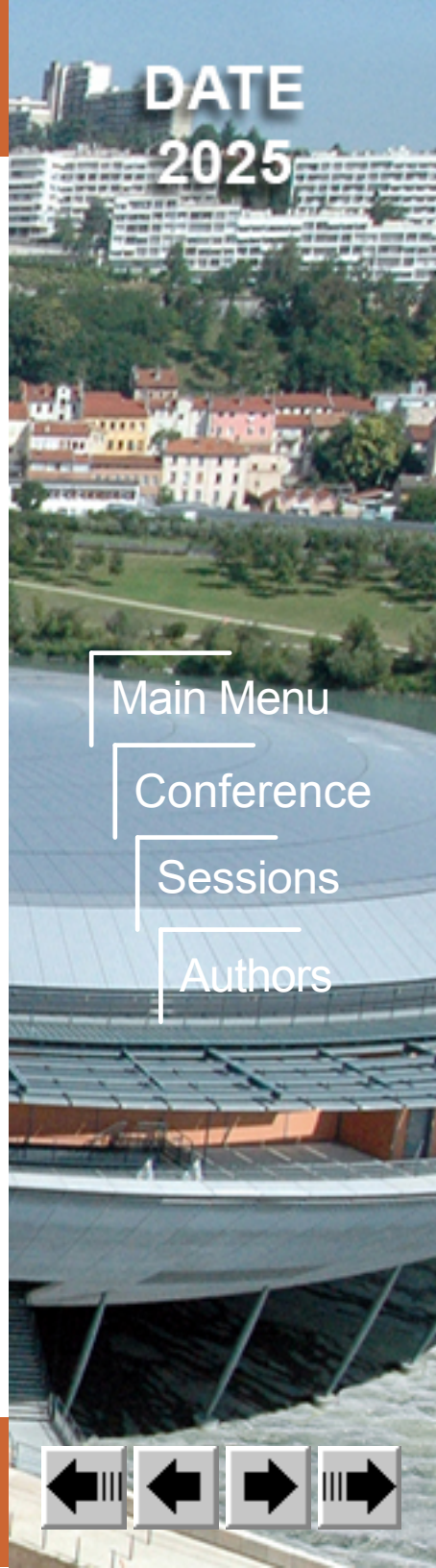
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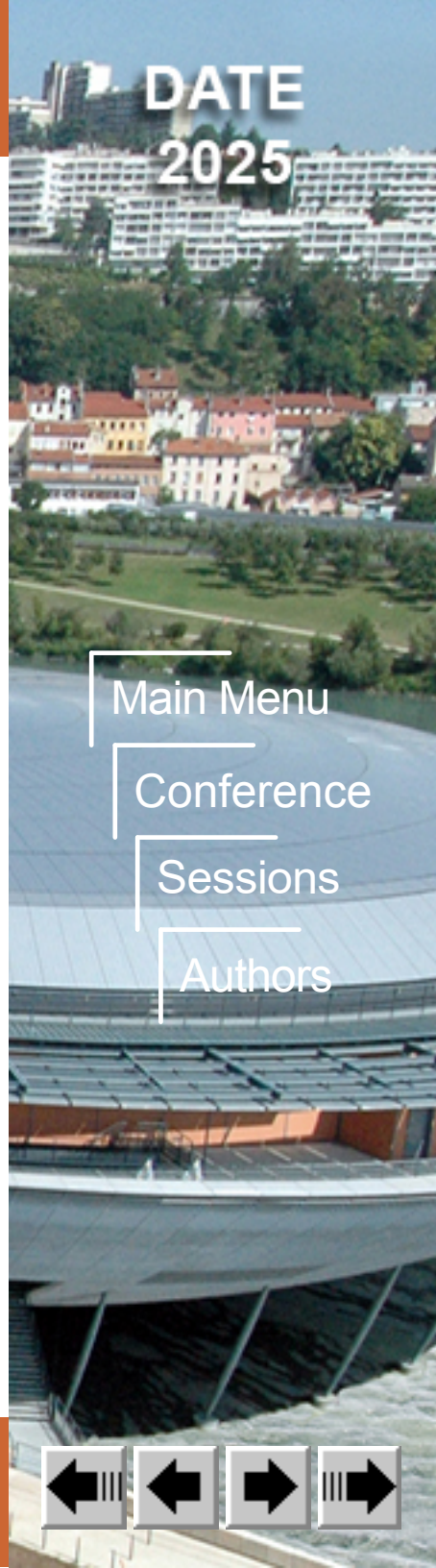
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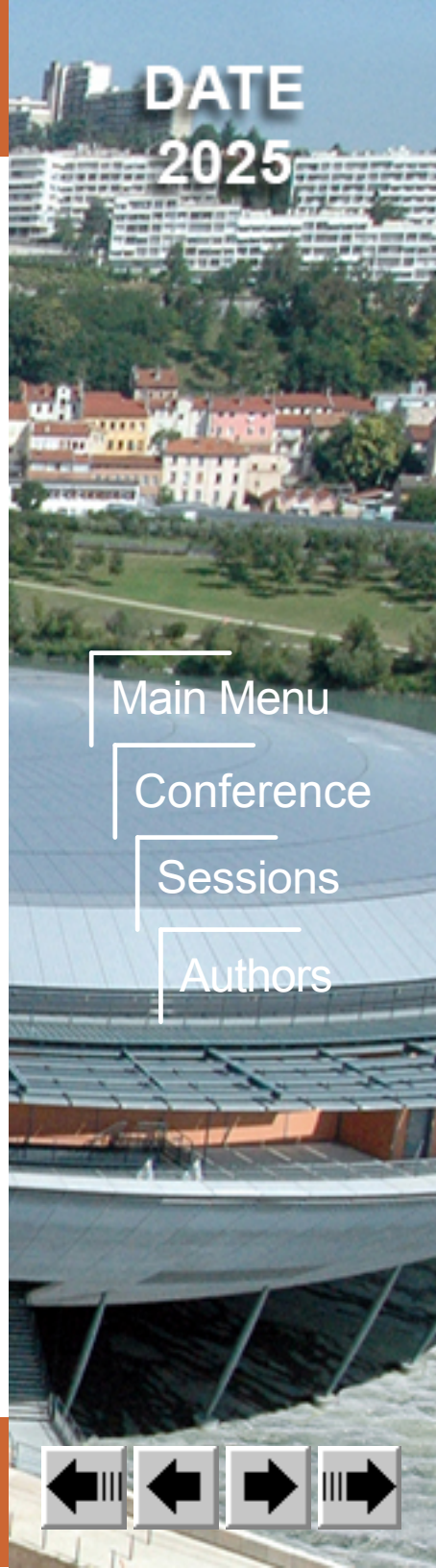
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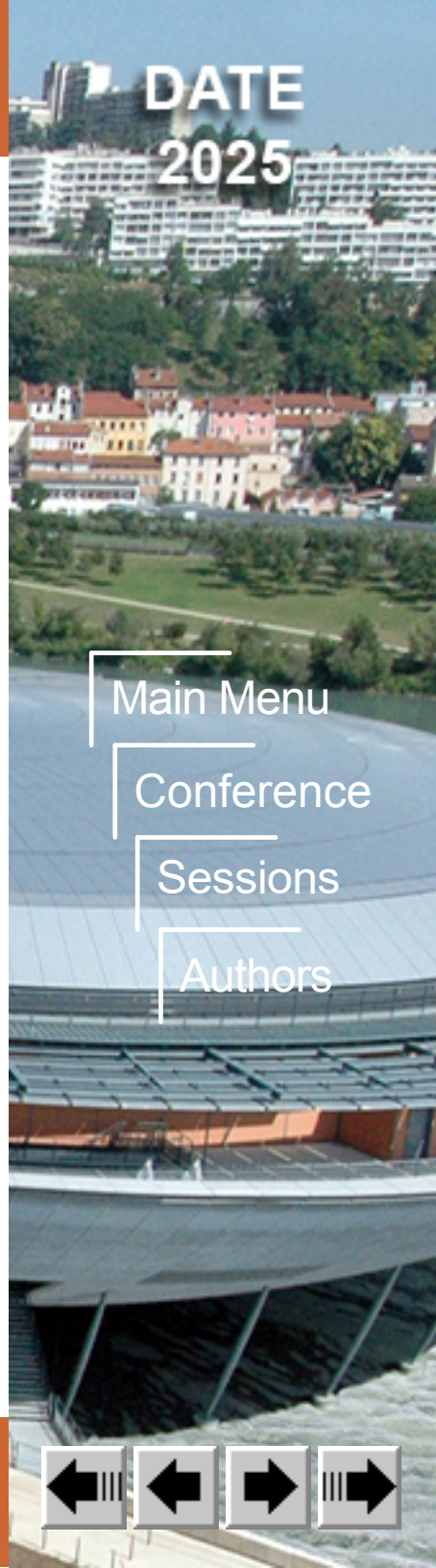
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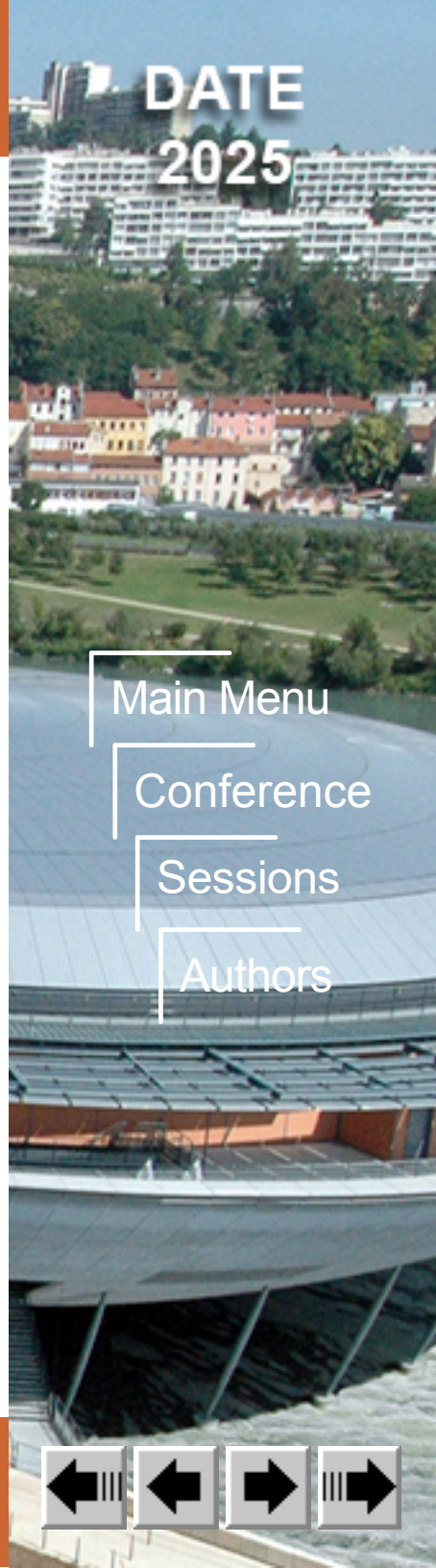
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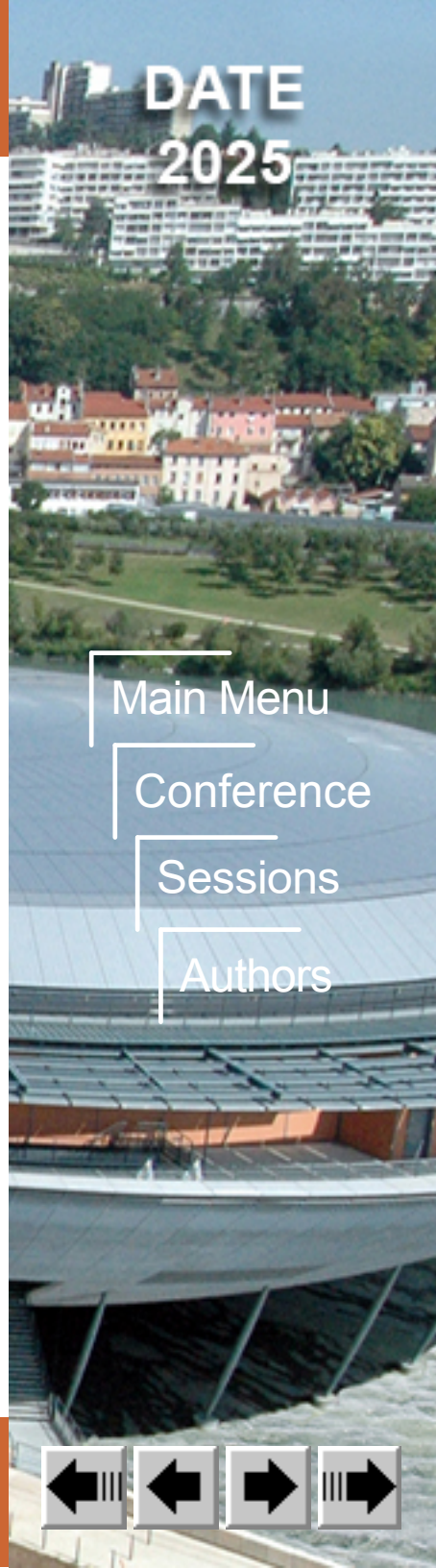
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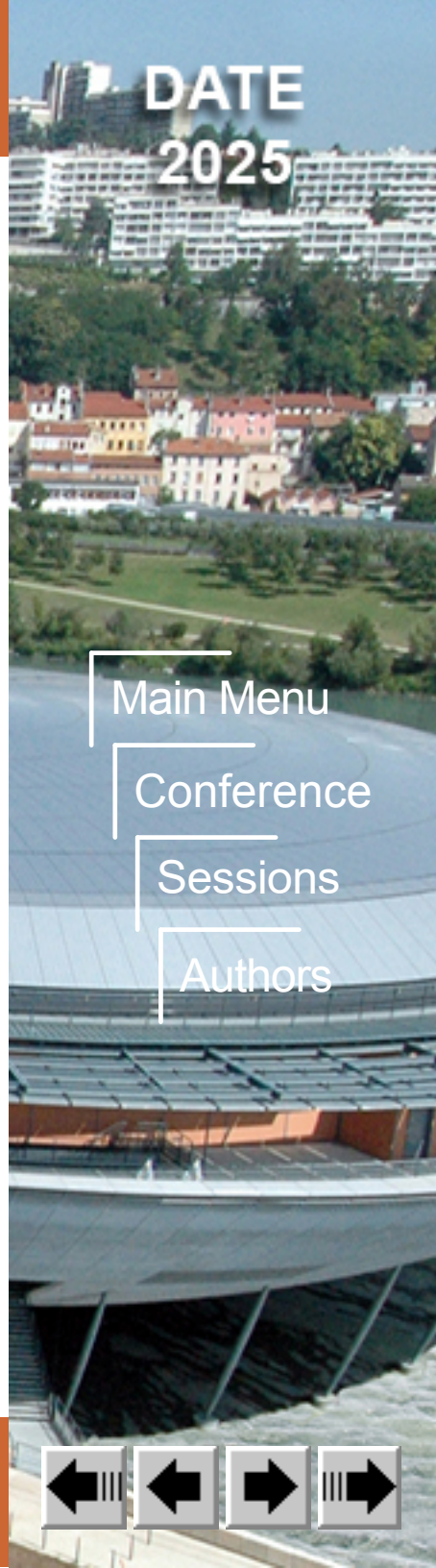
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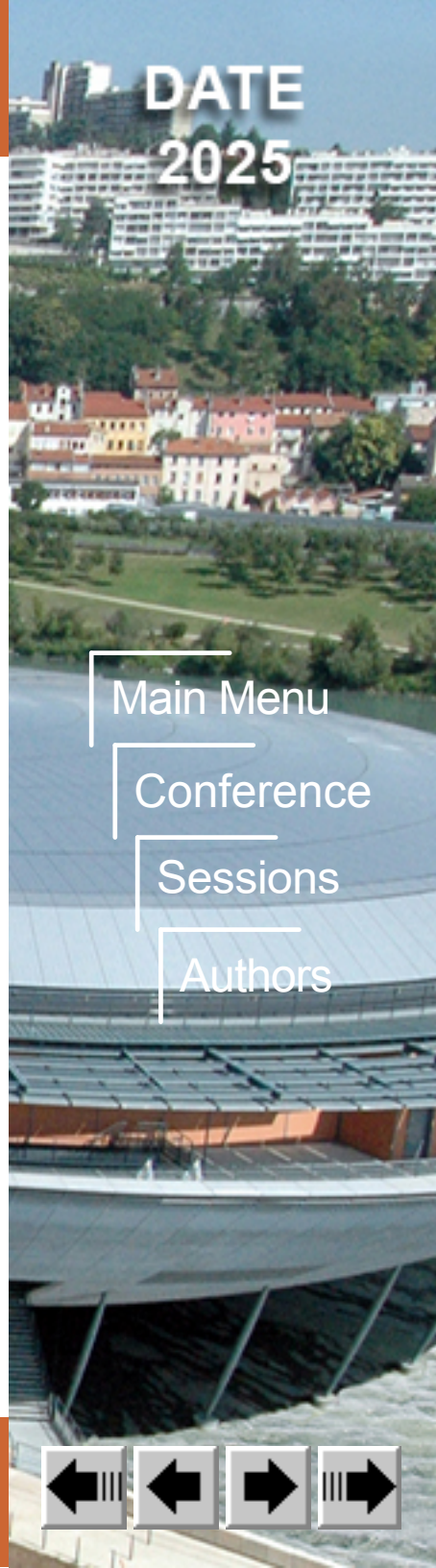
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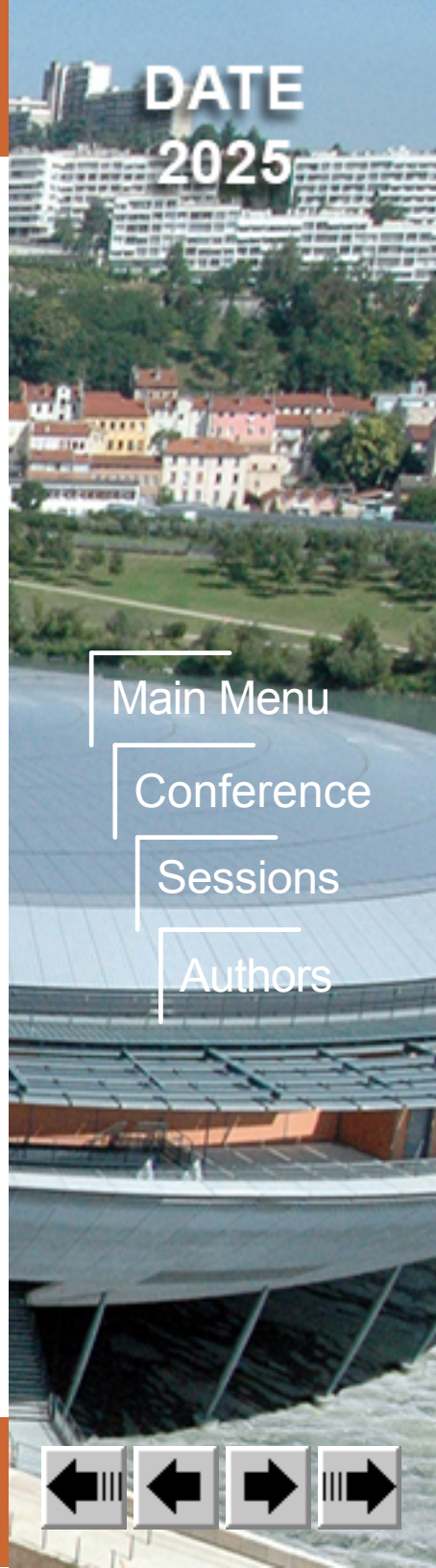
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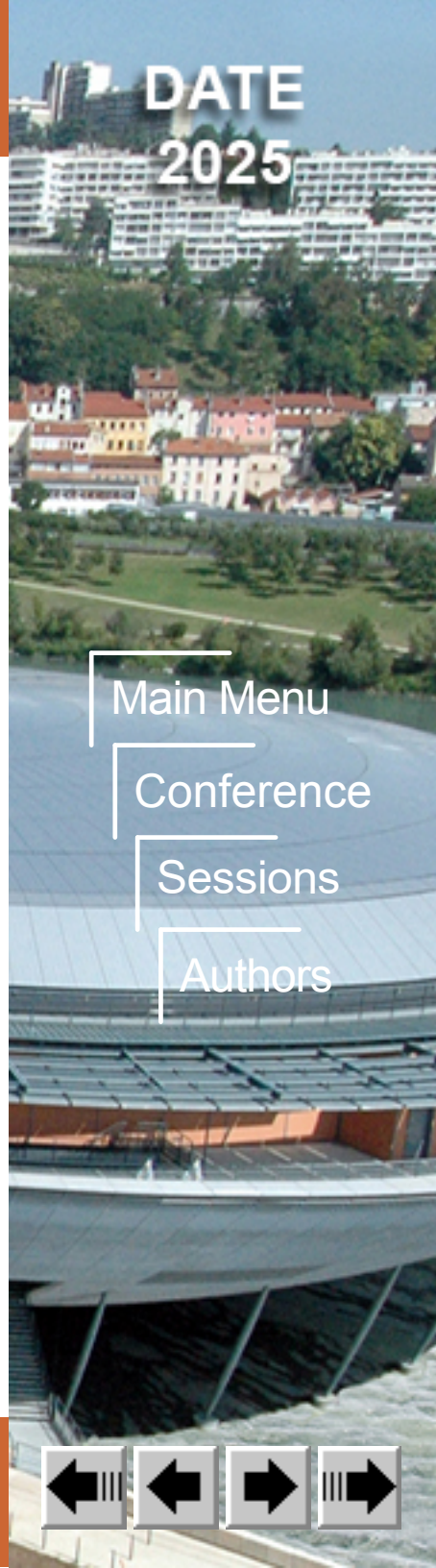
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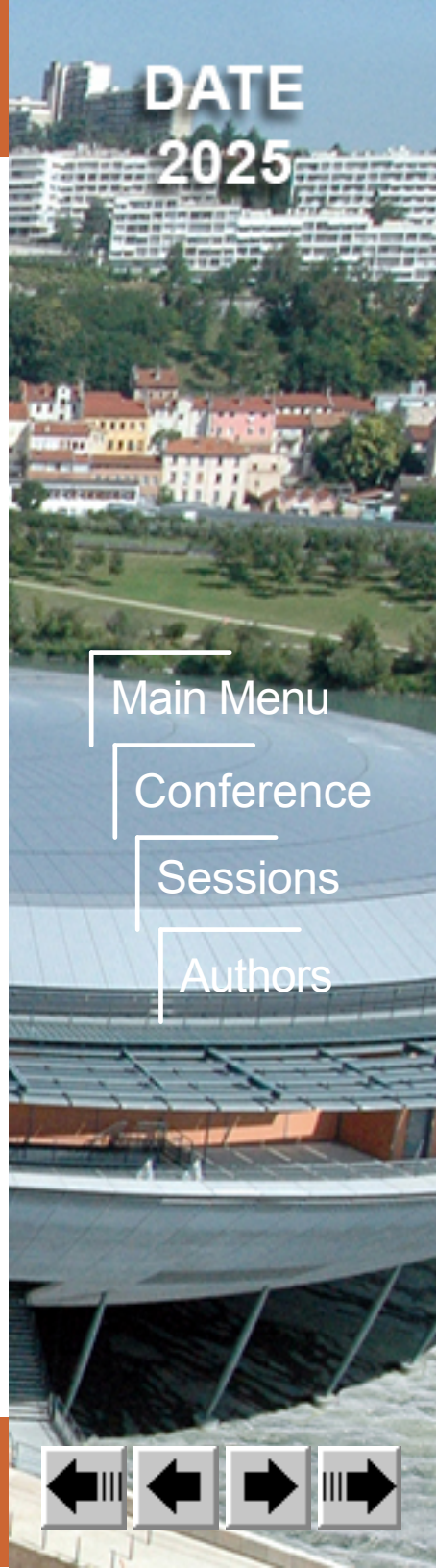
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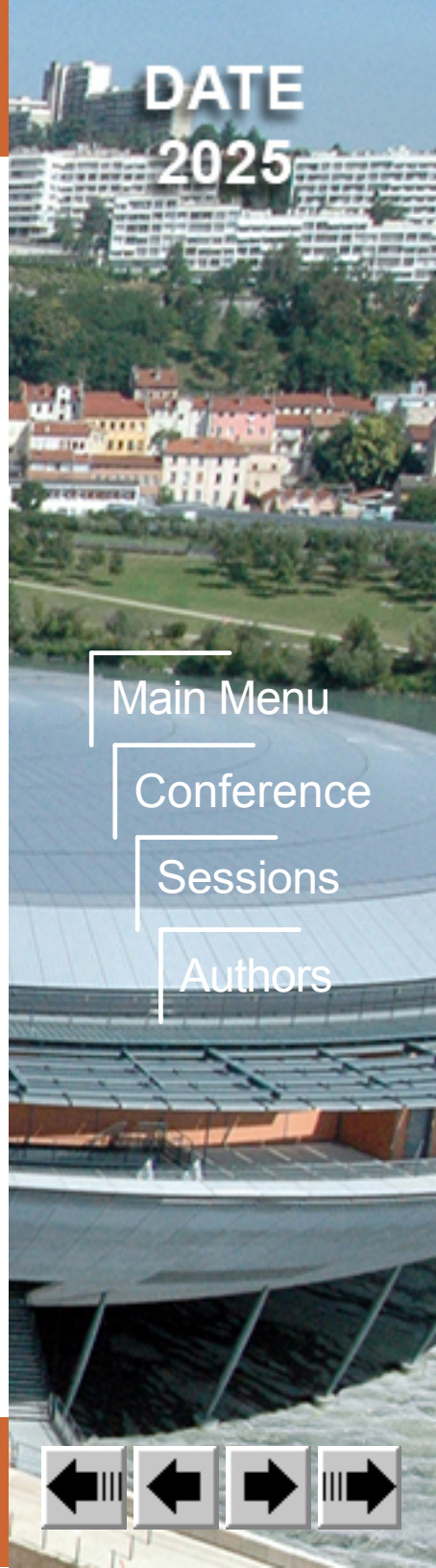
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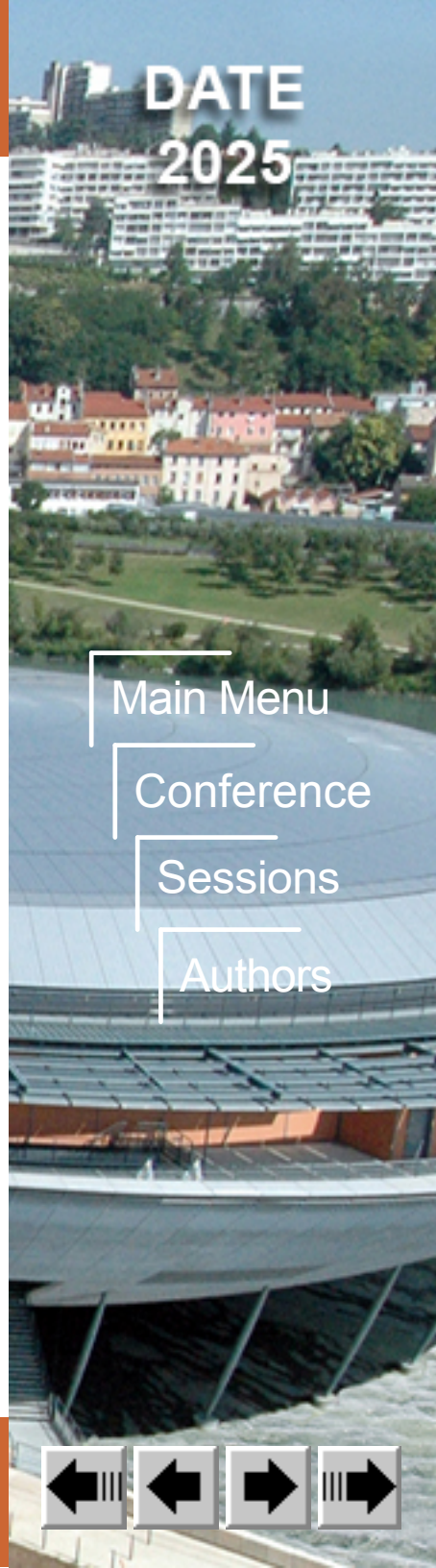
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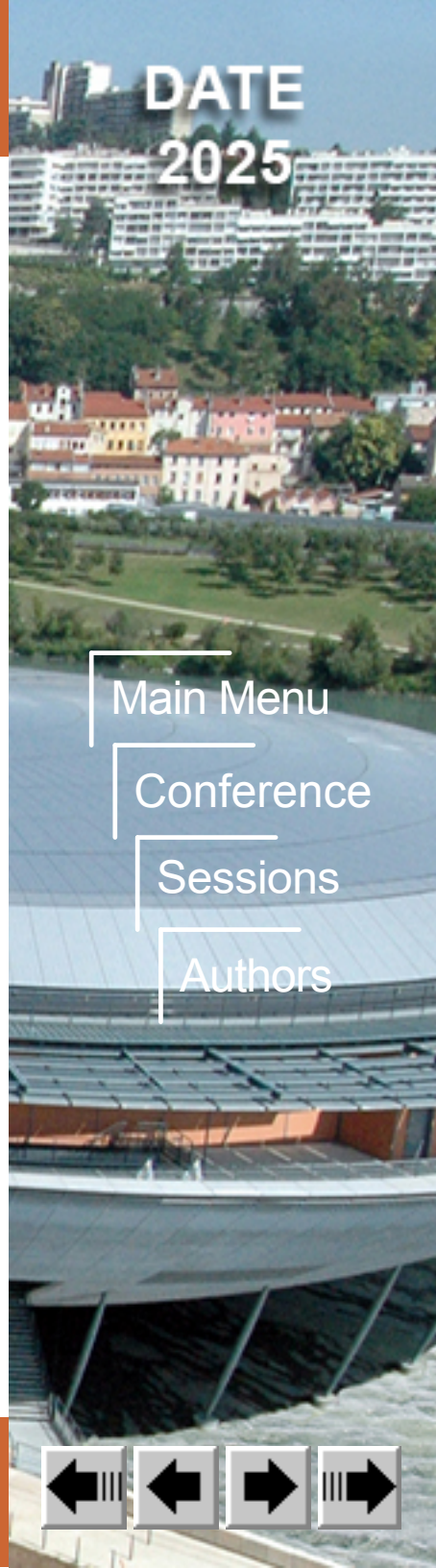
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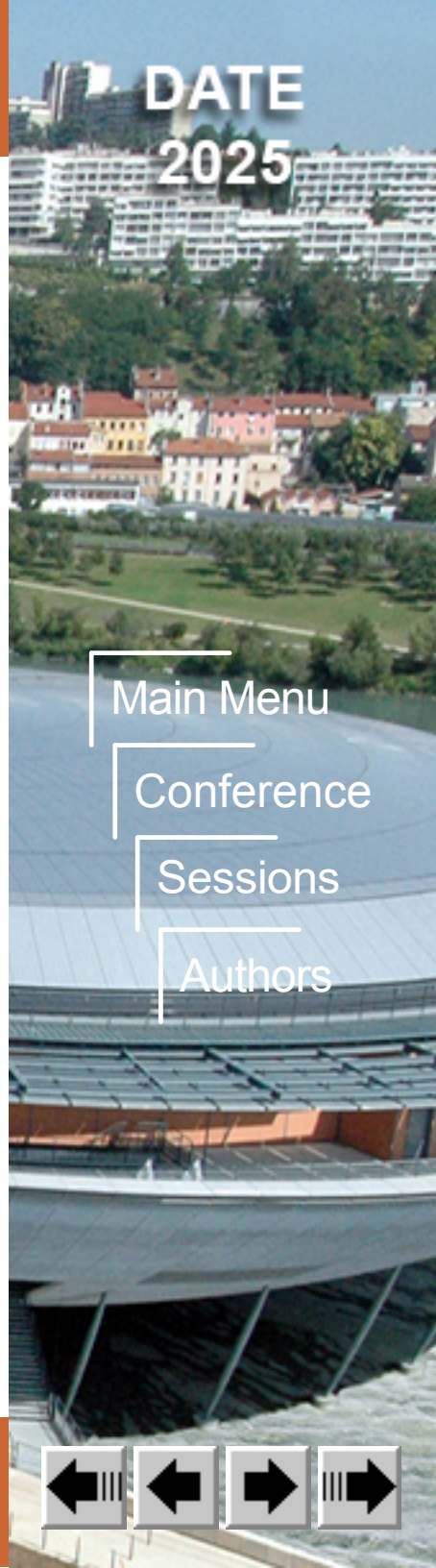
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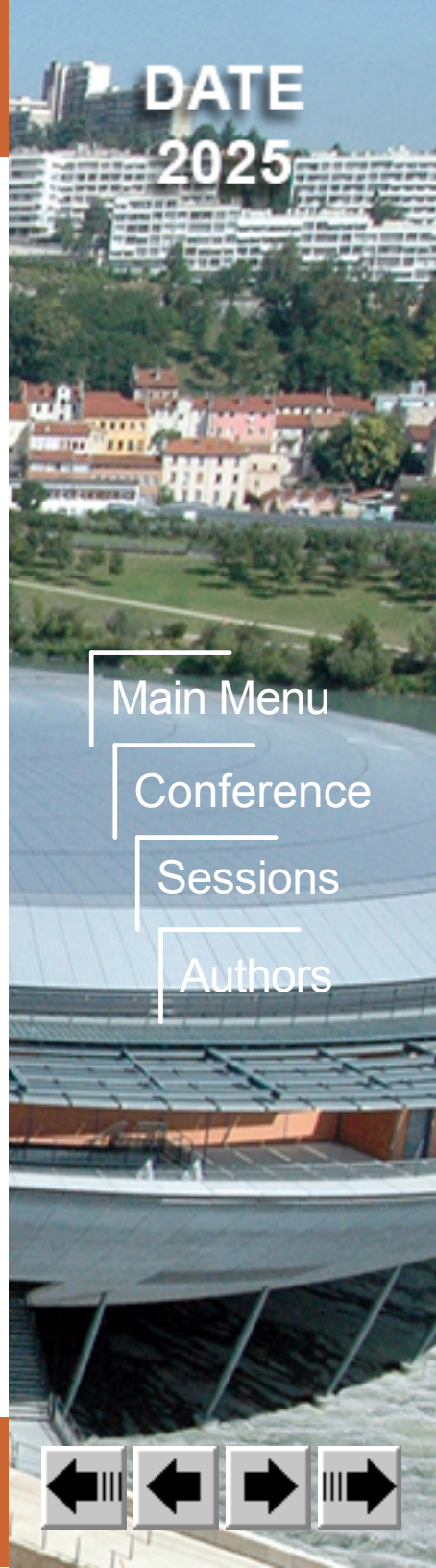
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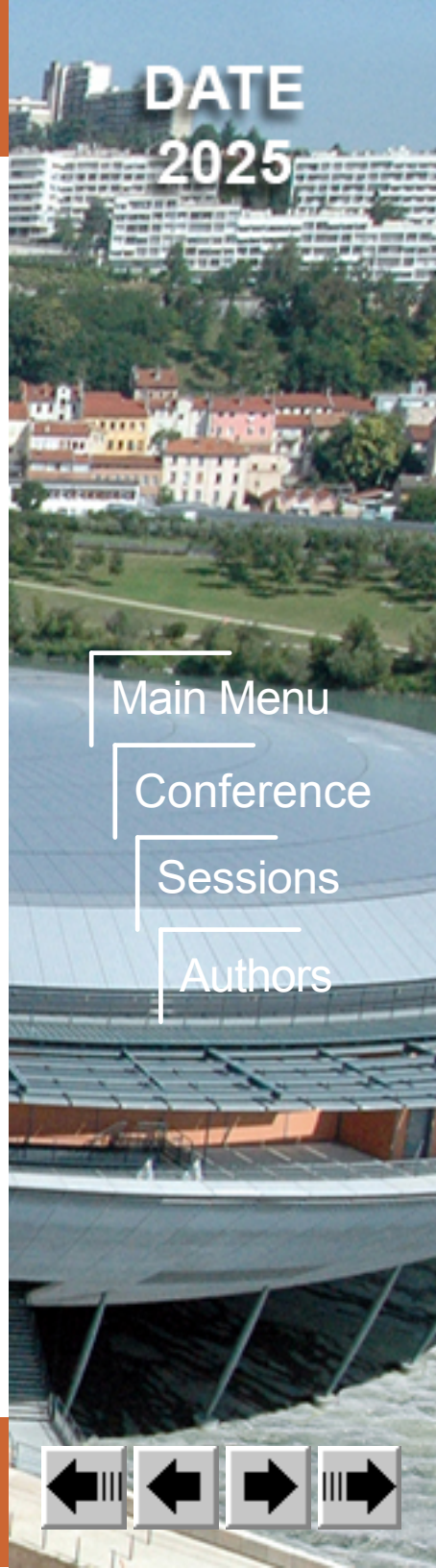
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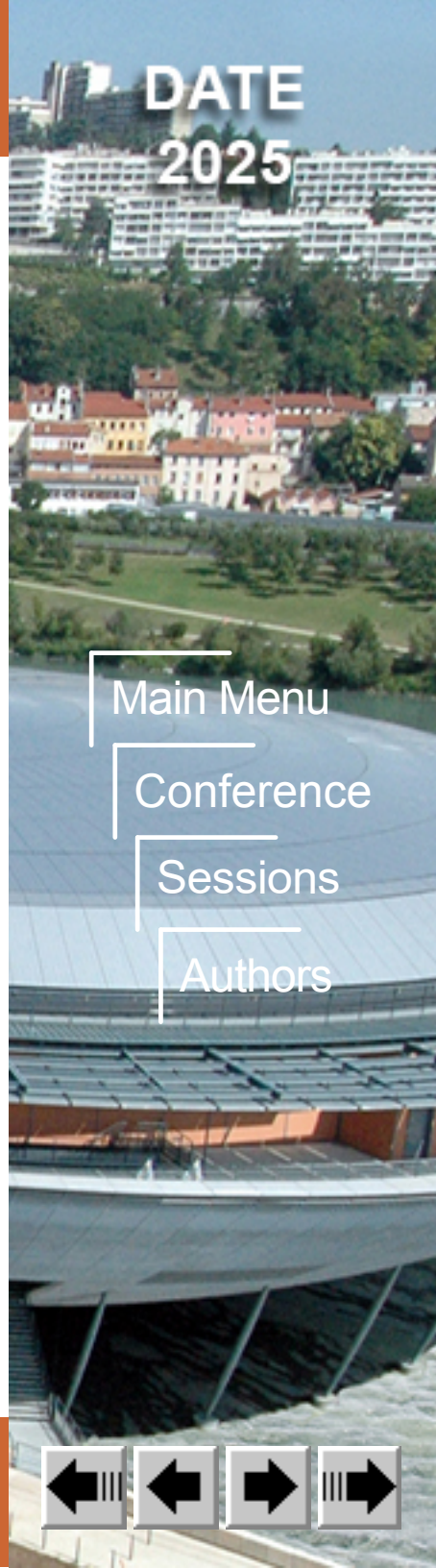
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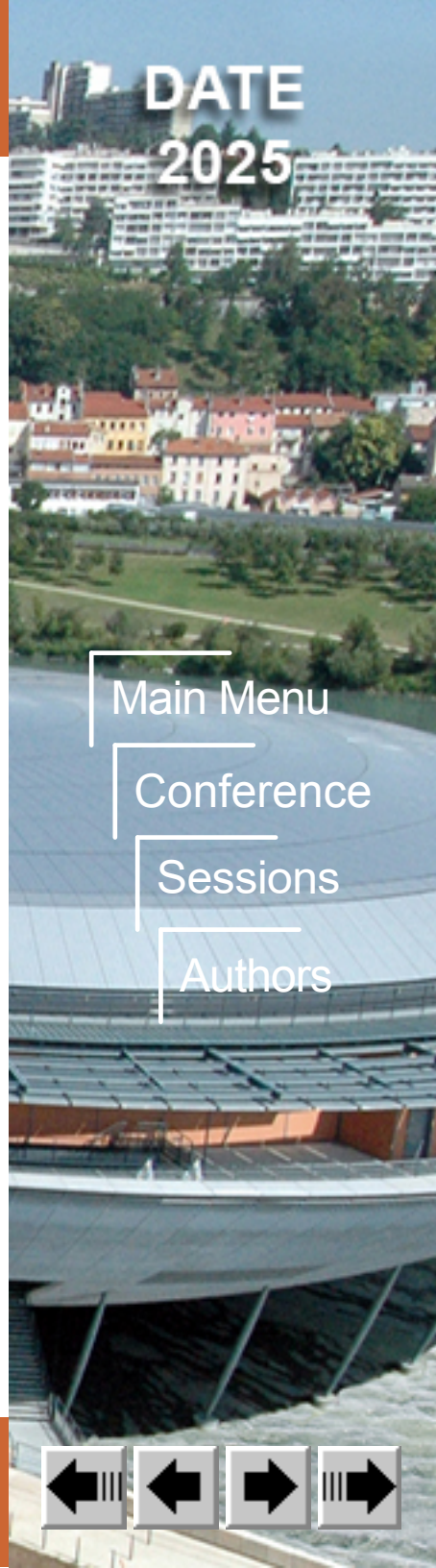
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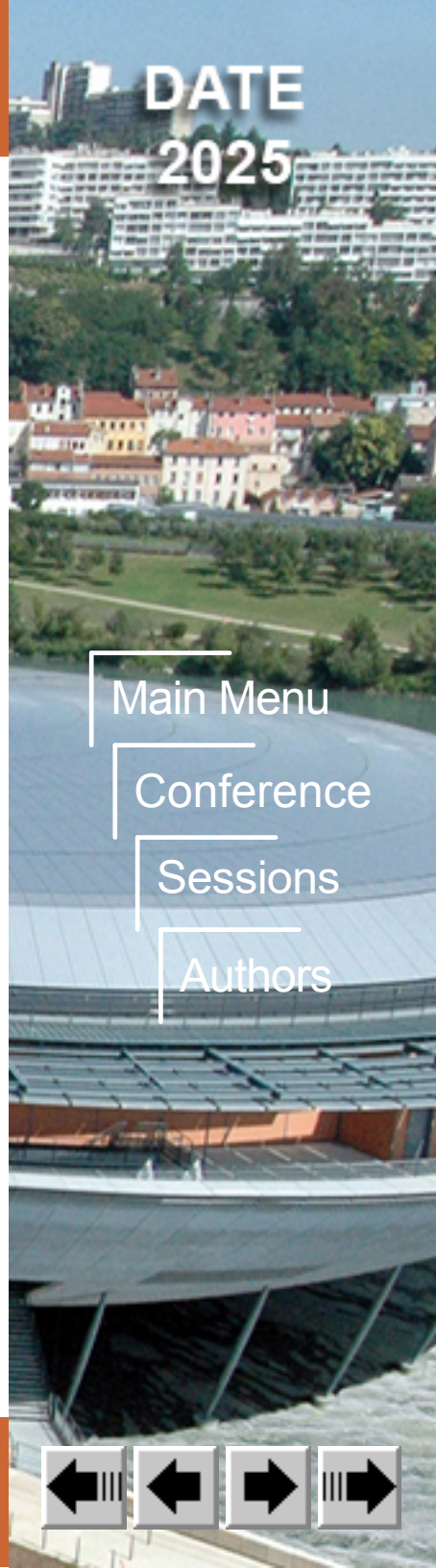
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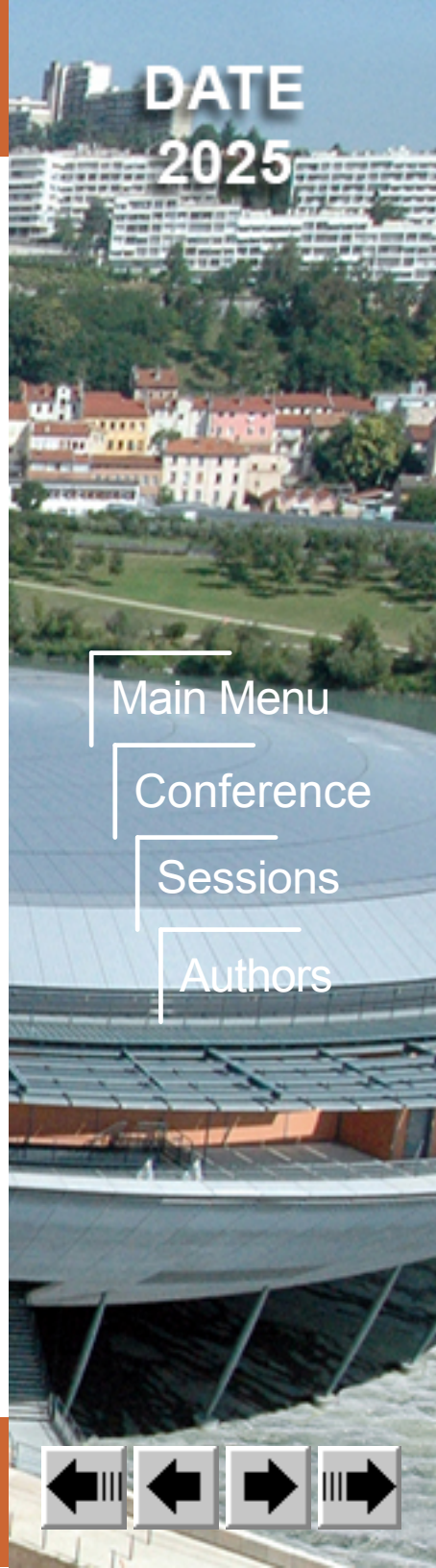
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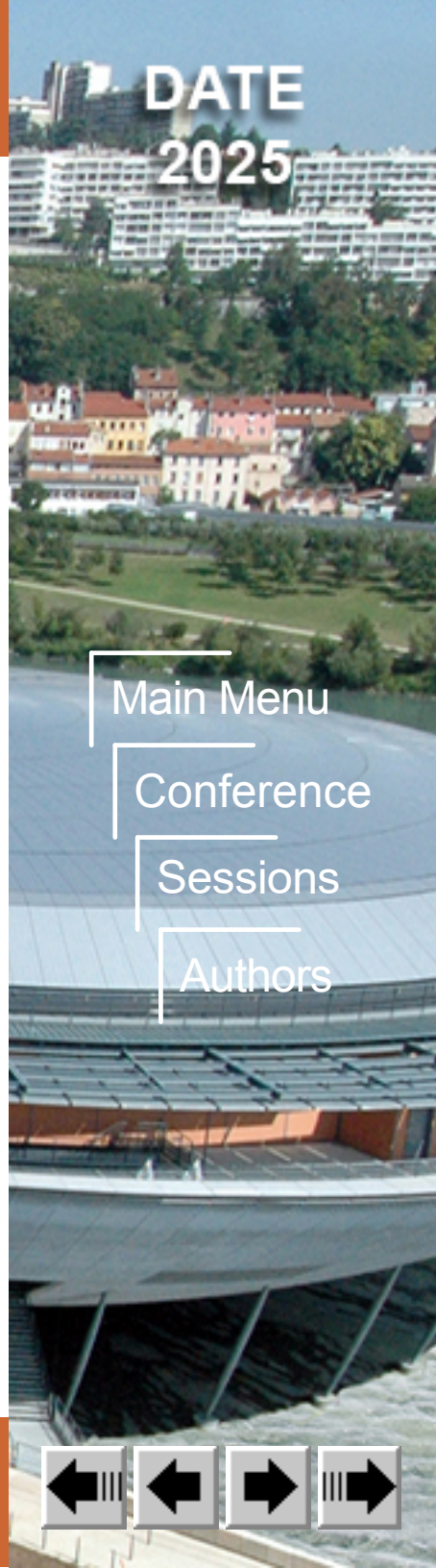
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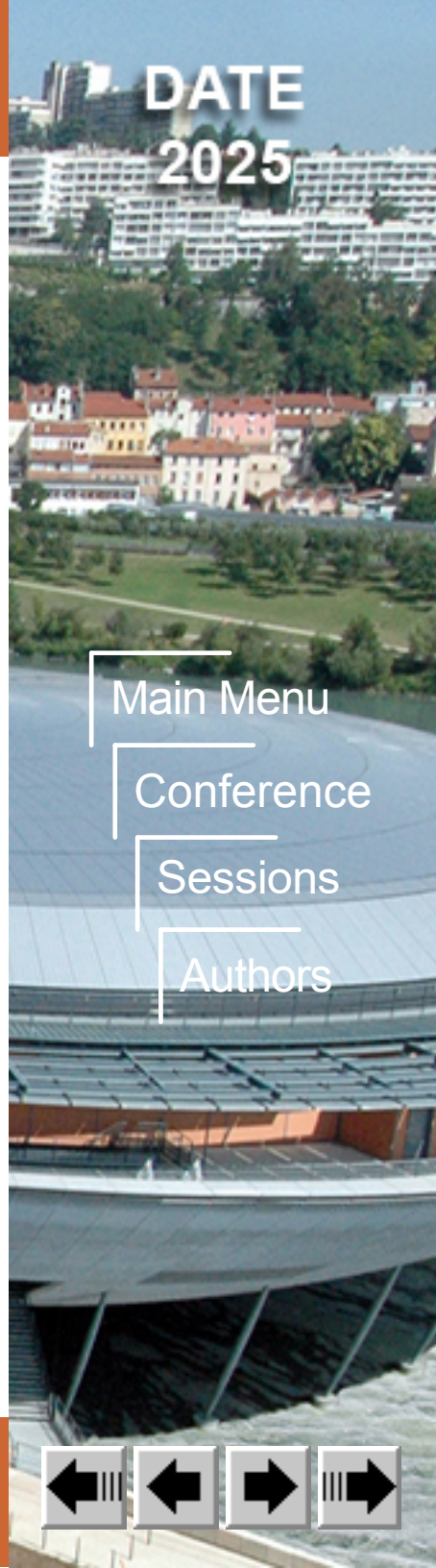
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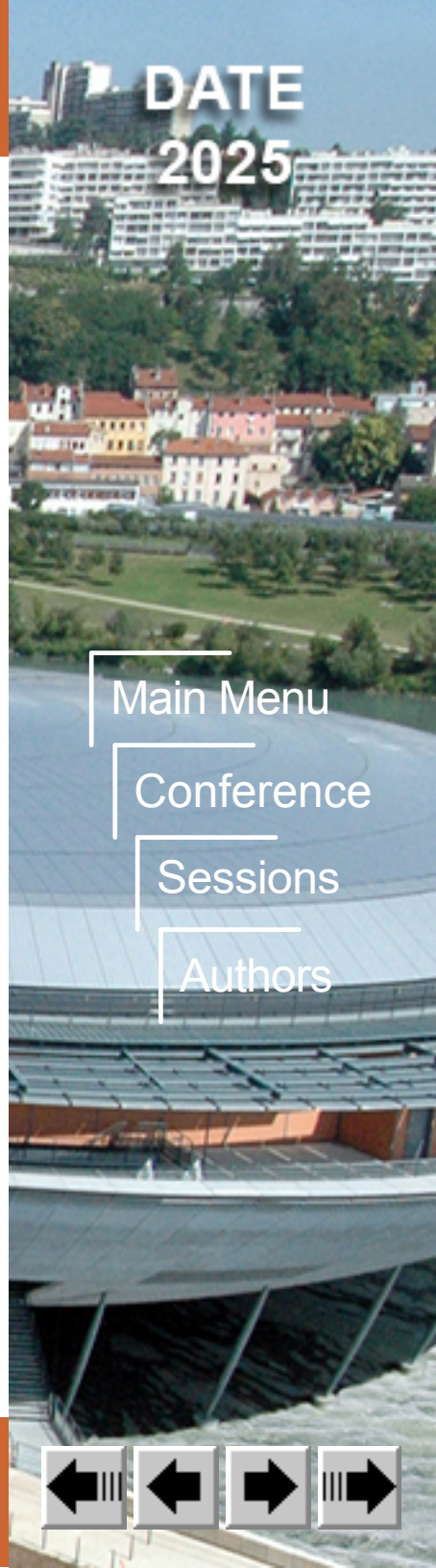
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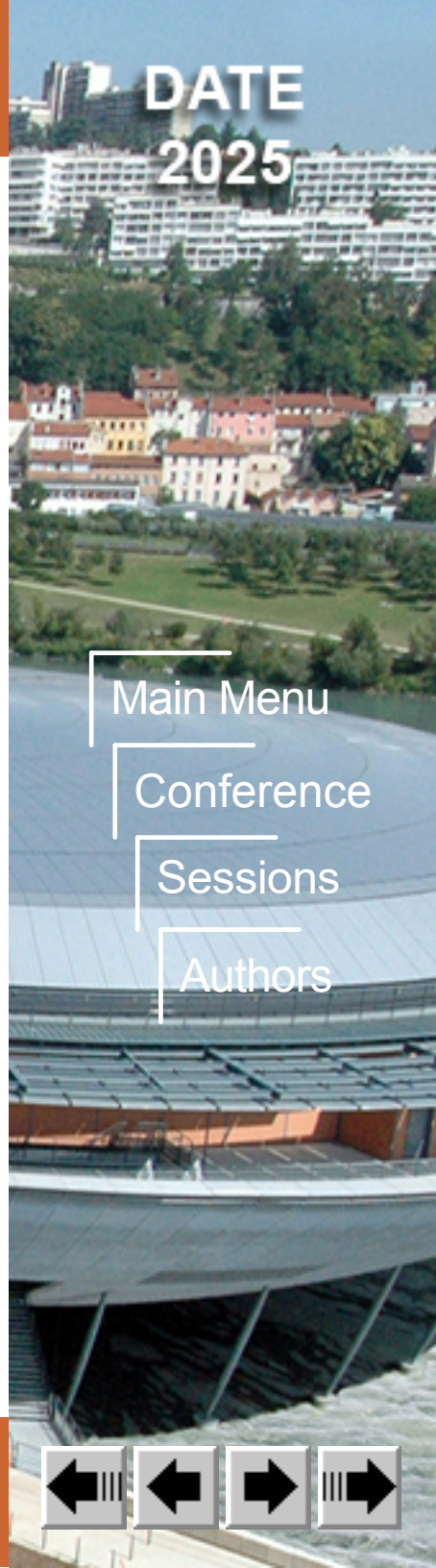
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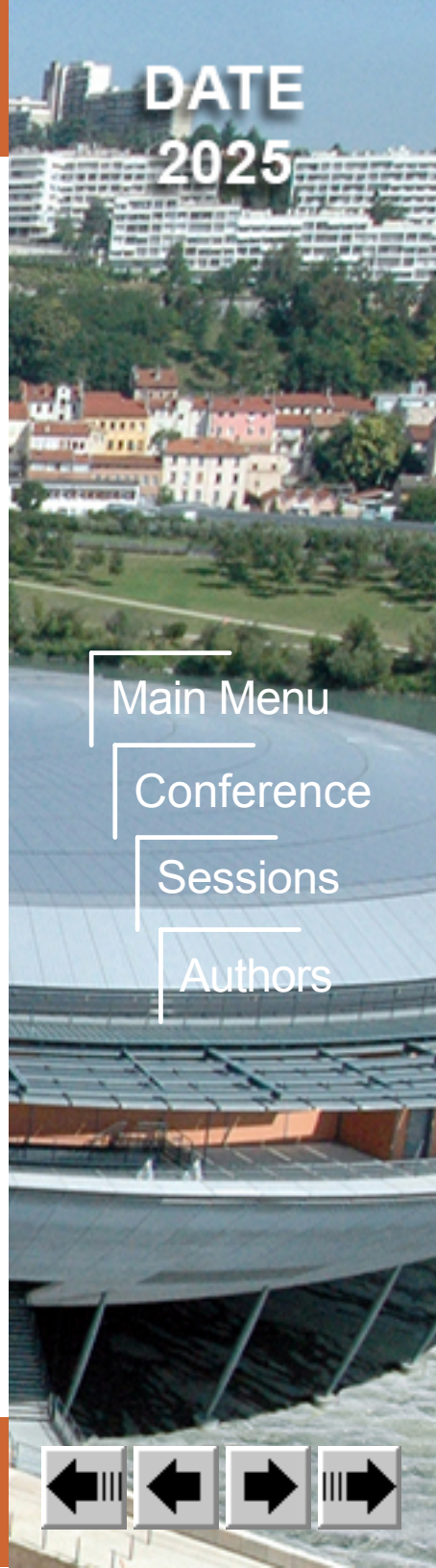
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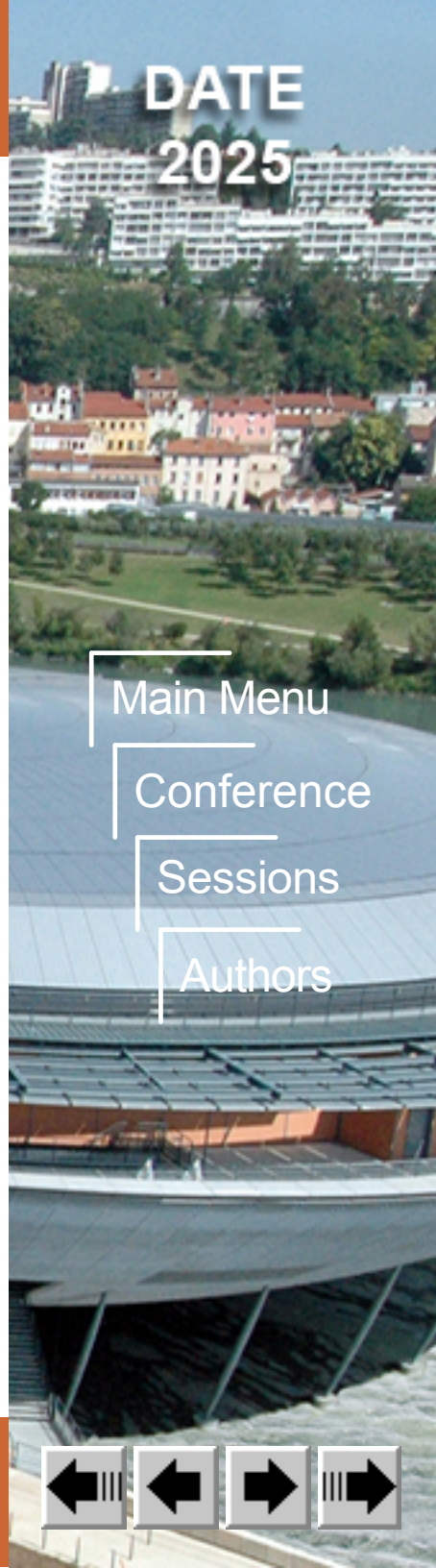
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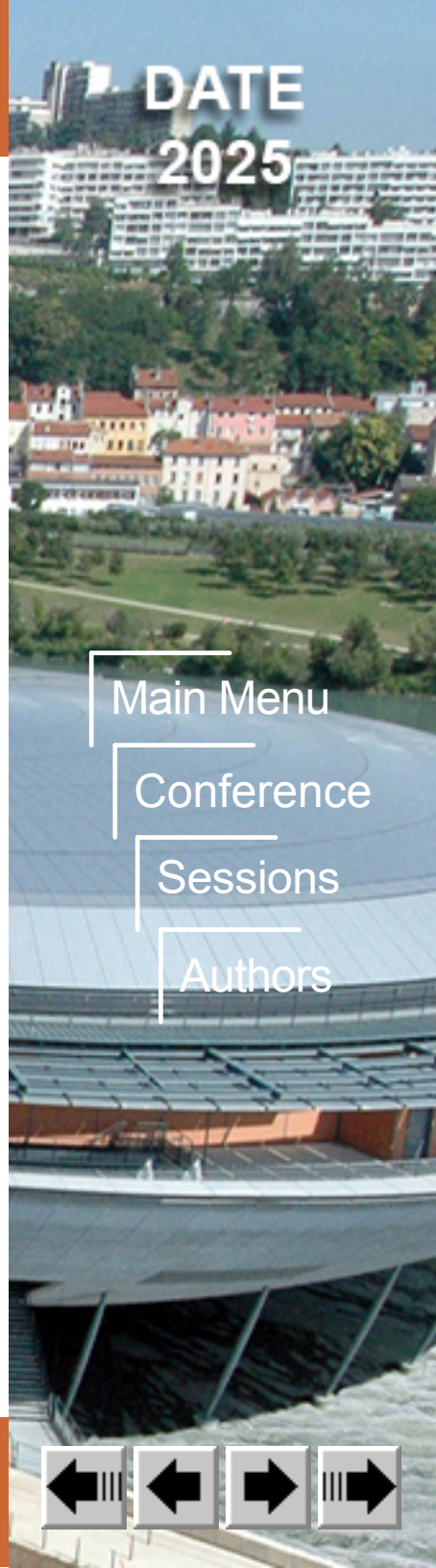
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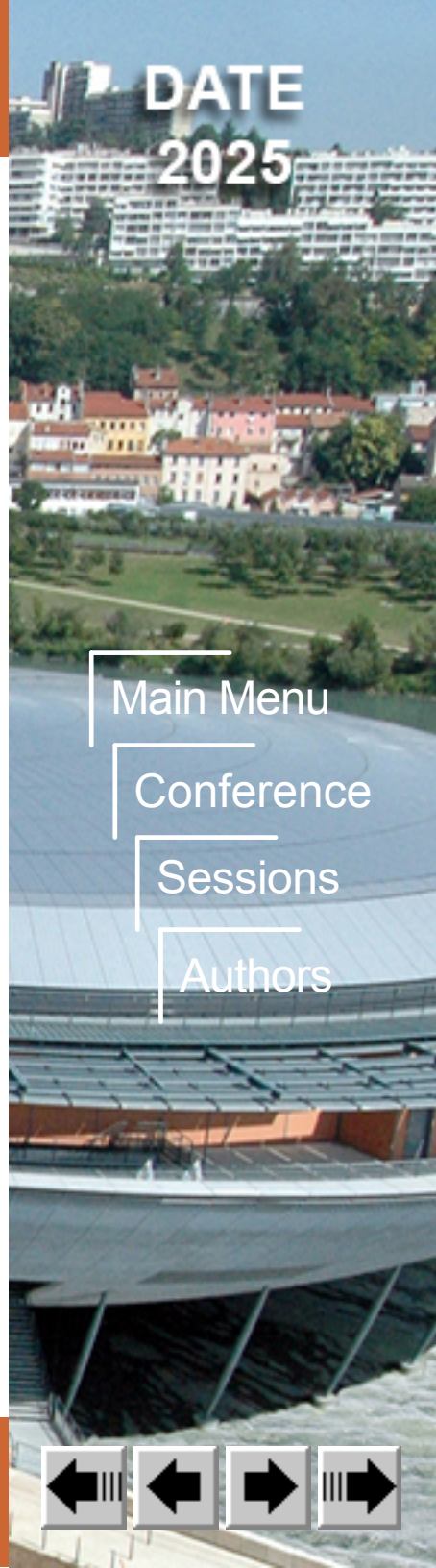
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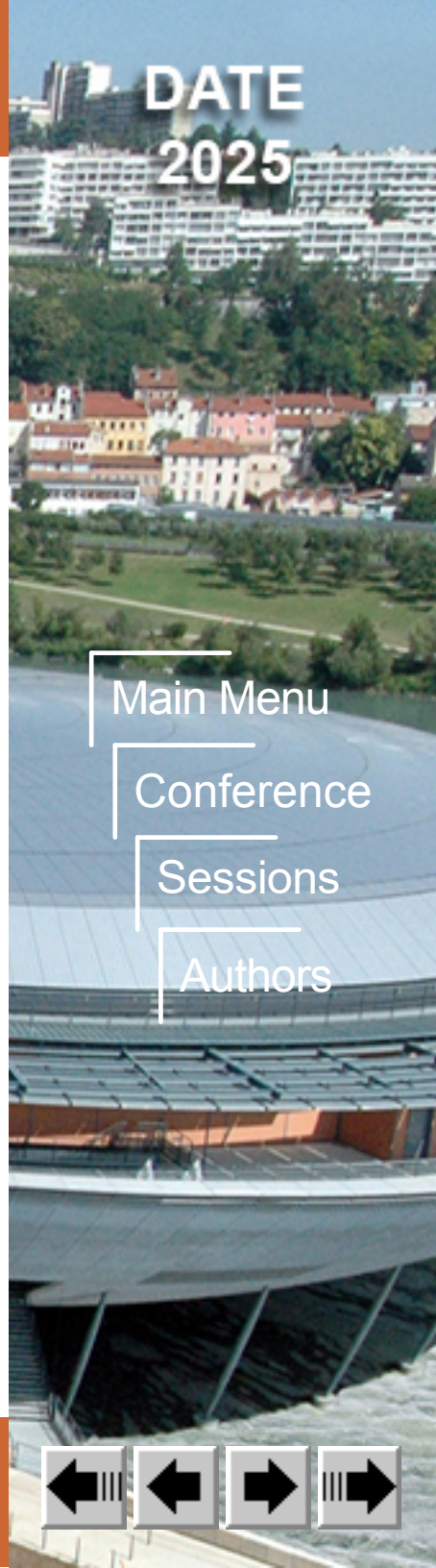
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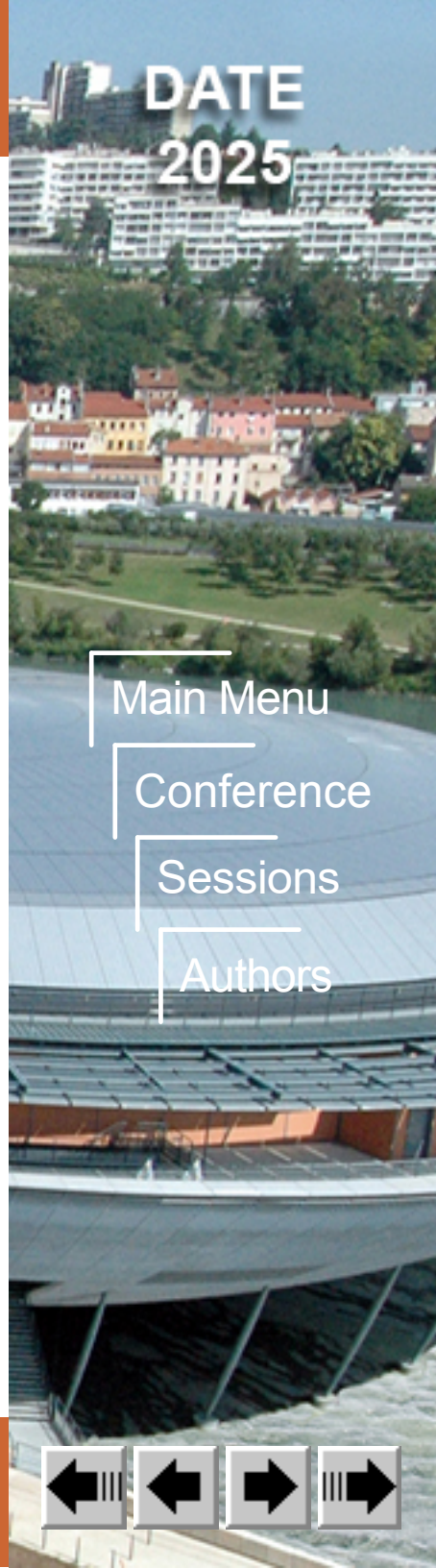
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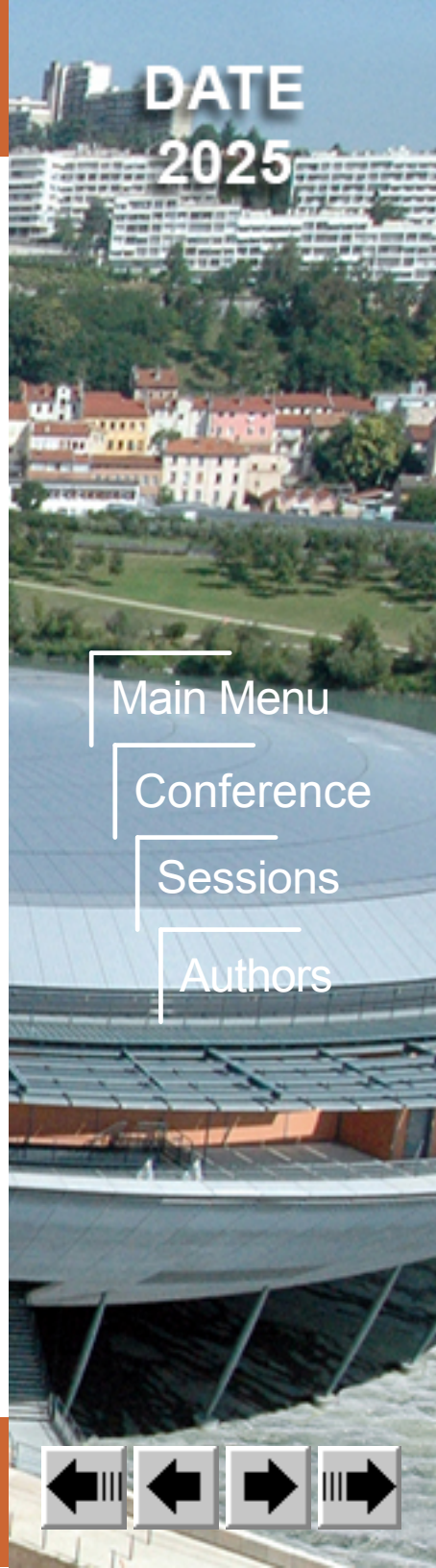
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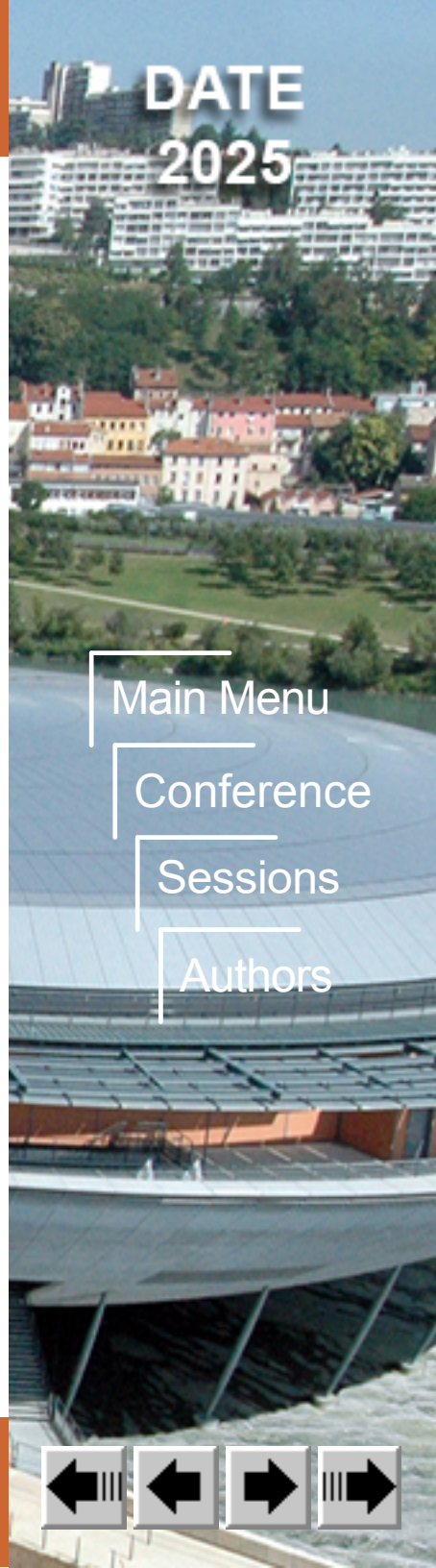
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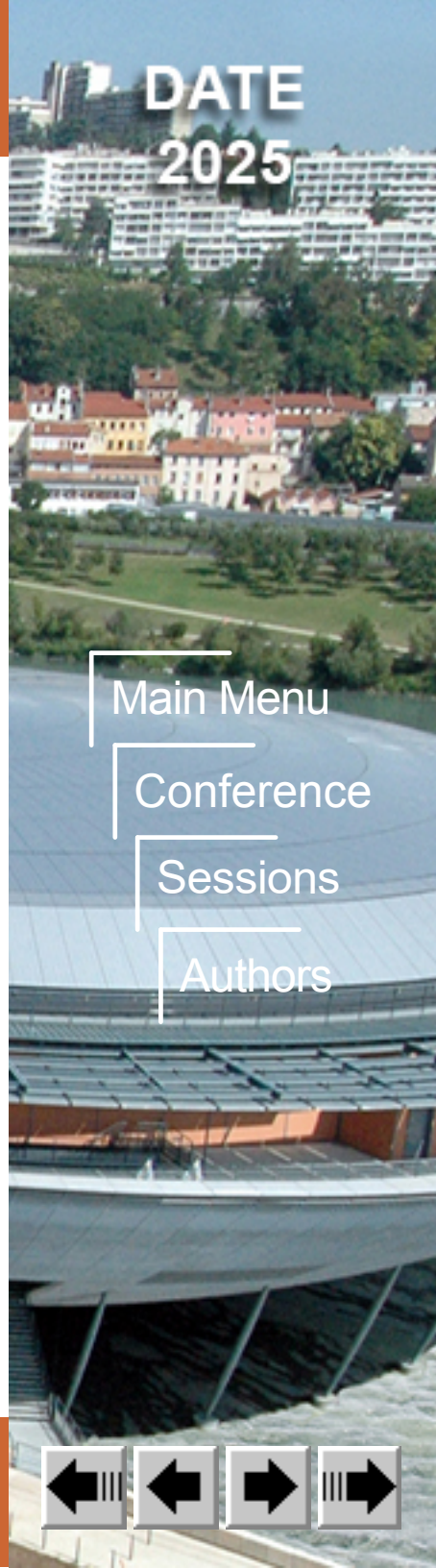
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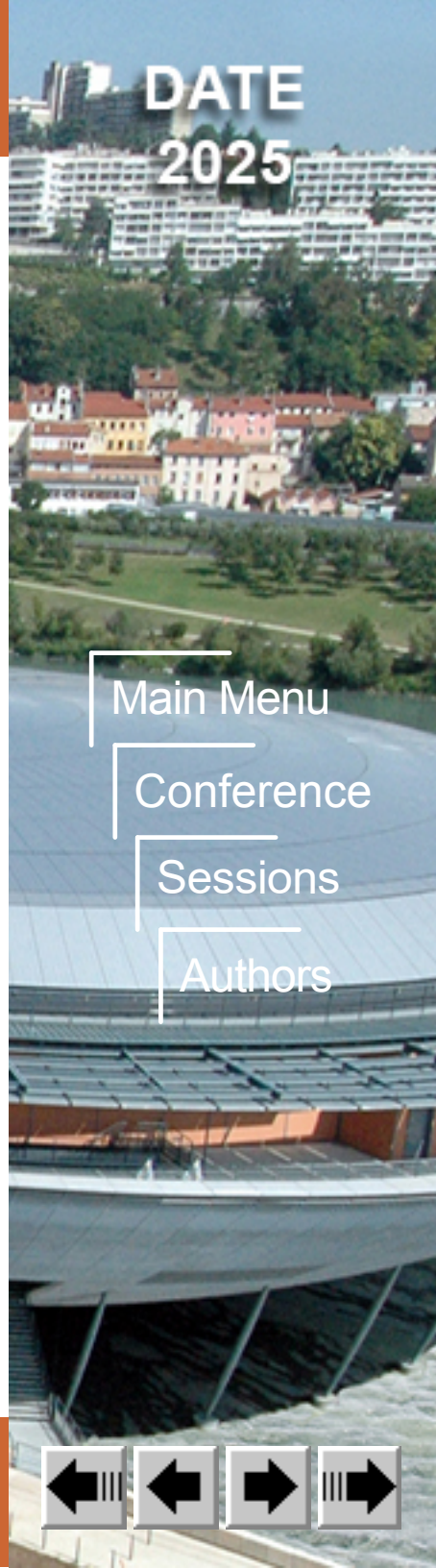
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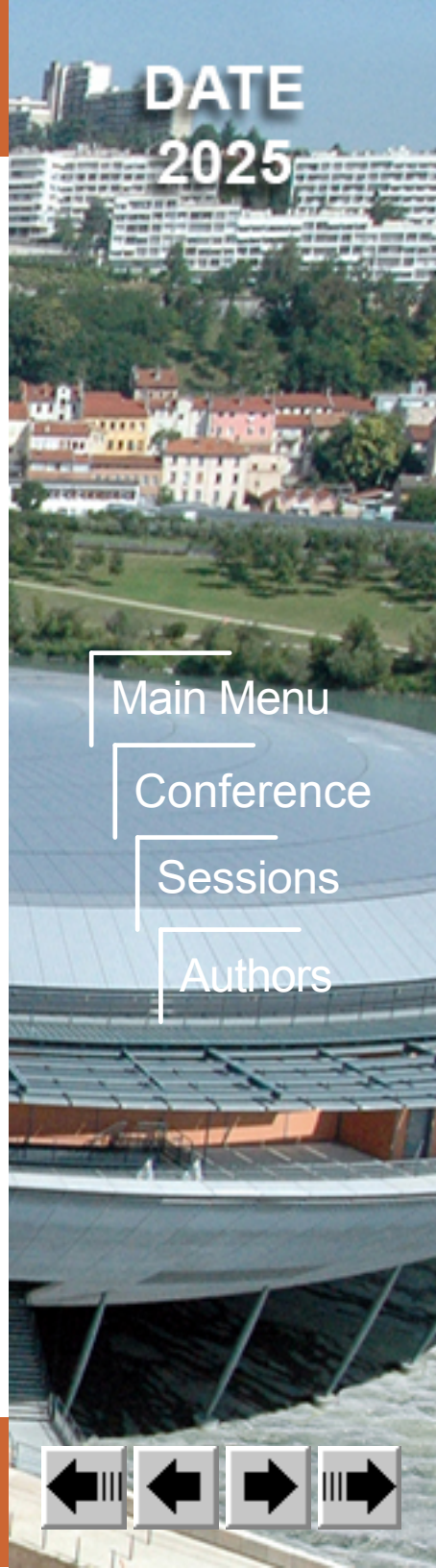
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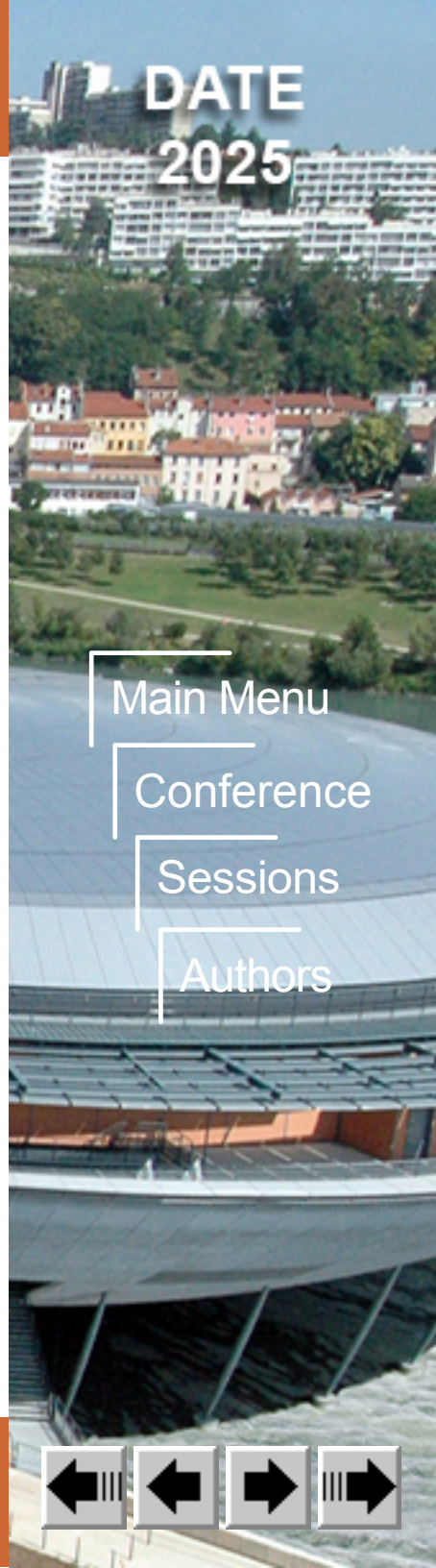
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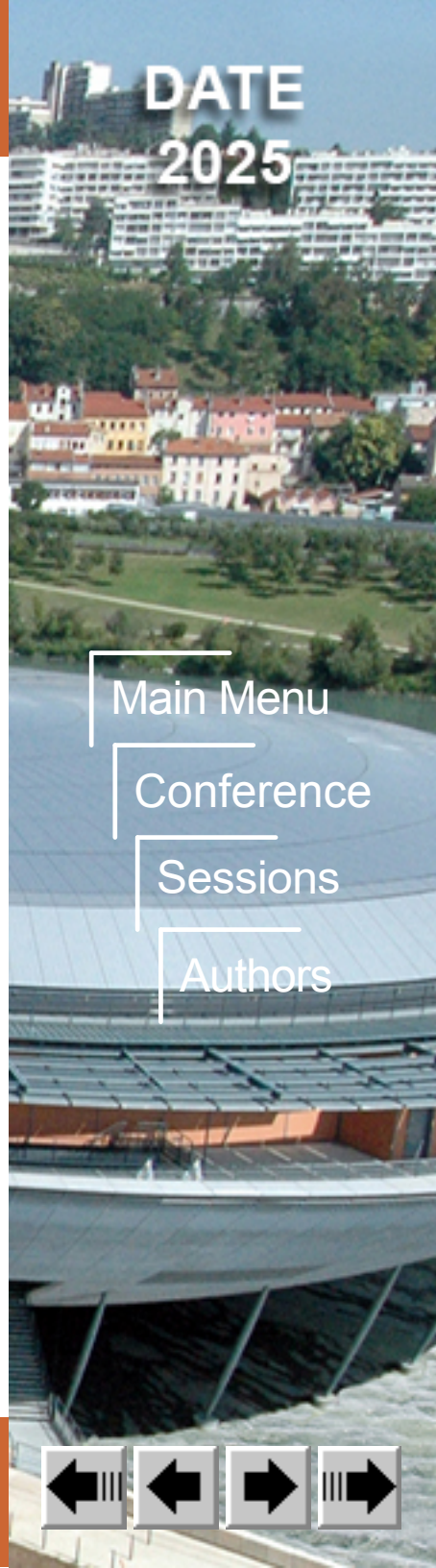
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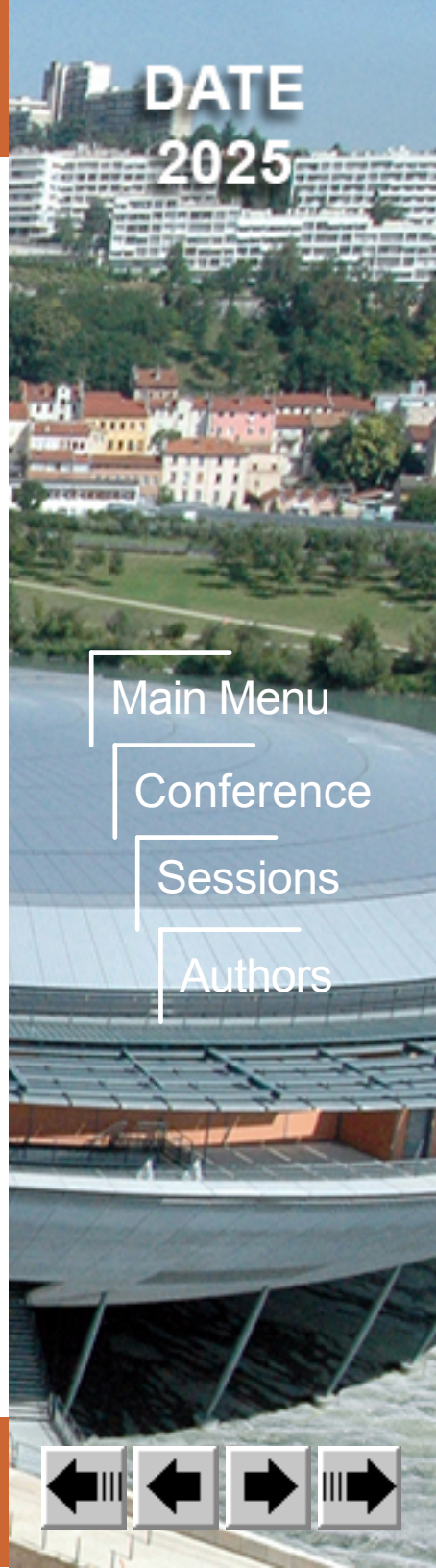
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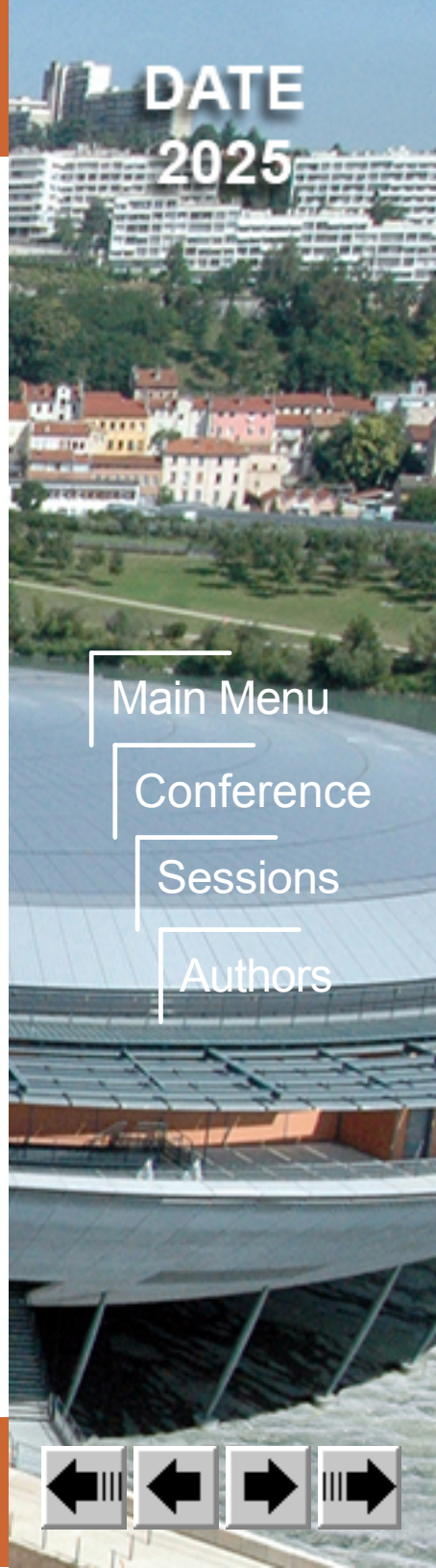
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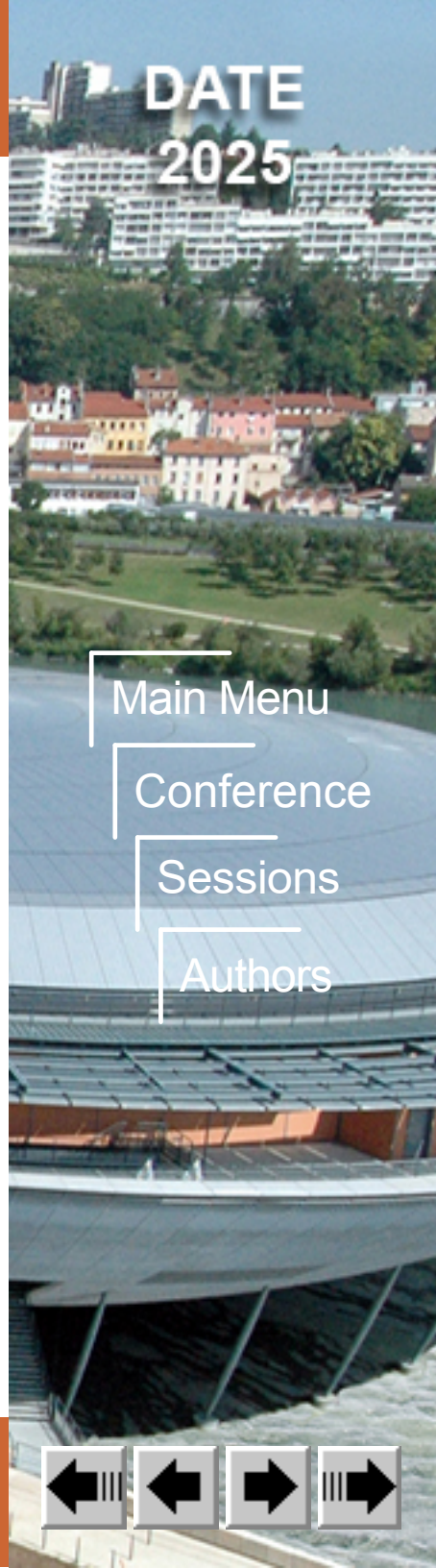
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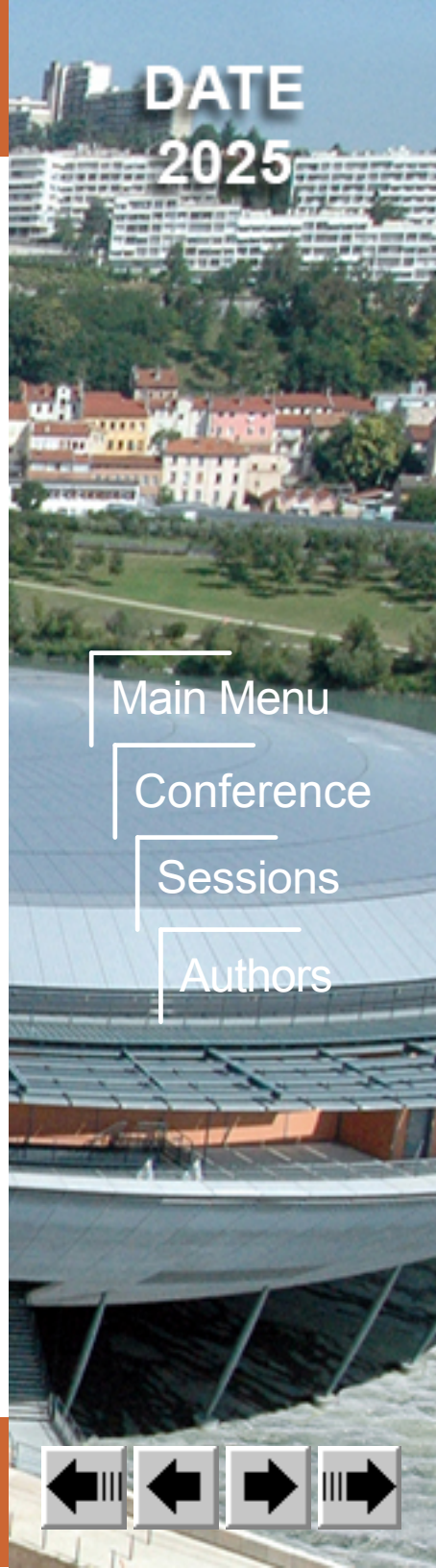
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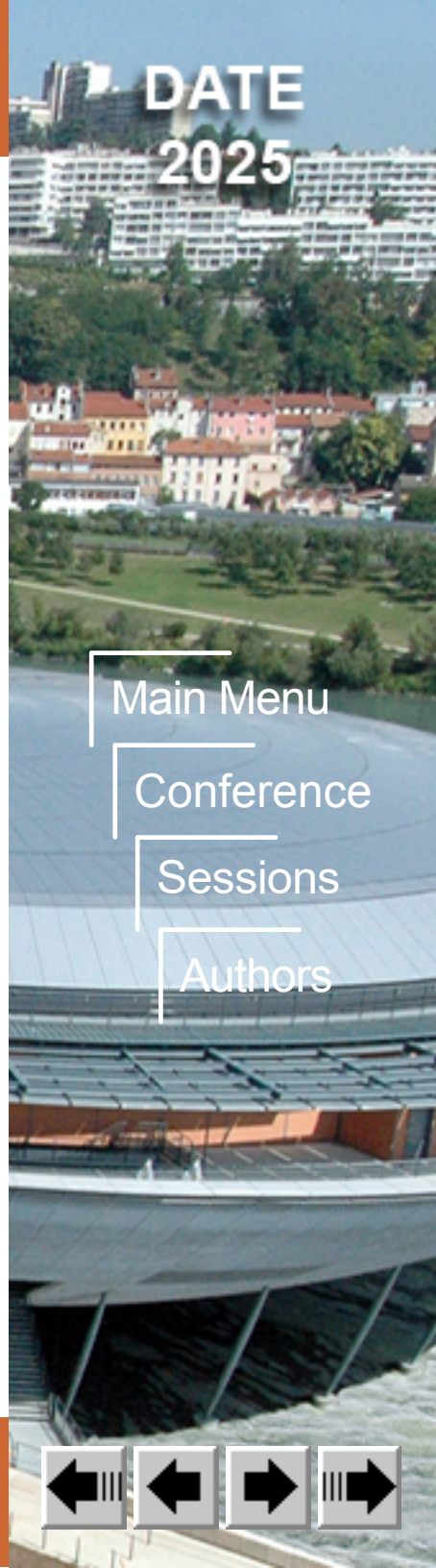
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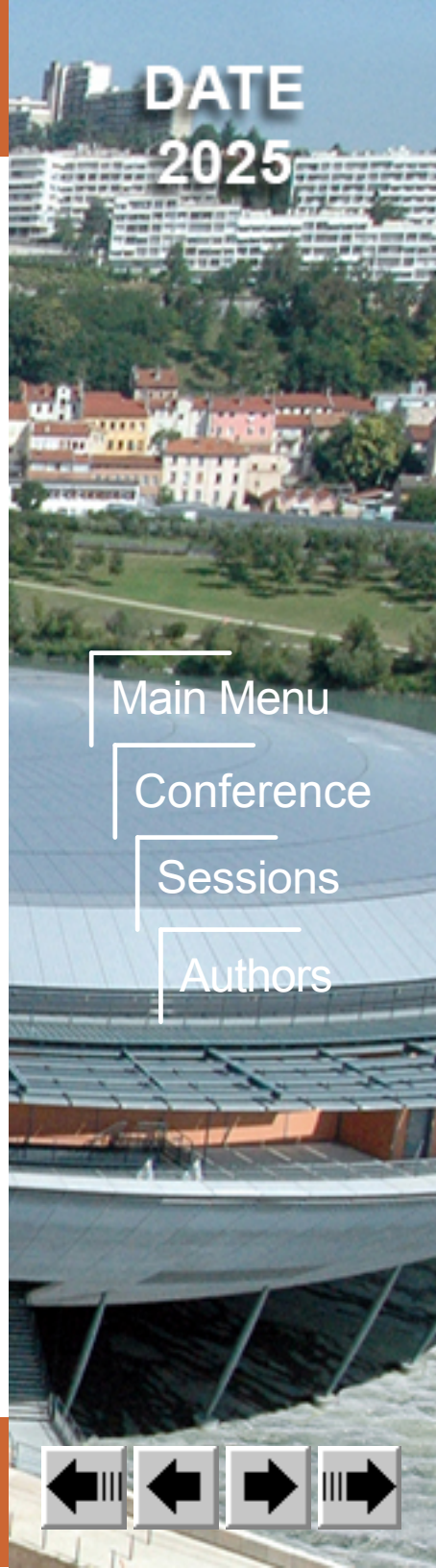
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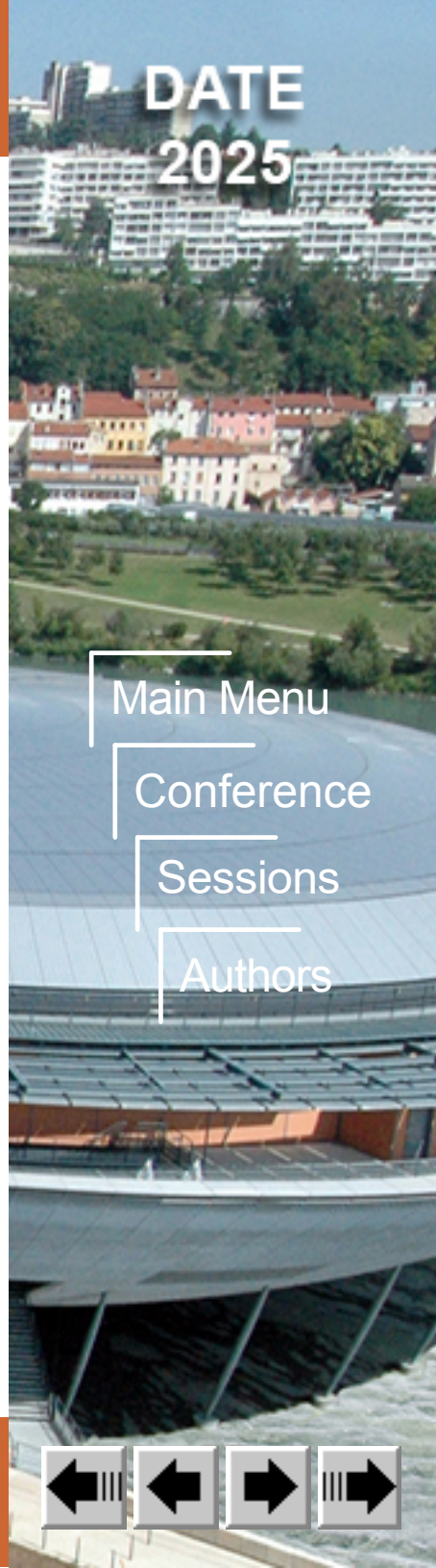
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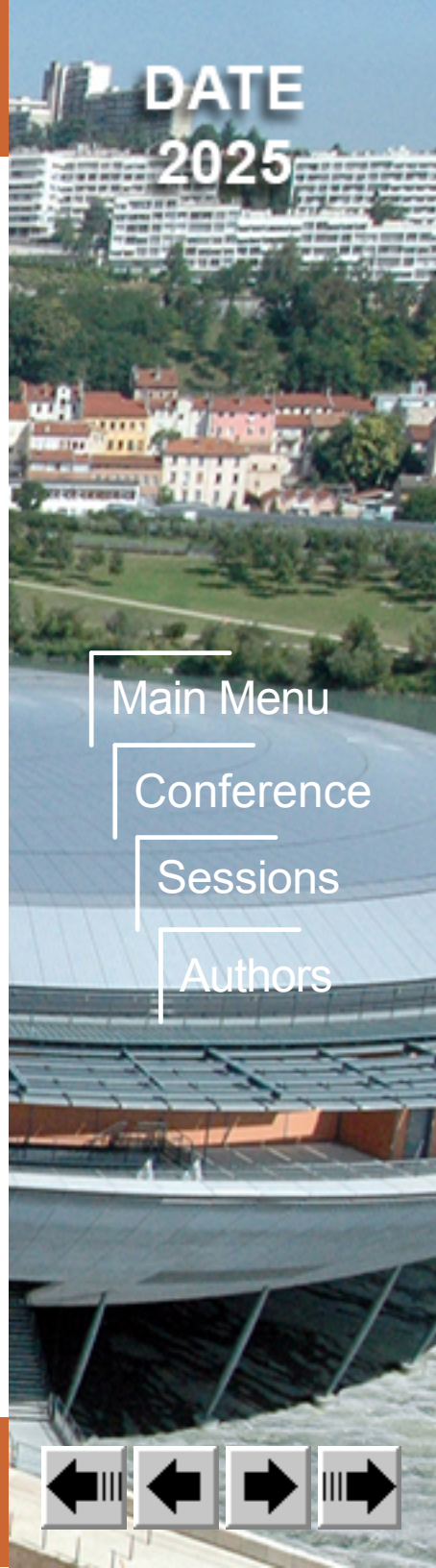
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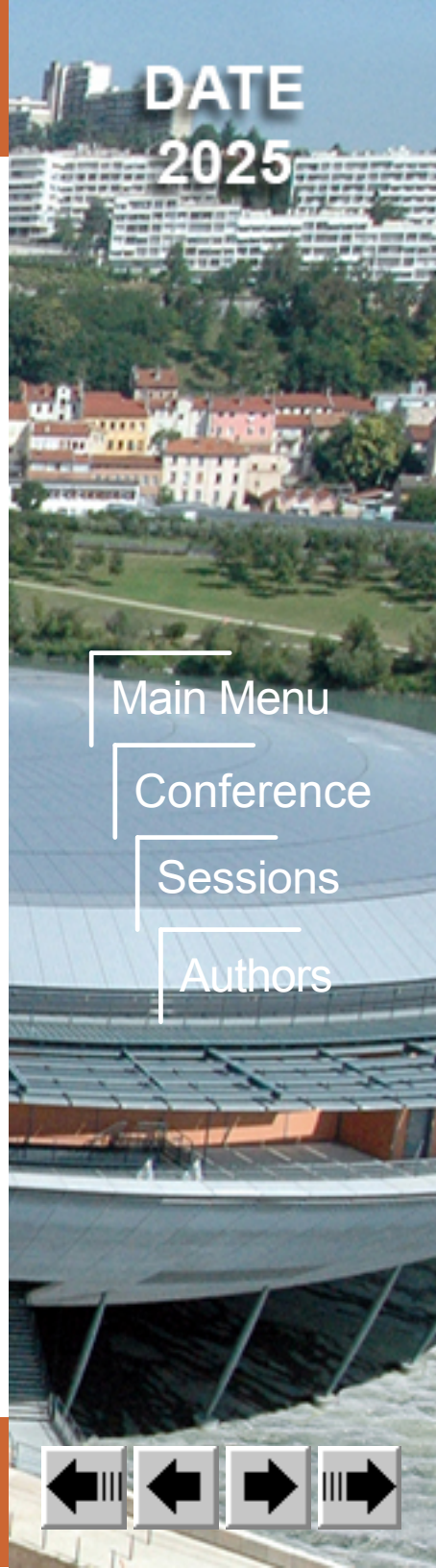
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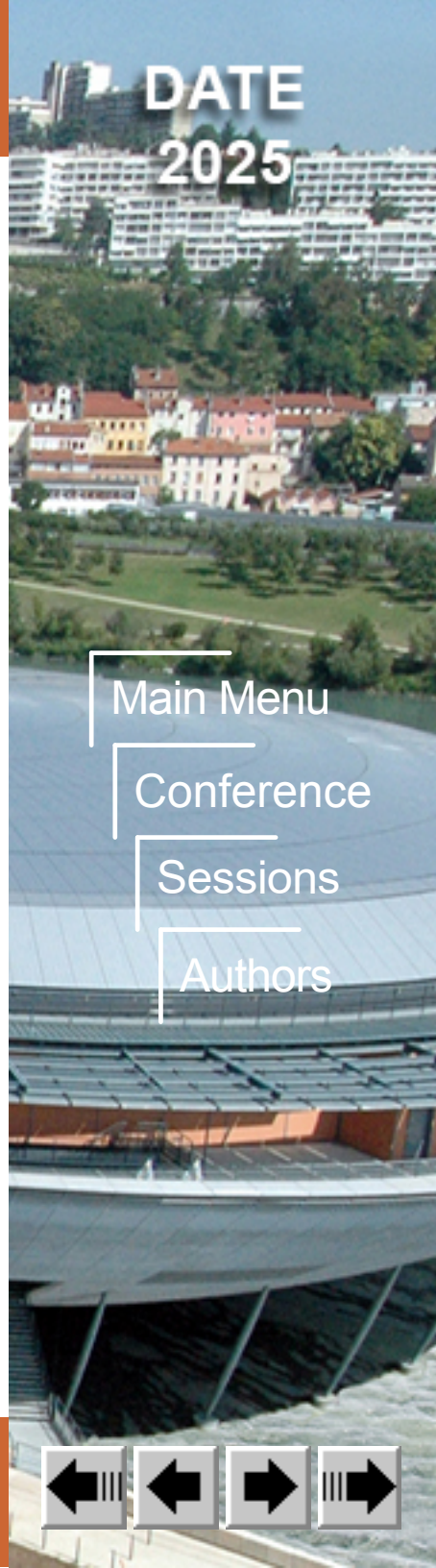
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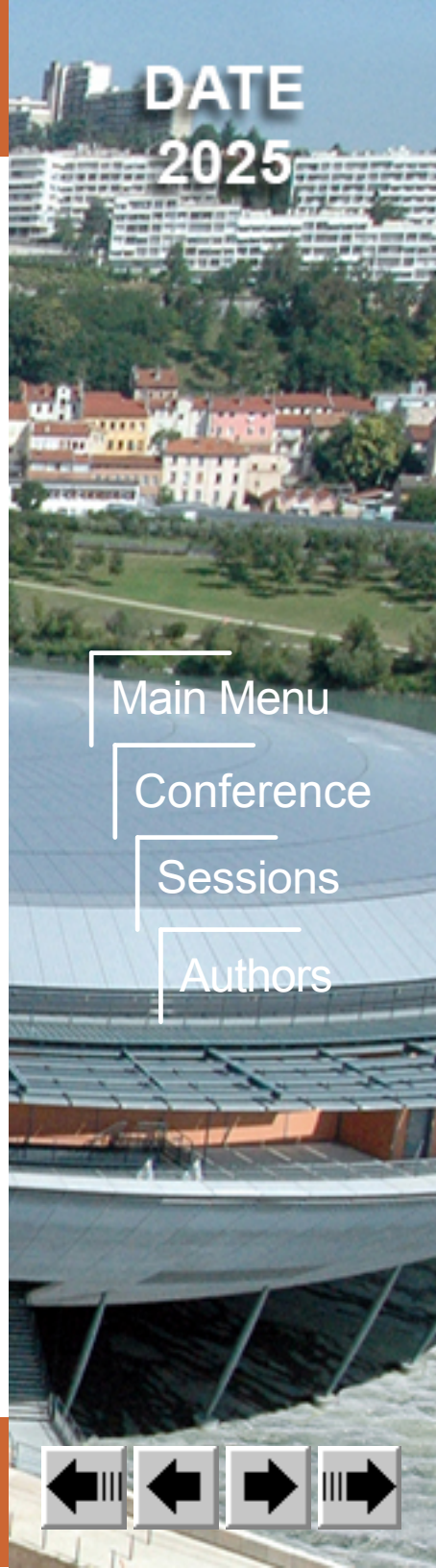
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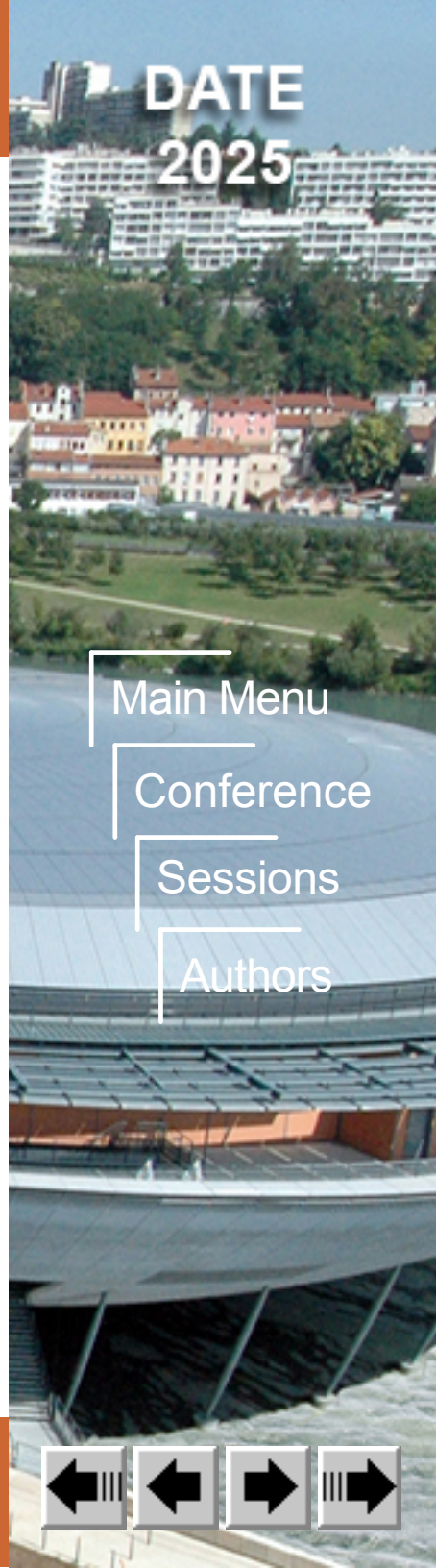
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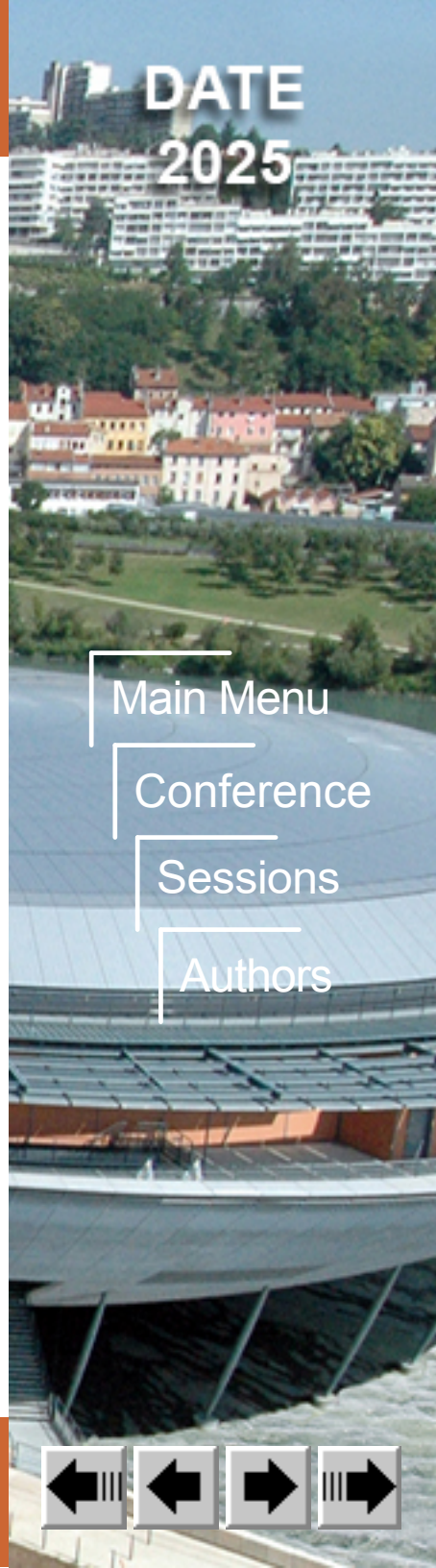
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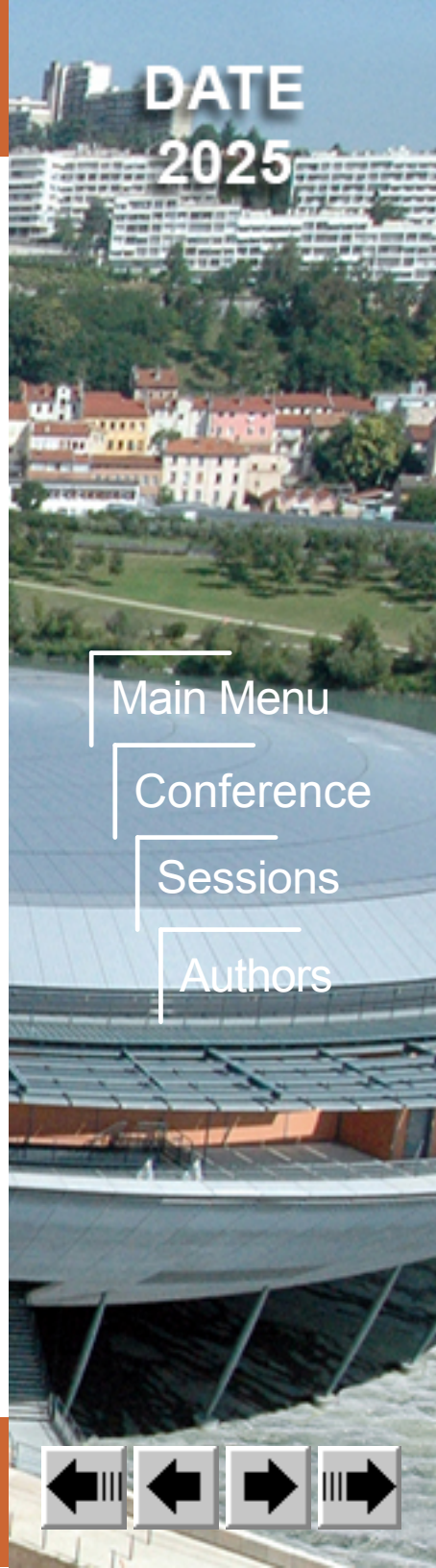
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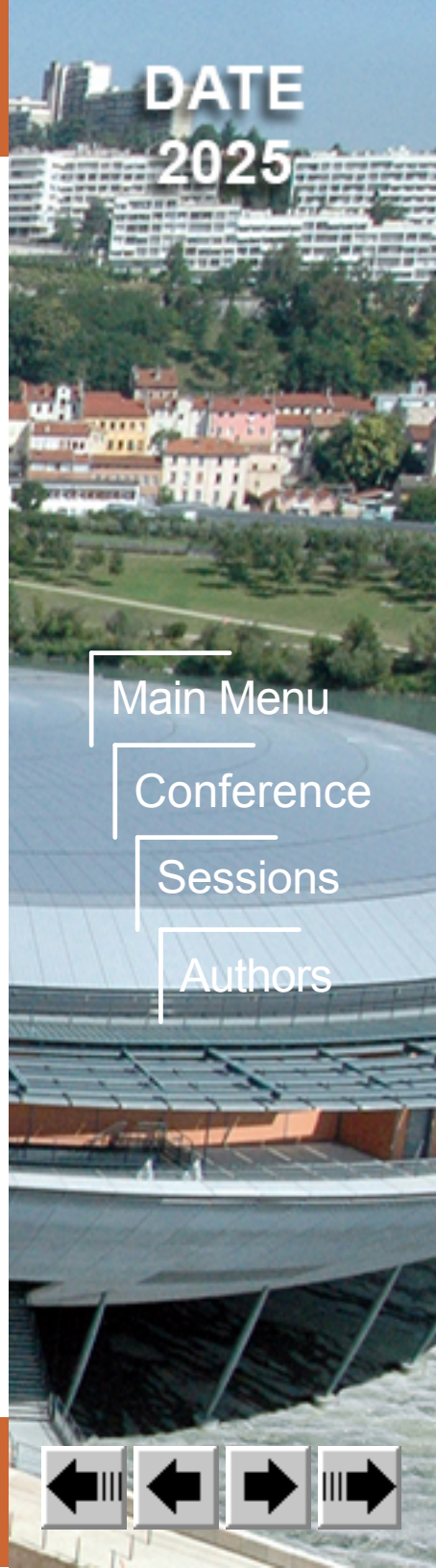
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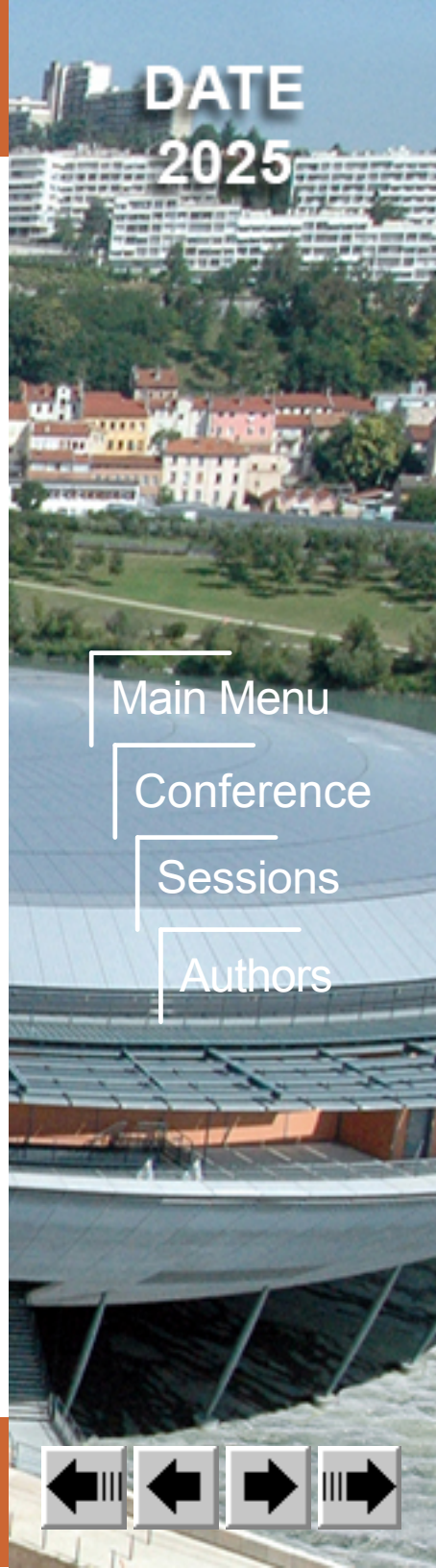
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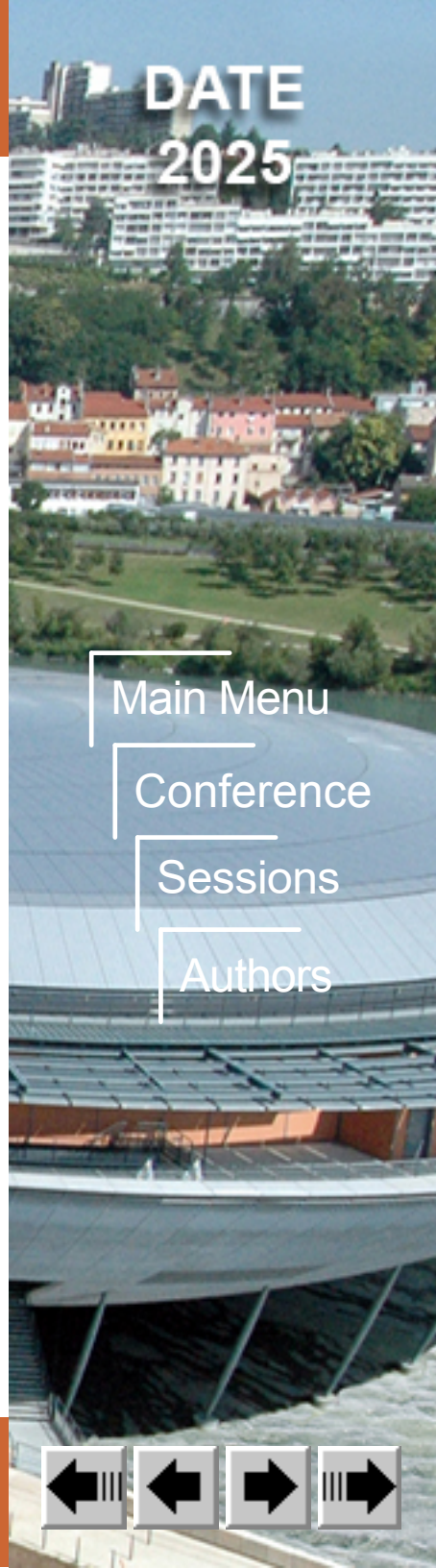
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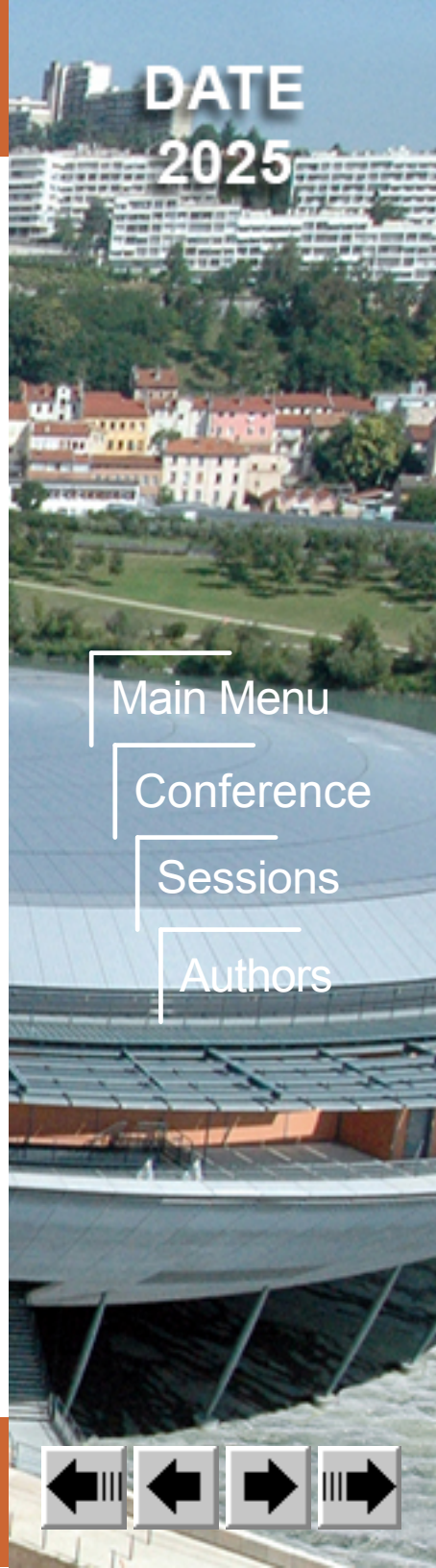
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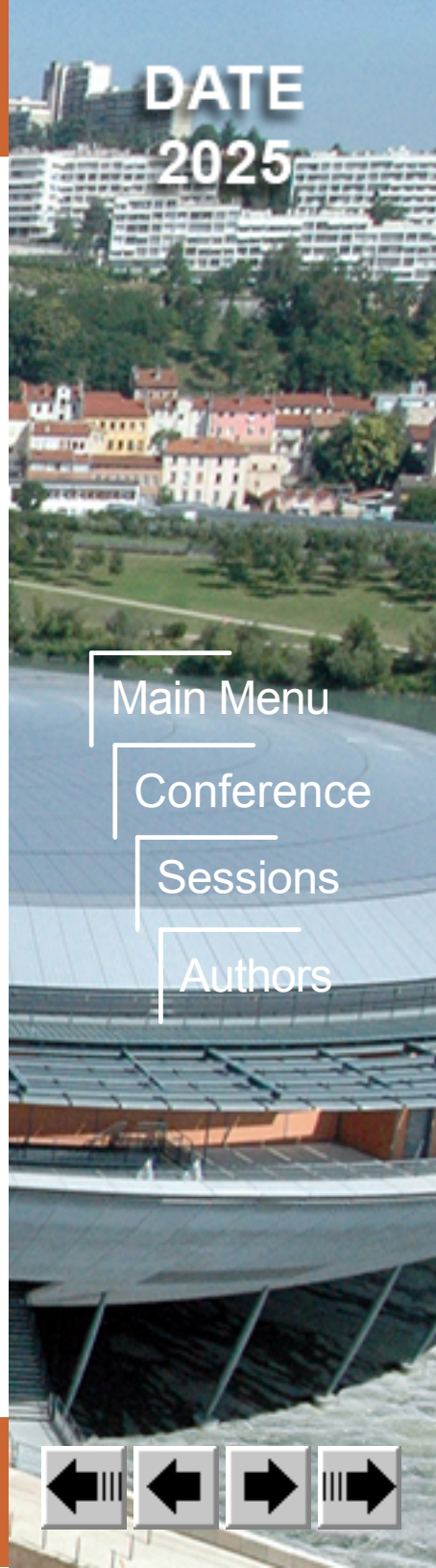
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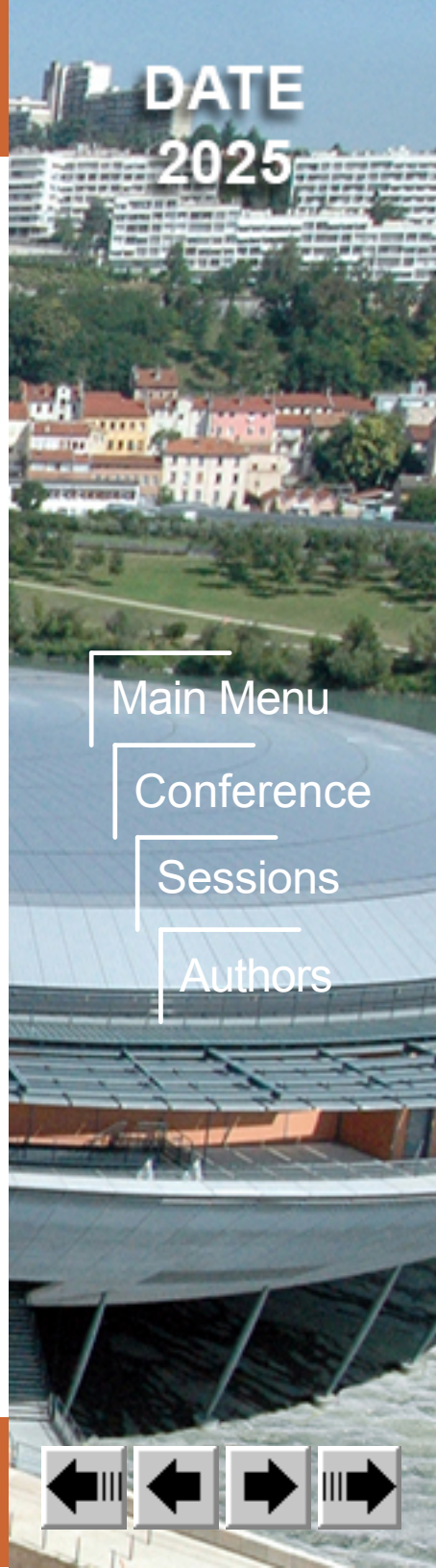
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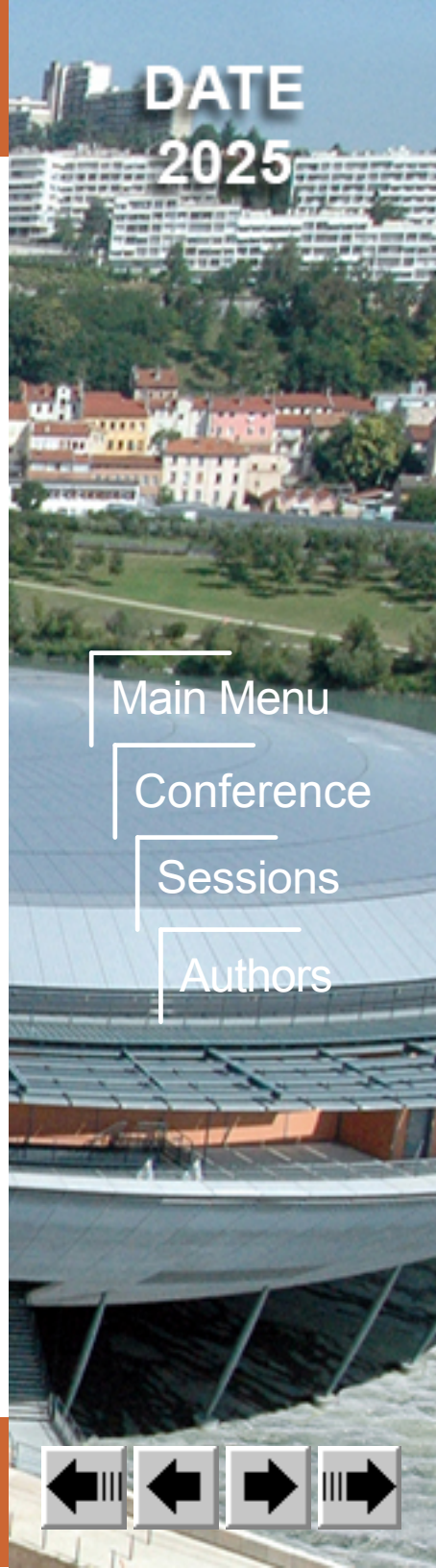
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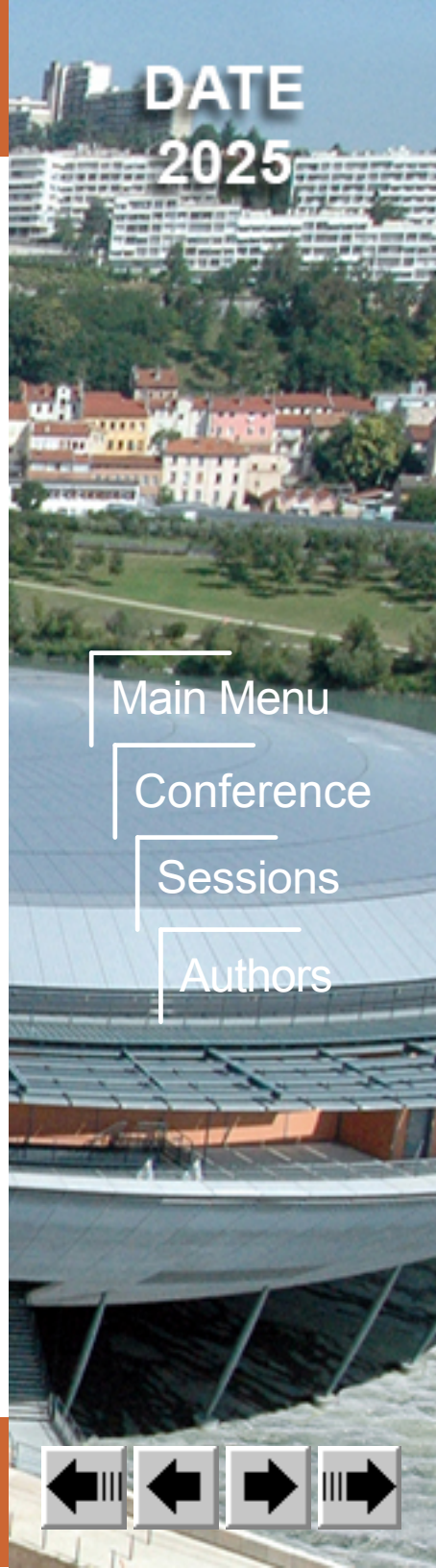
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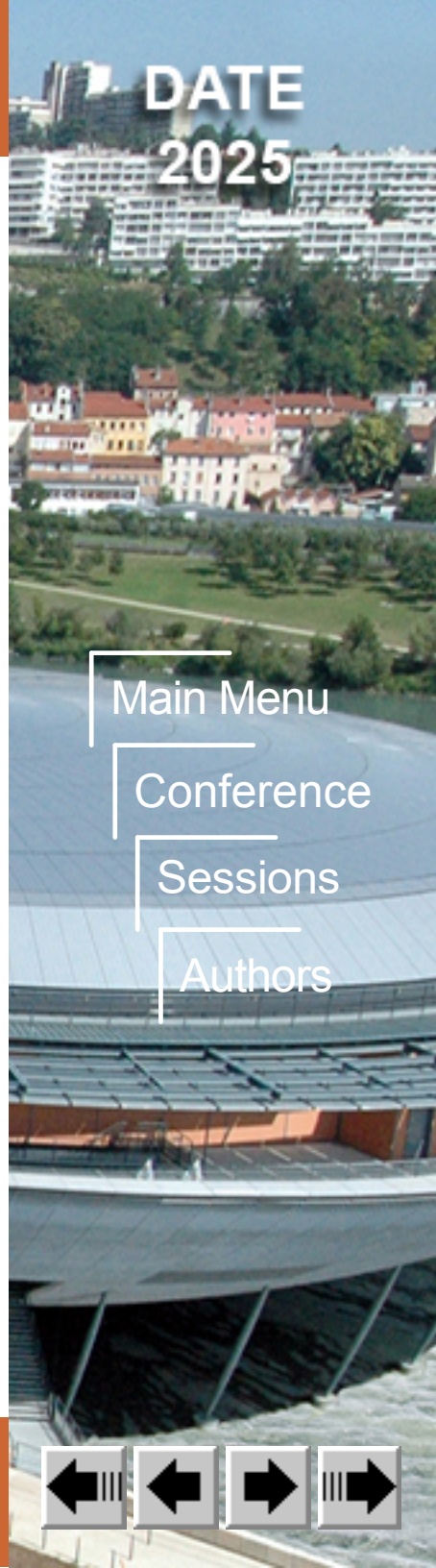
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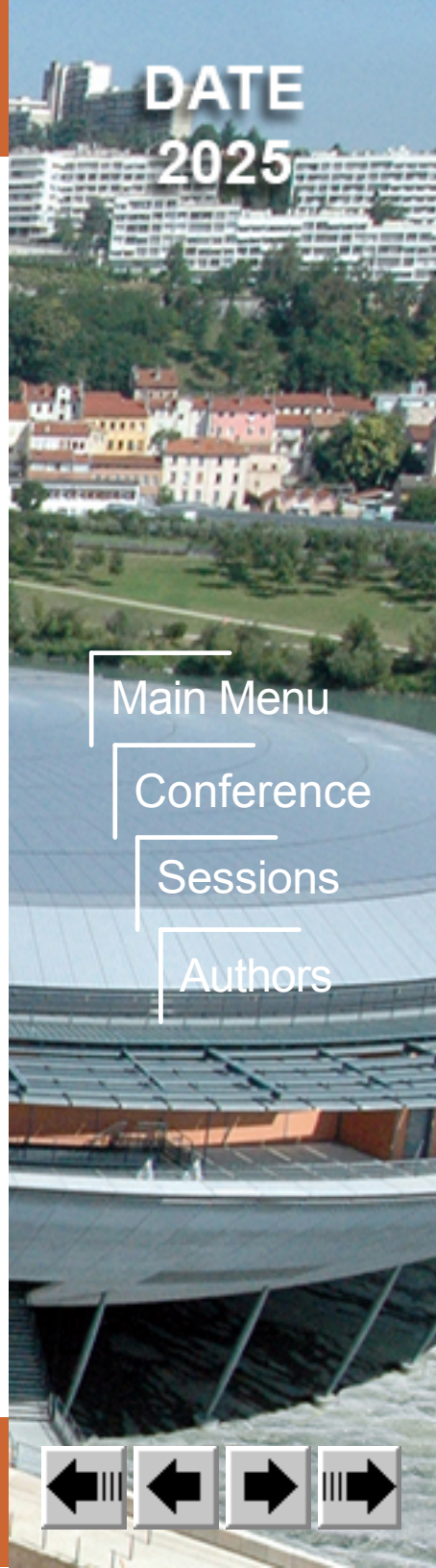
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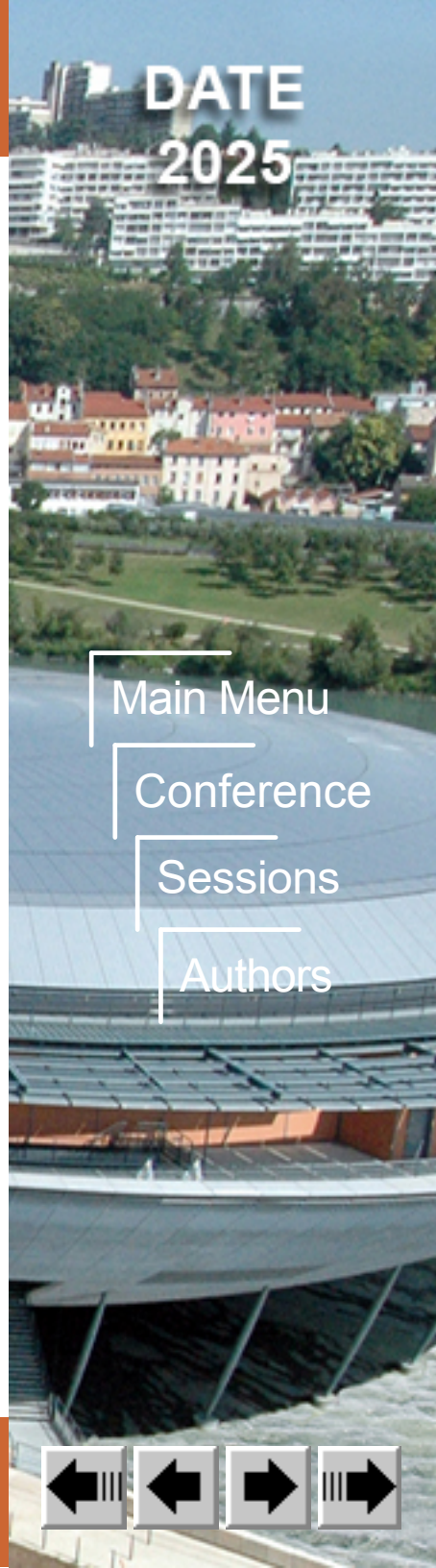
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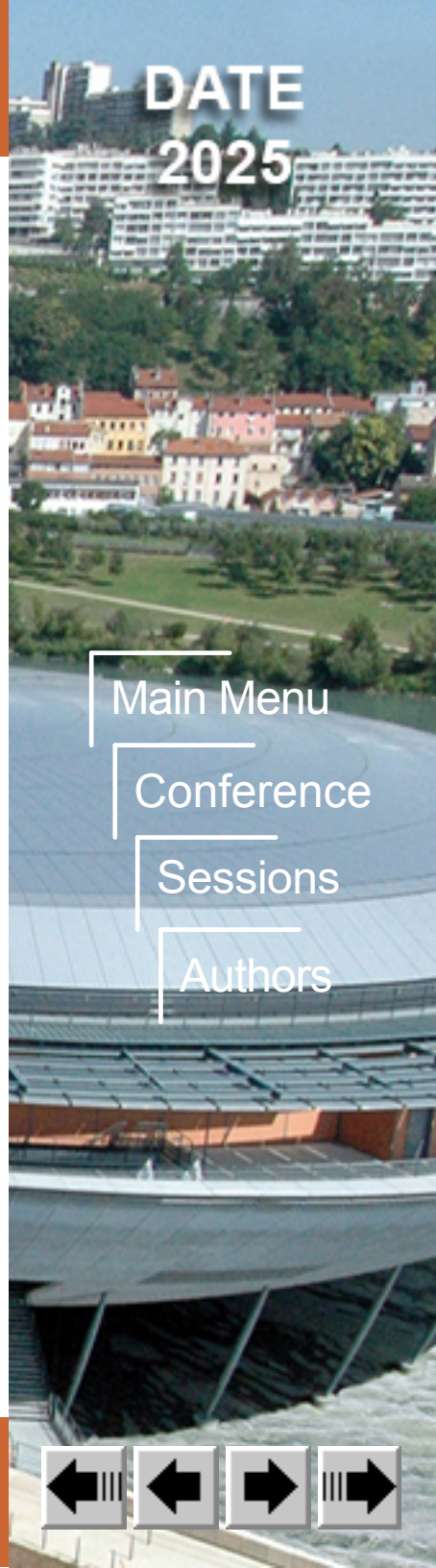
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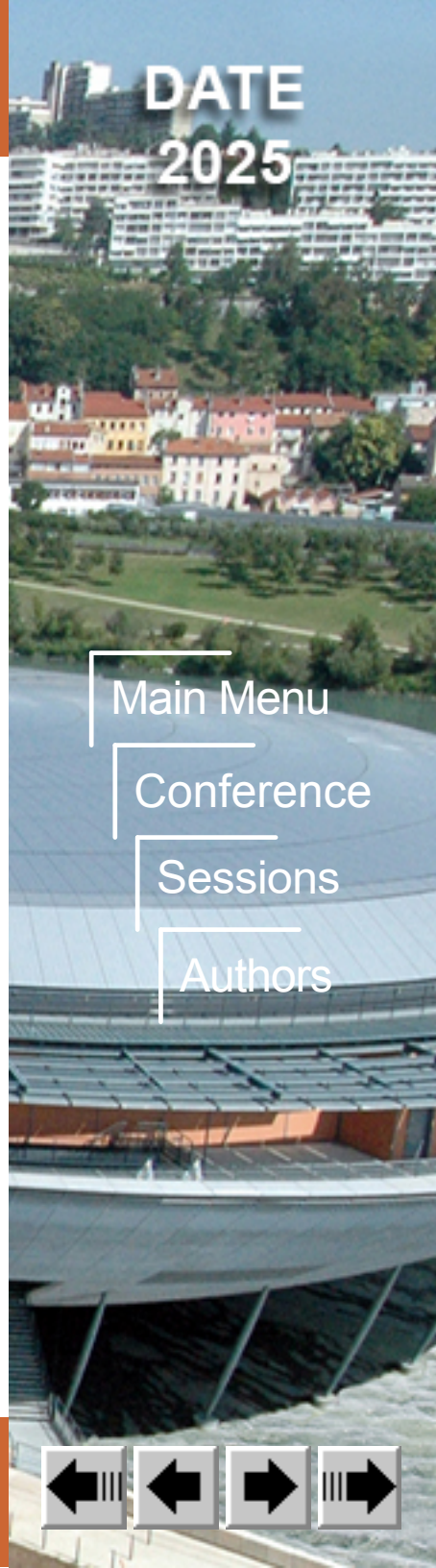
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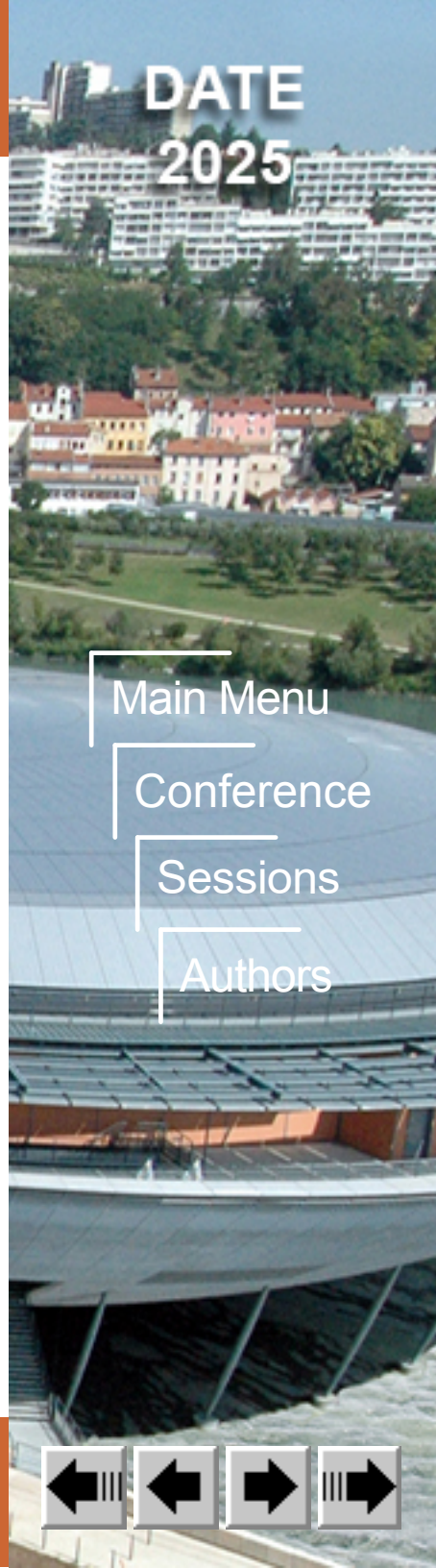
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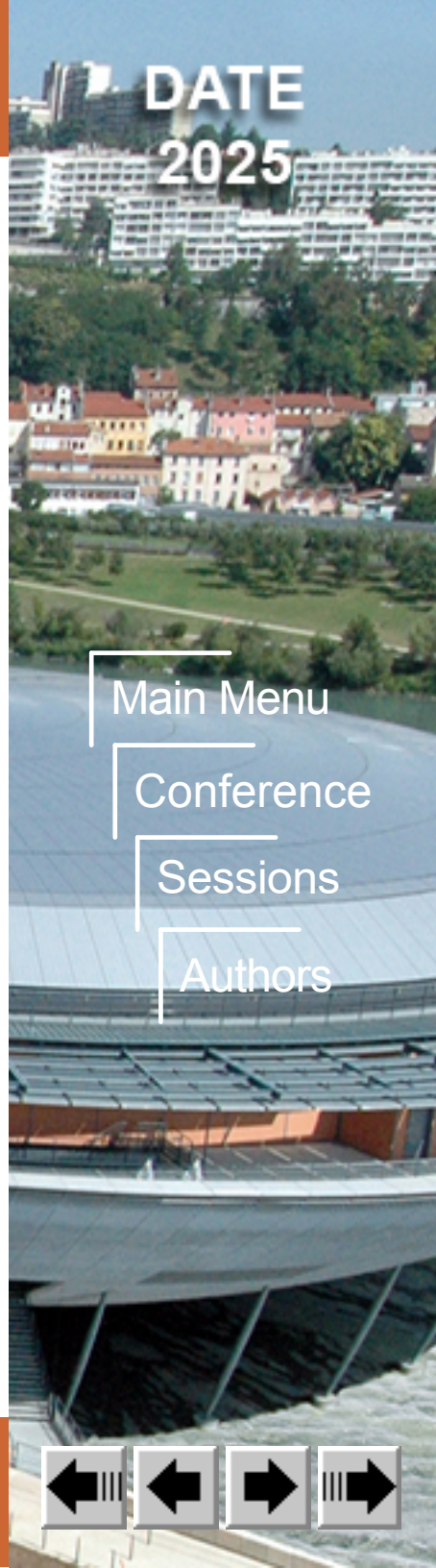
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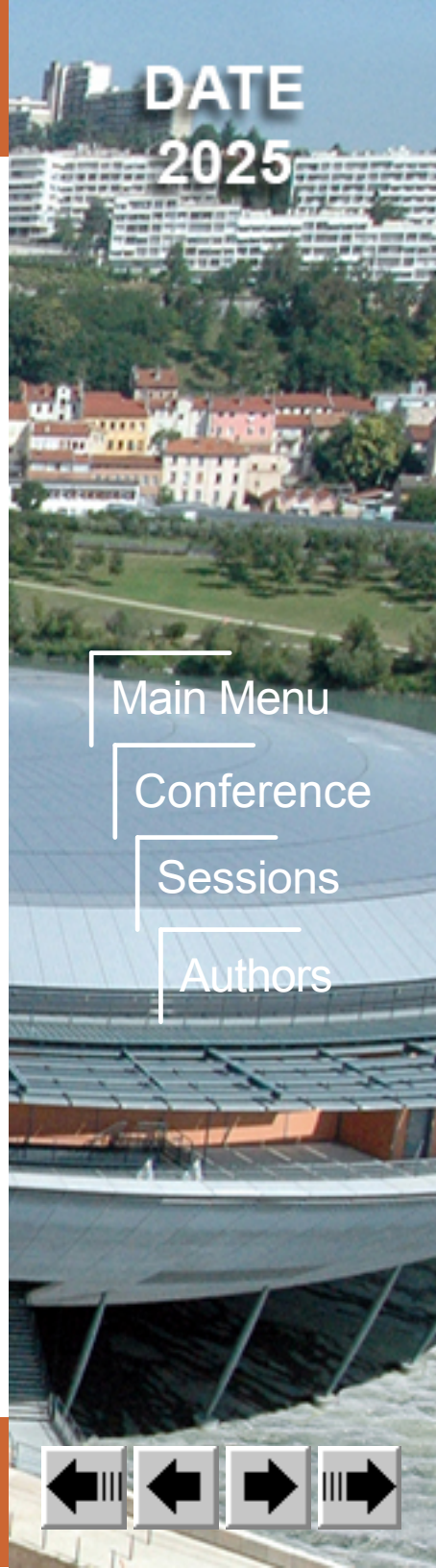
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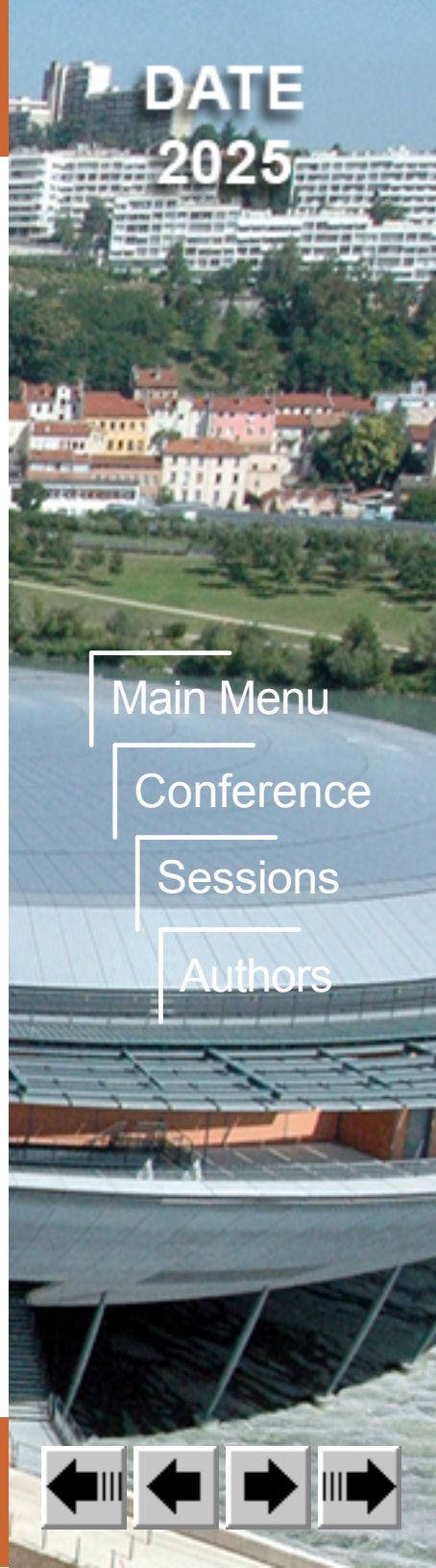
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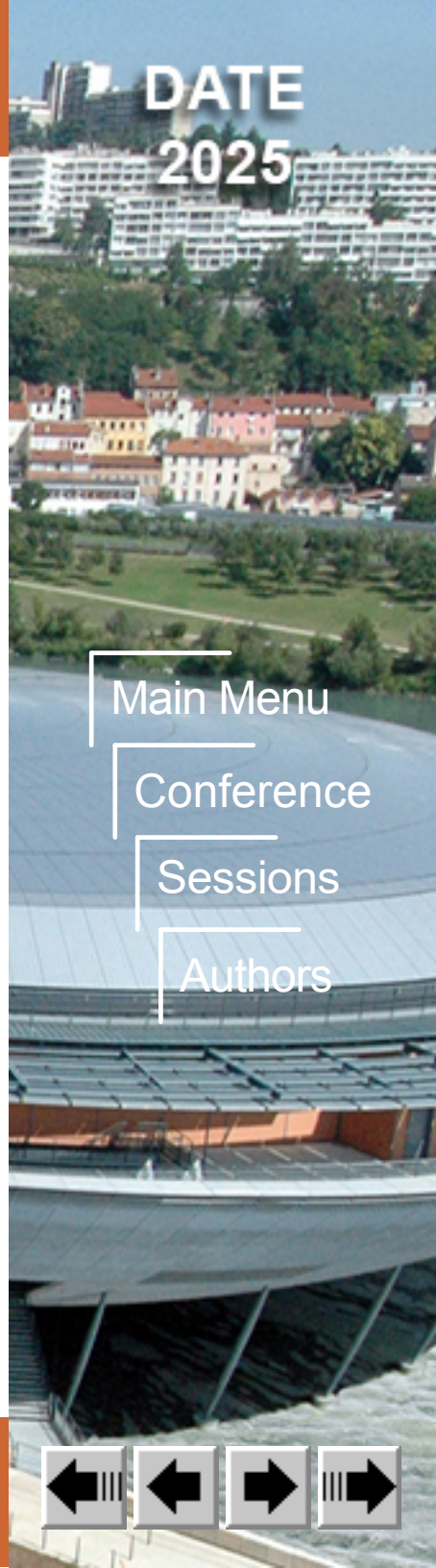
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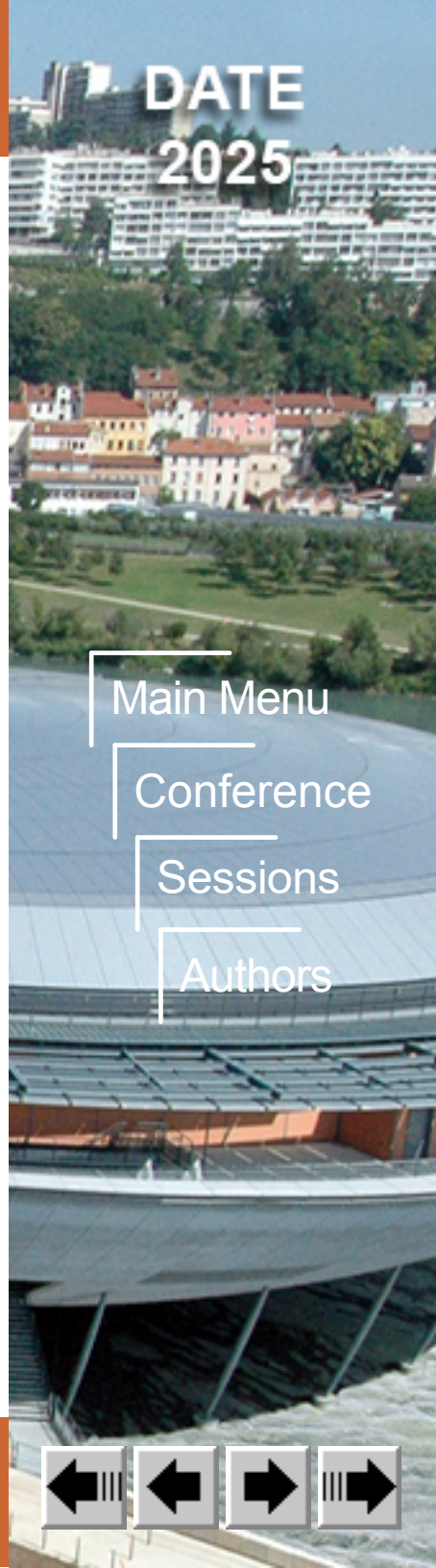
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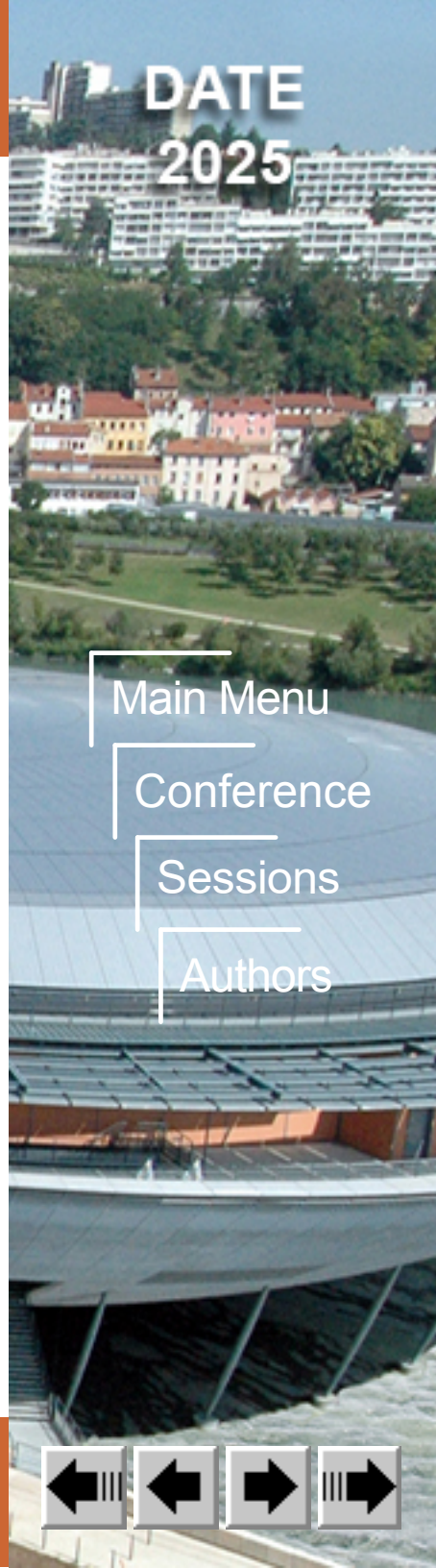
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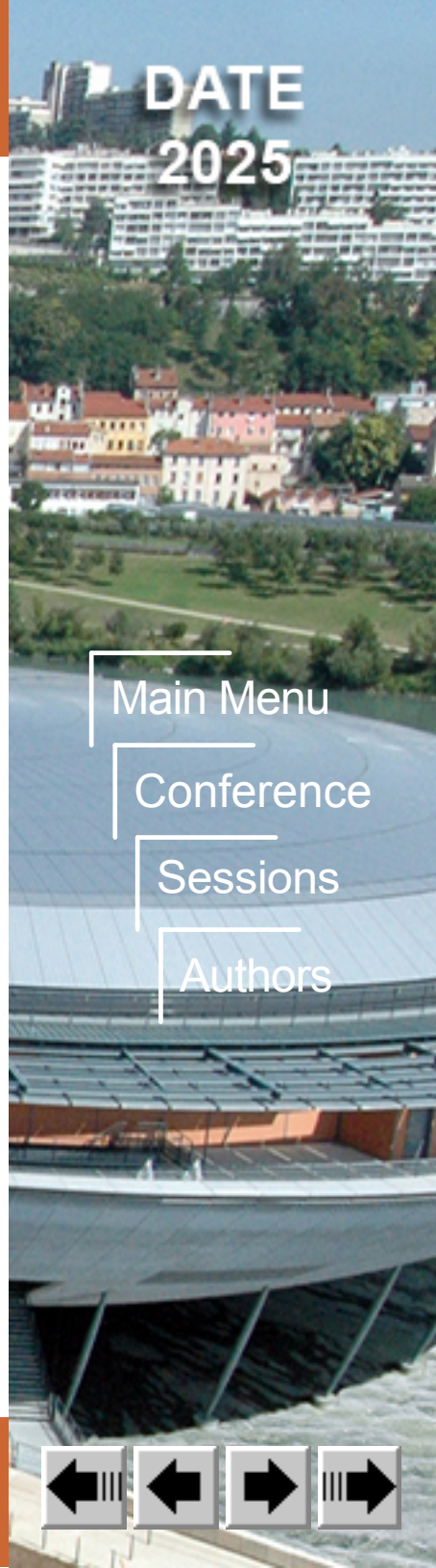
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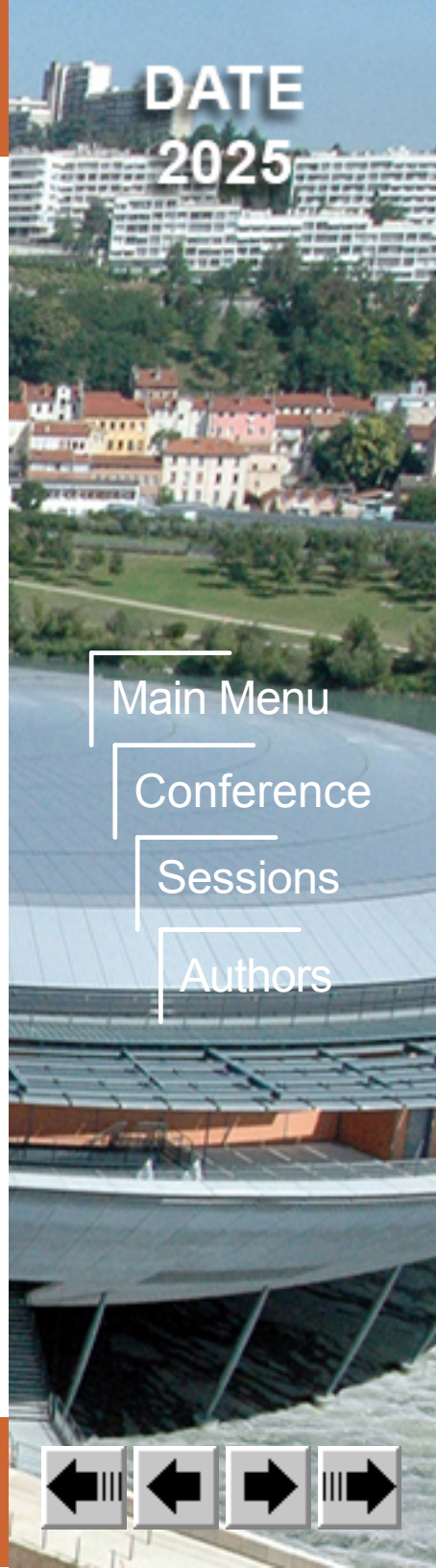
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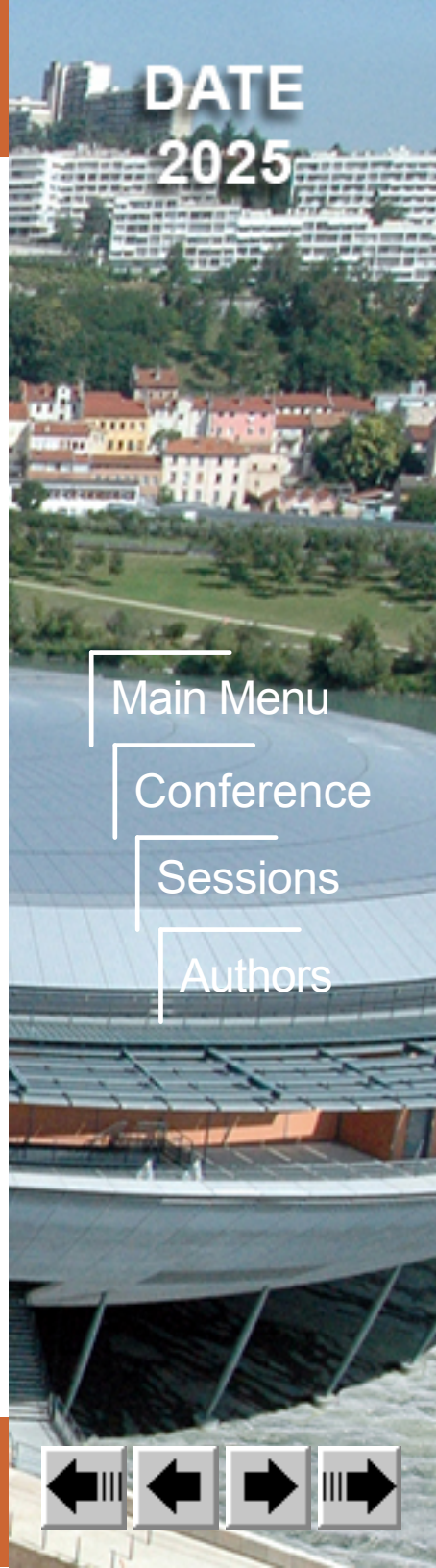
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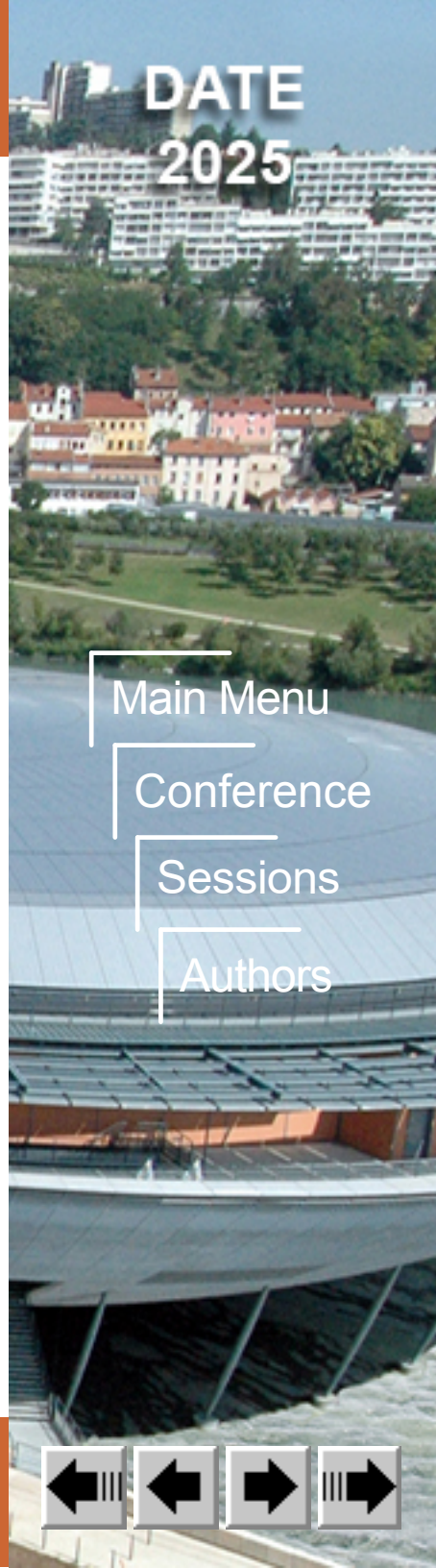
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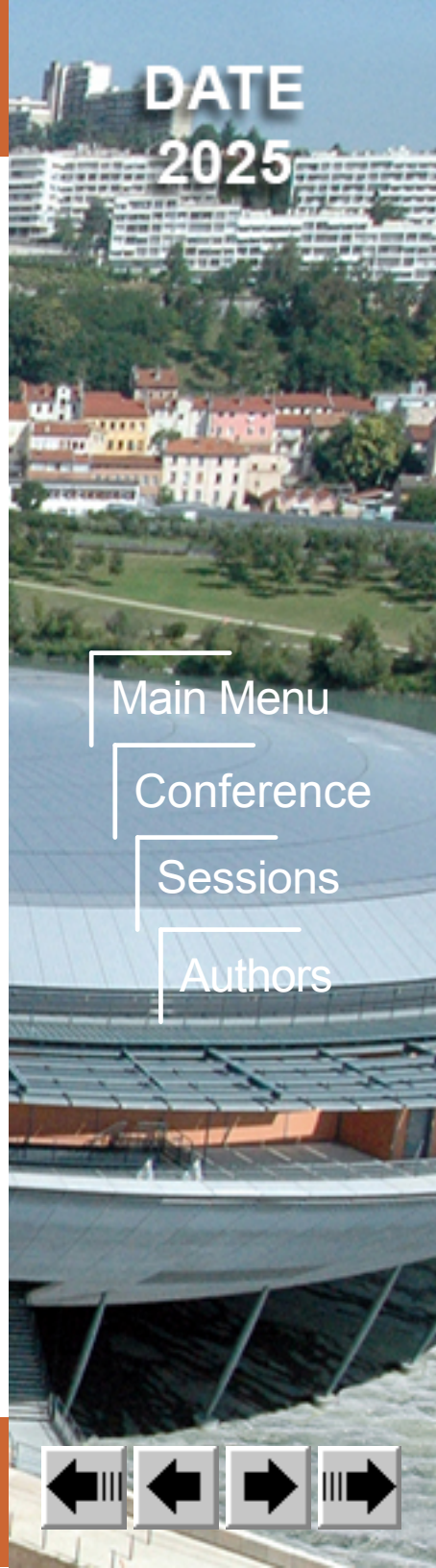
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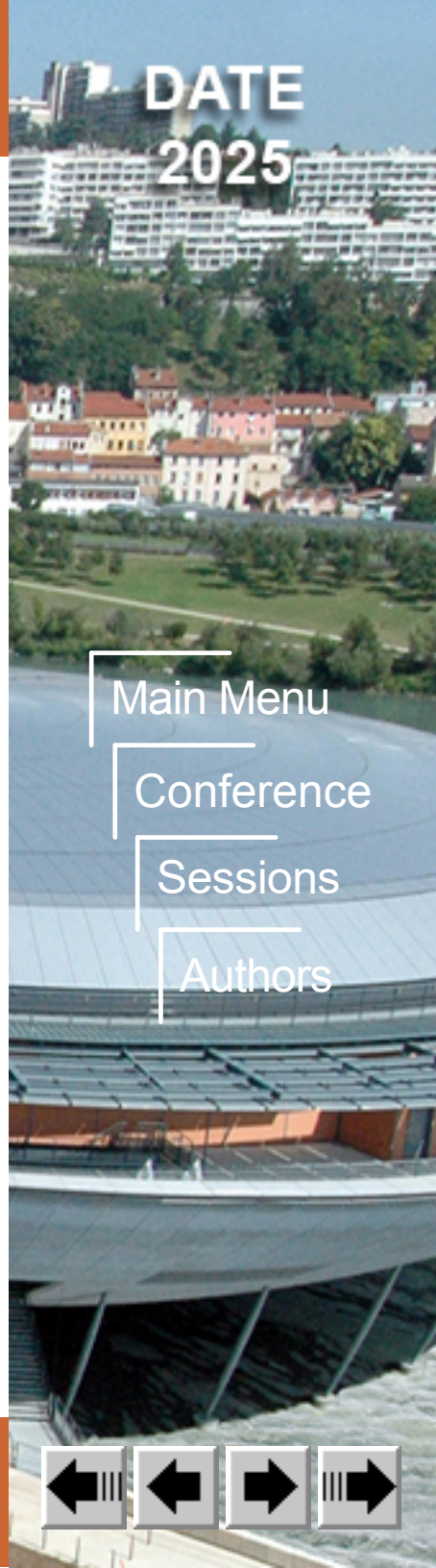
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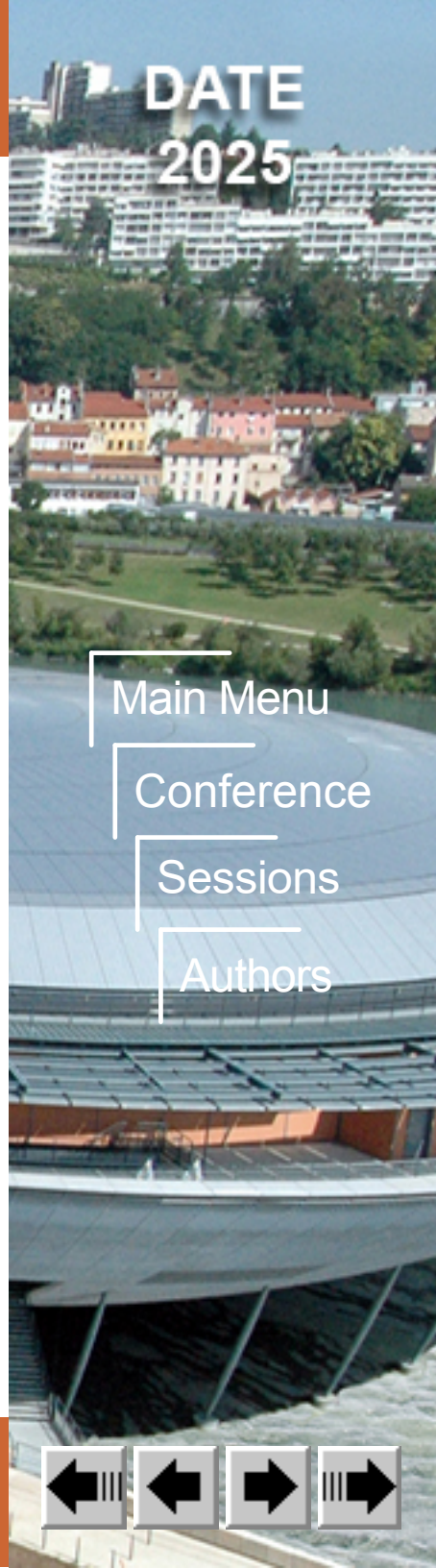
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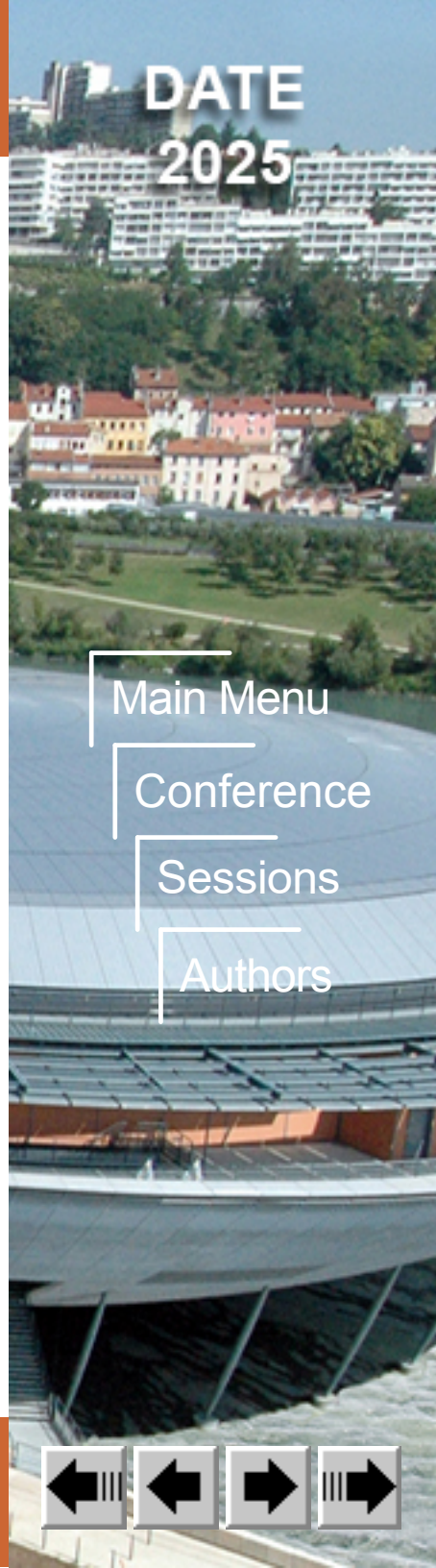
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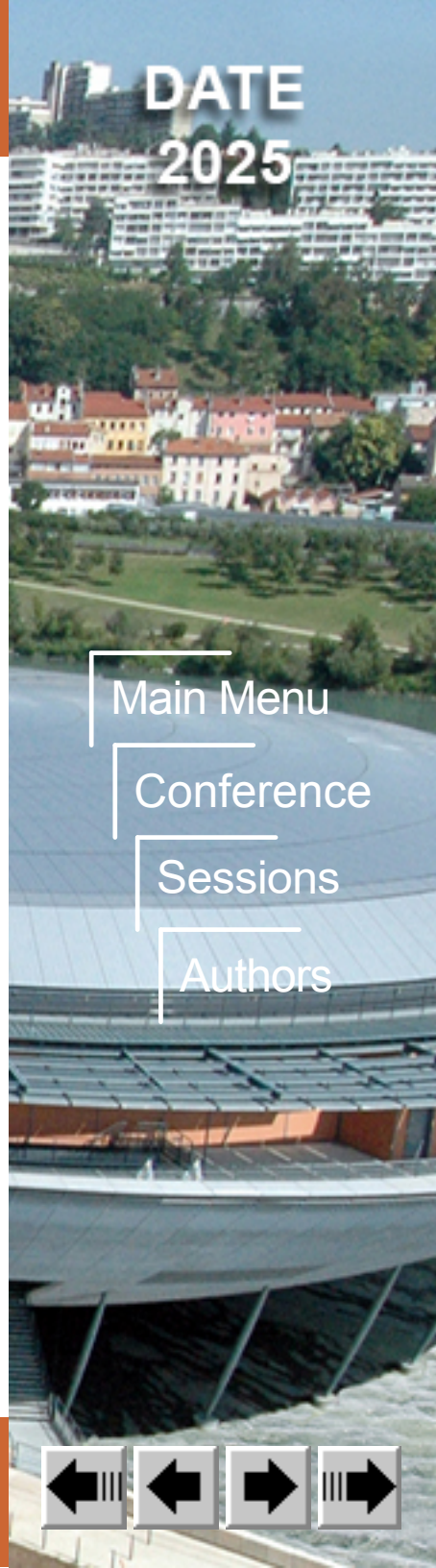
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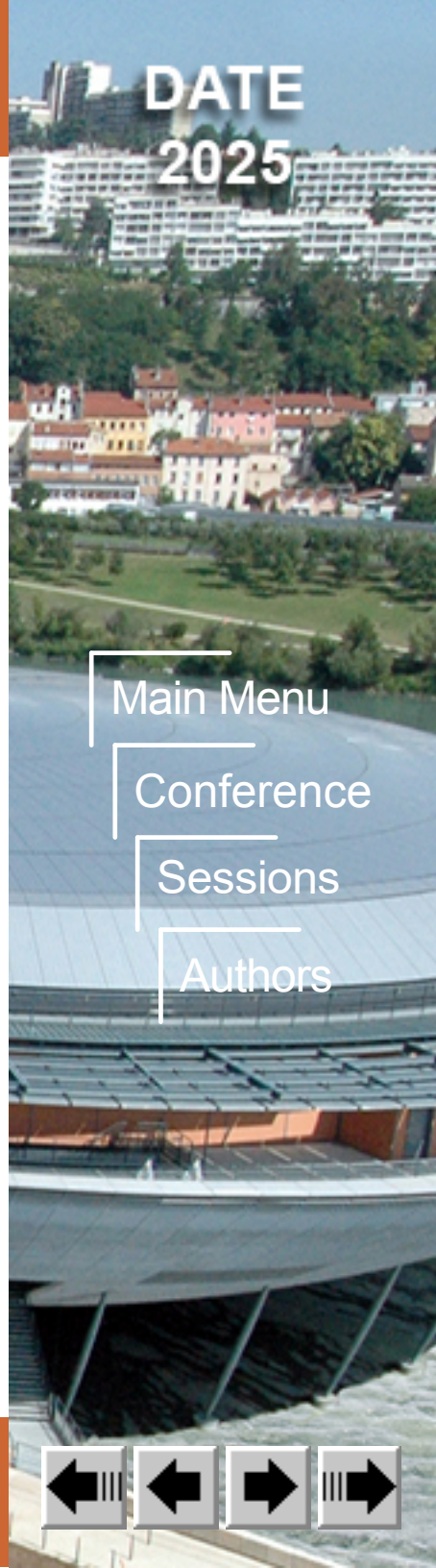
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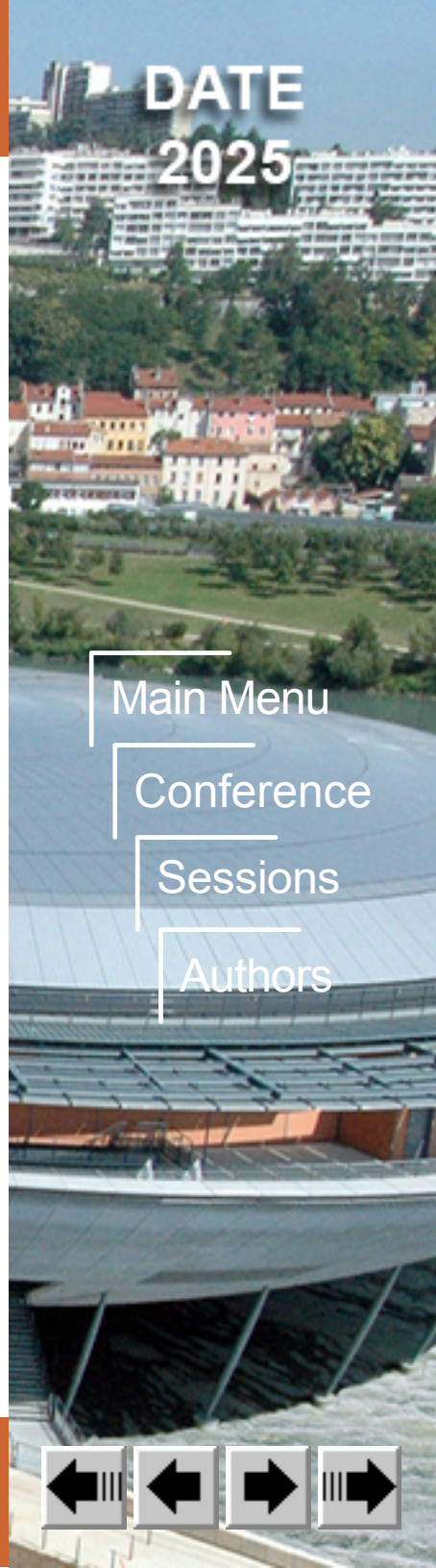
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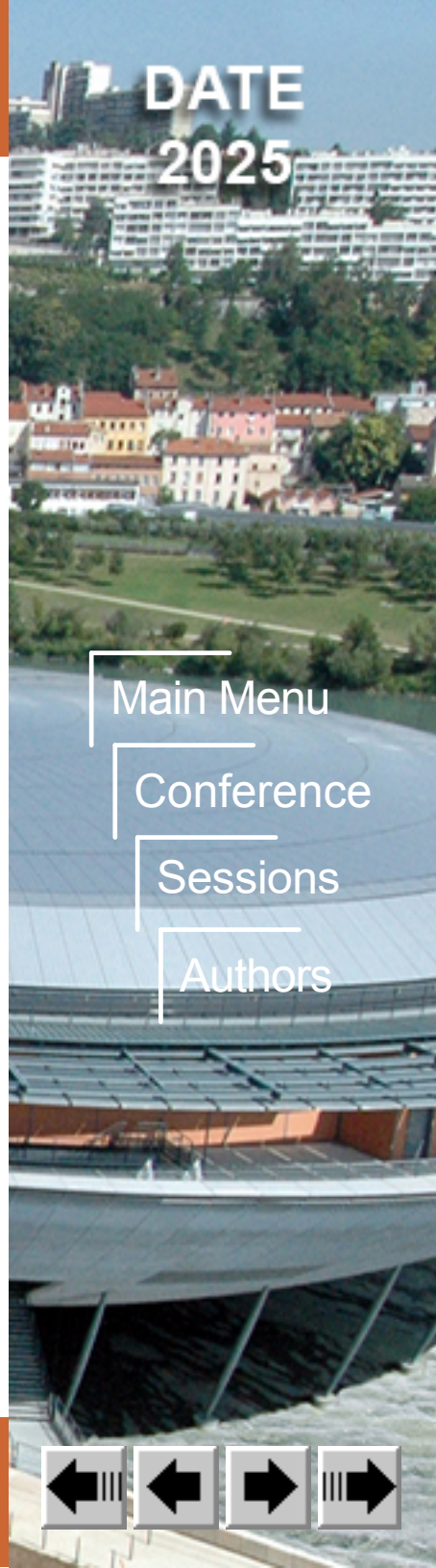
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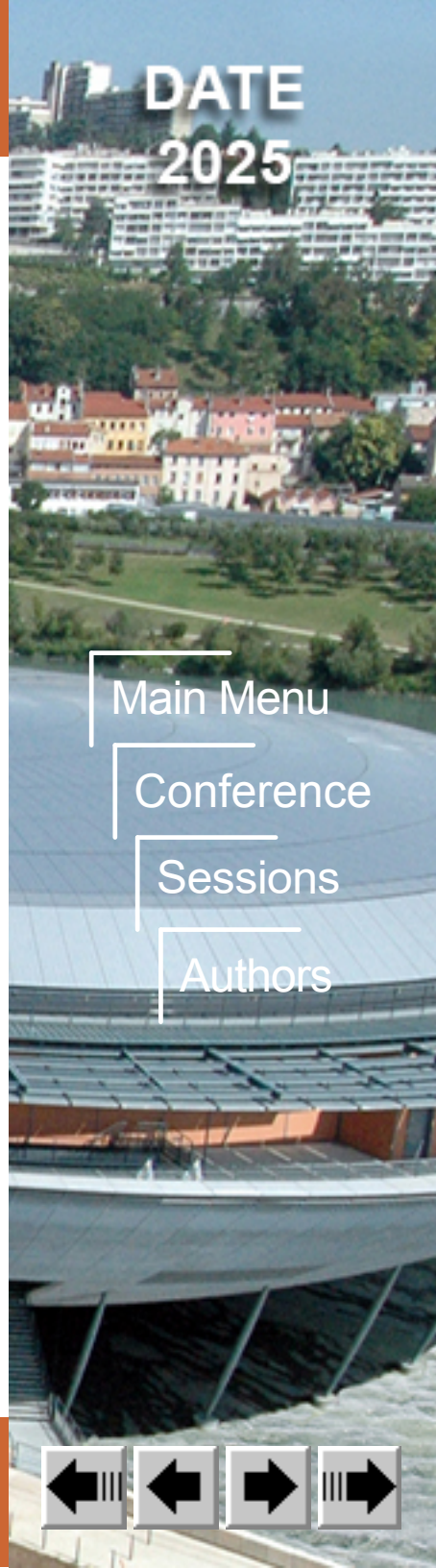
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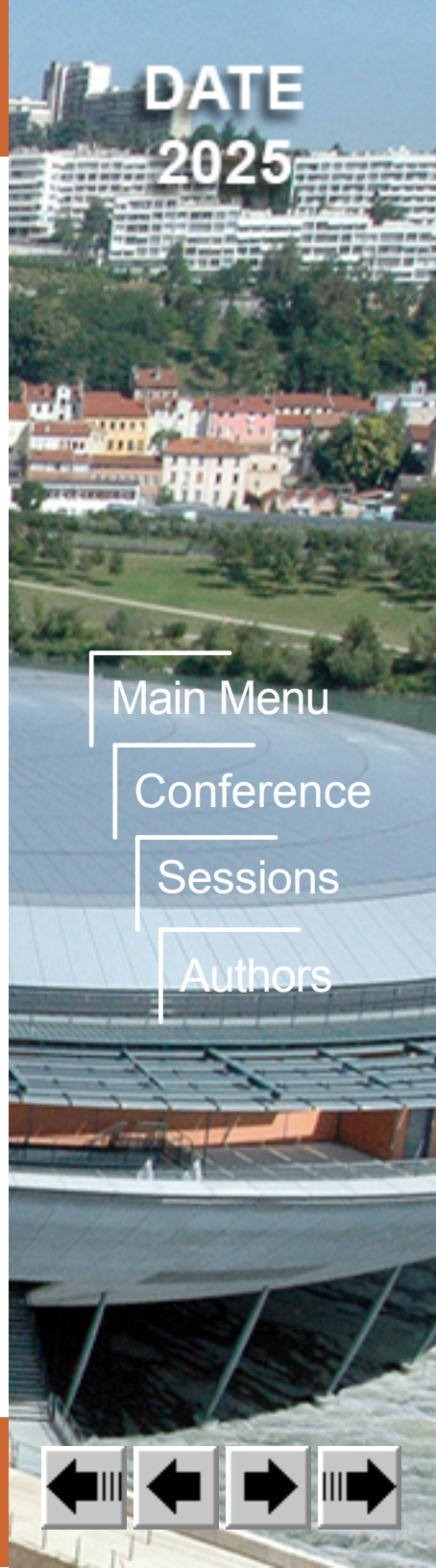
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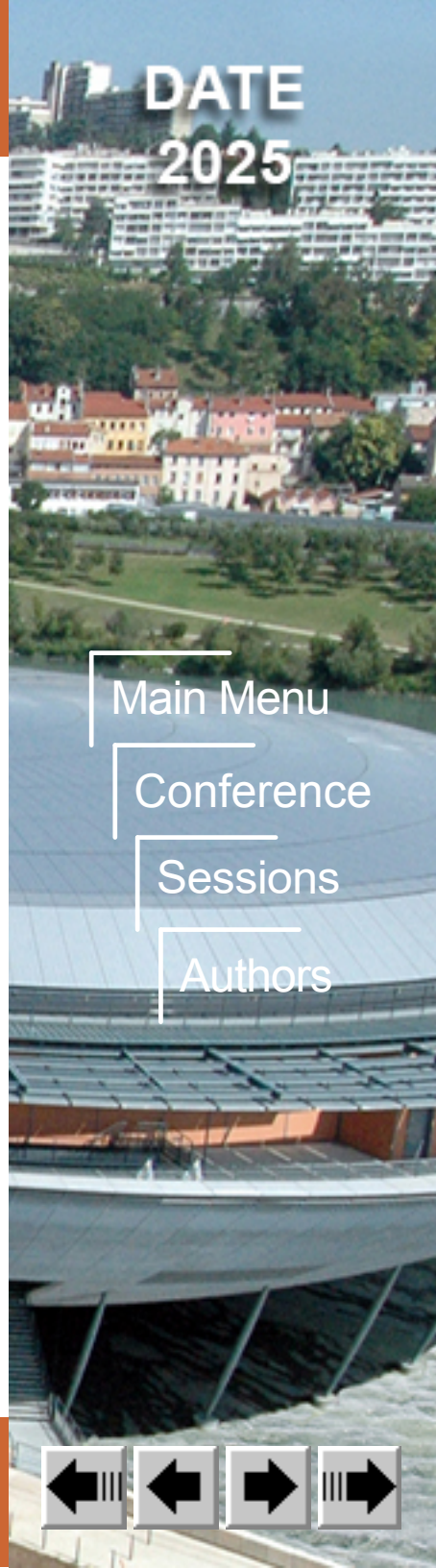
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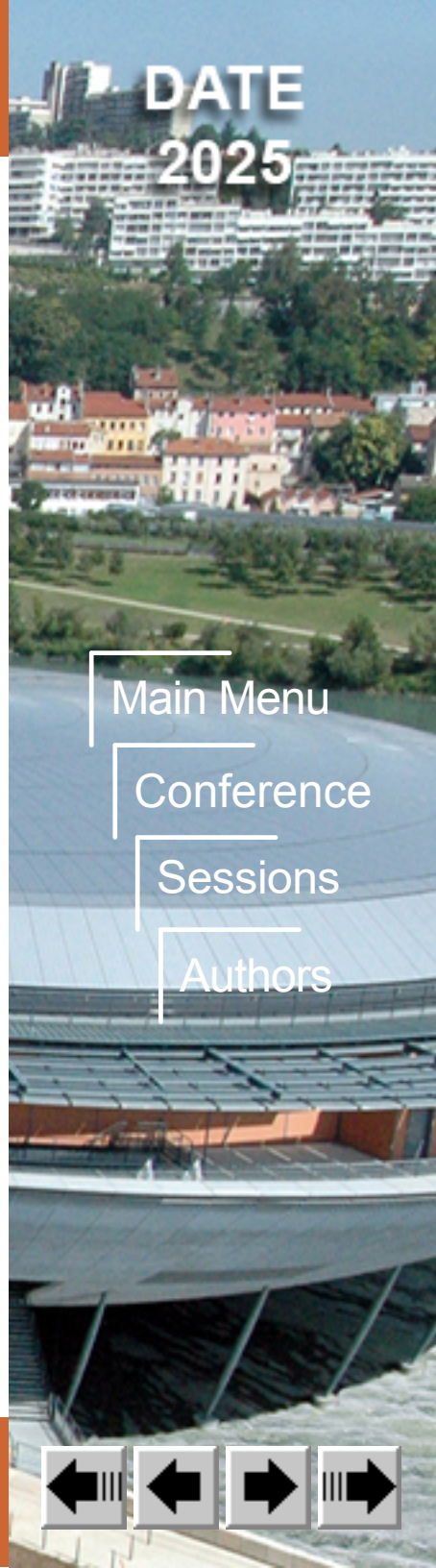
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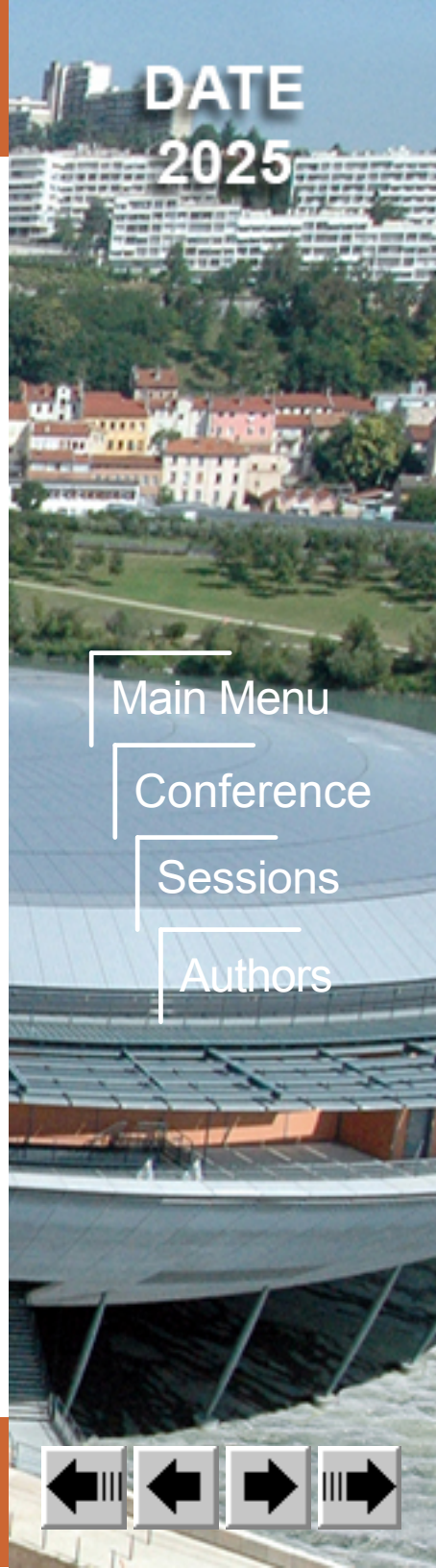
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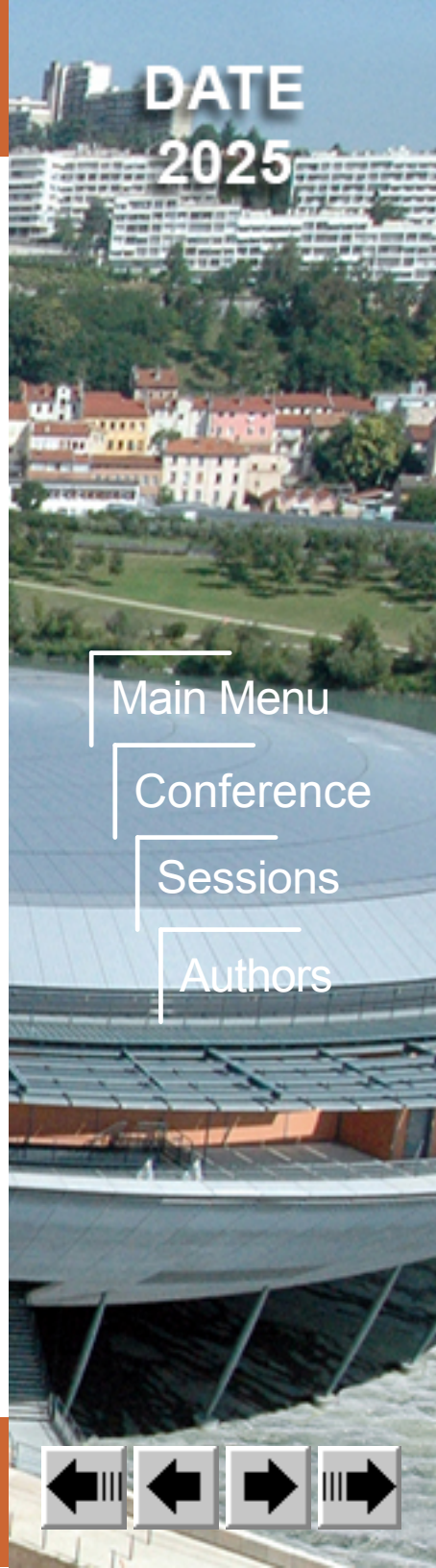
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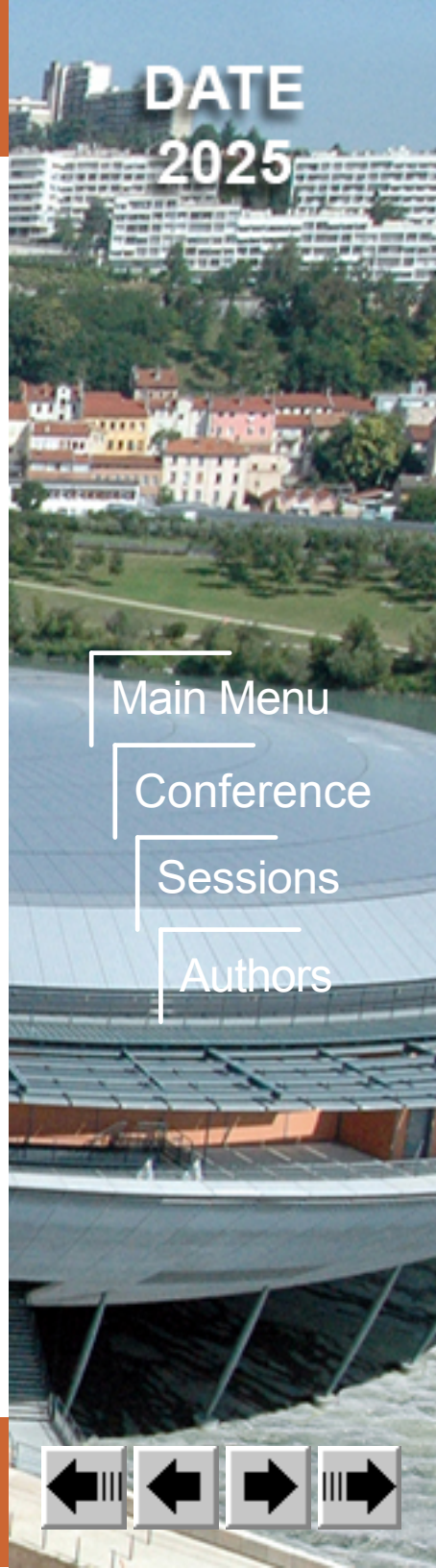
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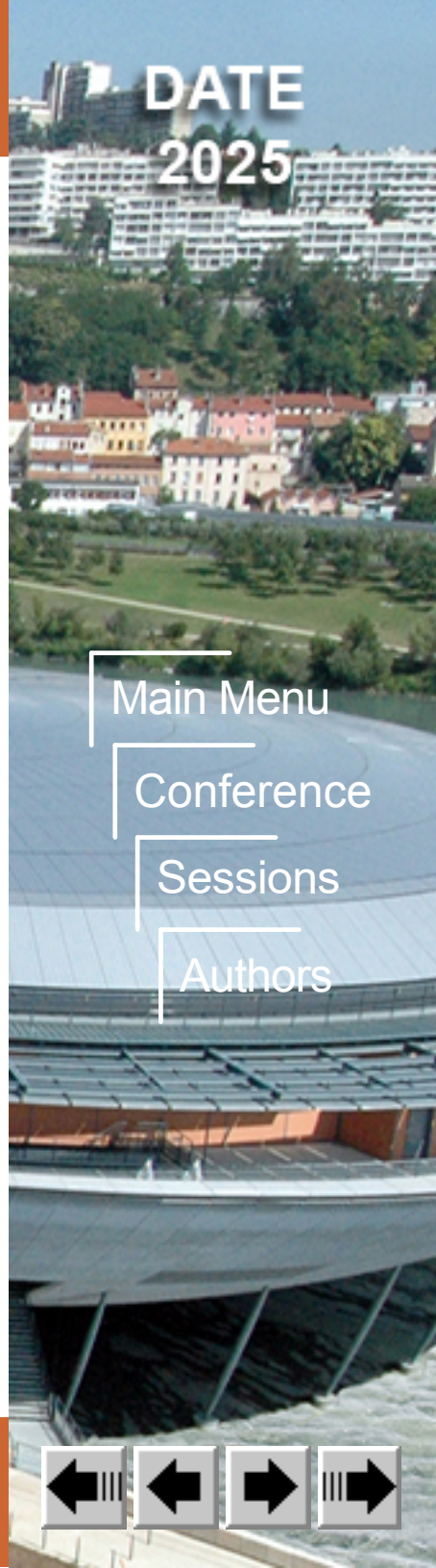
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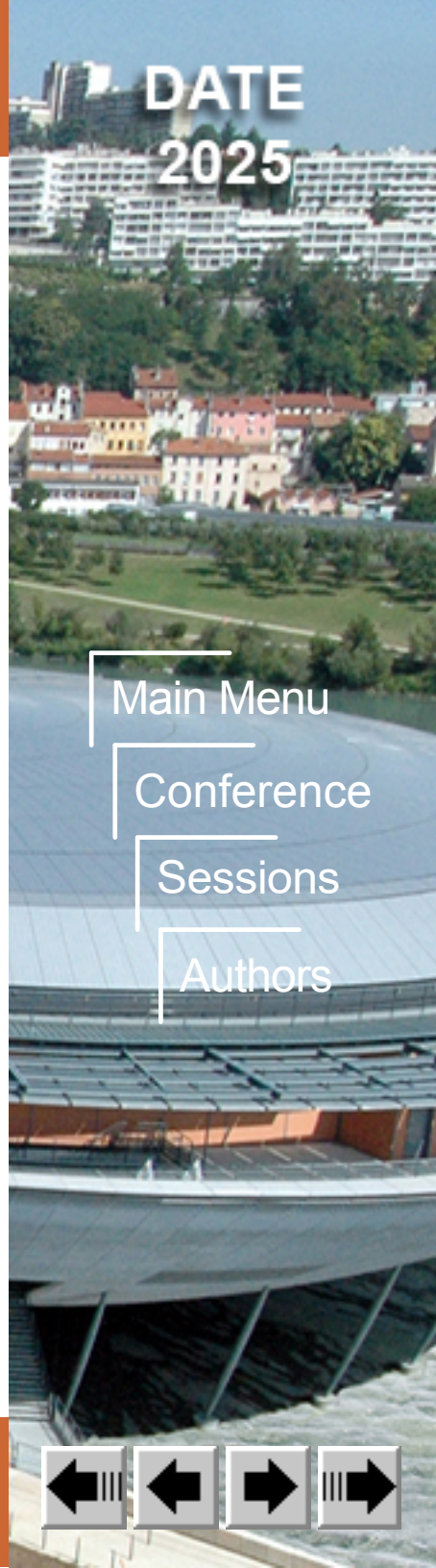
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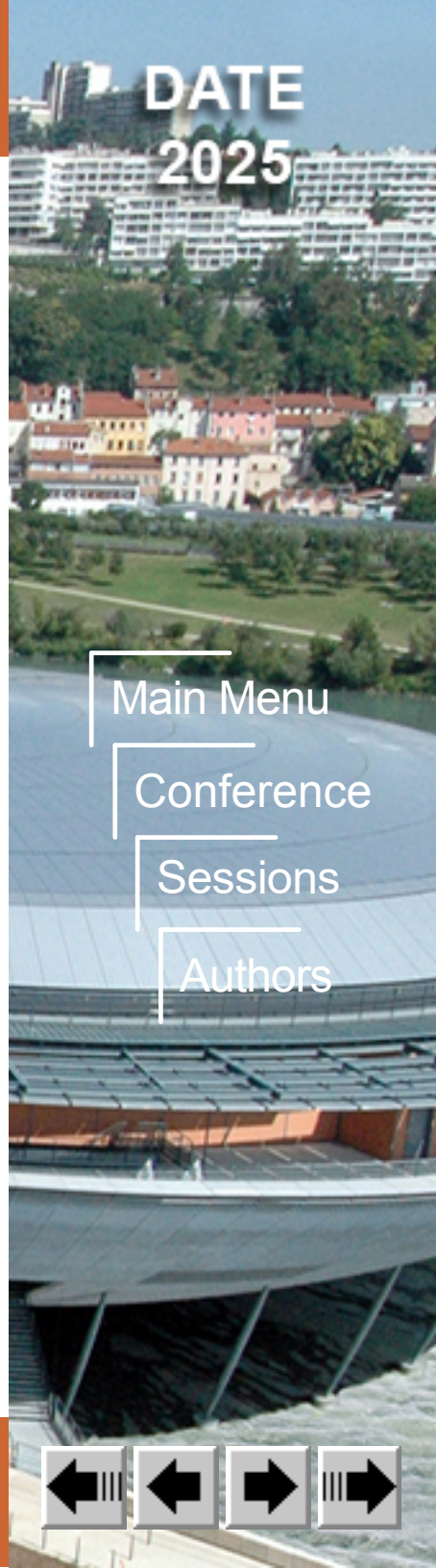
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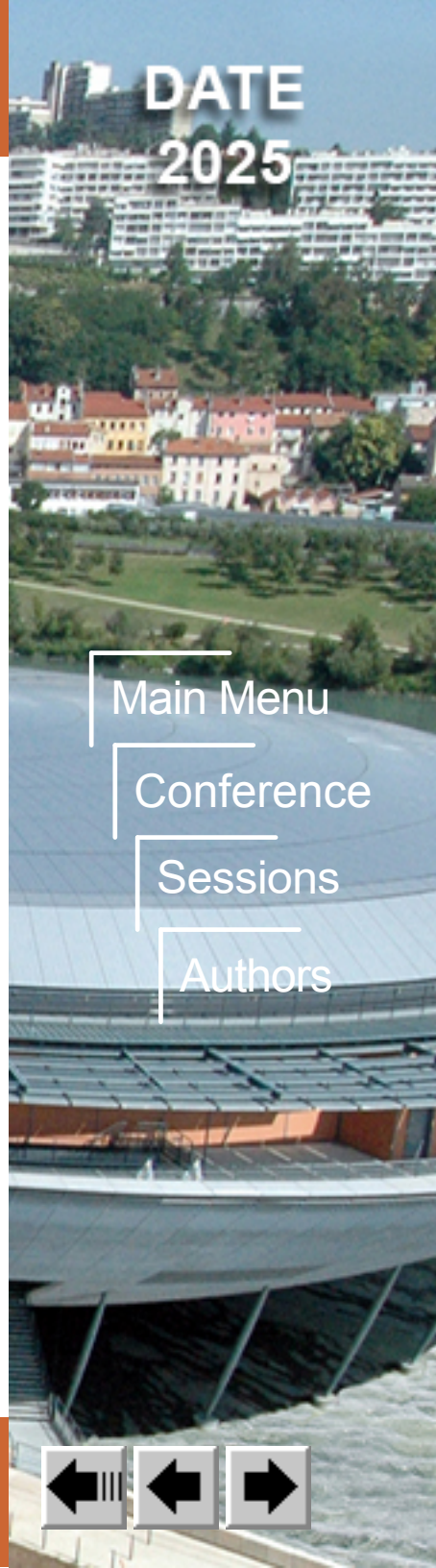
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