Printed Neuromorphic Computing for Ultra-Resource-Constrained Edge Intelligence

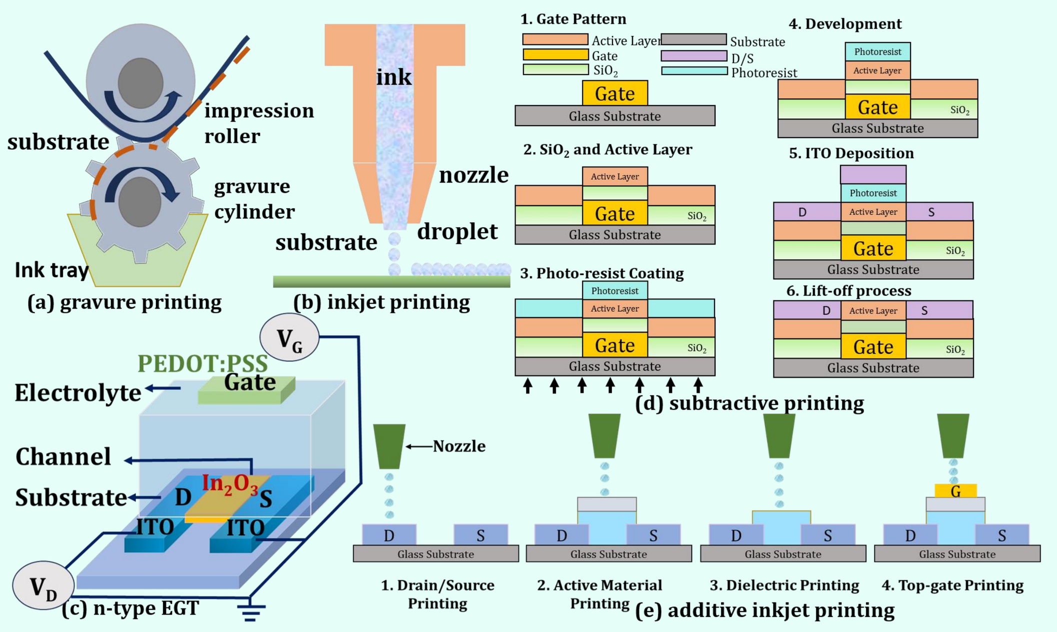
Chair of Dependable Nano Computing (CDNC)

BACKGROUND

Printed Electronics (PE)

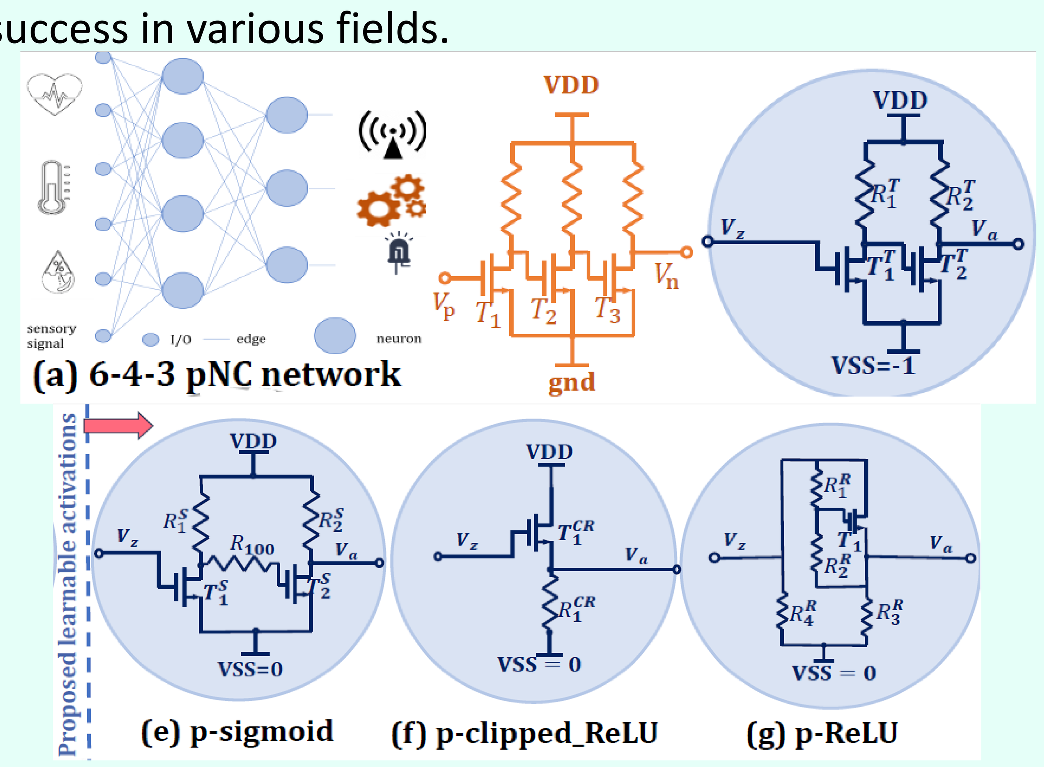
Printed Electronics has emerged as a promising alternative, using simple manufacturing techniques such as gravure-printing and jet-printing, by depositing functional inks onto flexible substrates, reducing manufacturing costs, time, and enabling features like nontoxicity, flexibility, biodegradability.

Compared to traditional silicon-based electronics, printed electronics offer unique advantages such as non-toxicity, lightweight, and flexibility. Thanks to the additive manufacturing, **highly-customized and bespoke** electronic devices can be fabricated.



Printed Neuromorphic Circuits (pNC)

Neuromorphic computing, inspired by human brain synapses, combines weighted-sum operations and non-linear activation, exhibiting strong expressiveness and success in various fields.



Printed neuromorphic circuits combine advantages of both PE and neuromorphic computing by implementing weighted-sum operations and activation functions (AFs) through crossbar and non-linear circuitry.

Crossbar weighted-sum: According to Kirchhoff's and Ohm's law, the output voltage of a crossbar can be expressed as a weighted-sum of the input:

$$V_z = \frac{g_1}{G}V_1 + \frac{g_2}{G}V_2 + \frac{g_3}{G}V_3 + \frac{g_b}{G}V_b$$

where $g_i = \frac{1}{R_i}$, G is the sum of g_i, $V_b \equiv 1V$.

Negative weight circuit: The weights in the crossbar rely on conductance, which cannot be negative. To emulate negative weights, a negative weight circuit is introduced,

$$(-w_i)\cdot V_i = w_i \cdot (-V_i) \leftarrow w_i \cdot \mathrm{neg}(V_i)$$

with $\mathrm{neg}(V_{\mathrm{in}}) = -\left(\eta_1^{\mathrm{N}} + \eta_2^{\mathrm{N}} \cdot \tanh\left((V_z - \eta_3^{\mathrm{N}}) \cdot \eta_4^{\mathrm{N}}\right)\right)$, where $\boldsymbol{\eta}^{\mathrm{N}} = [\eta_1^{\mathrm{N}}, \eta_2^{\mathrm{N}}, \eta_3^{\mathrm{N}}, \eta_4^{\mathrm{N}}]$ is the auxiliary parameter determined by physical quantities $\boldsymbol{q}^{\mathrm{N}} = [R_1^{\mathrm{N}}, R_2^{\mathrm{N}}, R_3^{\mathrm{N}}, R_4^{\mathrm{N}}, R_5^{\mathrm{N}}, T^{\mathrm{N}}]$.

E.g. AFs: Tanh-like circuit: The characteristic curve can be described by a modified tanh function:

$$V_a = \eta_1^{\mathrm{A}} + \eta_2^{\mathrm{A}} \cdot \tanh\left((V_z - \eta_3^{\mathrm{A}}) \cdot \eta_4^{\mathrm{A}}\right)$$

where $\boldsymbol{\eta}^{\mathrm{A}} = [\eta_1^{\mathrm{A}}, \eta_2^{\mathrm{A}}, \eta_3^{\mathrm{A}}, \eta_4^{\mathrm{A}}]$ is the auxiliary parameter determined by physical quantities $\boldsymbol{q}^{\mathrm{A}} = [R_1^{\mathrm{A}}, R_2^{\mathrm{A}}, T_1^{\mathrm{A}}, T_2^{\mathrm{A}}]$.

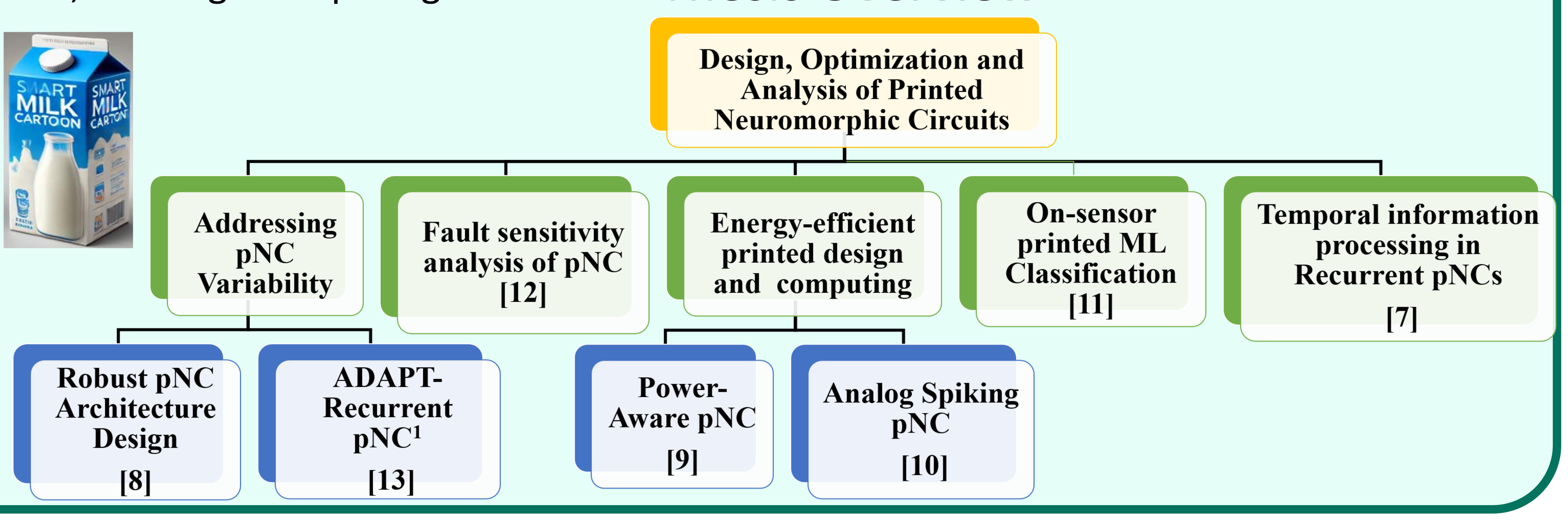
MOTIVATION

Problem Statement:

Addressing the inherent challenges of variability, fault tolerance, and energy limitations in printed electronics requires robust design strategies to ensure reliability and performance.

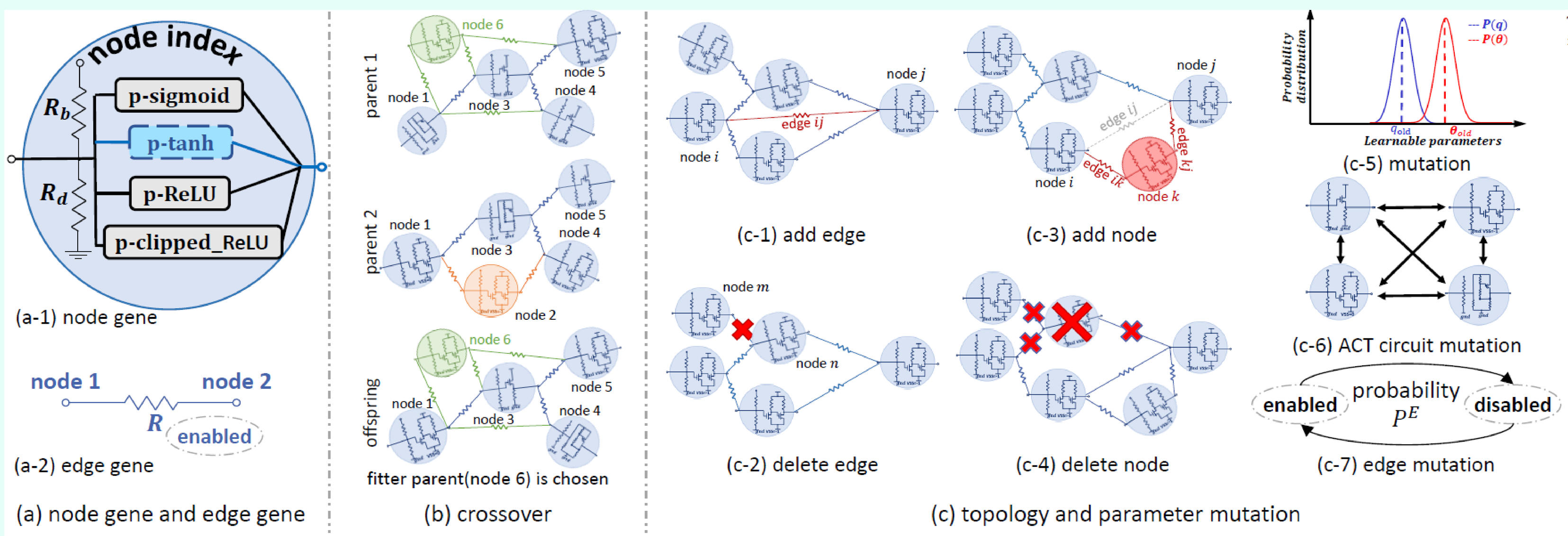
The main aim of this dissertation is to design and optimize printed neuromorphic circuits (pNCs) for robust, energy efficient, and scalable applications in IoT, wearables, and edge computing.

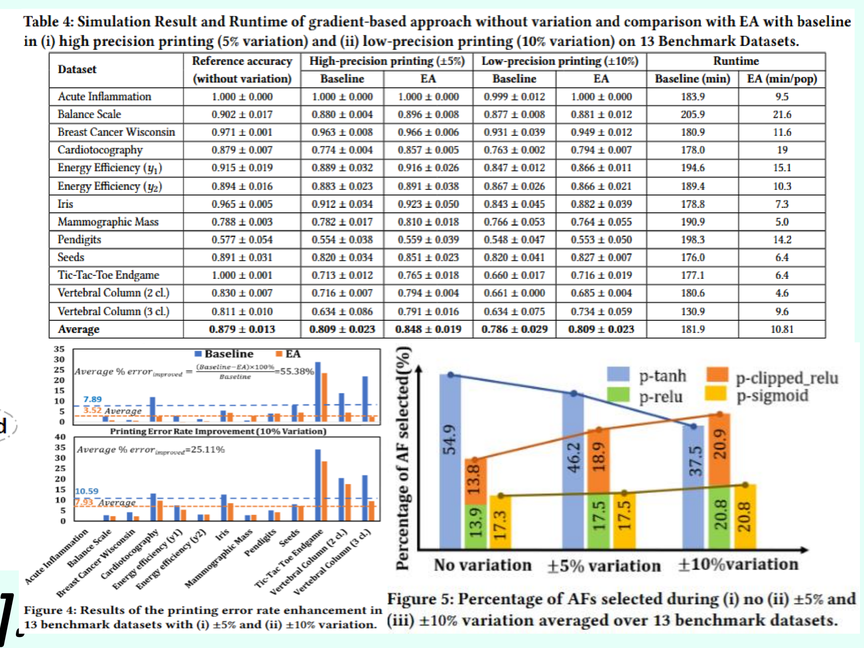
Thesis Overview



Addressing pNC's variability [ICCAD'24]:

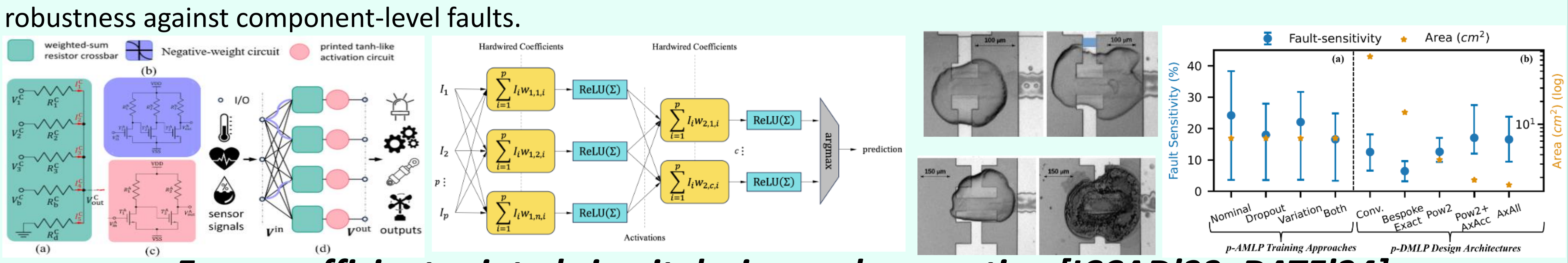
1 a. Proposes a **Neural Architecture Search (NAS)** framework to develop robust architectures that maintain functionality under process and environmental variations. It emphasizes a variation-aware design to ensure reliability across target PE applications.





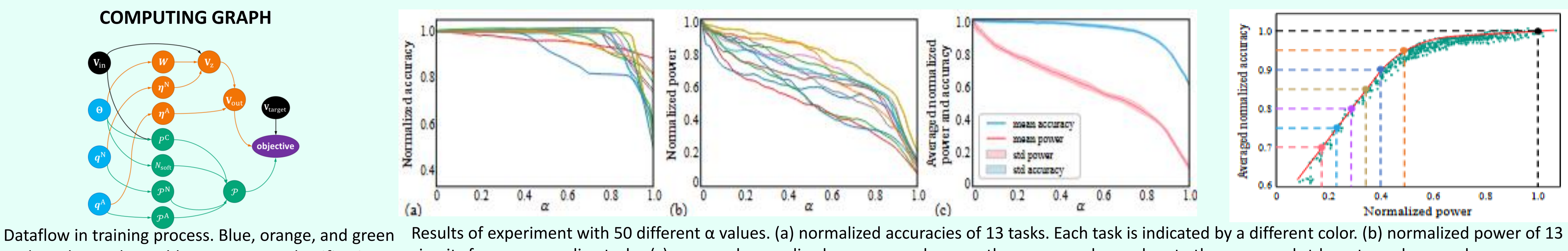
Fault sensitivity analysis of pNCs [ETS'24]:

2. Investigates fault sensitivity in printed MLP classifiers, identifying potential failure points, and proposes strategies to improve robustness against component-level faults.



Energy-efficient printed circuit design and computing [ICCAD'23, DATE'24]:

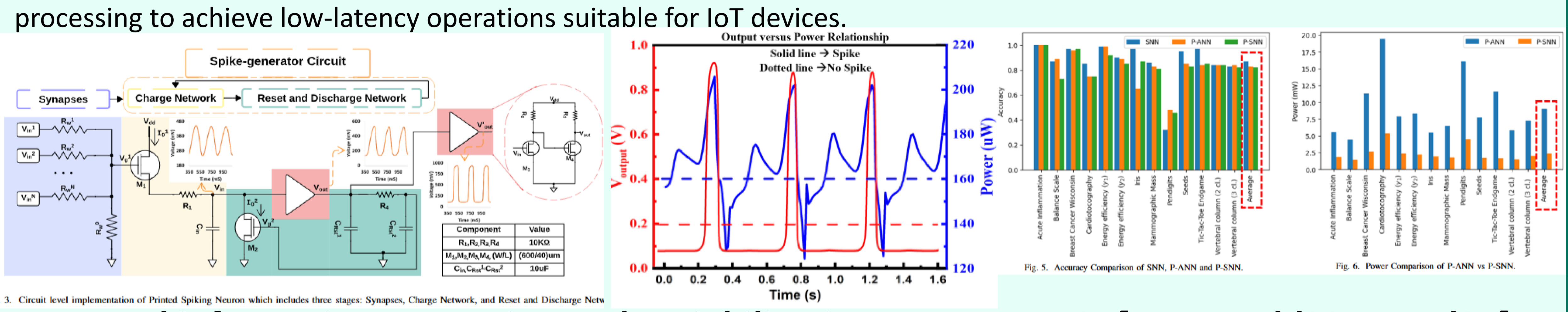
3 a. Introduces energy-efficient training methodologies, significantly reducing power without compromising performance



Dataflow in training process. Blue, orange, and green nodes relate to learnable parameters, classification accuracy, and power consumption.

Results of experiment with 50 different α values. (a) normalized accuracies of 13 tasks. Each task is indicated by a different color. (b) normalized power of 13 circuits for corresponding tasks. (c) averaged normalized accuracy and power, the curves and area denote the mean and std w.r.t. random seed

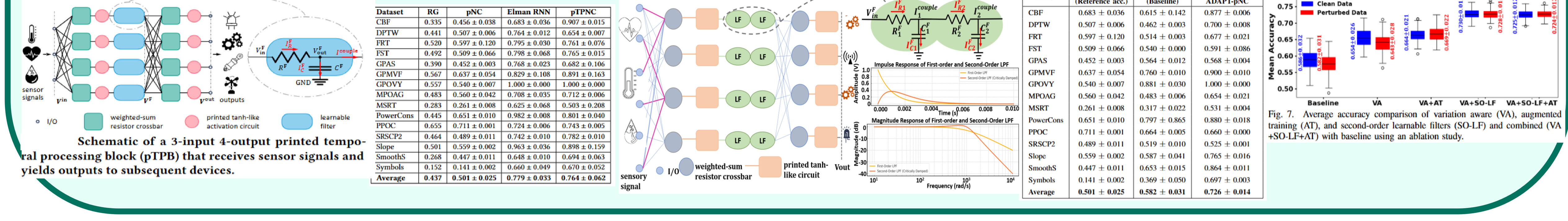
3 b. Develops **spiking neuromorphic circuits** for real-time, energy efficient computation, leveraging the benefits of analog processing to achieve low-latency operations suitable for IoT devices.



Temporal information processing and variability in recurrent pNCs [NanoArch'23, DATE'25]:

4 a. Introduces learnable filters for temporal signal processing in recurrent pNCs, allowing robust handling of time-series data and improving the adaptability of pNCs for dynamic applications.

4 b. Introduces adaptive temporal processing blocks **(ADAPT-pNC)** to mitigate printed device variability and noise using second-order learnable filters and data augmentation techniques for improved temporal data handling.



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