

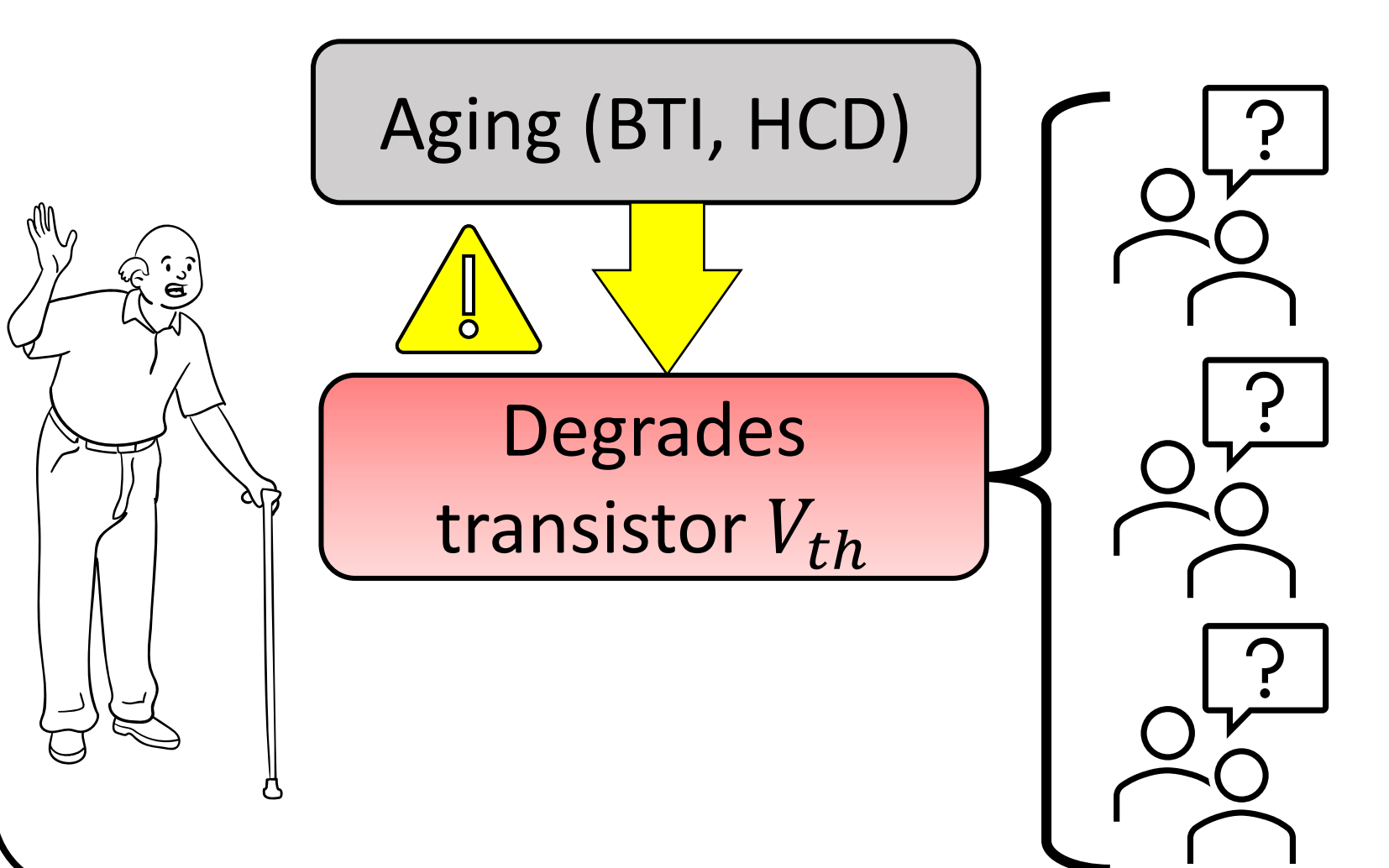
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INTRODUCTION

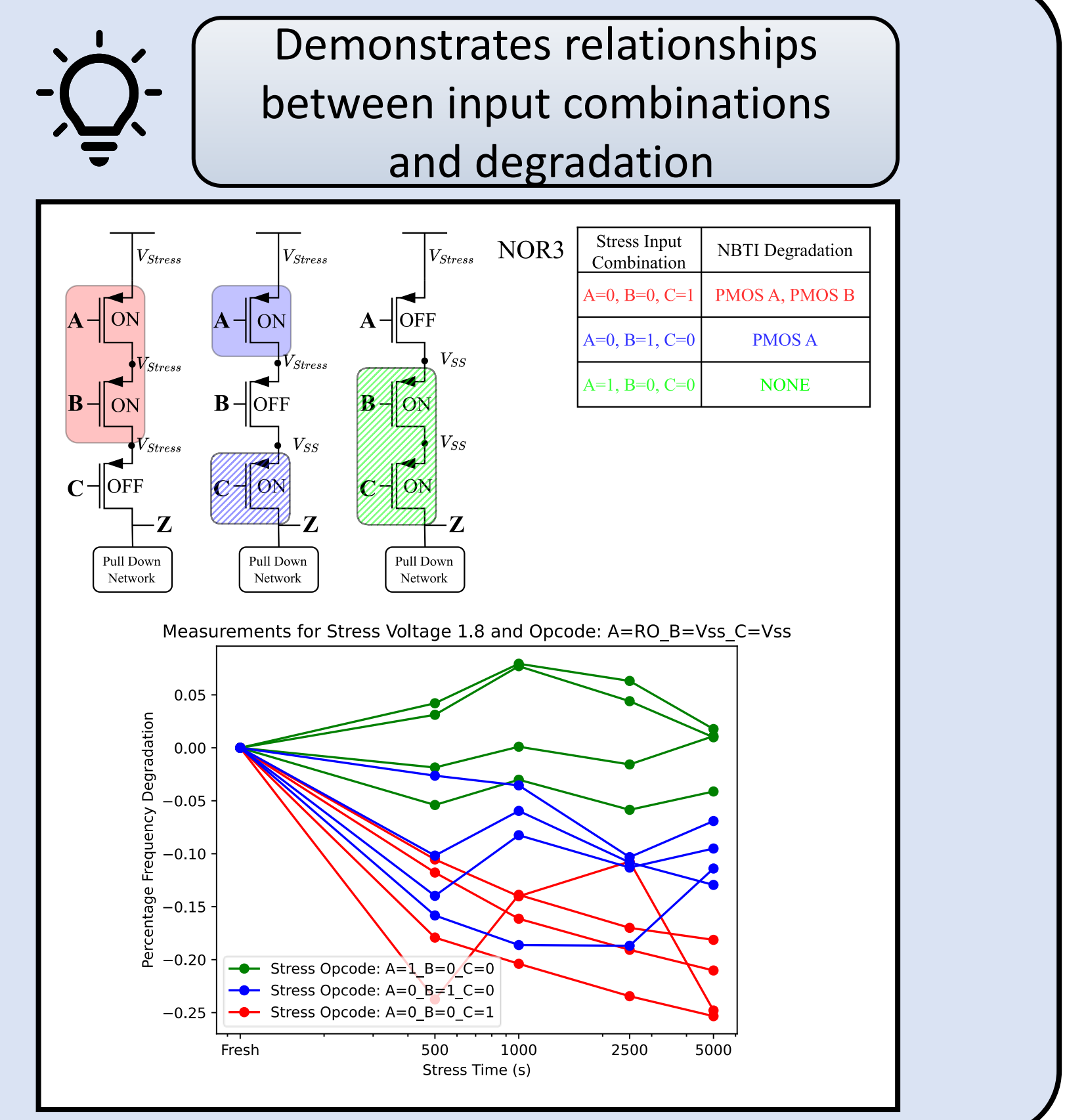
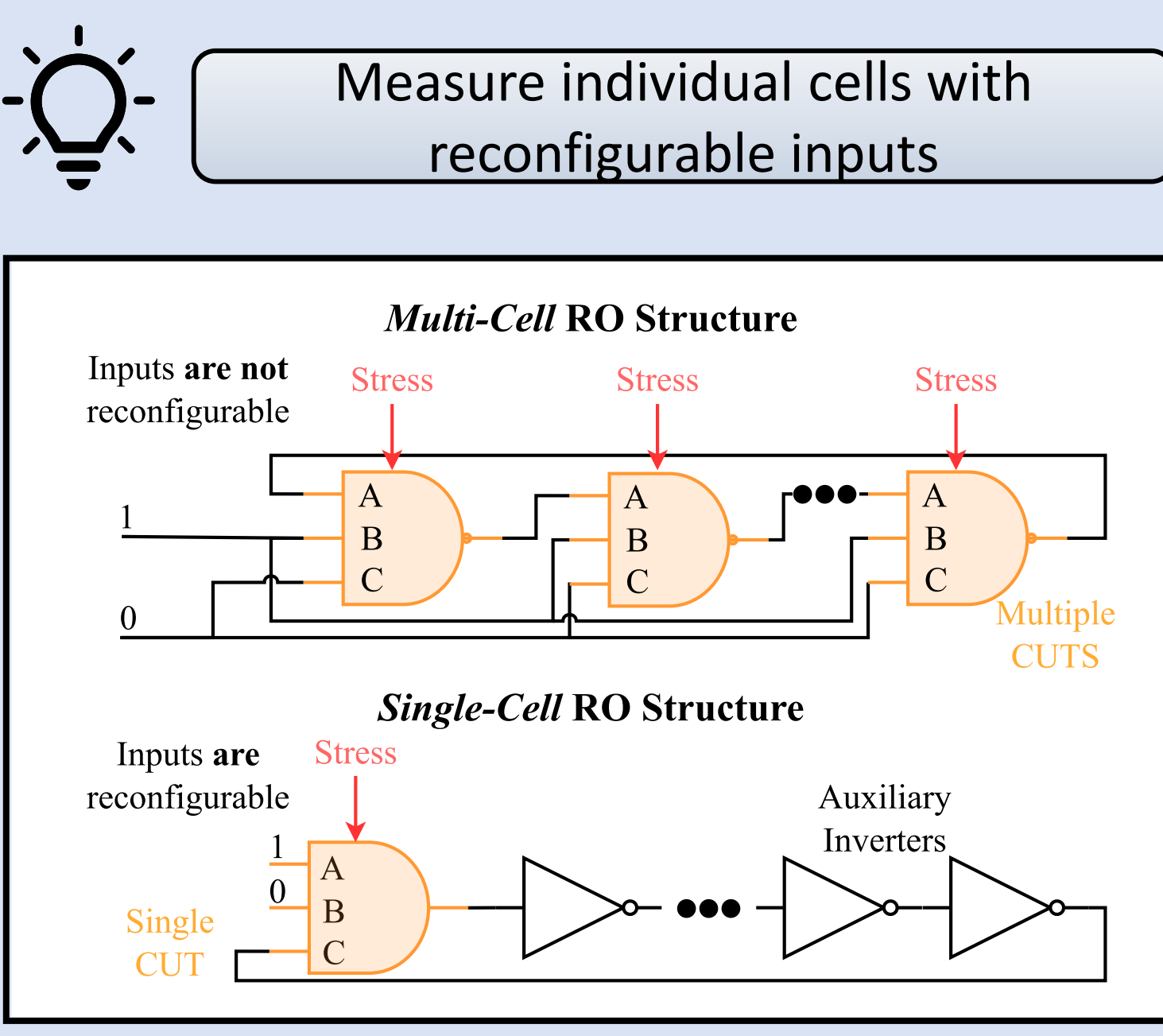
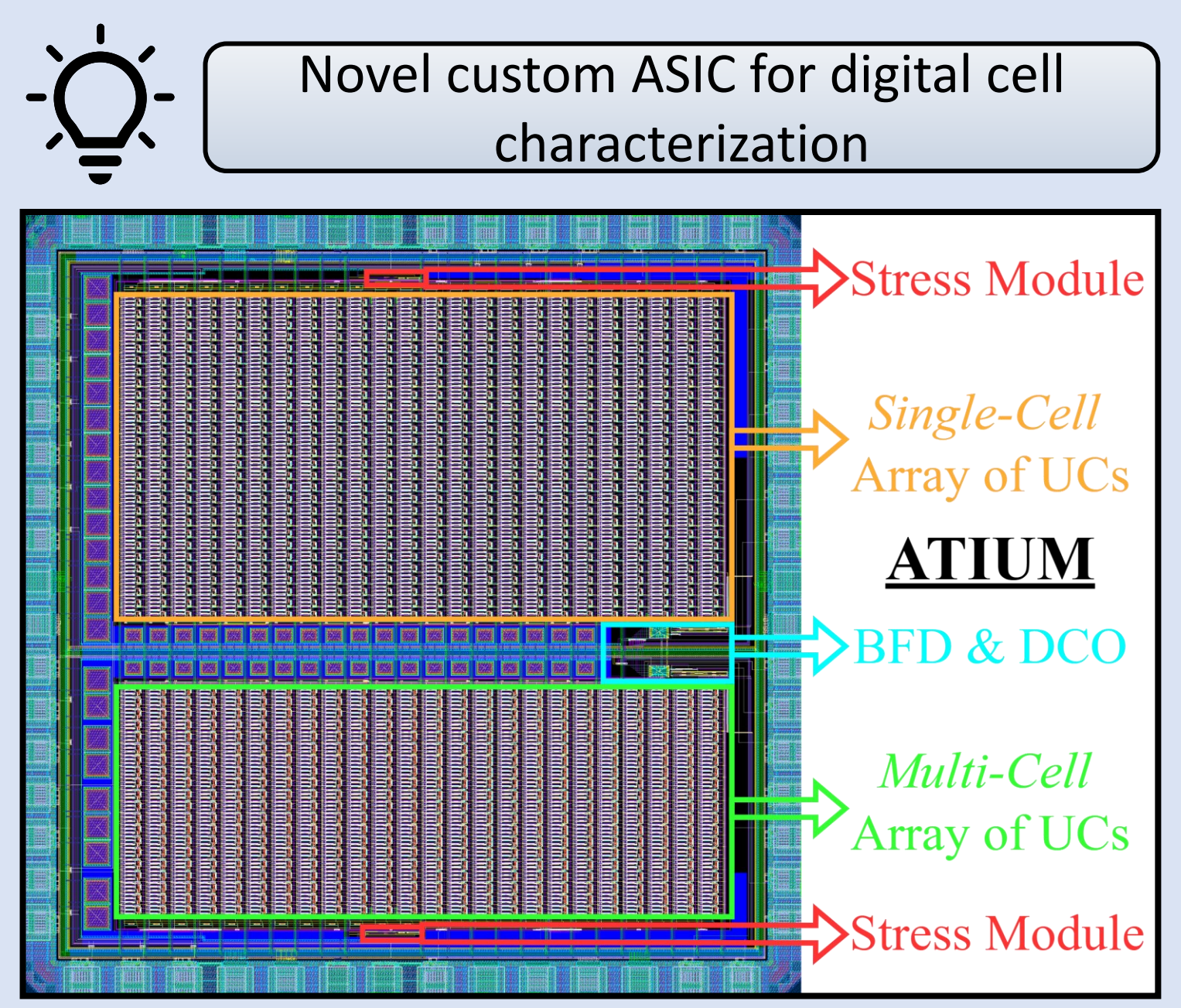
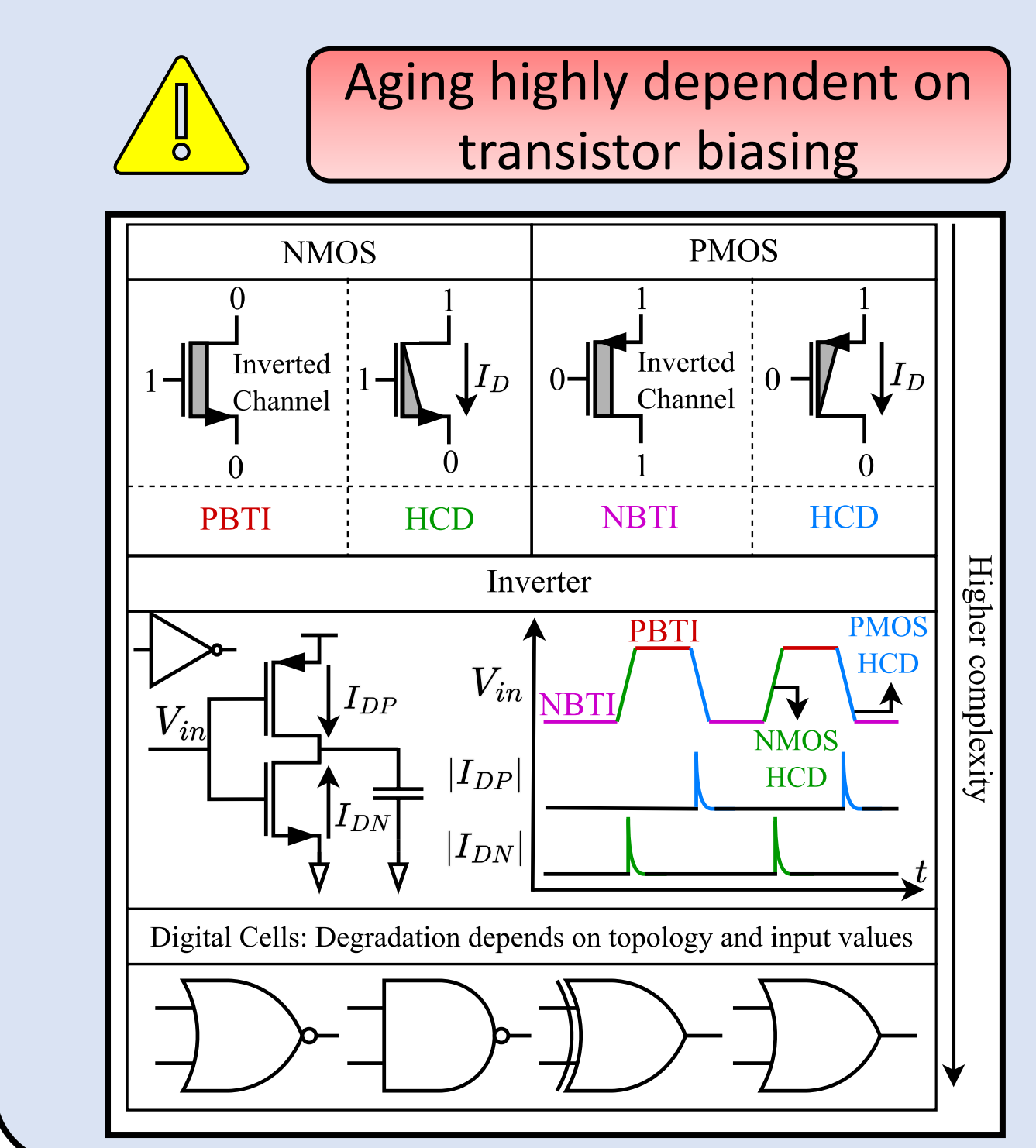


How does it affect digital circuits?
 How can we mitigate it?
 How can we take advantage of it?

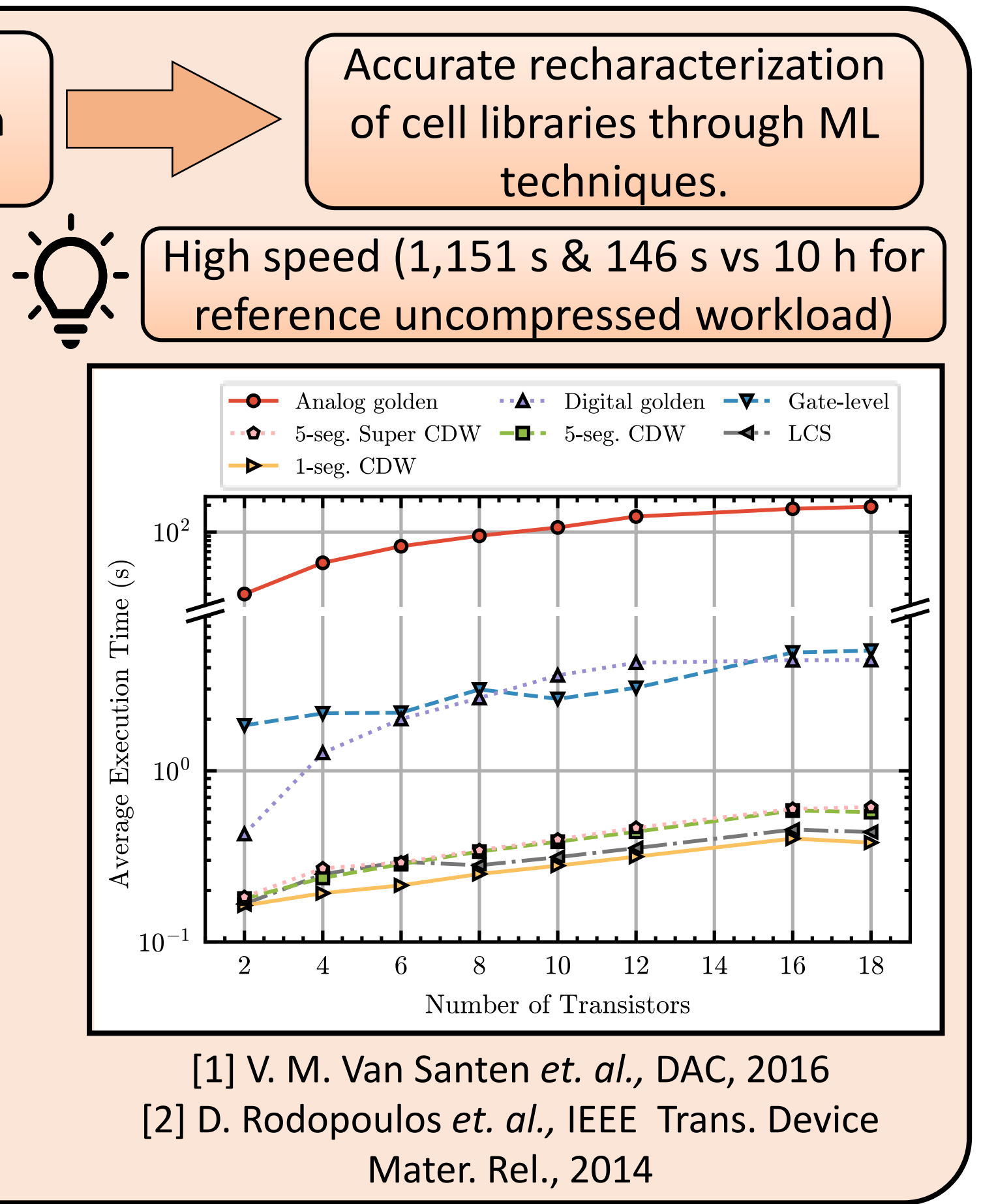
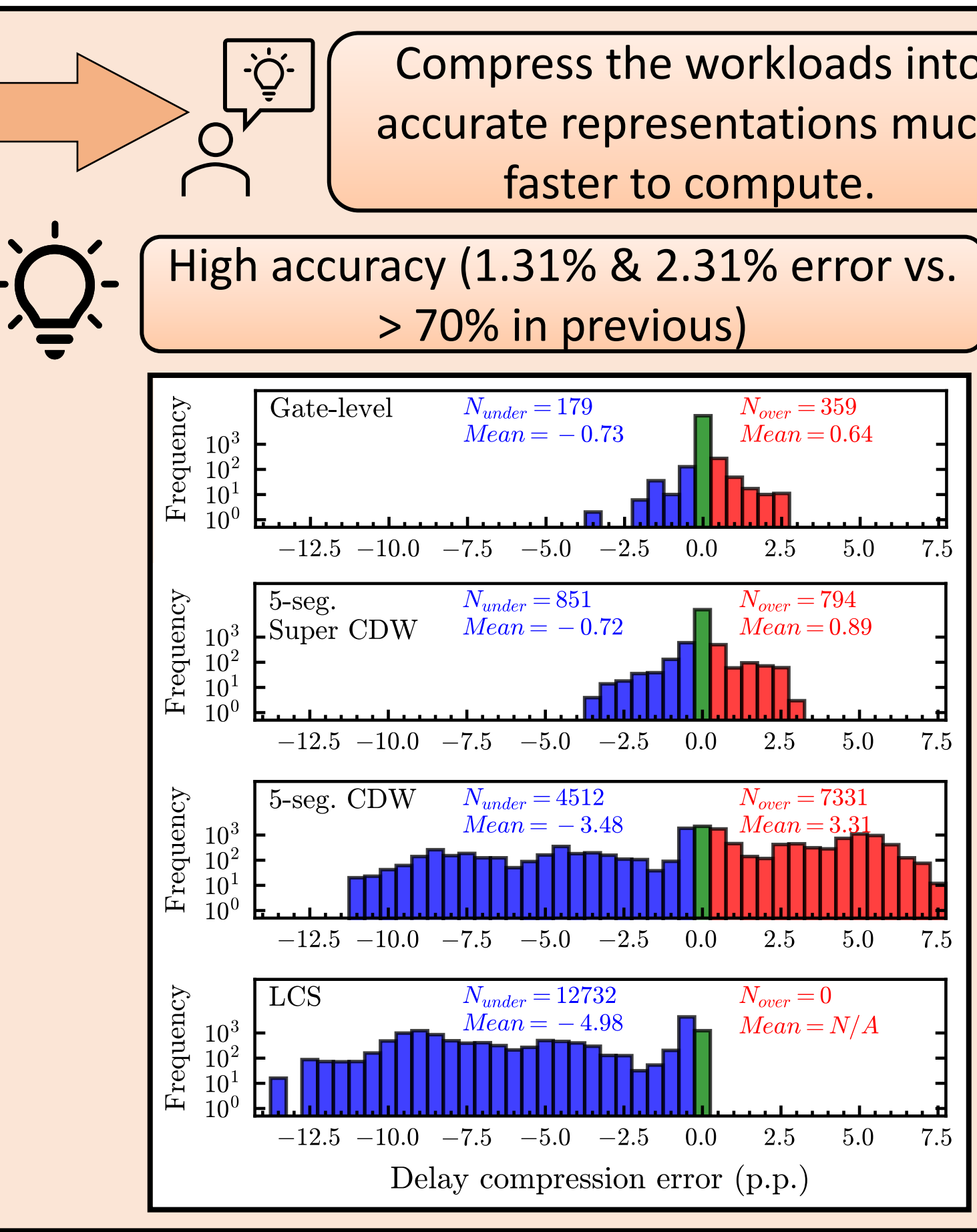
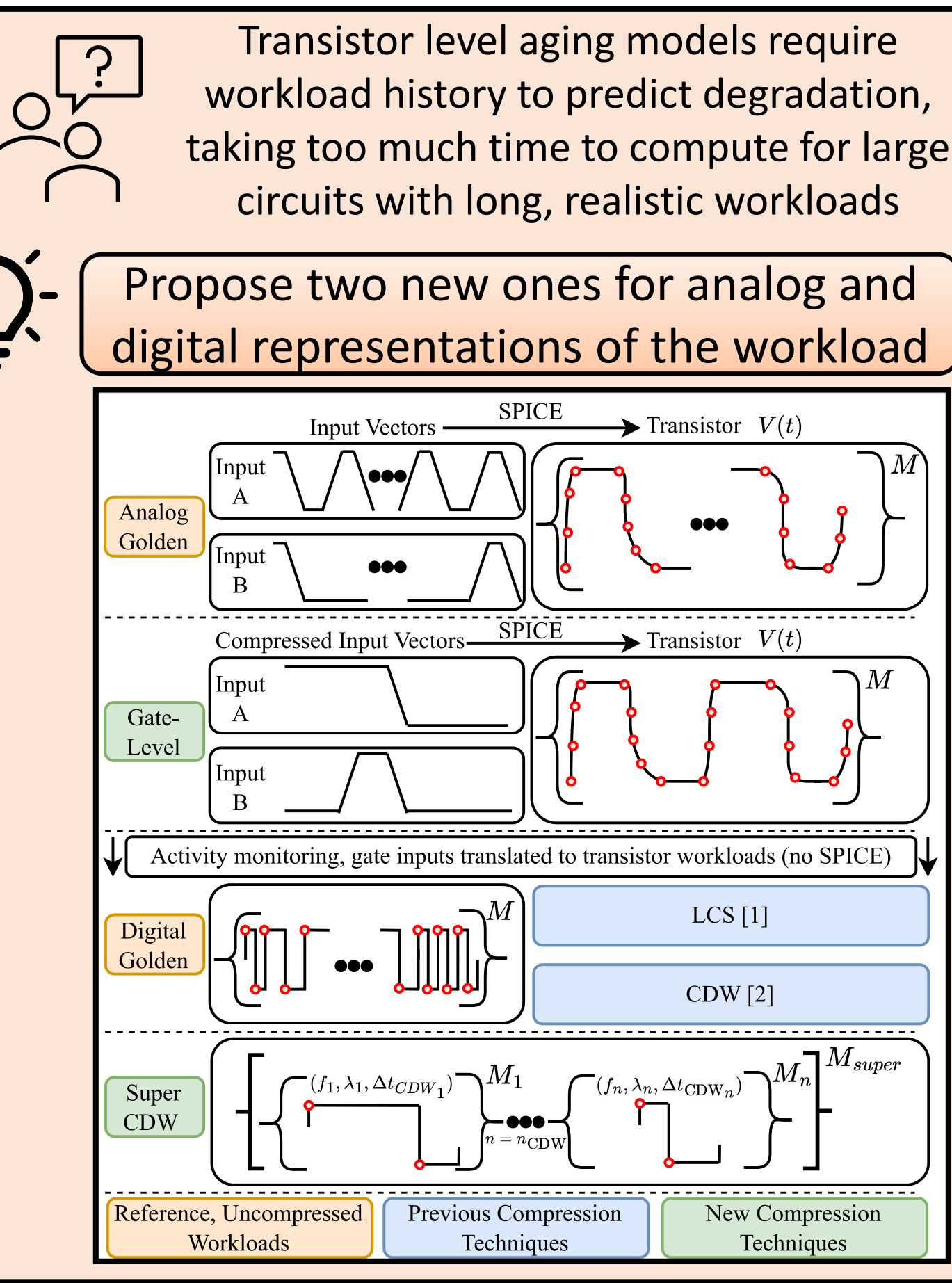
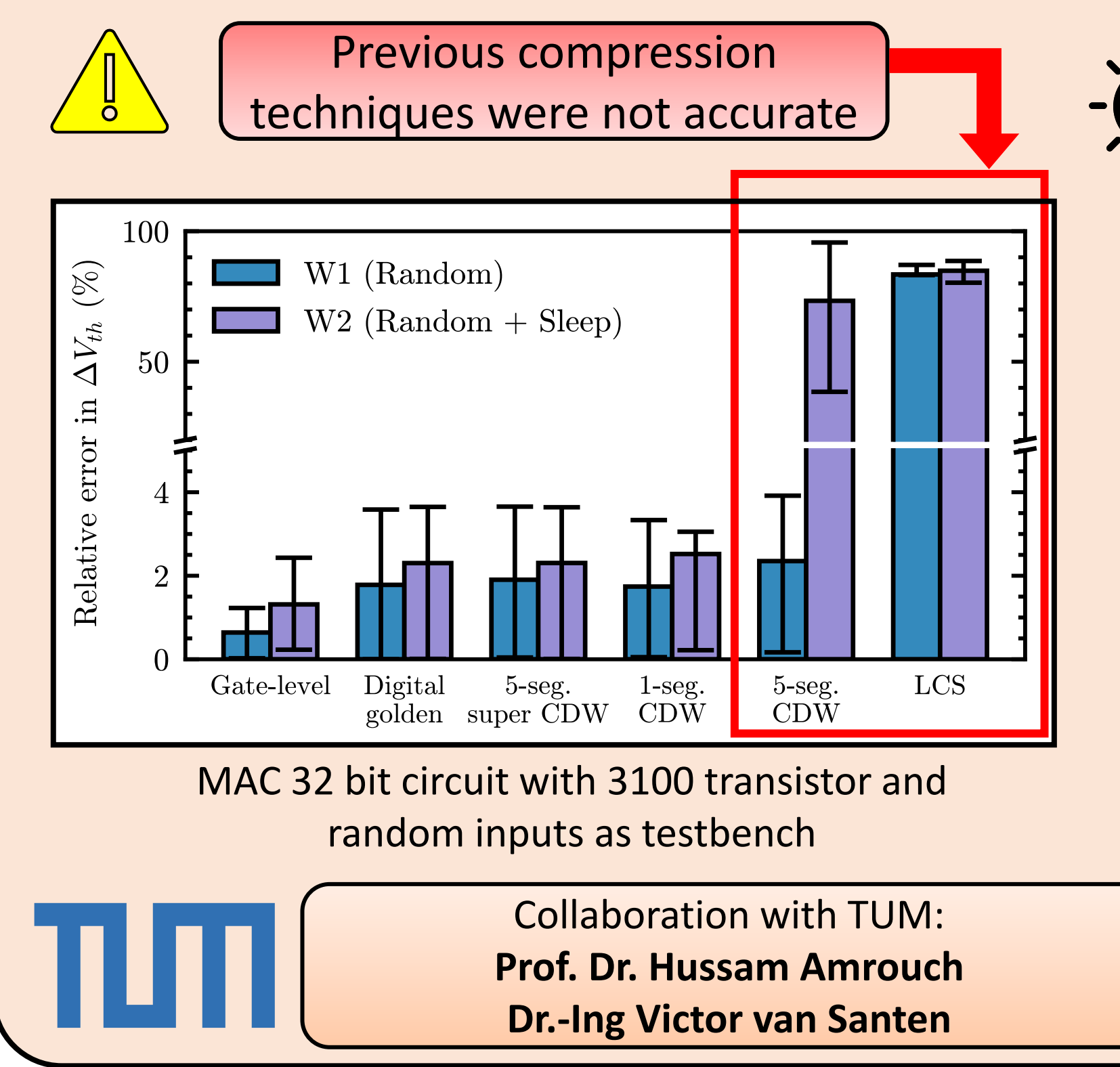
CONTRIBUTIONS

- Specialized, circuit focused characterization
- Novel methodology to scale aging predictions from the transistor level to the circuit level
- Use acquired knowledge to obtain reliable and cheap hardware fingerprints (PUFs)

CHARACTERIZATION



MITIGATION



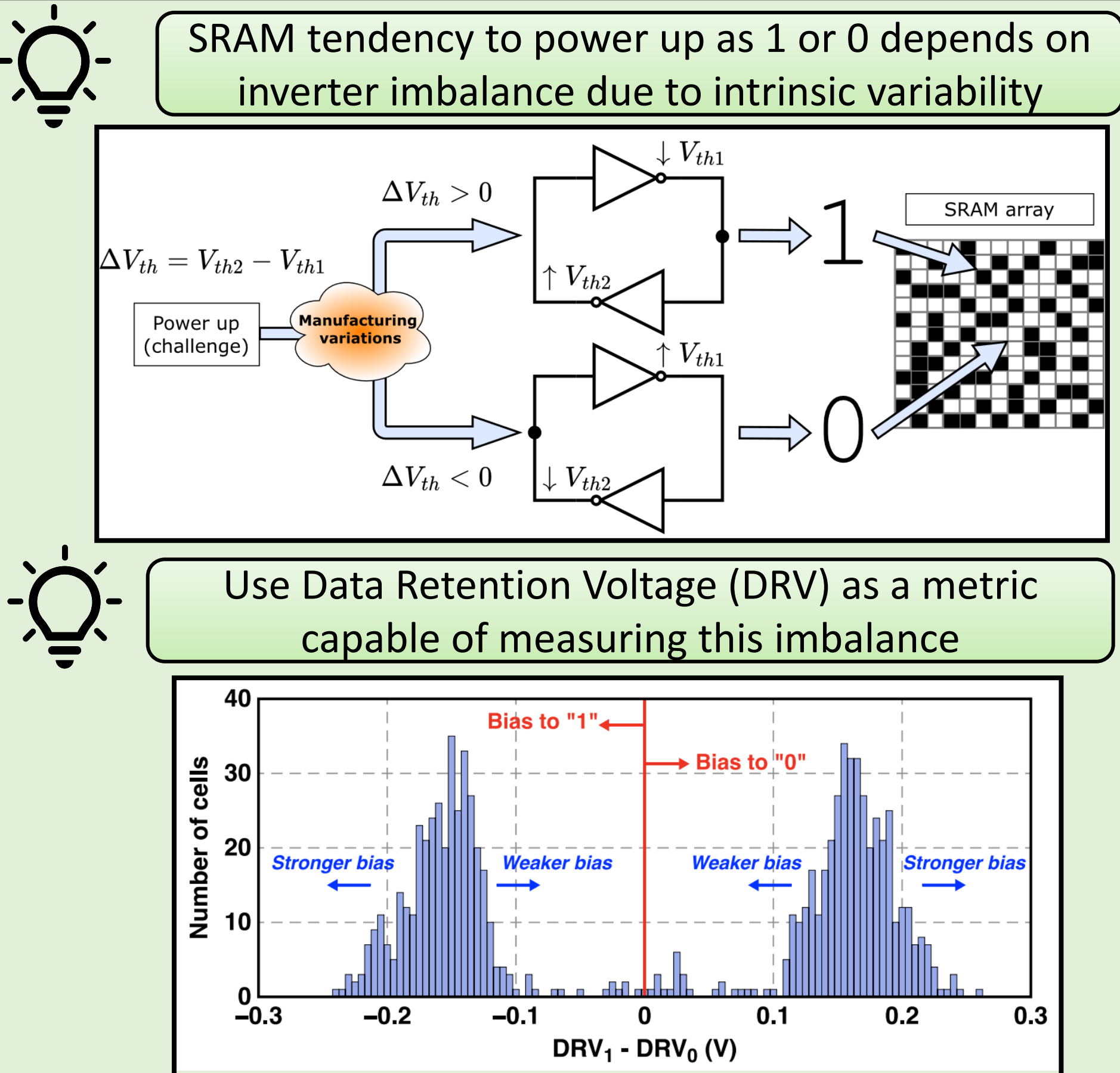
EXPLOITATION

PUFs provide a low-cost Root-of-Trust (RoT) for cryptographic algorithms

SRAM PUFs are the most popular due to their ease of implementation

Their raw implementation is unreliable (High Bit error rate, BER), requiring expensive Error Correcting Codes (ECCs)

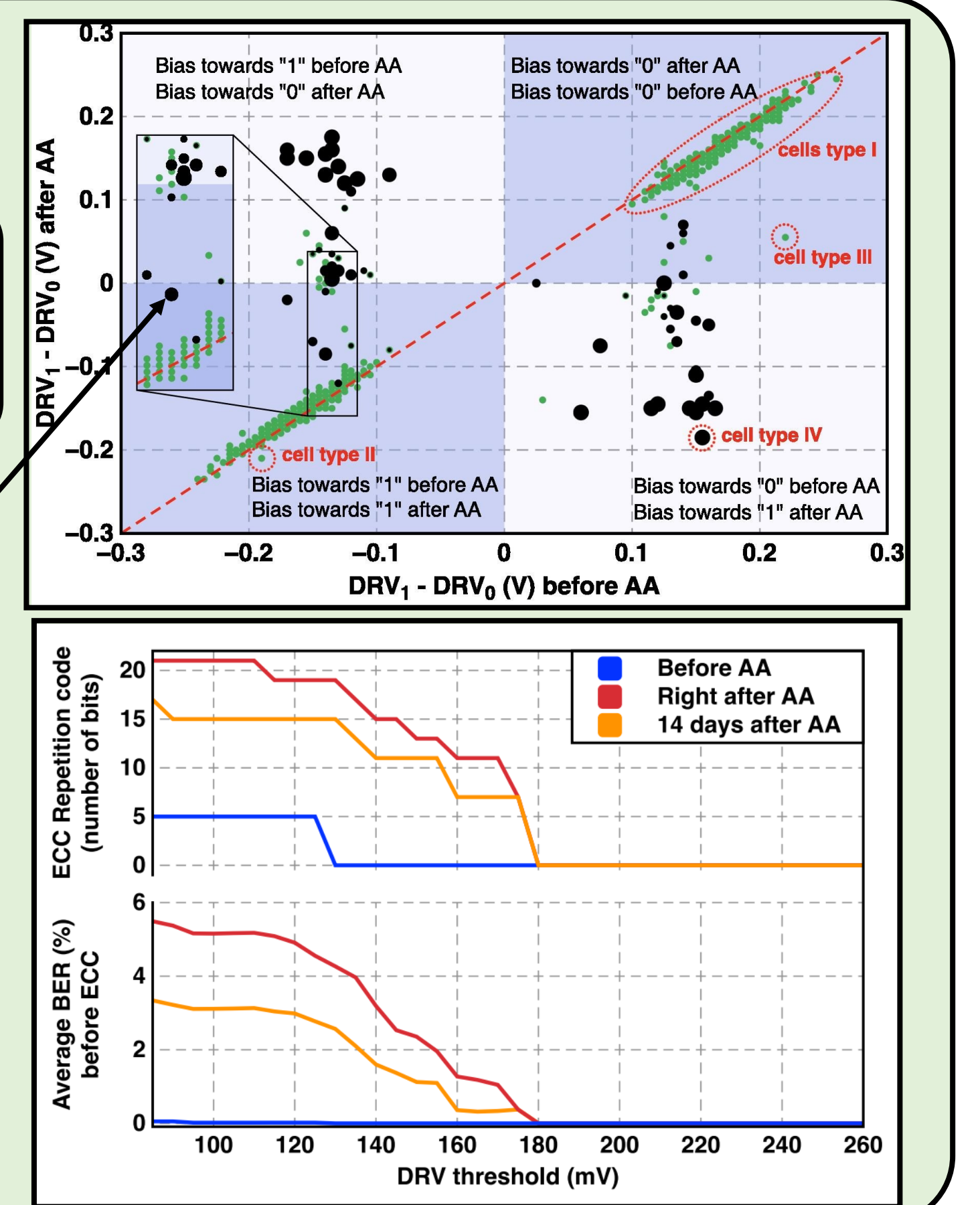
Use our knowledge on variability and aging to select the most reliable cells, which will stay reliable over time (against aging) and under different operating conditions



Measure the behavior of each cell after accelerated aging (AA), validating DRV as a classifier

Black dots represent unstable cells (BER > 0%) and the size of each black dot is proportional to the BER value.

Selecting the most reliable cells (Higher DRV threshold) eliminates the need for ECC



Acknowledgements

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Conclusions

- A novel custom ASIC capable of measuring aging in digital cells, demonstrating behavior previously only studied through simulations.
- Compression techniques to efficiently scale aging predictions to digital systems, outperforming previous approaches. These enable faster and more accurate predictions for aging-aware digital design, mitigating the impact of aging.
- Selection technique for reliable SRAM PUFs, capable of withstanding the effects of aging.