

System-Level Design in the Era of Brain-Computer Interfaces

PhD Forum 2025

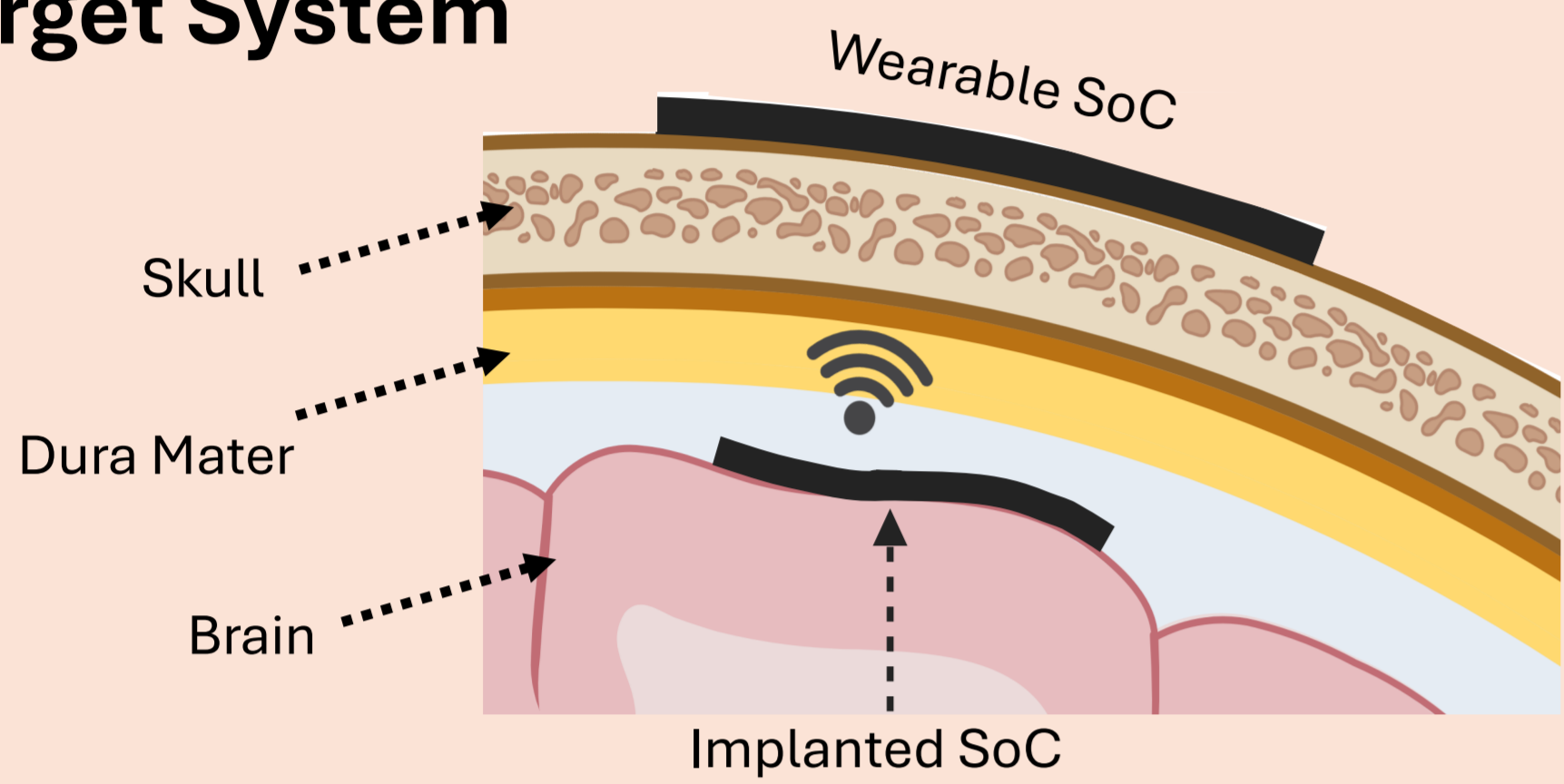
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“To unlock the full potential of the BCI field, BCI system development must be properly defined and standardized, with a **clear target BCI system**, an understanding of its **constraints**, and a distinction between **three overlapping time domains** that emphasize different levels of research and development, with progress continuing concurrently in each domain”

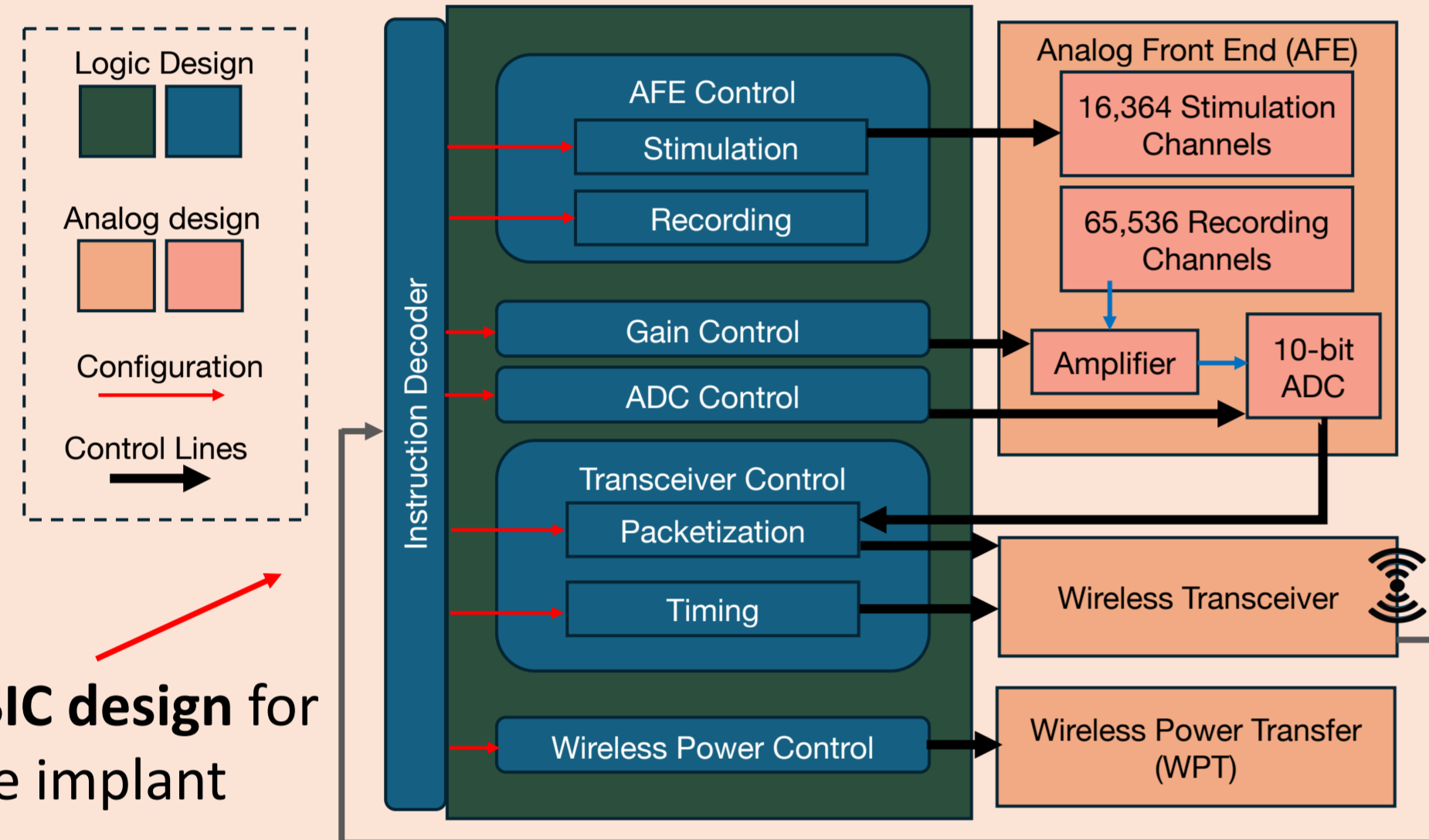
Pre-BCI

Contribution: Designing implant-based BCI systems that support large-scale data acquisition, wireless communication and a high-level of configurability

Target System

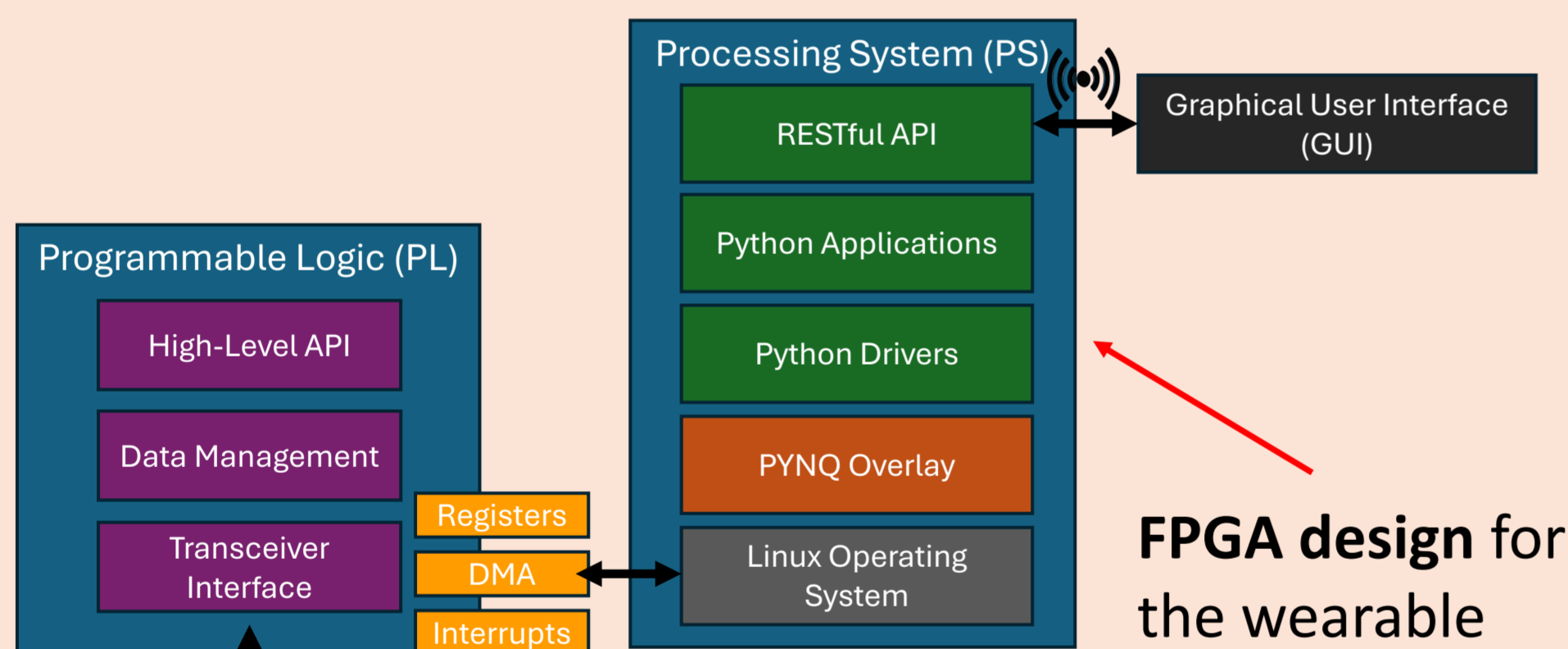


Custom Implanted Microcontroller

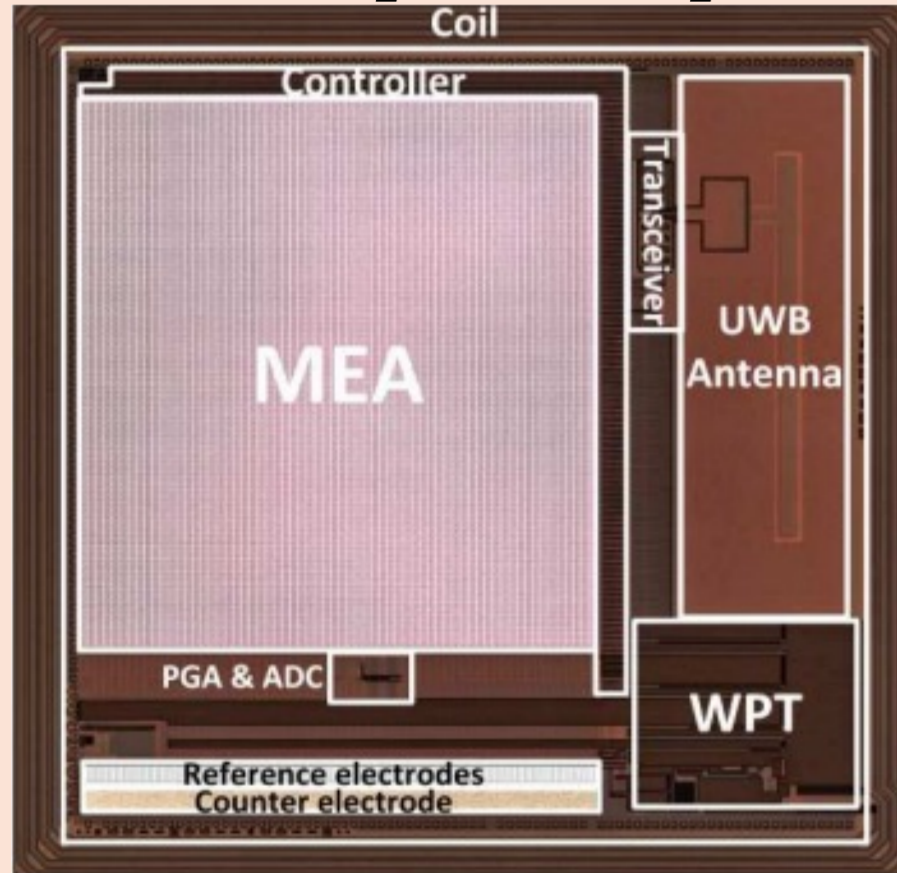


ASIC design for the implant

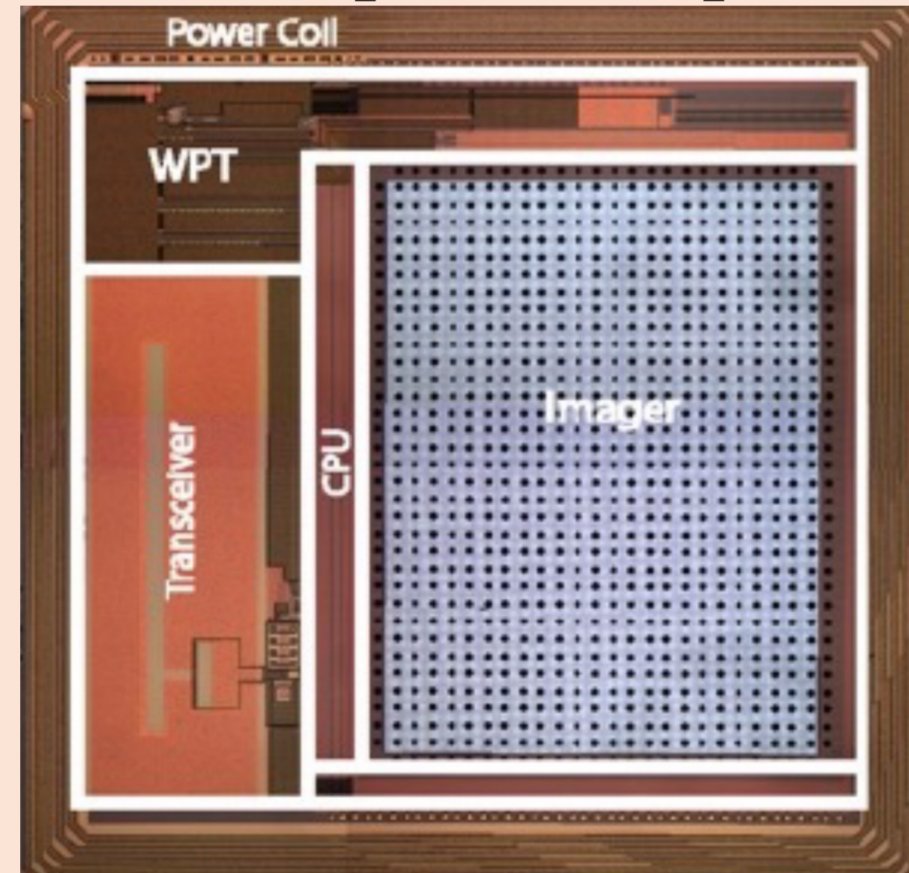
Custom Wearable Control Stack



BISC [VLSI'23]



IBISX [CICC'24]

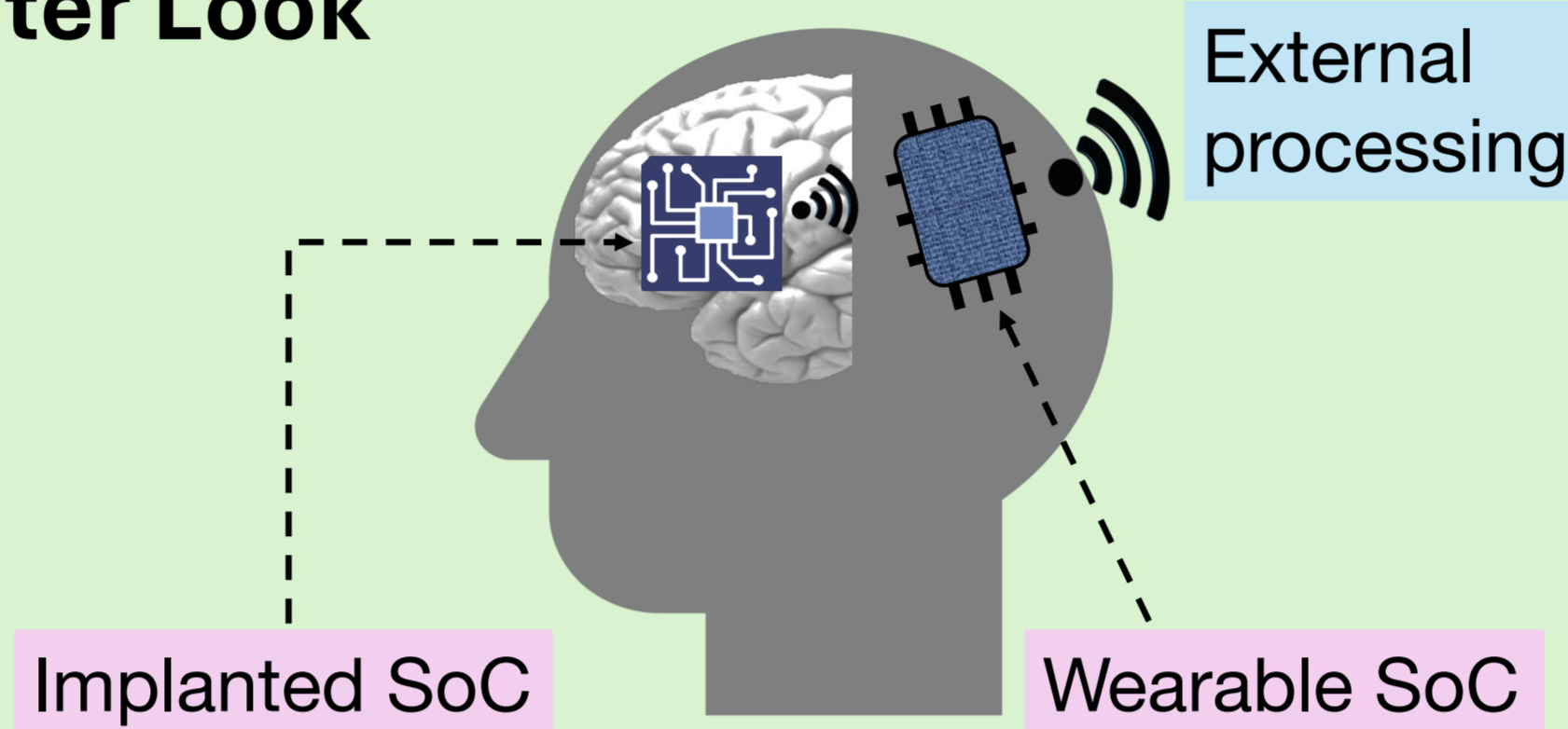


Two configurable BCI systems integrating two neural interfaces and tested successfully on animals

Intra-BCI

Contribution: Developing system-on-chip (SoC) design methodologies to integrate real-time computation and complete BCI applications into BCI systems

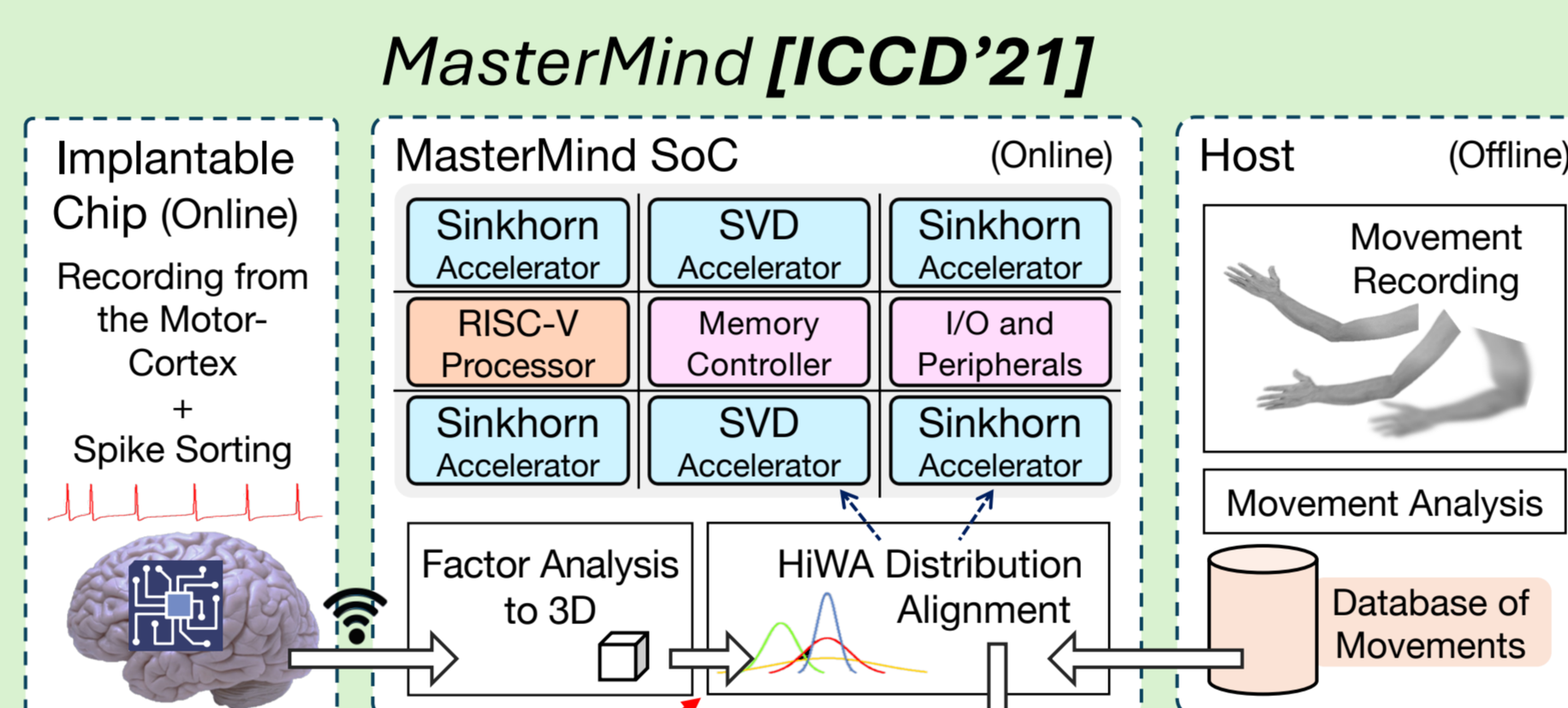
Outer Look



System Requirements/Constraints

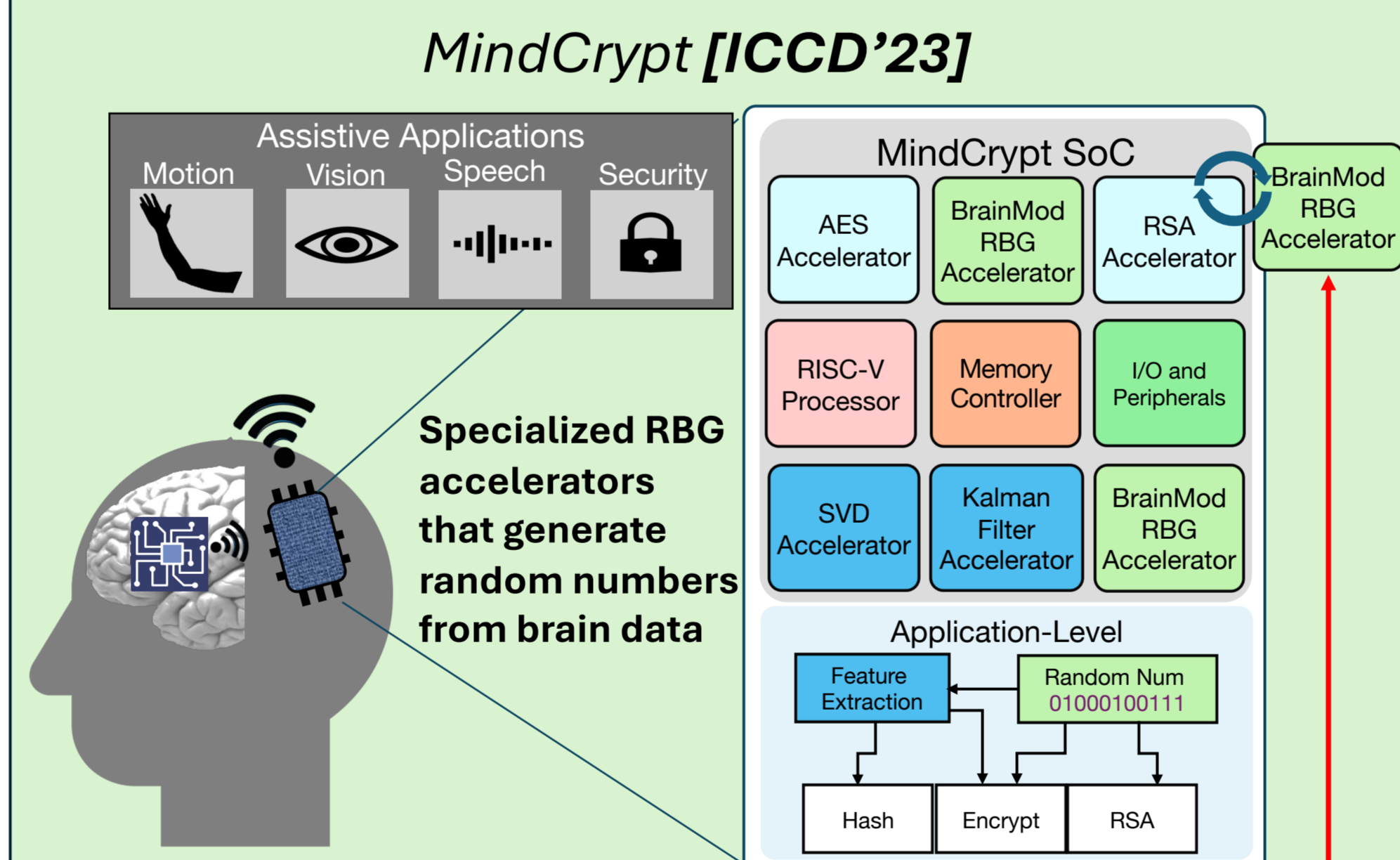
Low-Power: Wearable ~200mW, Implant $40 \frac{mW}{cm^2}$
Real-Time: Latency ~0.18 sec, Throughput 1-30KHz

Integration of BCI Applications



Heterogeneous SoC architecture Implements a many-accelerator machine learning algorithm in HW
Result: BCI applications can meet the low-power and real-time requirements of the BCI system and execute BCI algorithms

Supporting the System by Using the Brain as a Random Number Generator

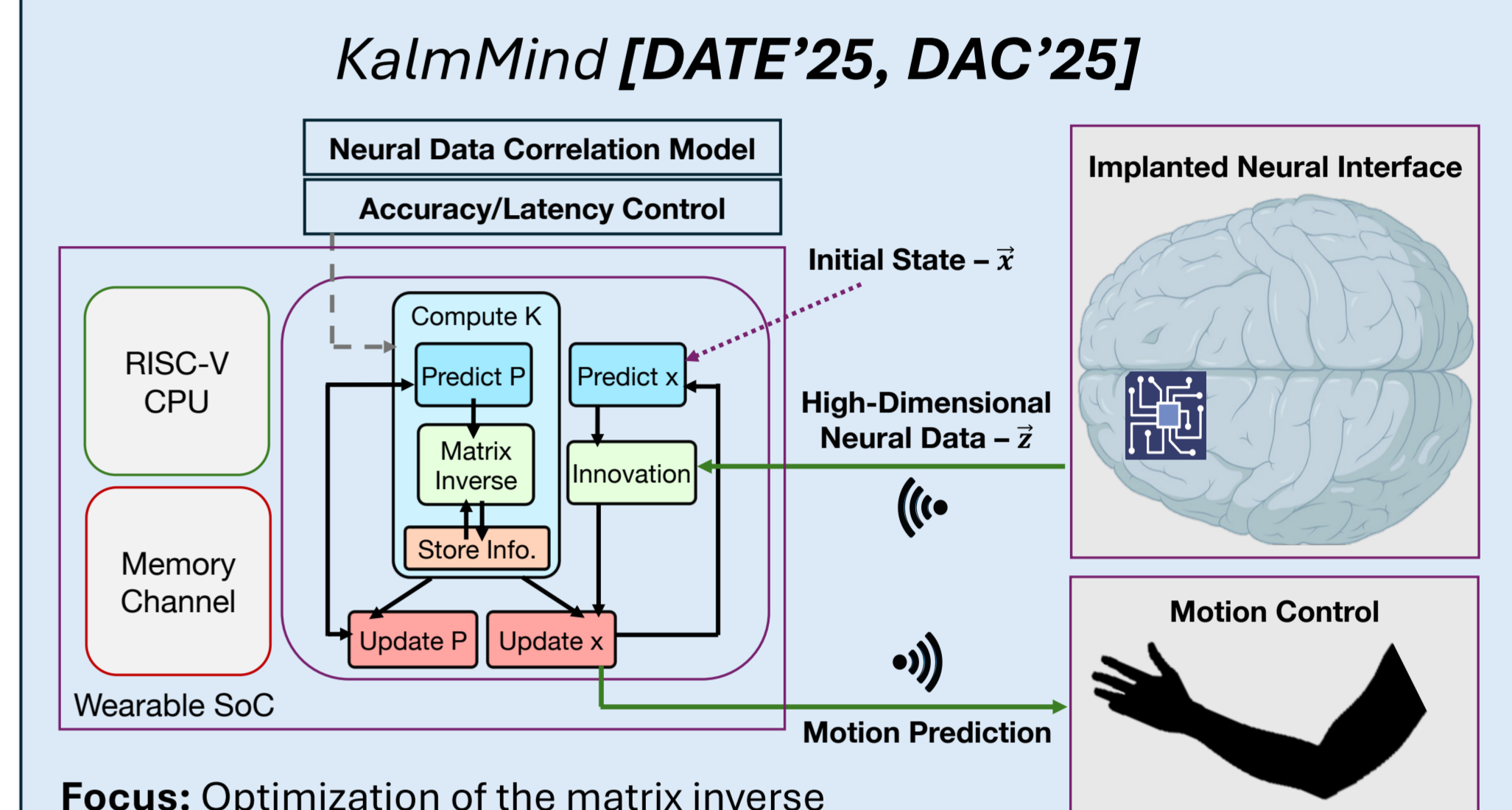


Multiplex accelerators at runtime with dynamic partial reconfiguration (DPR)
Result: BCI applications of machine learning and security can utilize efficient random number generation that is powered by the brain

Post-BCI

Contribution: Specializing computational data flows to interact seamlessly with the biological brain through BCI algorithm-hardware co-design and integrating brain-inspired computation in heterogeneous SoCs

Specializing the Kalman Filter for BCI

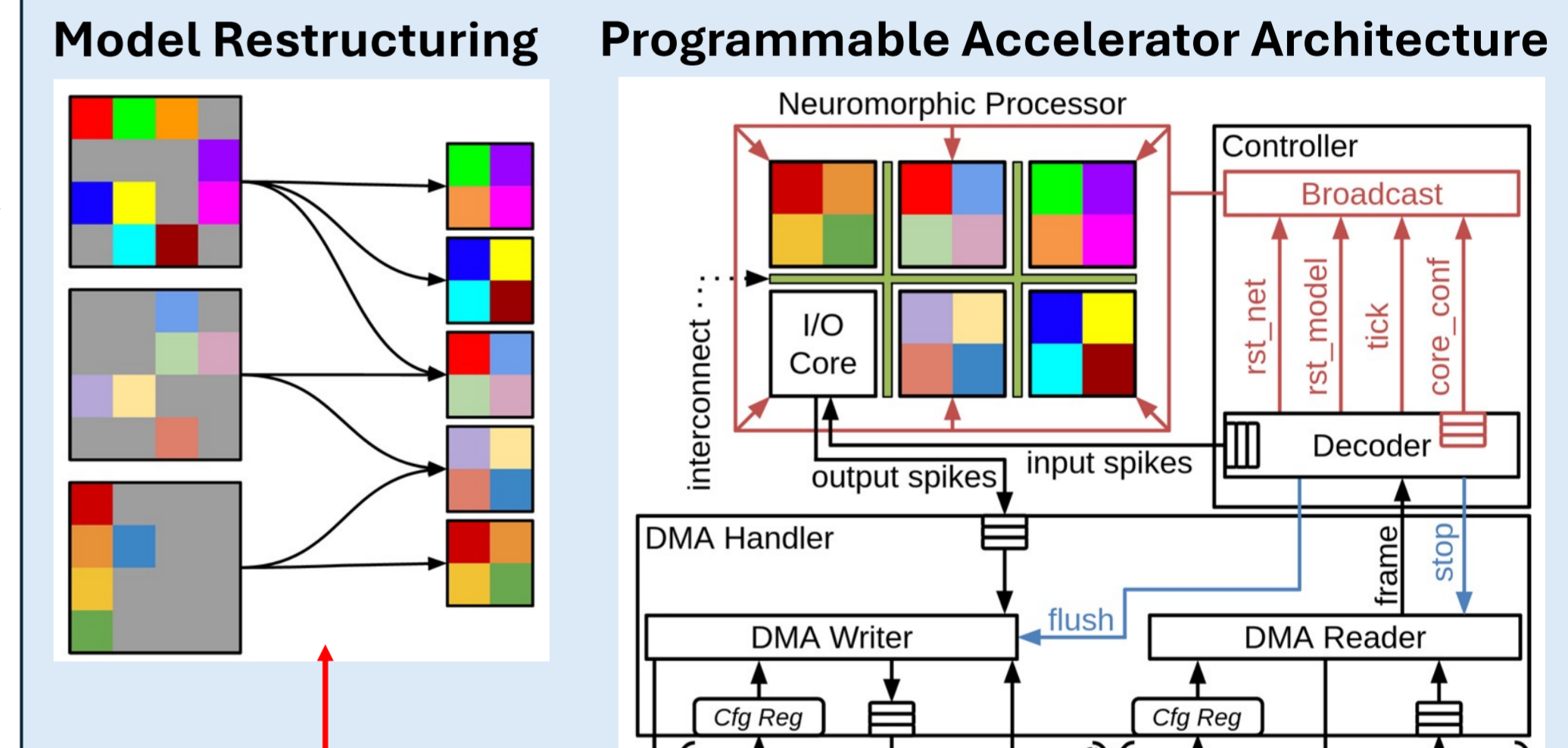


Focus: Optimization of the matrix inverse implementation in hardware with a combination of approximation and calculation techniques relying on spatiotemporal correlation in neural data

Result: Algorithm-Hardware co-design of the Kalman Filter algorithm enables to fine tune the tradeoff between accuracy and energy efficiency at runtime and specialize the computation for a specific BCI application and a specific BCI system

Integrating Neuromorphic Computing in Heterogeneous SoCs

SpikeHard [CASES ESWEK'23]



Find clusters of neurons and axons in SNNs and solve a bin packing optimization problem to find an optimized hardware architecture for the SNN

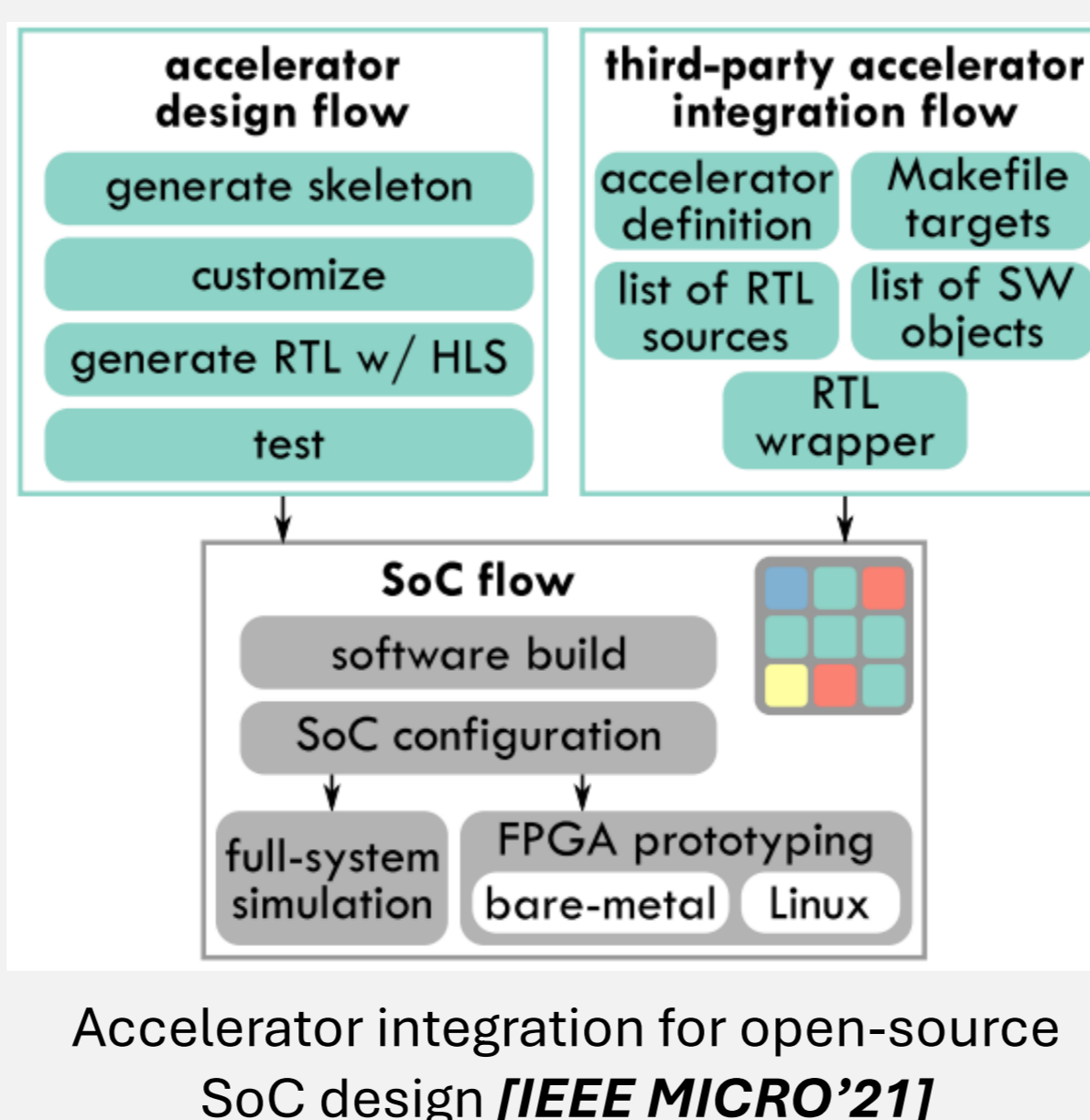
Encapsulate the SNN hardware architecture with a custom controller and a DMA handler in order to integrate as a programmable accelerator in a heterogeneous many-accelerator SoC

Ultimate Goal: Enable the integration of Neuromorphic hardware with other machine learning approaches in the same system and open a pathway for implementing complex computational dataflows for next-generation BCI systems

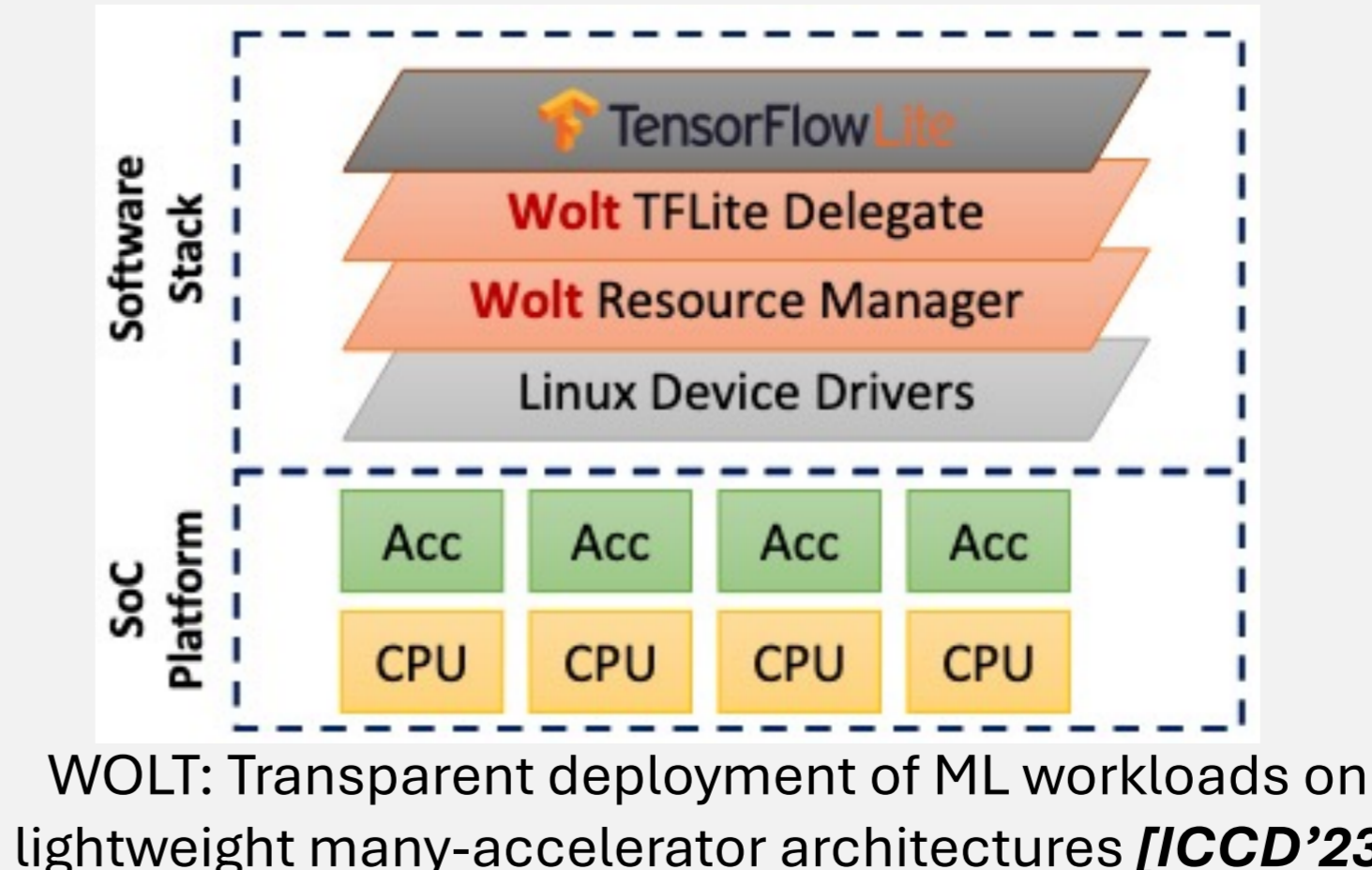
Conclusion

The purpose of my work is to bridge the gap between the current state of BCI applications and the realization of practical BCI systems. I believe that simultaneously addressing the three domains—Pre-BCI, Intra-BCI, and Post-BCI—is essential for unlocking the full potential of the BCI field

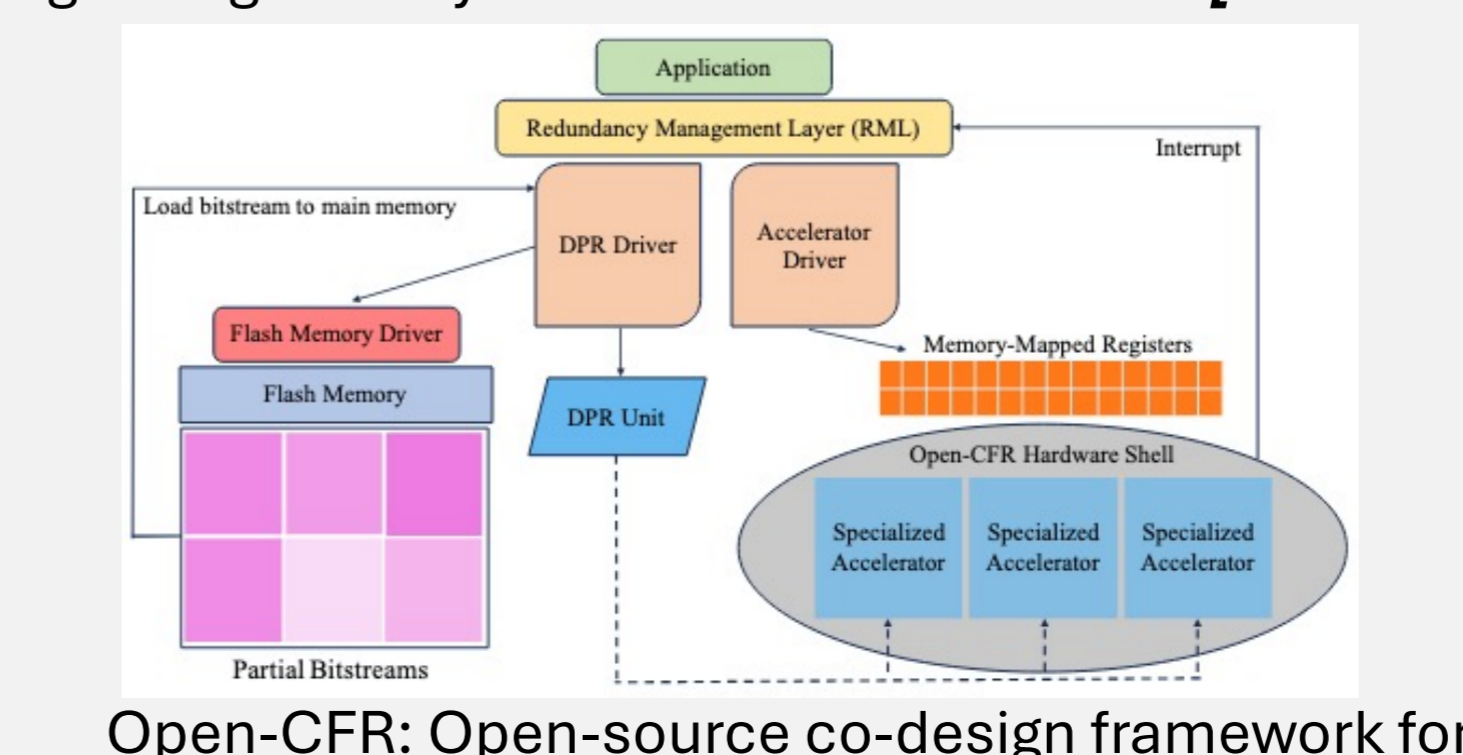
Additional Work



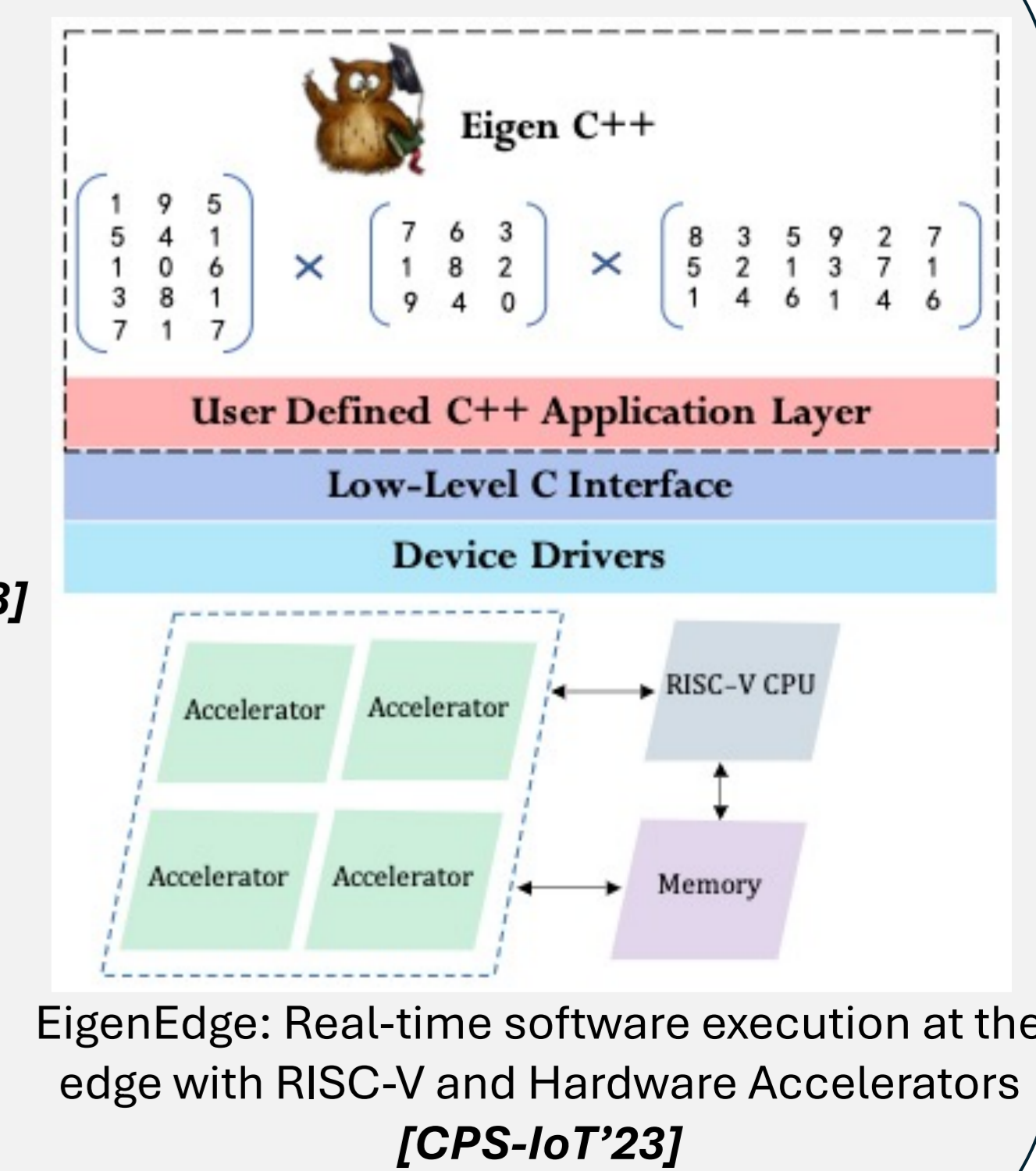
Accelerator integration for open-source SoC design [IEEE MICRO'21]



WOLT: Transparent deployment of ML workloads on lightweight many-accelerator architectures [ICCD'23]



Open-CFR: Open-source co-design framework for redundancy with DPR in COTS FPGA SoCs [SCC'24]



EigenEdge: Real-time software execution at the edge with RISC-V and Hardware Accelerators [CPS-IoT'23]