Chair for Design Automation
TUM School of Computation, Information and Technology
Technical University of Munich

Physical Design for Field-coupled Nanocomputing

Simon Hofmann, *Supervisor:* Robert Wille

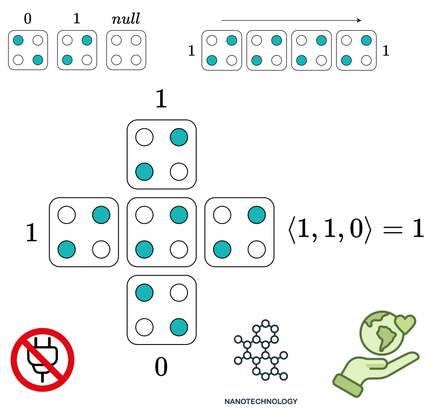
simon.t.hofmann@tum.de

https://www.cda.cit.tum.de/research/nanotech/

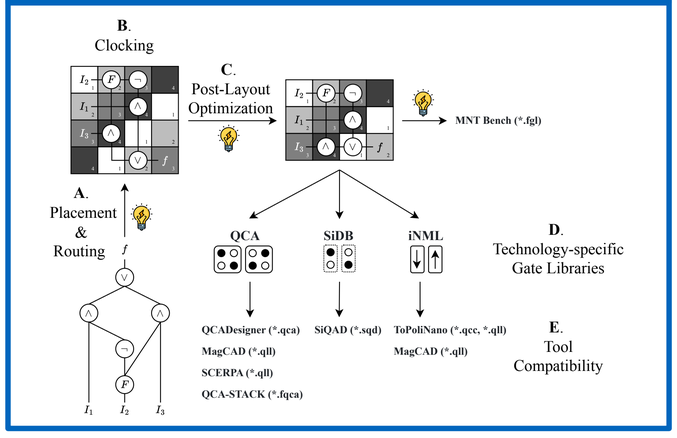
Abstract

The growing demand for computational power, coupled with the limitations of *Moore's Law* and rising energy consumption of CMOS technologies, necessitates alternative computing paradigms that are environmentally-friendly. **Field-coupled Nanocomputing (FCN)** offers a promising solution by utilizing physical field interactions for ultra-low-power computation at the nanoscale.
This poster showcases **novel physical design algorithms**, which achieve average **area reductions of up to 70%** and, for the first time, enable **post-layout optimization** as well as the inclusion of **discretionary cost objectives**. Additionally, the developed **software tools for physical design, co-design, and benchmarking**, significantly advances design automation for FCN.

Wires and Gates

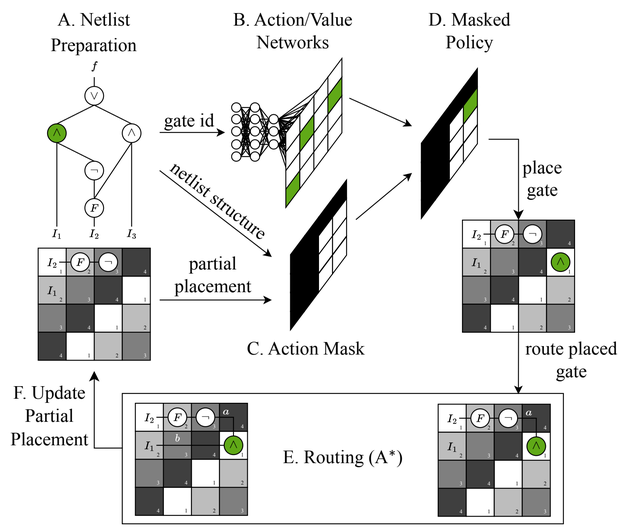


Physical Design Flow



Physical Design: *NanoPlaceR*

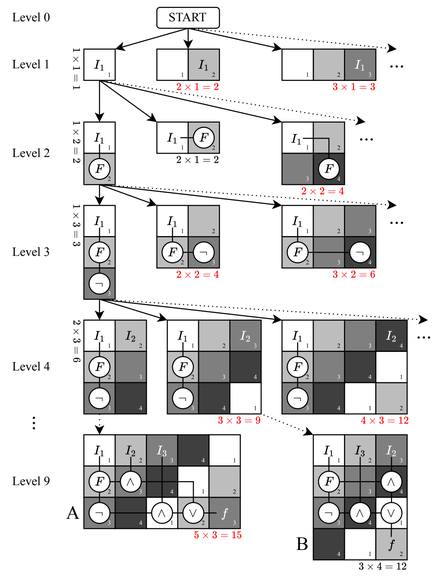
Layout generation using Reinforcement Learning



59% average area reduction compared to SOTA (*ortho)* and **technology-independent**

Physical Design: *GOLD*

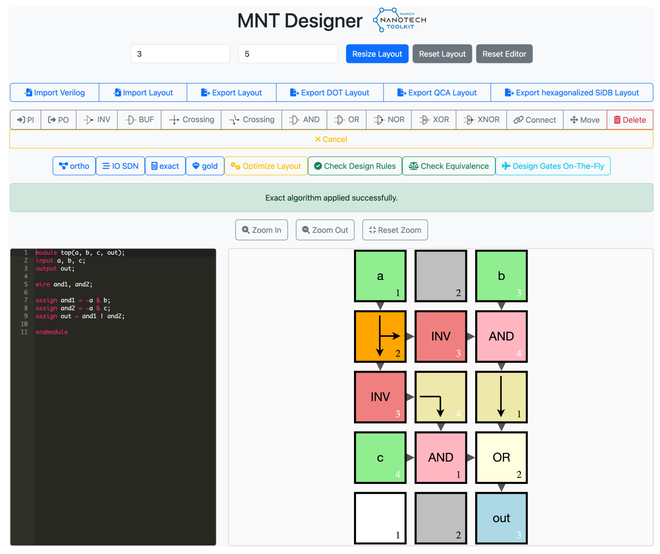
Layout generation using search algorithms



24% average area reduction compared to *NanoPlaceR* and **460 times faster**

Software Tool: MNT Designer

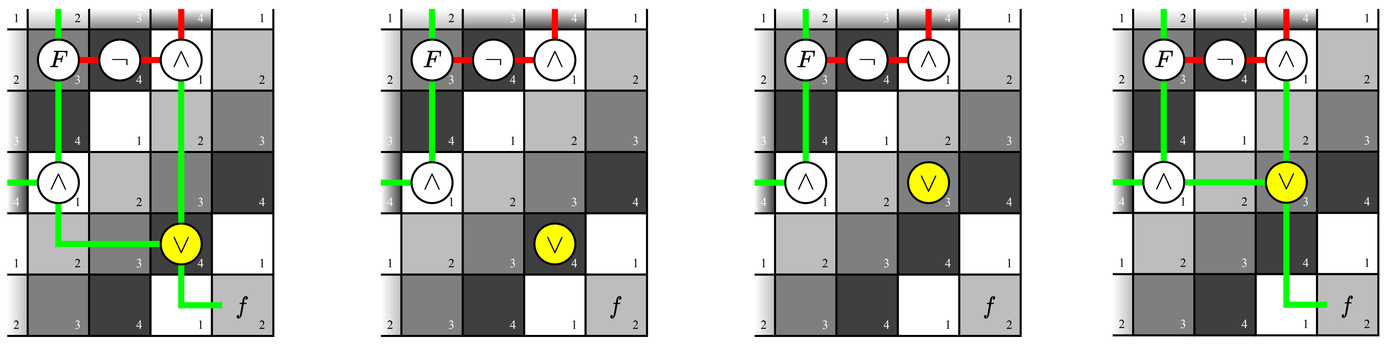
Co-Design: Verilog to atoms



15% area reduction over the best known automatically generated layout for the benchmark function *cm82a*

Post-Layout Optimization: Gate Relocation

Move gates to better positions to save area



1. Choose gate for relocation.
2. Remove wiring to connected gates.
3. Relocate to better position.
4. Rewire gate based on new position.

52% (20%) average area reduction compared to *ortho* (*NanoPlaceR*)

Open Source Tools

fiction

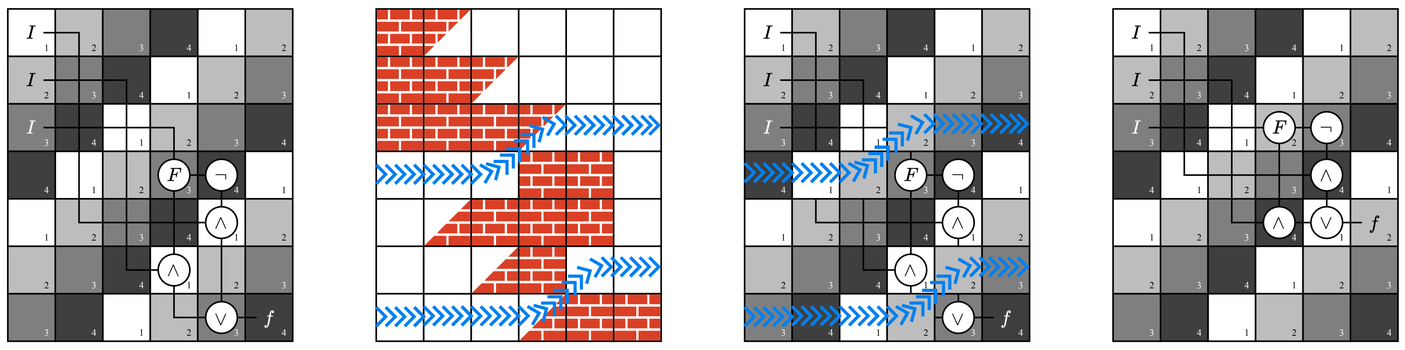
MNT Designer

MNT NanoPlaceR

MNT Bench

Post-Layout Optimization: Wiring Reduction

Wires have the same cost as gates



1. Layout for the 2:1 MUX created by the heuristic *ortho*.
2. Added obstructions and two possible cuts for wiring removal.
3. Wires on the cut paths are deleted, leaving behind gaps.
4. Resulting gaps are closed by compacting the layout.

32% average area reduction compared to *ortho*

Accomplishments

- **1 Journal Publication (TCAD)**
- **10 Conference Publications + 3 under Review**
  2 x NANOARCH 23 2 x DATE
  3 x ASP-DAC 2025 (+ 3 under review)
  1 x NANOARCH 23 1 x ISQED
  1 x LASCAS 2025
  (nominated for **Best Paper Award**)
- Collaboration with *University of British Columbia*, *Infineon*, and *Sony AI*
- Creator and maintainer of 3 open-source frameworks
- Contributor to the open-source framework *fiction*
- (Guest-) Lecturer at *TUM*, *University of Bremen*, and *UFMG*

Chair for Design Automation
TUM School of Computation, Information and Technology
Technical University of Munich
https://www.cda.cit.tum.de