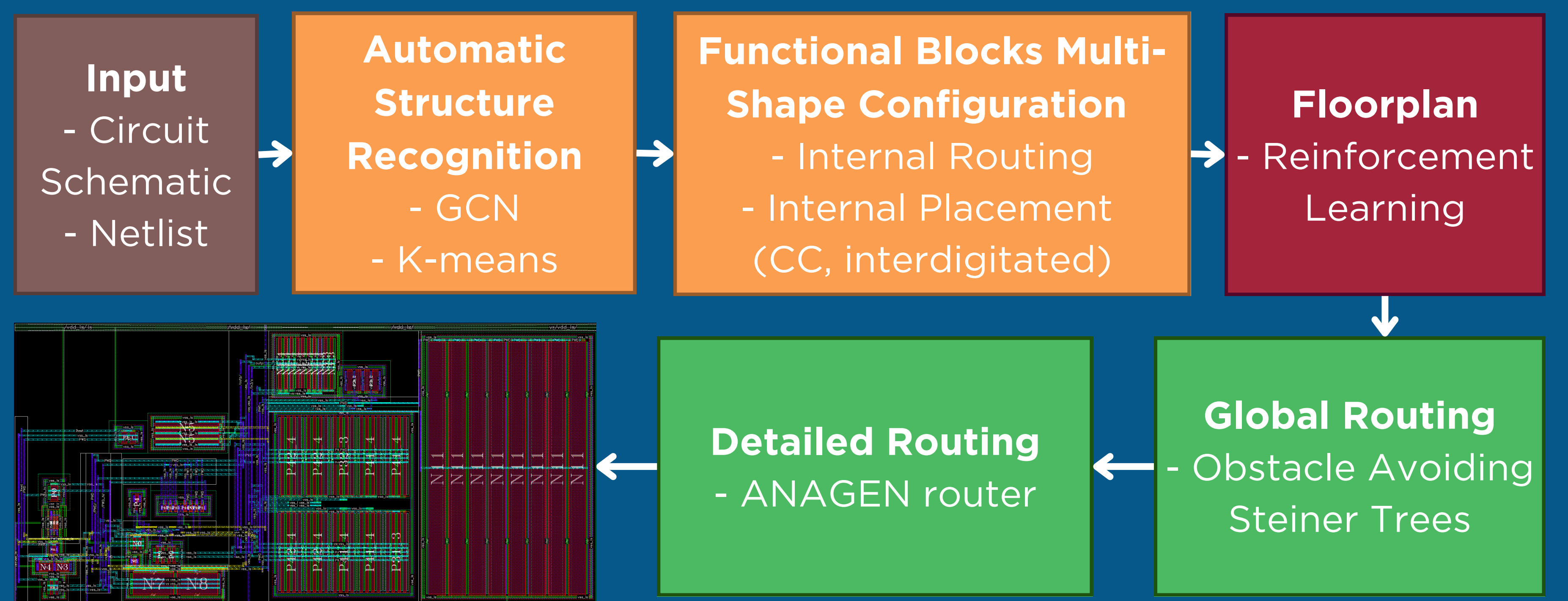


1 Introduction

- Layout of analog circuits is a complex task that heavily relies on human expertise
- Placing components (**floorplanning**) and connecting them (**routing**) requires weeks of interactions among engineers
- Past methods based on metaheuristics [1] lack of experience reuse
- Can learning-based do better?

2 Overview



3 Methods

Reinforcement Learning (RL) [2]

- Agent decides circuit blocks location
- Optimizes for minimum **area** occupation and proxy wirelength (**HPWL**)
- Accounts for topological constraints satisfaction (**symmetry, alignment**)
- Can be used alone or combined with Simulated Annealing (SA), Relational Graph Neural Networks (**R-GCN**)

Obstacle Avoiding Steiner Trees (OARSMT)

- Minimum **wirelength**
- **Obstacle** avoidance guarantee
- Full compliance with **ANAGEN** [3]

5 Conclusions

What we understood

- **RL** based floorplanning algorithms can **optimally** handle topological **constraints**
- Leverage of past experience and R-GCN provides strong **transfer capabilities**
- **OARSMT** effectiveness in outlining routing **guides** for ANAGEN router

What we are seeking

- Feedback from **noise** and **parasitics**
- **Performance** related **metrics**

4 Results

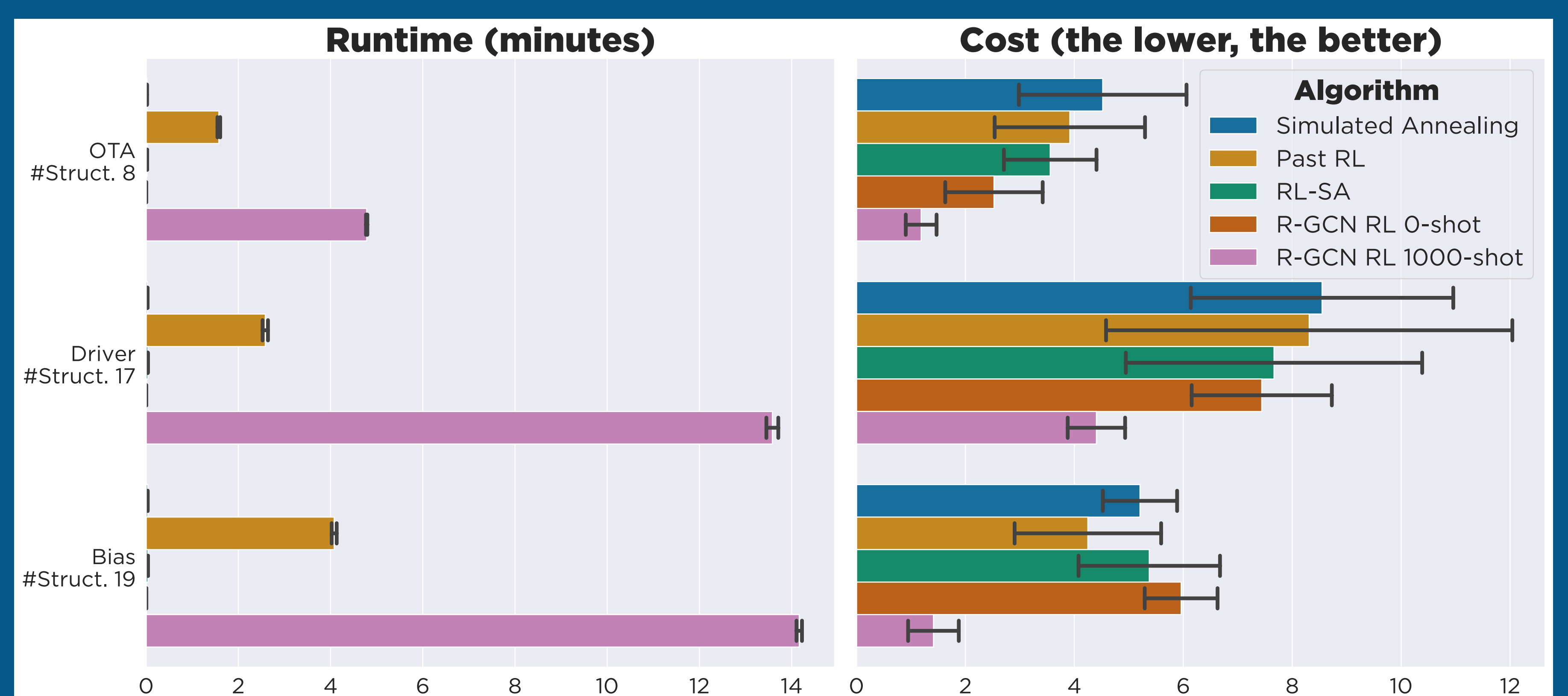


Fig. 1: Runtime and floorplan cost comparison of metaheuristic vs proposed approaches

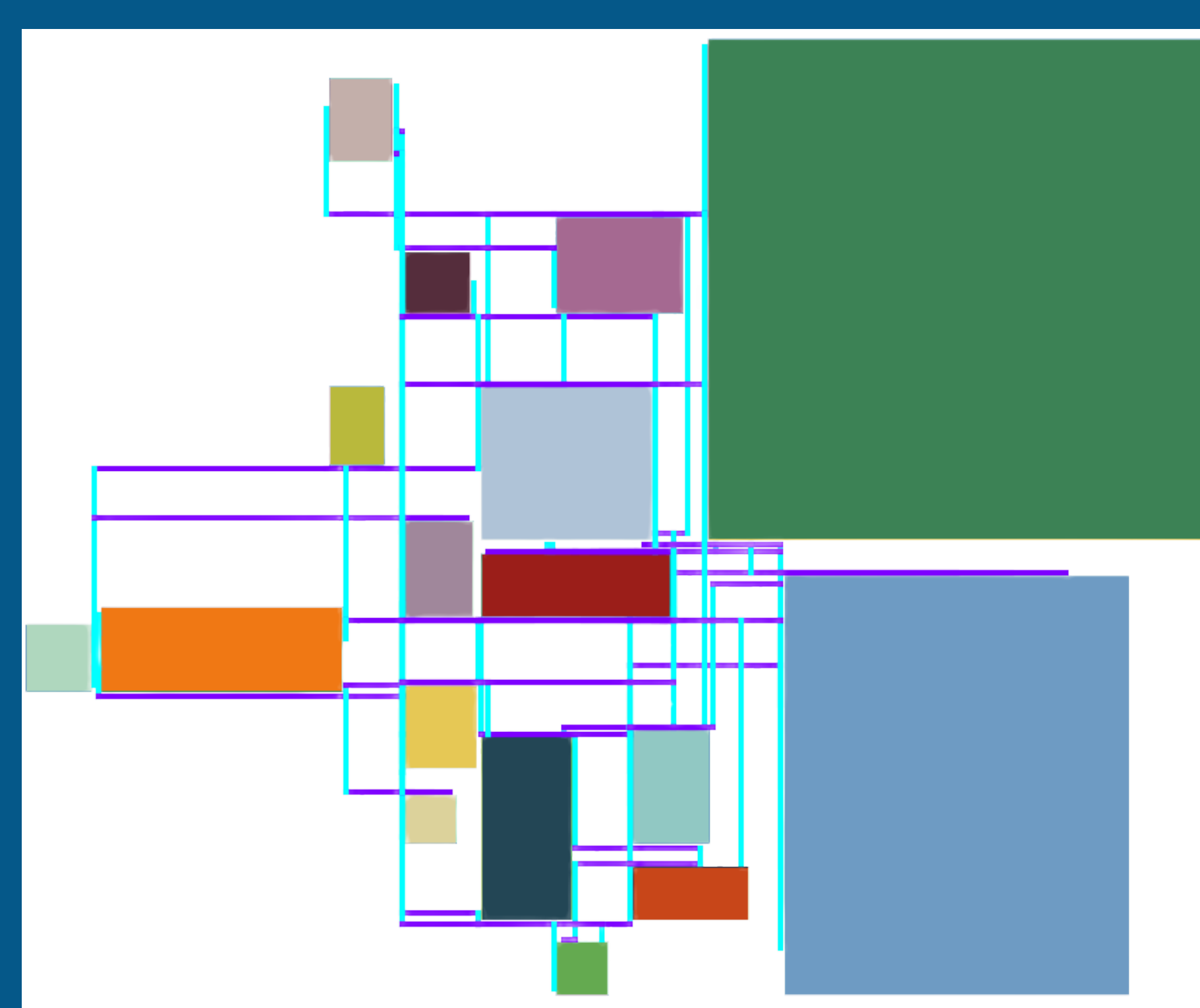


Fig. 2: RL floorplan and OARSMT global routing

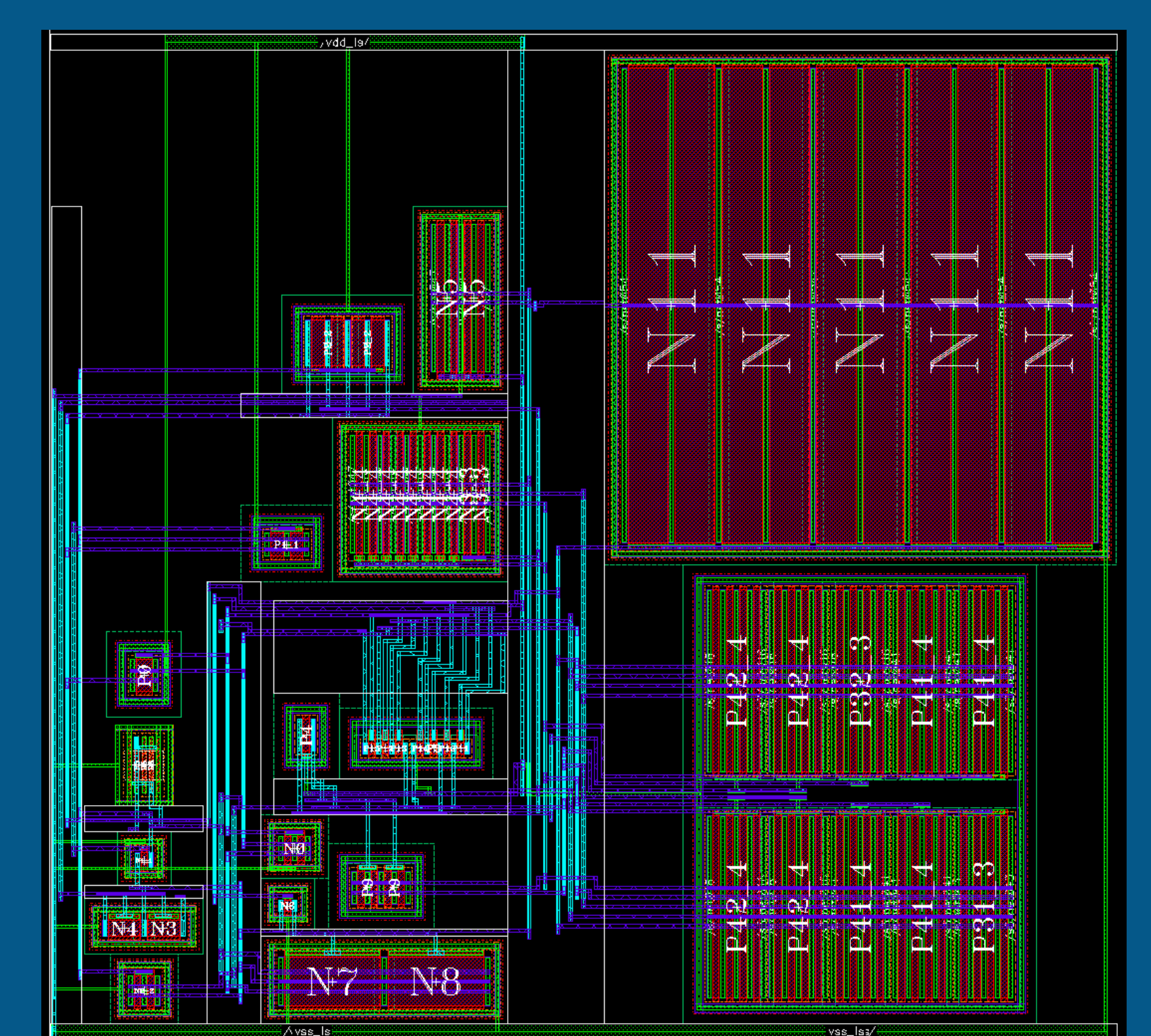


Fig. 3: Resulting layout in Virtuoso

- Cost-wise, learning-based approaches outperform SA
- Layout runtime is reduced by **67.3%** vs manual approach on average
- Pipeline is applicable to diverse circuit types and topologies

References

- [1] R. B. Singh et al. "A review on VLSI floorplanning optimization using metaheuristic algorithms", ICEEOT 2016.
 [2] B. Yang et al. "Miracle: Multi-Action Reinforcement Learning-Based Chip Floorplanning Reasoner", DATE 2024.
 [3] F. Passerini et al. "ANAGEN: A Methodology for ANALog Circuit GENeration", CICC 2021.

Acknowledgments

I am deeply grateful to my supervisor, Luca Bortolussi, for his guidance and support throughout my PhD research. I also extend my sincere thanks to my co-supervisors at Infineon, Mirjana Videnovic-Misic and Husni Habal, and all the other colleagues for their invaluable assistance and encouragement.