

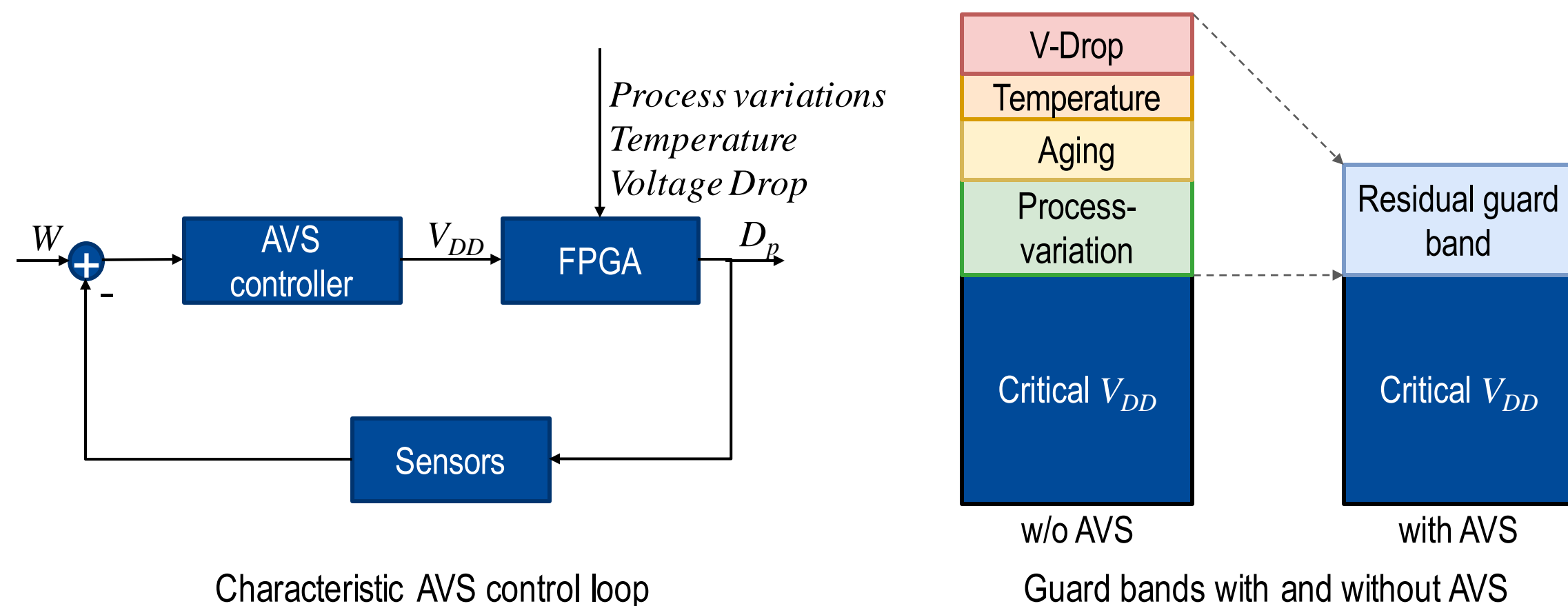
Contributions to Improve the Energy Efficiency of FPGA-based Applications

Specific requirements for AVS on FPGAs

- Sensors that are not based on standard logic gates but on dedicated transistor level designs generally cannot be mapped to the logic resources of an FPGA.
- The special features of FPGA hardware implementations must be taken into account. For example, if the supply voltage is lowered, the integrity of SRAM cells must not be impaired, as these cells define the logical function of the LUT and the routing.
- The critical paths of future application designs are not known to the manufacturer of the FPGA. Consequently, techniques that require knowledge of both the application design and the process technology used cannot be applied.

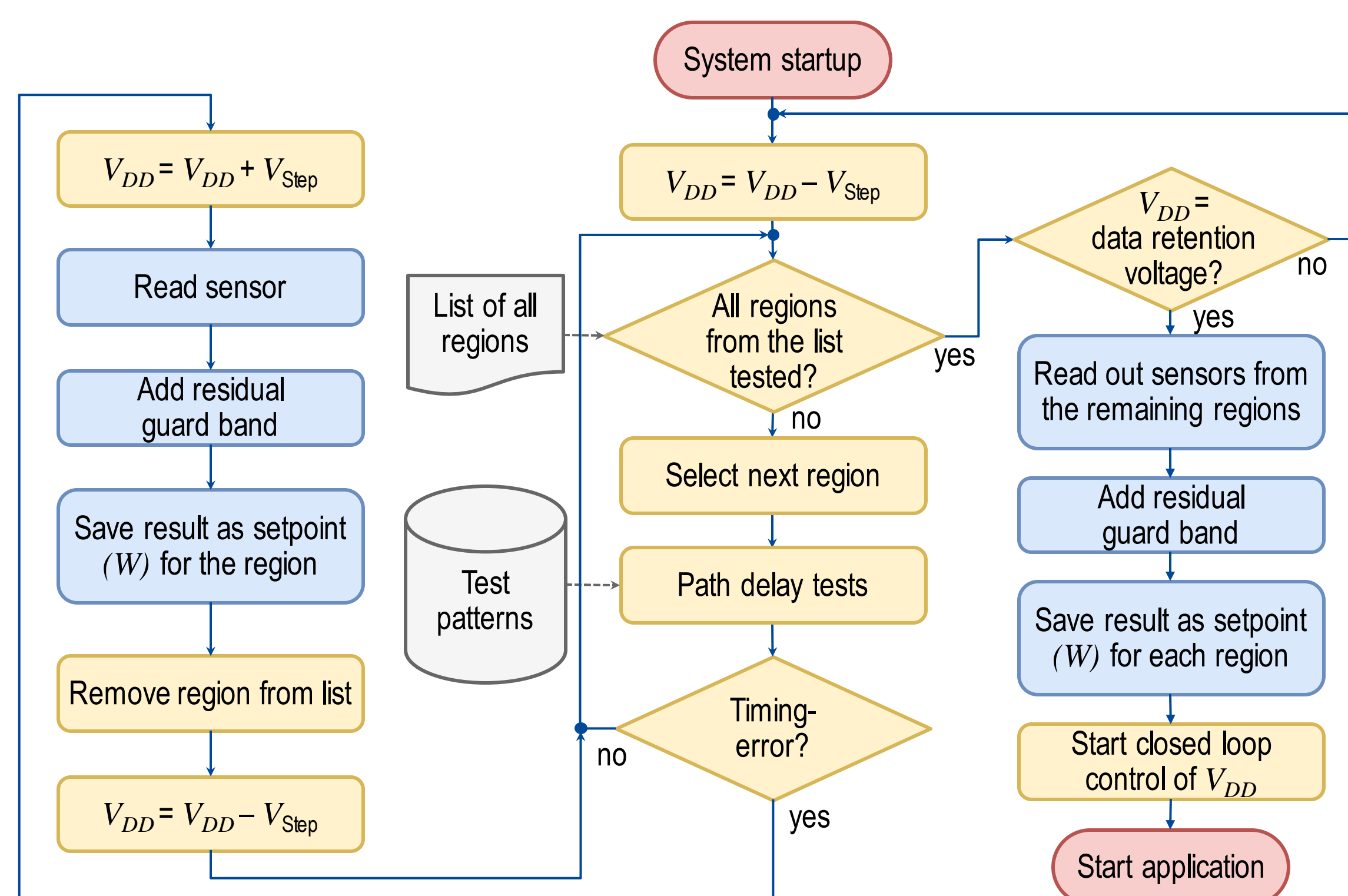
Sensor Calibration

How to determine the setpoint W of the AVS control loop?



We propose an offline calibration procedure:

- Conduct path delay tests at gradually lowered V_{DD} to determine the critical supply voltage
- Determine and add a residual guard band for fast fluctuations
- Divide the FPGA in regions with one sensor per region
- Applicable to arbitrary online sensors; we use ring oscillators



Sensor Placement

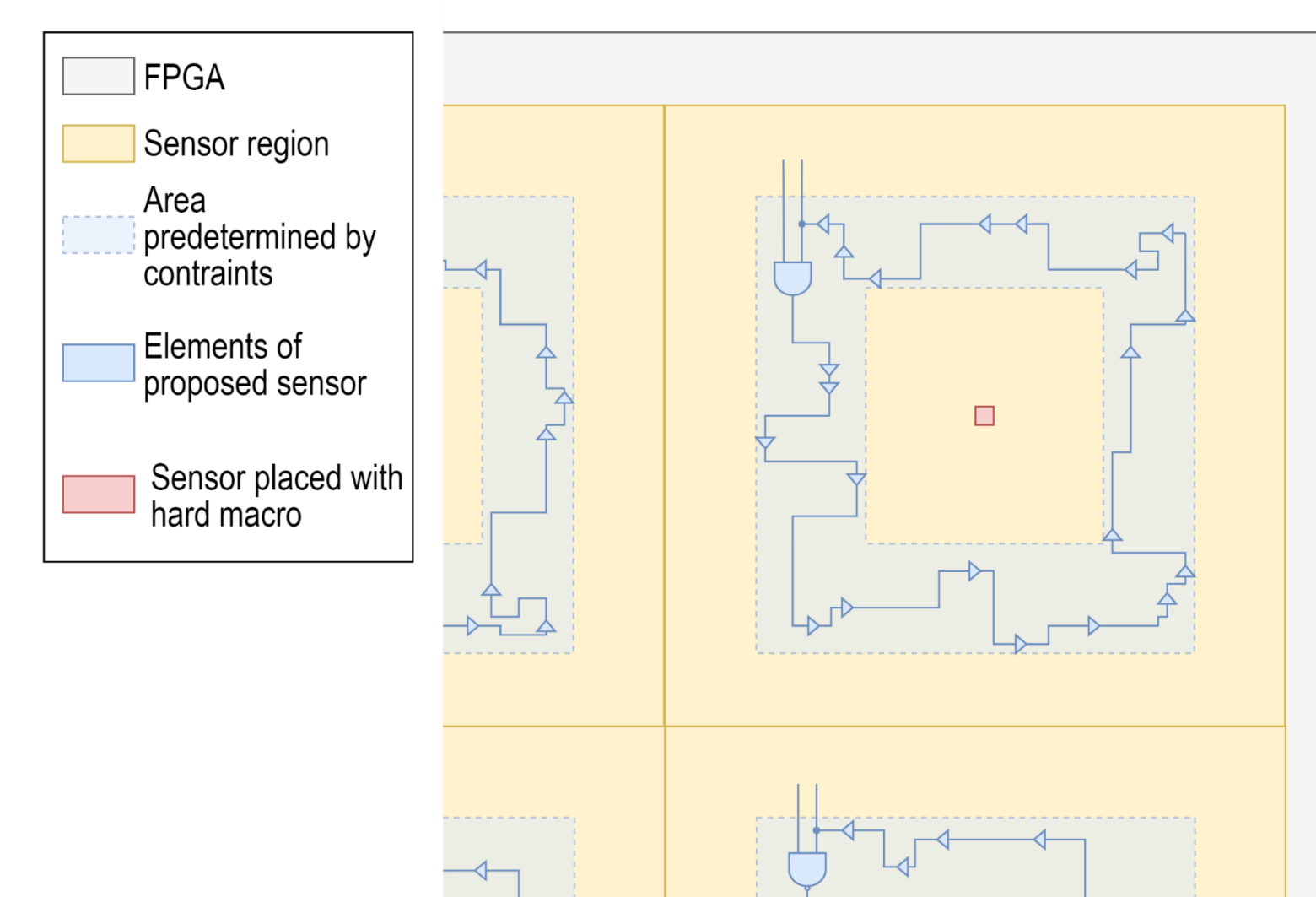
Prevalent method of sensor placement on FPGAs

- Every single instance of the sensor design is placed and routed identically by means of hard macro, directed routing or manual placement
- Authors frequently try to achieve a high spatial and temporal resolution



- FPGA resources are blocked for the sensor and cannot be used for the application design
- Difficulty to place the sensors on multiple types of FPGAs
- Sensors need to be small and tend to use very few global routing resources; Sometimes global routing is even avoided completely

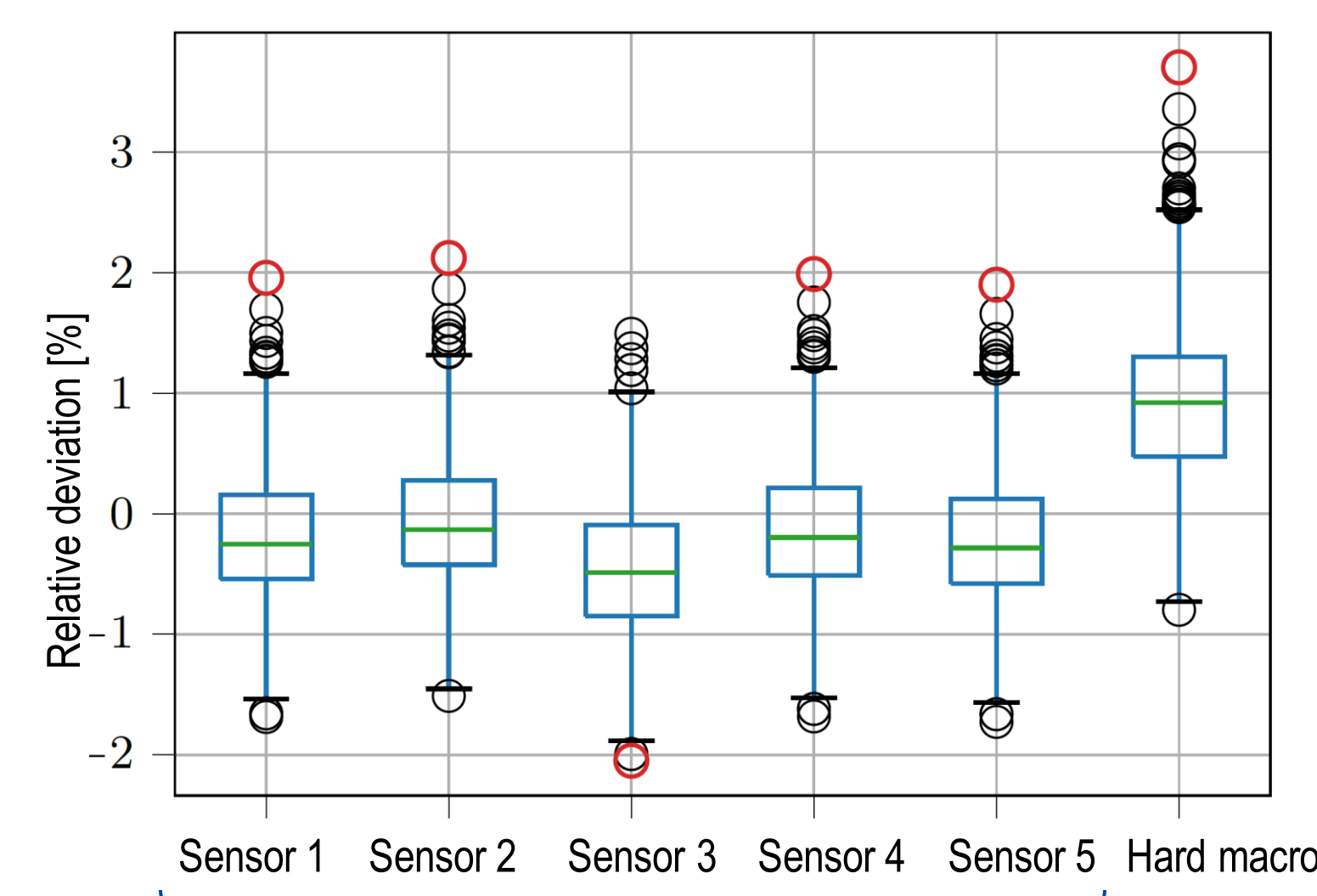
Hypothesis: Calibration allows to omit the placement as hard macro



Schematic comparison of sensor placement using hard macro and the free placement within an area proposed in this work; published in [2]

Idea: Only constrain the basic shape and a region for each sensor element

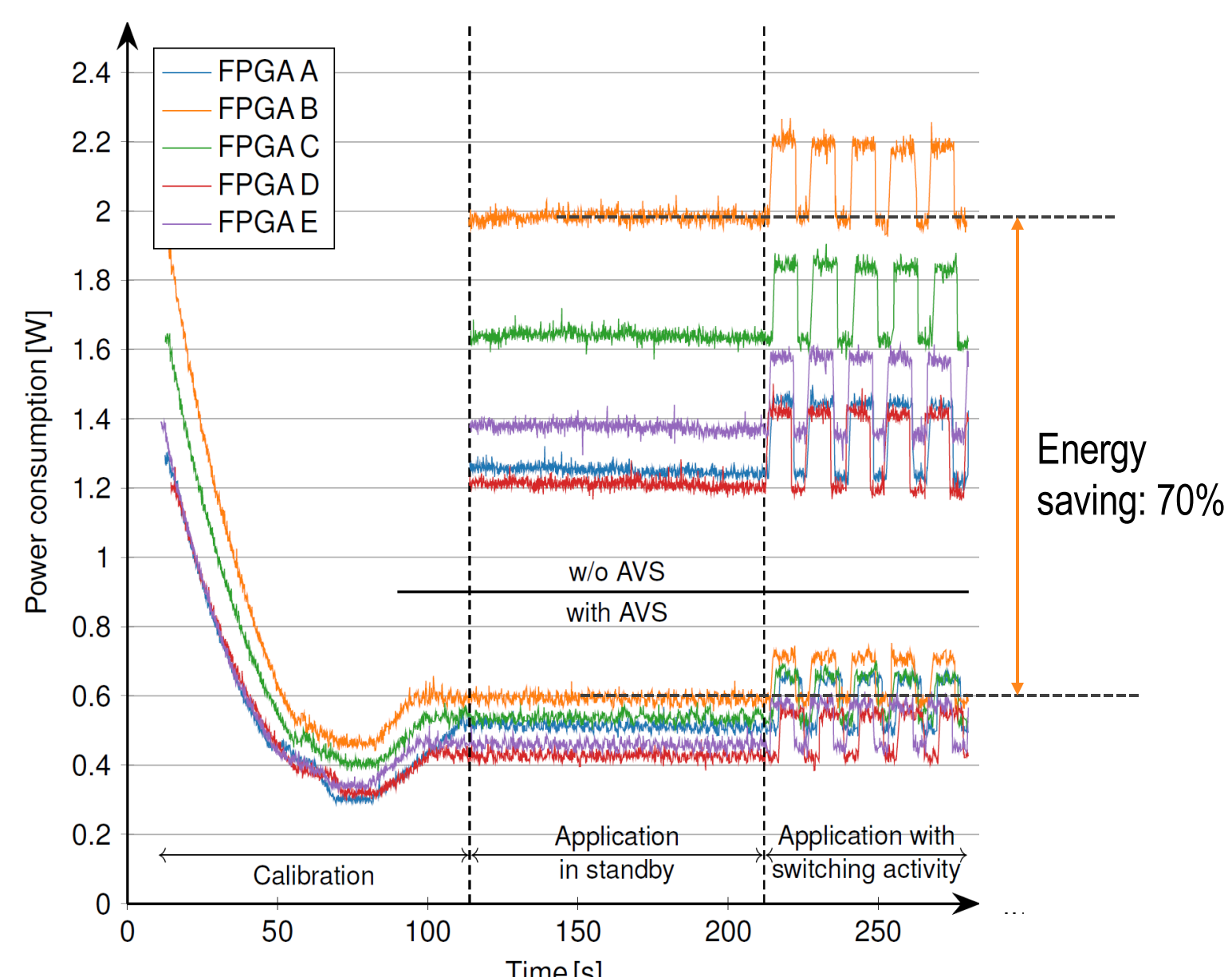
- Each element of a sensor is constrained with LOC...RANGE constraints
- Sensors differ in the details of their shape, i.e., the placement of their elements



Exemplary evaluation of a sensor region; Largest relative deviation of each sensor in terms of absolute value highlighted in red; published in [2]

Our experiments show that, given a suitable sensor calibration, it is possible to use relaxed constraints for AVS sensors

Results



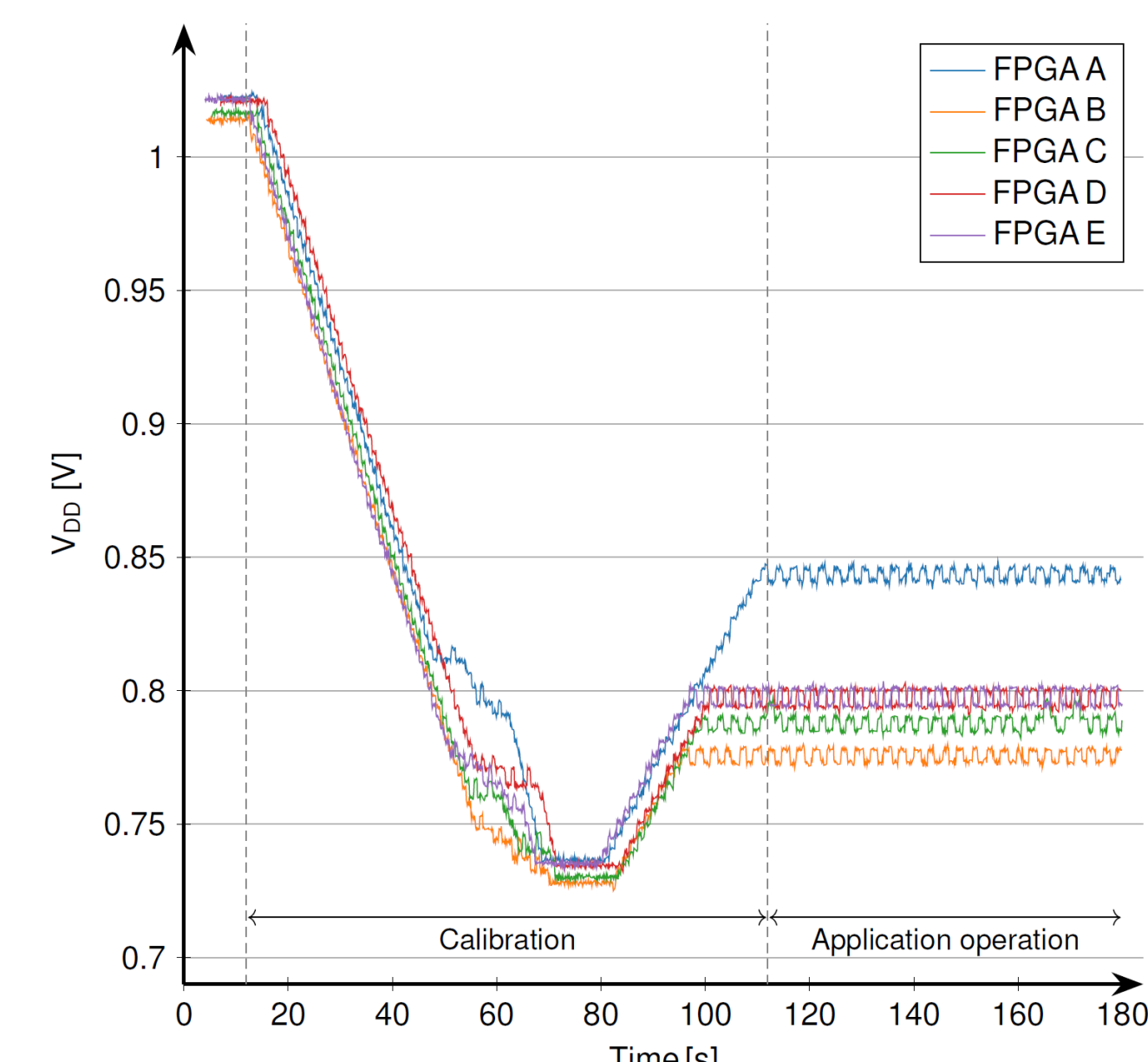
Power consumption with and without the proposed AVS; adapted from [1]

Experimental Setup:

- Overall AVS approach tested on 5 identical FPGA Boards (Xilinx ML605)
- Two application designs:
 - small, with low switching activity (shown in figures)
 - Big with very high switching activity

Results:

- V_{DD} can be reduced by an average of 21%
- Energy Savings of 51%-66% depending on the application design
- Applies a residual guard band
- Calibration covers variation of the clock tree
- Calibration covers aging



Monitored V_{DD} with our AVS approach on five identical FPGAs; adapted from [1]

[1] C. Niemann: Beiträge zur Steigerung der Energieeffizienz FPGA-basierter Anwendungen. PhD thesis. Universität Rostock, 2023

[2] C. Niemann, M. Rethfeldt, D. Timmermann: „A Novel Strategy for Flexible Placement and Routing of AVS Sensors on FPGAs“ In: 2023 33rd International Conference on Field-Programmable Logic and Applications (FPL), 2023, pp. 339–344