

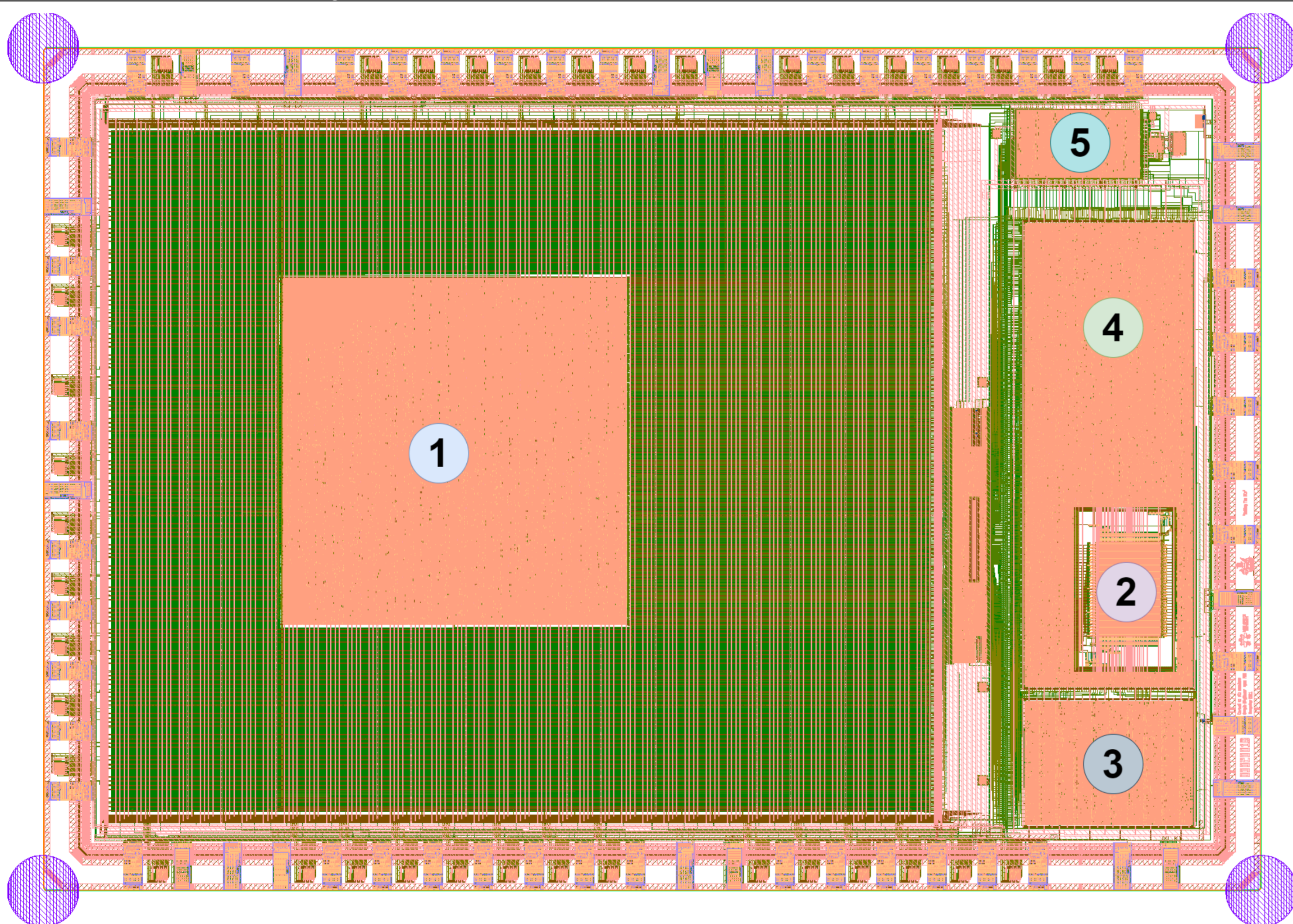
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Introduction

Until very recently, custom **Application-specific Integrated Circuits (ASICs)** designs were very rare for small and medium companies due to the overall **prohibitive cost** of their production, which could only be afforded by few large companies. This high cost comes mainly from the very expensive commercial **Electronic Design Automation (EDA)** tools used in the chip designing process. However, recently there have been government-funded initiatives such as DARPA's **OpenLane/OpenROAD** which supported the production of a fully **open-source** EDA toolchain from hardware description languages (HDL) down to GDSII files.

In this work, we introduce the design, implementation and first bring-up results of **Space Shuttle**, an open source test vehicle for the reliability assessment of the **SkyWater 130nm PDK**, and the evaluation of the Open EDA toolchains for space designs.

Space Shuttle Architecture

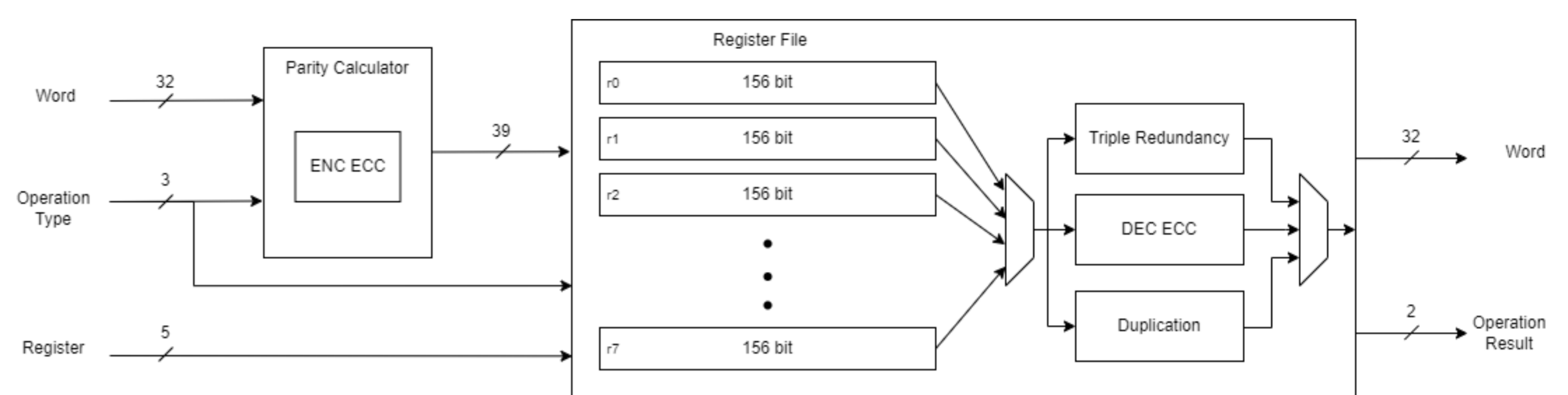


The ASIC is divided in two main areas, the user area ① and the harness area ②,③,④,⑤.

Our design was implemented in the user area with the following features:

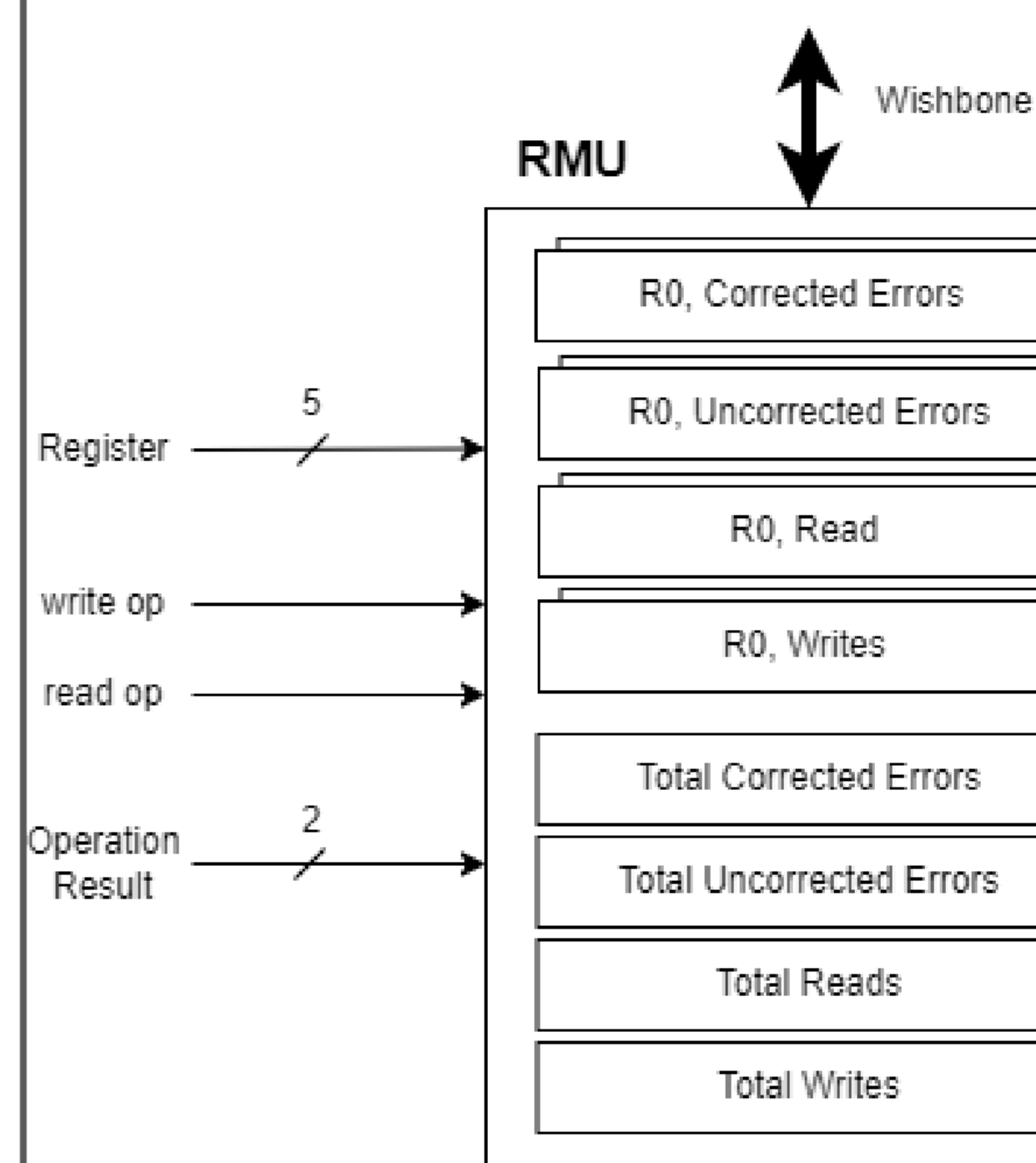
- A register file with 32 registers, each 32-bit wide, implemented with flip-flops, organised in 8 banks which can be used in parallel.
- 4 different protection mechanisms and one non-protected storage mechanism each of which can be enabled selectively and combined with others:
 - Error Correction Code (ECC) SECDEC
 - Triple Redundancy
 - Shadow Register [1]
 - ECC Shadow Register [2]
 - No protection
- Duplicated Reliability Monitoring Unit: Individual 32-bit counters per register, reporting the number of write and read operations performed.
- The output of the memory and the result of the verification is sent to the GPIO pins of the chip.

Register File Design



A register file is a performance critical circuit of processors. For this reason, Space Shuttle has a single cycle read and single cycle write latency. However, due to the area constraints imposed by the limitations of the EDA tooling, we had to limit the design to a single read or write port. Depending on how the user wants to store the data, the different modules either transform the data (ECC) or pass them directly to the register file.

RMU Design

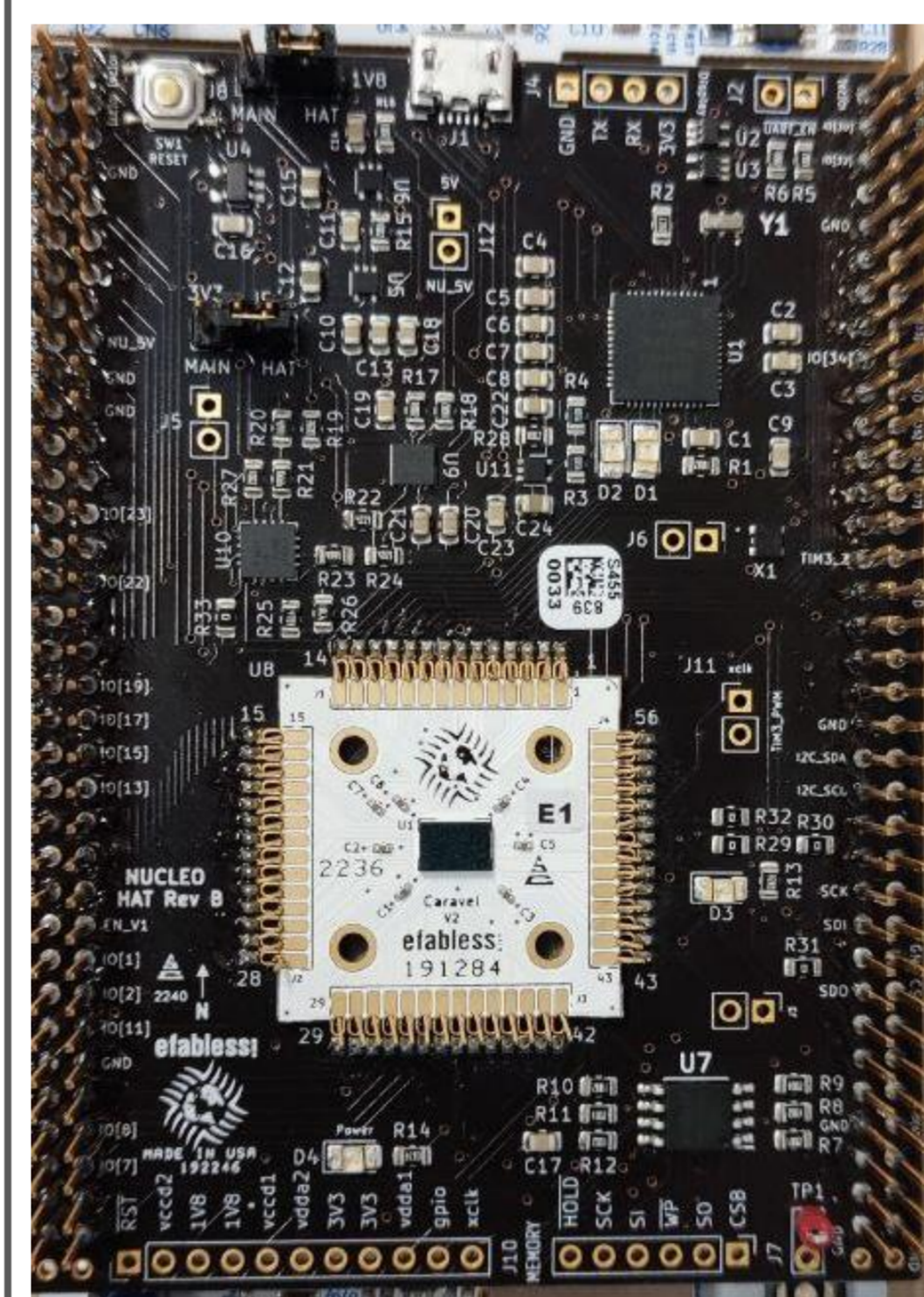


The reliability monitoring units (RMUs) is a set of 32 bit counters to track the reliability of the register. Types of measured events:

- Corrected errors
- Uncorrected errors
- Reads
- Writes

These events are counted in total and per each of the 32 registers.

Evaluation



The design was taped out in Google sponsored MPW2 in 2021[3]. The chips arrived end of February 2023.

During manufacturing was discovered by the OpenLane team that all of the chips suffer from hold violations so in order to mitigate those effects the chip was undervolted from the nominal 1.8V to 1.6V.

We verify the design in simulation and in silicon by applying fault injections using software commands.

Conclusion and Future Work

Both our pre-silicon simulation results as well as our postsilicon verification with fault injection indicate that Space Shuttle is fully functional under normal operation conditions. Next, Space Shuttle will be evaluated under radiation testing.

[1] M. Nicolaidis, "Time Redundancy based Soft-error Tolerance to Rescue Nanometer Technologies,"
 [2] A. Bouajila et al, "An Architecture and an FPGA Prototype of a ReliableProcessor Pipeline Towards Multiple Soft-and Timing Errors,"
 [3] I. Rodriguez, "Space Shuttle Test Repository," 2021. [Online]. Available: https://github.com/jaquerinte/caravel_radiation_harden