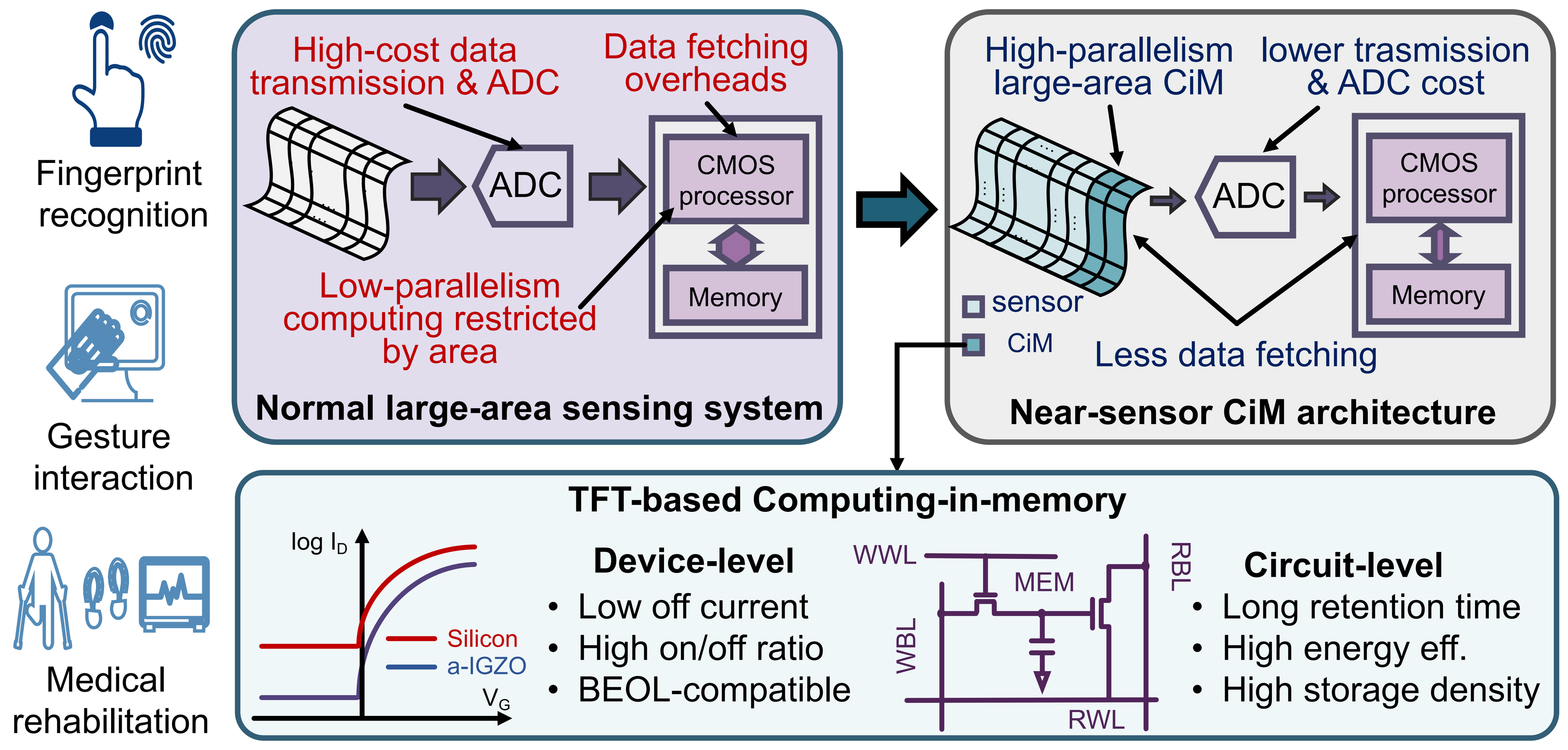
Thin-Film Compute-In-Memory Circuits and Systems for Large-Area Sensing Applications

Jialong Liu (Advisor: Huazhong Yang and Xueqing Li)
Department of Electronic Engineering, BNRist, Tsinghua University, Beijing, China
E-mail: liujl19@mails.tsinghua.edu.cn

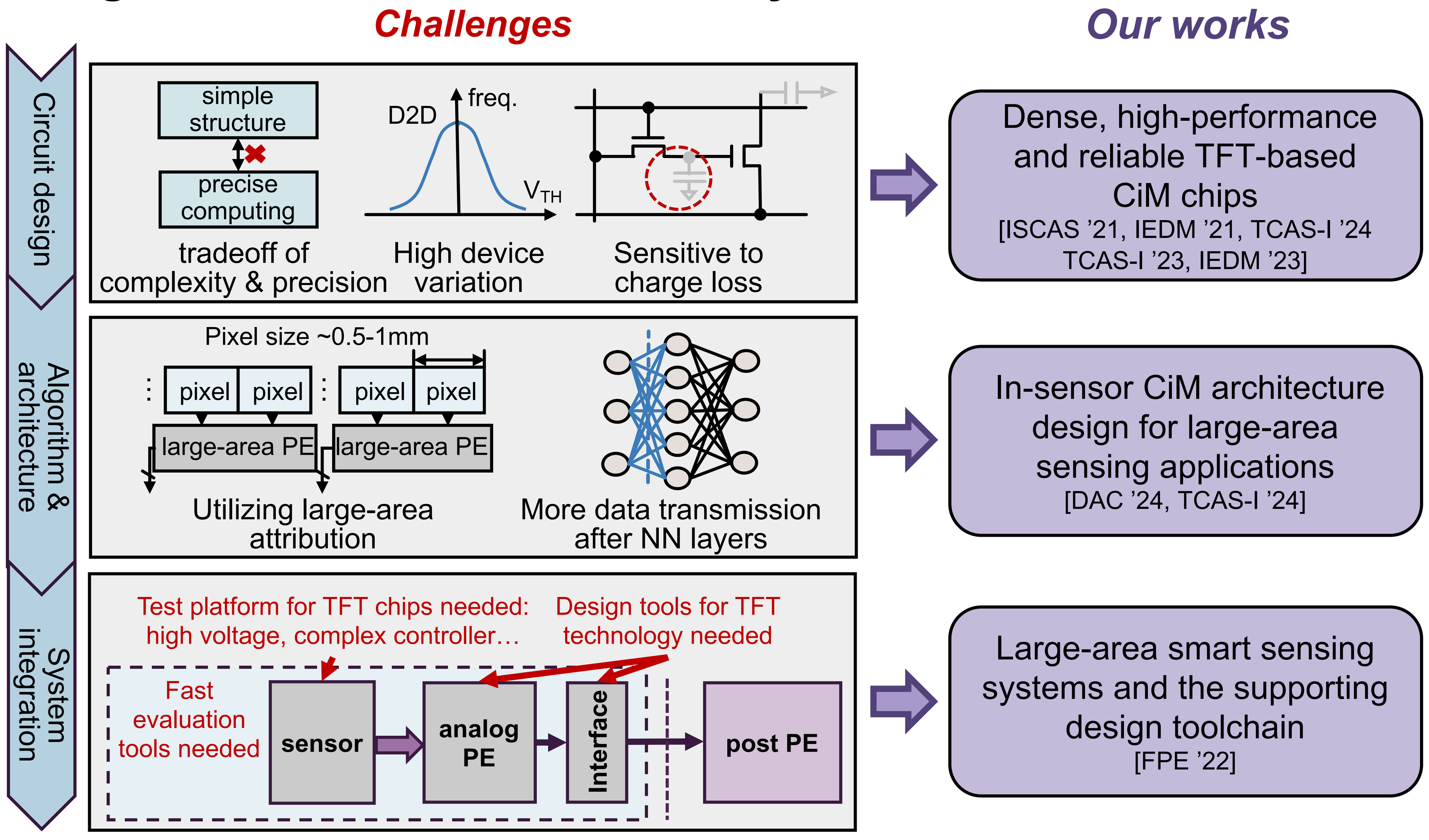
Process more data in emerging sensing scenarios

■ Thin-film transistor (TFT)-based in/near-sensor computing

- Large-area integration of sensors, memory and processors
- Ideal candidate for low-power compute-in-memory (CiM)
- Reduction of data transmission & ADC conversion



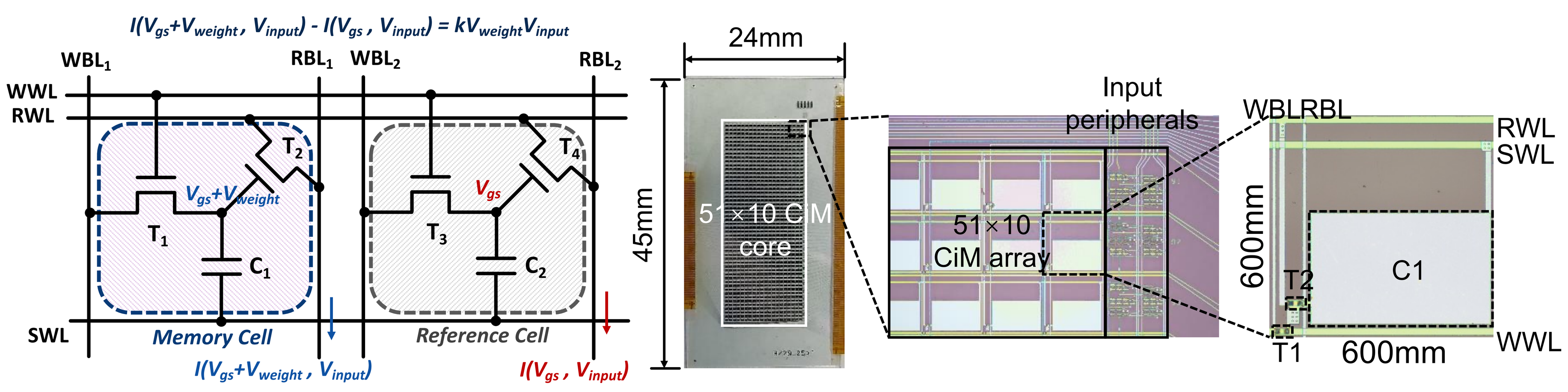
■ Cross-layer exploration with perspectives from circuit, algorithm & architecture and system levels



TFT-based CiM design with device/chip fabrication

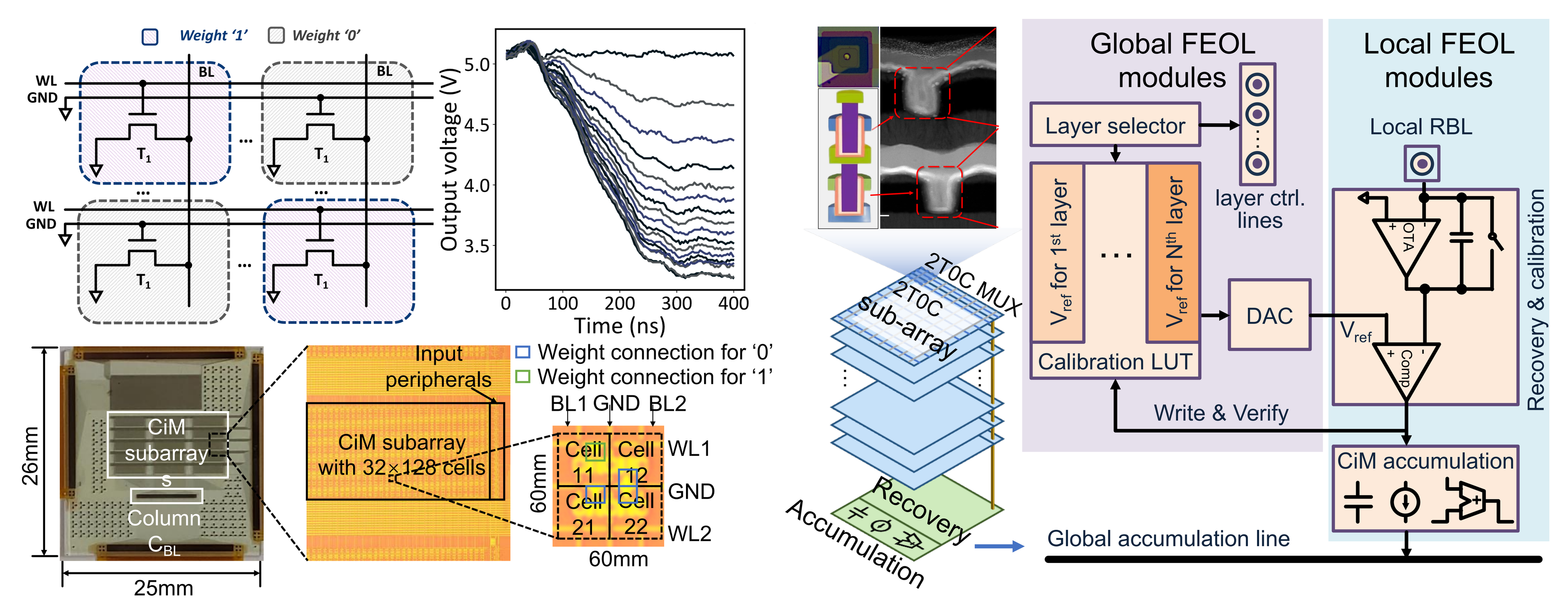
■ Better computing precision (ISCAS '21 [1],TCAS-I '24 [2])

- 51×10 eDRAM CiM array with 8μm IGZO TFT (ret. time ~100s)
- High-precision 64-stage MAC operation with INL<1.5LSB



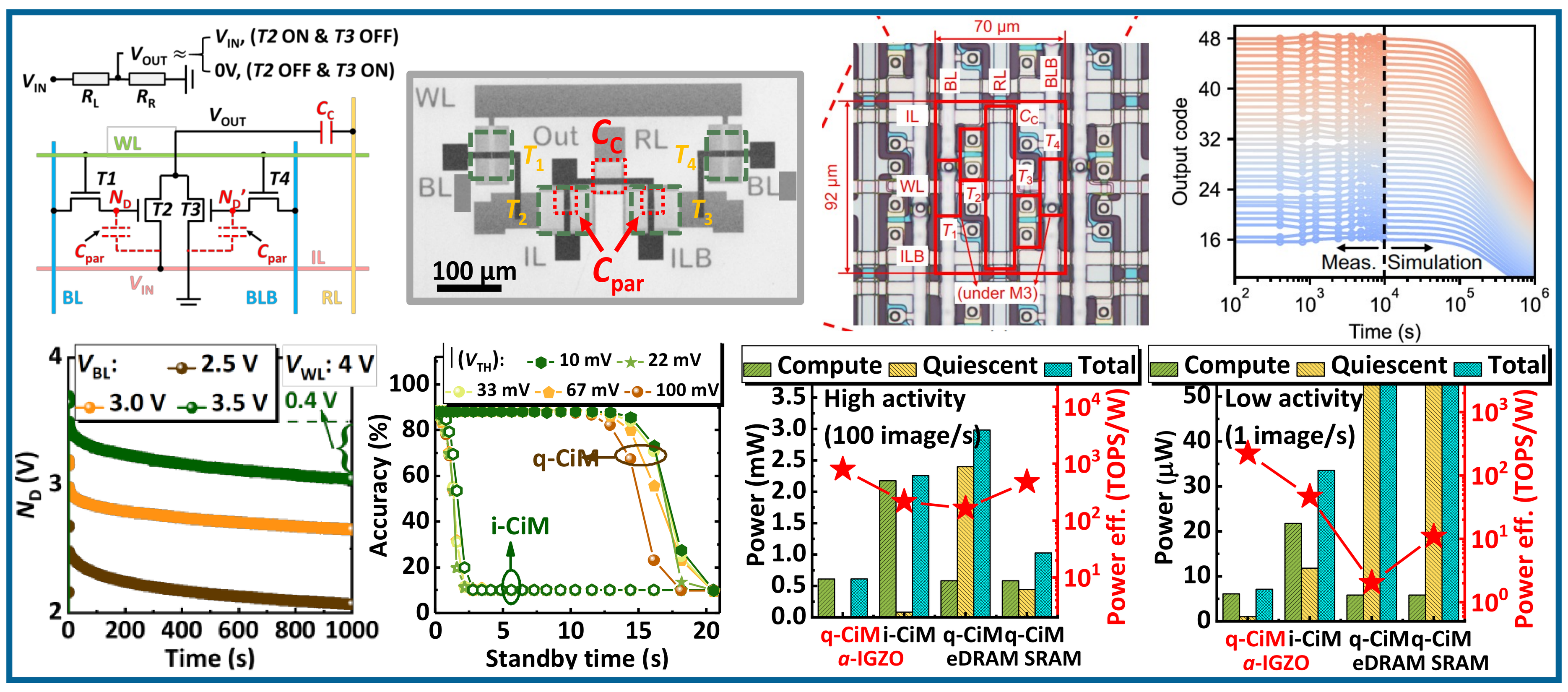
■ Better memory density (TCAS-I' 24 [2], IEDM '23 [6])

- Dense memory cell: 128×32 ROM CiM array with 4μm LTPS TFT
- 3D stacking: 2T0C 4F^2 CAA eDRAM w/ local CiM & recovery units



■ Better robustness & retention (IEDM '21 [3], TCAS-I' 23 [5])

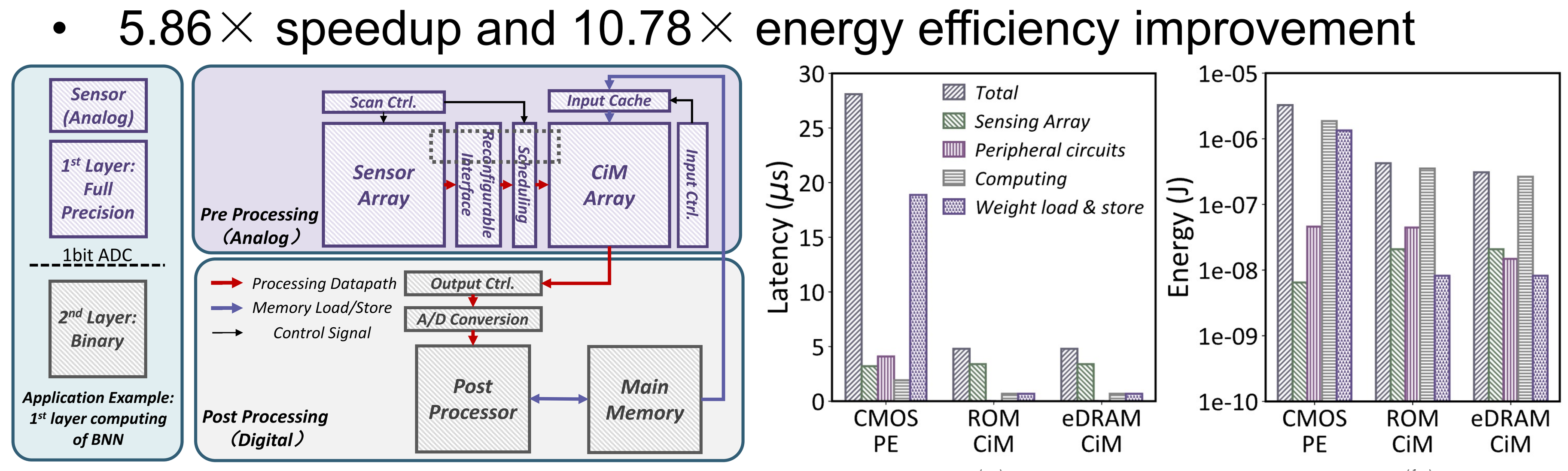
- Device & chip demonstration of charge-domain eDRAM CiM
- Great robustness to PVT-induced variation & charge leakage
- Charge-domain computing without DC power



Architecture design for large-area smart sensing

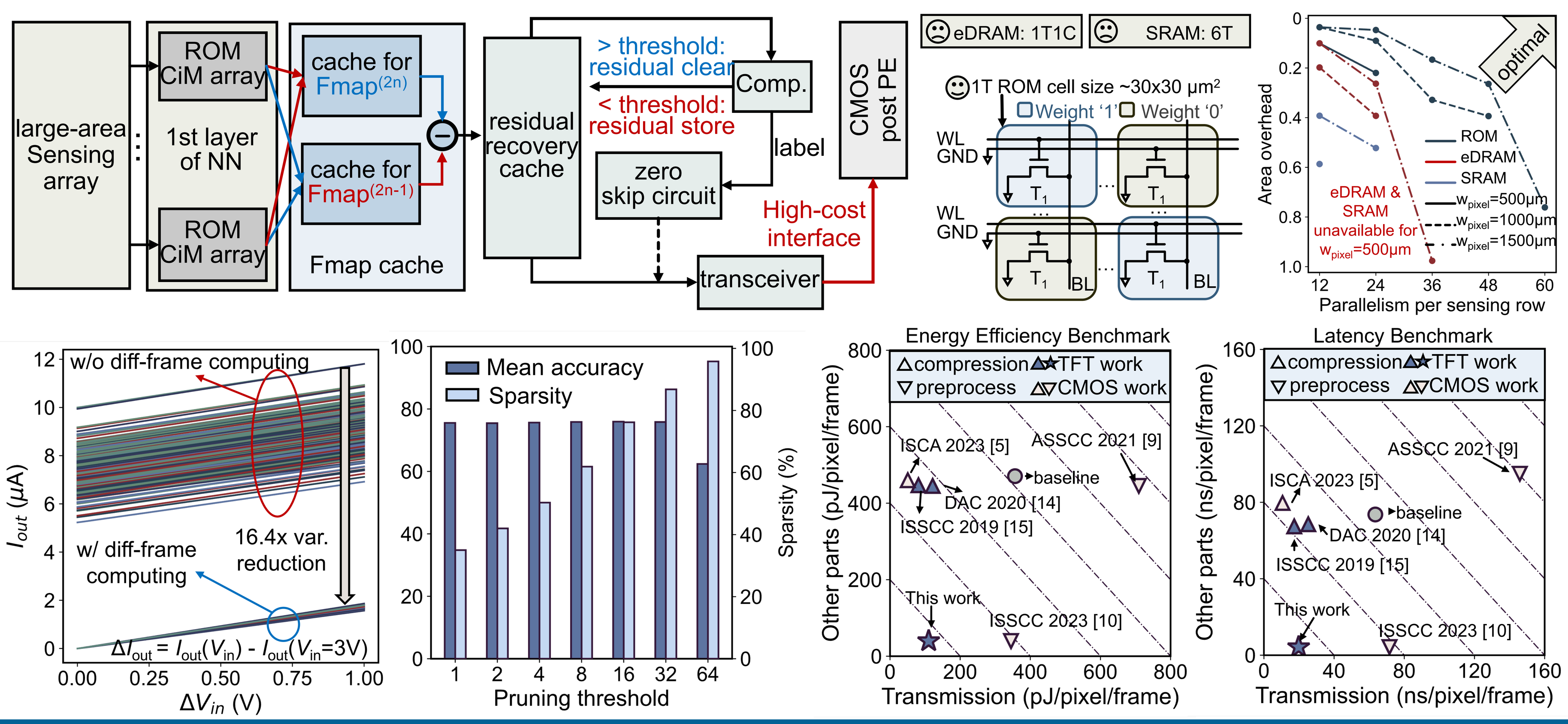
■ Implementing 1st layer of BNN for data transmission/ conversion reduction (TCAS-I '24 [2])

- Replace high-precision ADC with simple comparators
- 5.86× speedup and 10.78× energy efficiency improvement



■ Processing & output compression for general NN models (to appear at DAC '24 [4])

- Differential-frame computing for high reliability and output sparsity
- Bio-inspired pruning to increase sparsity by 30% on average
- Simultaneous acceleration and data compression with 3.85× speedup and 5.10× energy efficiency improvement



Toolchain for TFT-based system integration

Simulator
Behavior-level in-pixel/near-sensor computing simulation

Test platform
Multi-channel large-scale array measurement for high-voltage TFT chips

Design tool
Circuit Simulation/ DRC/LVS/PEX for TFT technology

Literature survey [7]
TFT-based CiM survey on process/circuits/ system/applications

Credits announcement

- In work [3], device fabrication is credited to Prof. Xiao Gong's group; in work [6], device fabrication is credited to Prof. Di Geng's group. Chip fabrication in [2][5] is credited to TIANMA Semiconductor Company.
- The presenter takes the main credits in [1][2][3][4], and is also involved in [5][6][7], which are mainly credited to Wenjun Tang, the presenter's colleague.
- The presenter and Wenjun Tang contribute equally to the toolchain for TFT-based system integration.

Acknowledgement: This work was supported in part by the National Key Research and Development Program of China under Grant 2019YFA0706100; in part by NSFC under Grant U21B2030, Grant 92264204 and Grant 82151305.

References: [1] J. Liu *et al.*, ISCAS 2021; [2] J. Liu *et al.*, TCAS-I 2024; [3] J. Liu *et al.*, IEDM 2021; [4] J. Liu *et al.*, to appear in DAC 2024; [5] W. Tang, J. Liu *et al.*, TCAS-I 2023; [6] W. Tang*, C. Chen*, J. Liu* *et al.*, IEDM 2023; [7] W. Tang, J. Liu *et al.*, FPE 2022.