PhDF.20: Power-supply noise monitoring to evaluate embedded VRMs and Si-backside buried Decaps

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1. Critical issue of power supply noise

- Power Integrity(PI) and Signal Integrity(SI) problem
  - Stability of power supply
  - Quality of signals across circuits
- Security problem
  - Cause of side-channel (SC) leakage

Need to monitor and manage power-supply noise

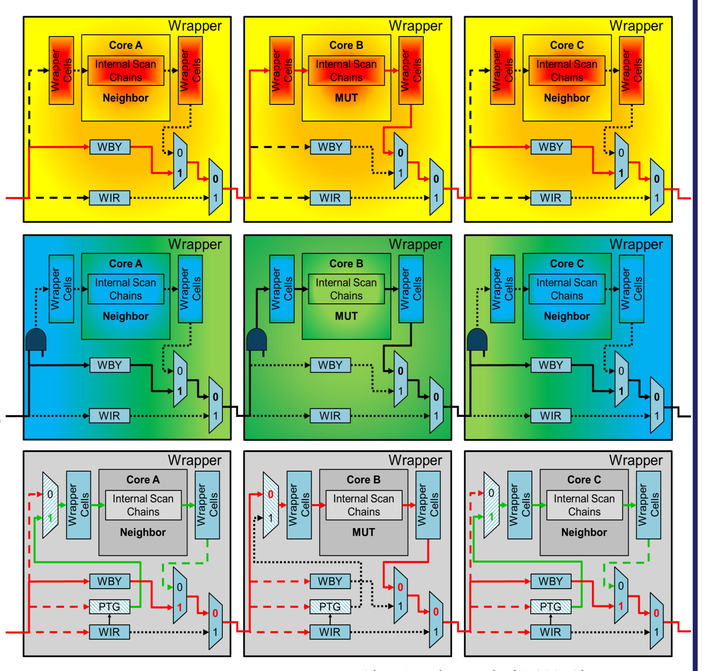
2. On-chip power supply noise monitoring to evaluate embedded VRMs (IEEE D&T 2022)

- Power-supply noise problem in modular testing

(Pessimistic)
- Neighbors randomly toggling
- Excessive IR-drop
  → Too many test fails

(Optimistic)
- Quiet down neighbors
- No IR-drop
  → Too many test passes

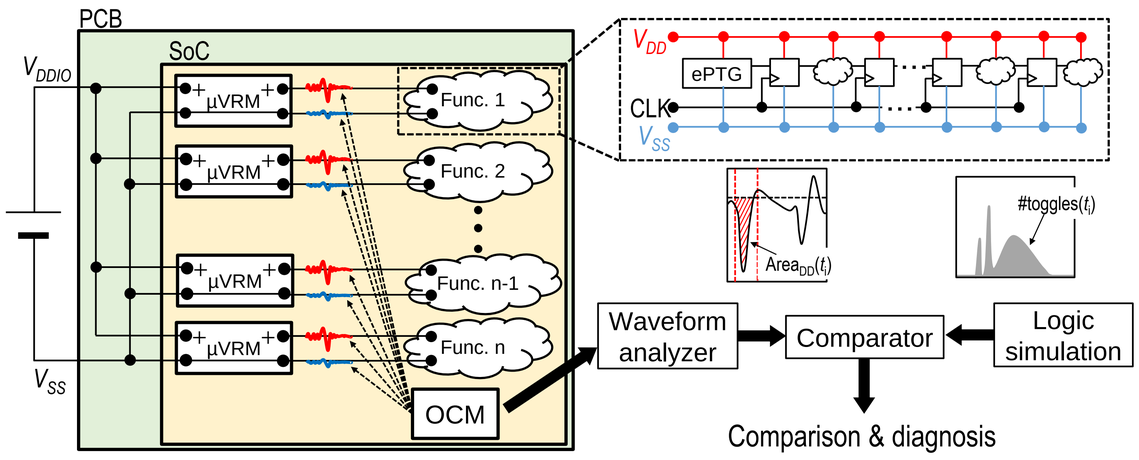
(Realistic)
- Embedded programmable toggle generator (ePTG)
- Realistic IR-drop



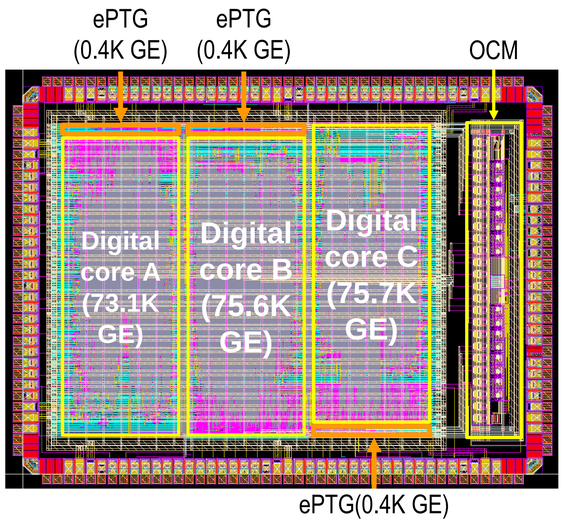
Leonidas Katselas et al., (ITC2018)

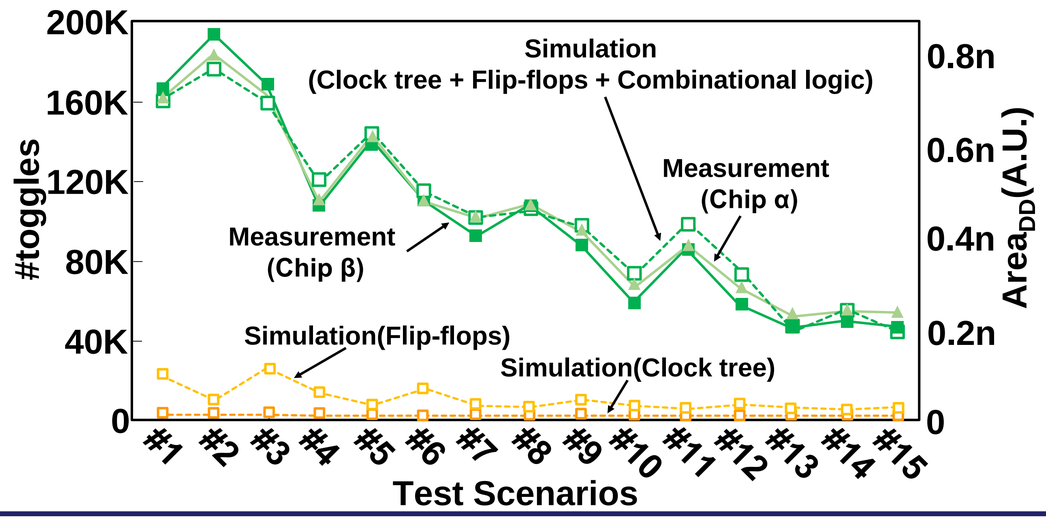
- Toggle generators in VLSI SoC chips
  - Emulating background switching activity during test
  - Equalizing PS noise to improve resiliency against power SC attacks

- Mechanisms to confirms the proper amount of toggles



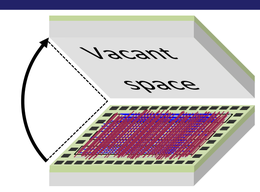
- Prototype chip and evaluation result
  - 180nm CMOS
  - 4mm X 3mm
  - The feasibility of the proposed diagnostic method



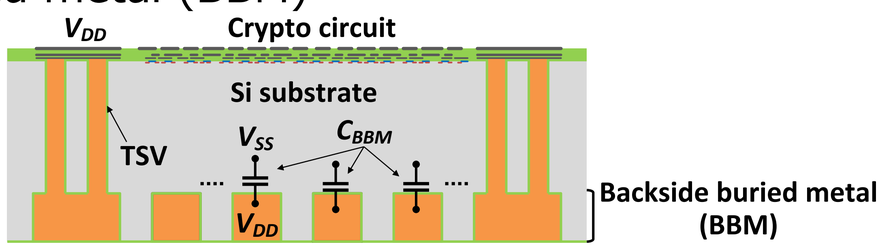


3. Power-supply noise suppression using Si-backside buried decaps (IEEE TED 2021)

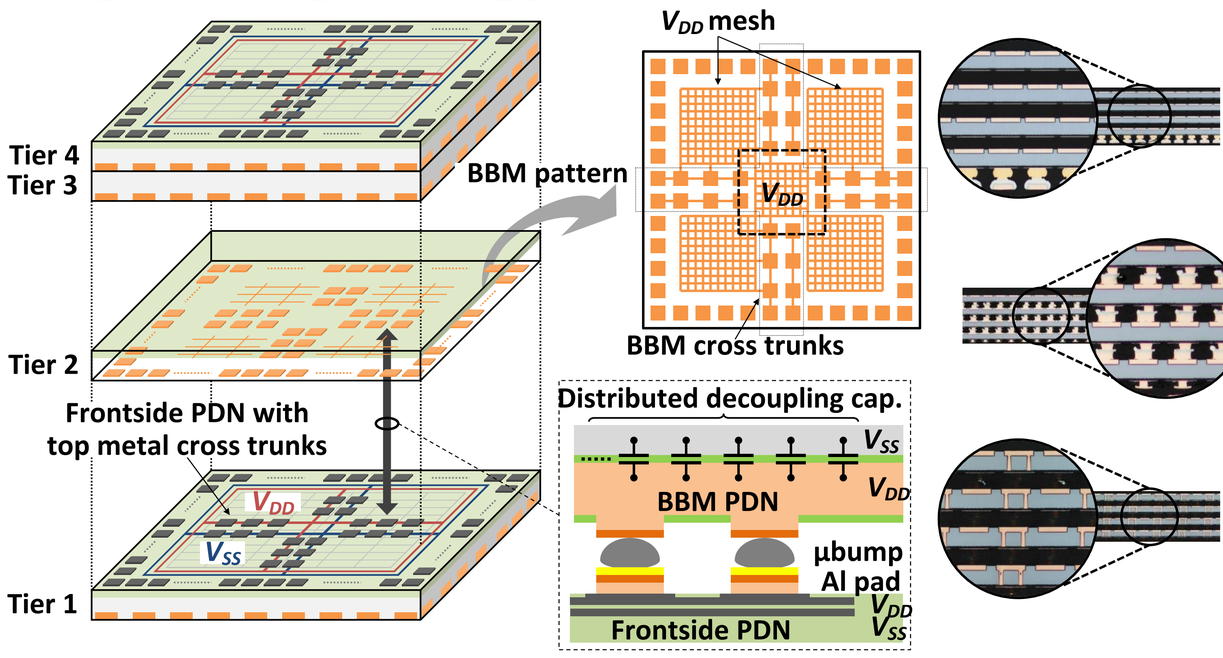
- Utilization of Si-backside
  - Vacant space over front-side circuitry
  - Design constraints free



- CMOS power delivery network (PDN) with back-side buried metal (BBM)



- 3D CMOS PDN with BBM

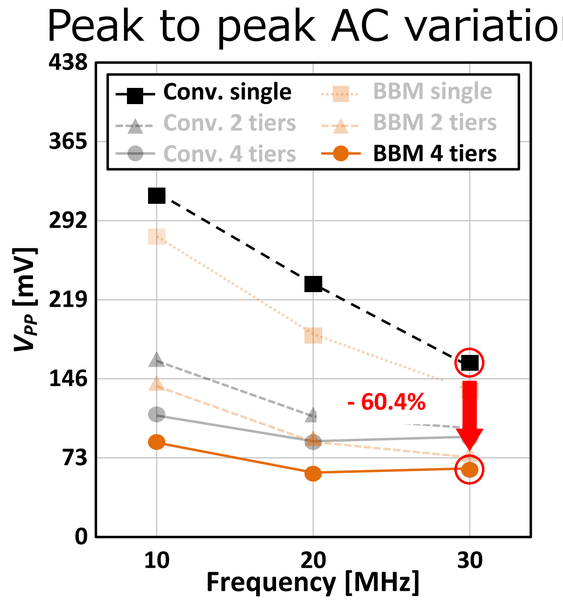


- Comparisons with universal PDK capacitors

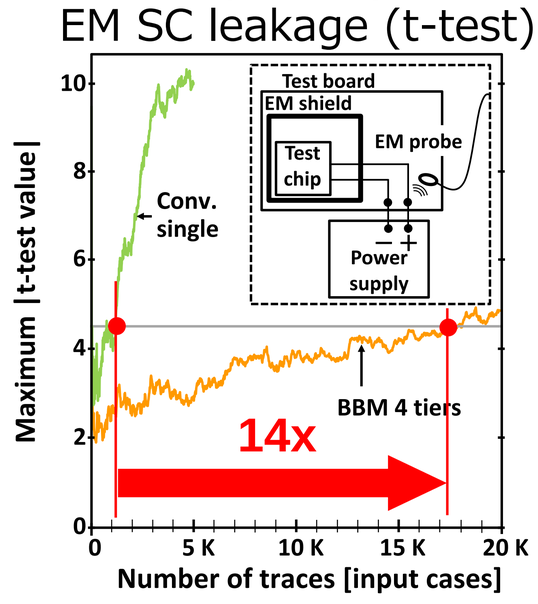
Element	BBM (this work)	MOM (130nm PDK)	MIM (180nm PDK)	Gate cap. (130nm library)
Unit capacitance	Mesh #1 L=15 µm S=35 µm 0.18 fF/µm² / Mesh #2 L=15 µm S=10 µm 0.25 fF/µm²	≈ 1 fF/µm²	≈ 2 fF/µm²	≈ 4.2 fF/µm²
Density	≈ 100 % (Filled with meshes)	< 90 %	< 70 %	< 20 %
Capacitance per 1mm²	Mesh #1: 0.18 nF/mm² / Mesh #2: 0.25 nF/mm²	0.9 nF/mm²	1.4 nF/mm²	0.84 nF/mm²
Area overhead	No area-overhead	All metal and device layers occupied	Top 2 metal layers occupied	M1 and device layers occupied

- Power noise suppression and SC leakage mitigation

Peak to peak AC variation



EM SC leakage (t-test)



4. Conclusion

Two techniques which can be applied to SI/PI problem and security (SC leakage) problem

- On-chip IR drop evaluation technique
  - Technique for detailed analysis of power supply noise
- IR-drop suppression using packaging technique
  - Suppressed dynamic IR drops in 60.4% and 14x increase in #EM traces for t-value > 4.5

This work has been supported by JSPS KAKENHI Grant No. JP22H04999 and by SECOM Science and Technology Foundation.

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