

# Integrating Biological and Artificial Neural Networks Processing on FPGAs



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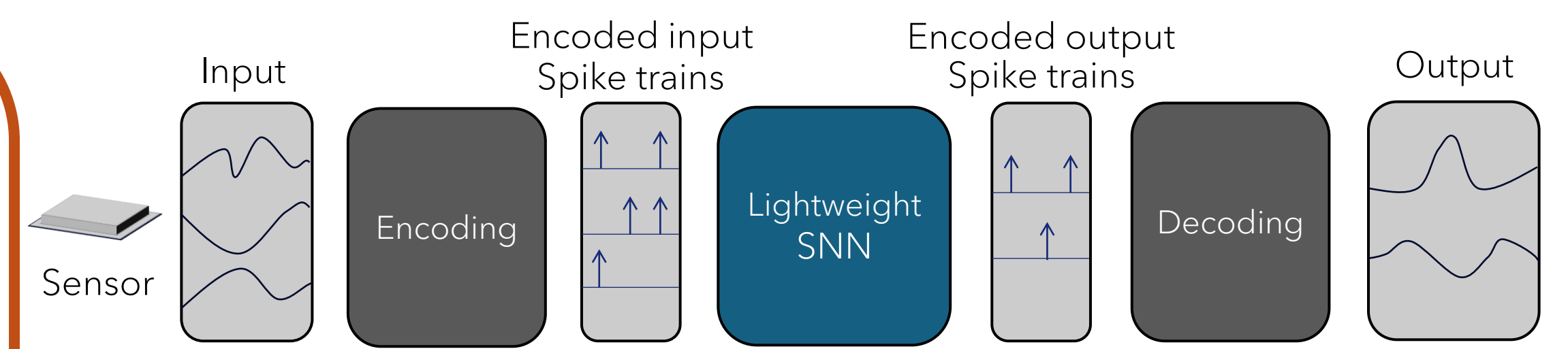
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**INTRODUCTION.** Neural interfaces are rapidly gaining momentum in the current bioengineering landscape, due to new sensing technology and AI capable of extracting neural activity information.

Nevertheless, these instruments pose significant requirements in terms of processing capabilities, especially when focusing on embedded implementations.

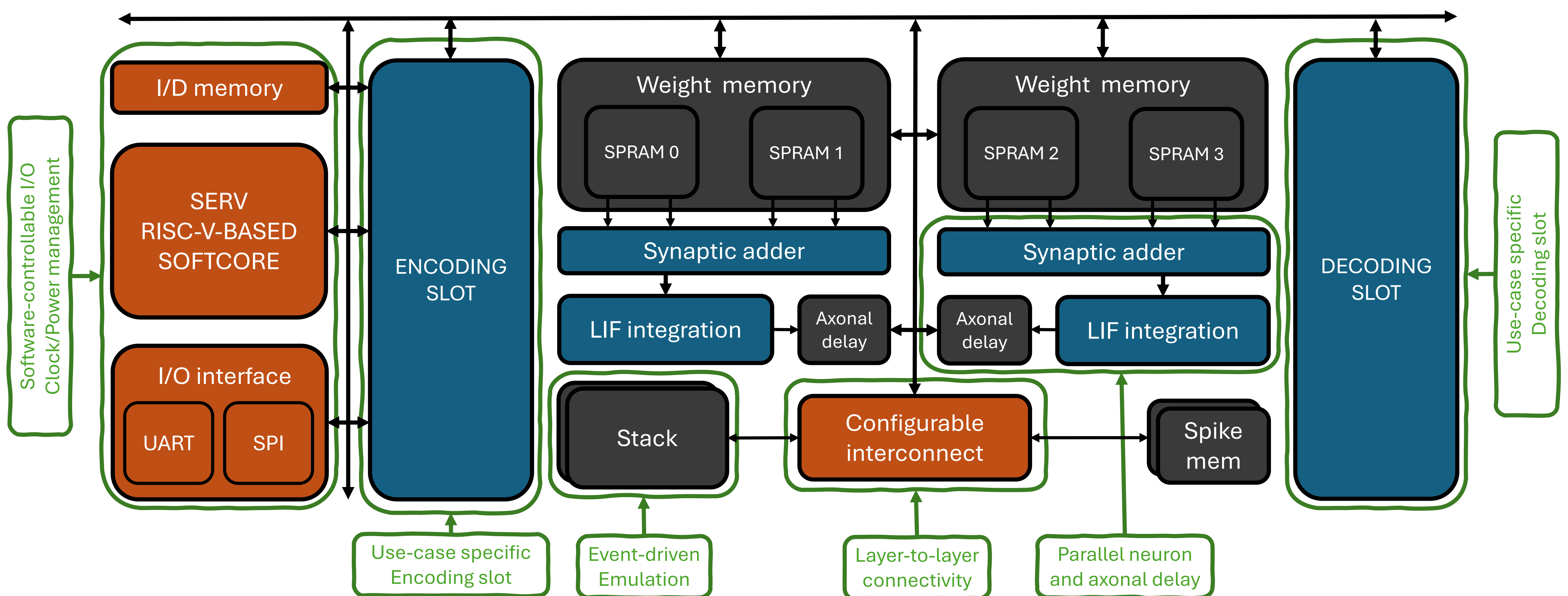
Thus, a promising technology serving as a substrate is represented by FPGAs, that enable the use of configurable logic, organizable memory blocks, and parallel DSPs.



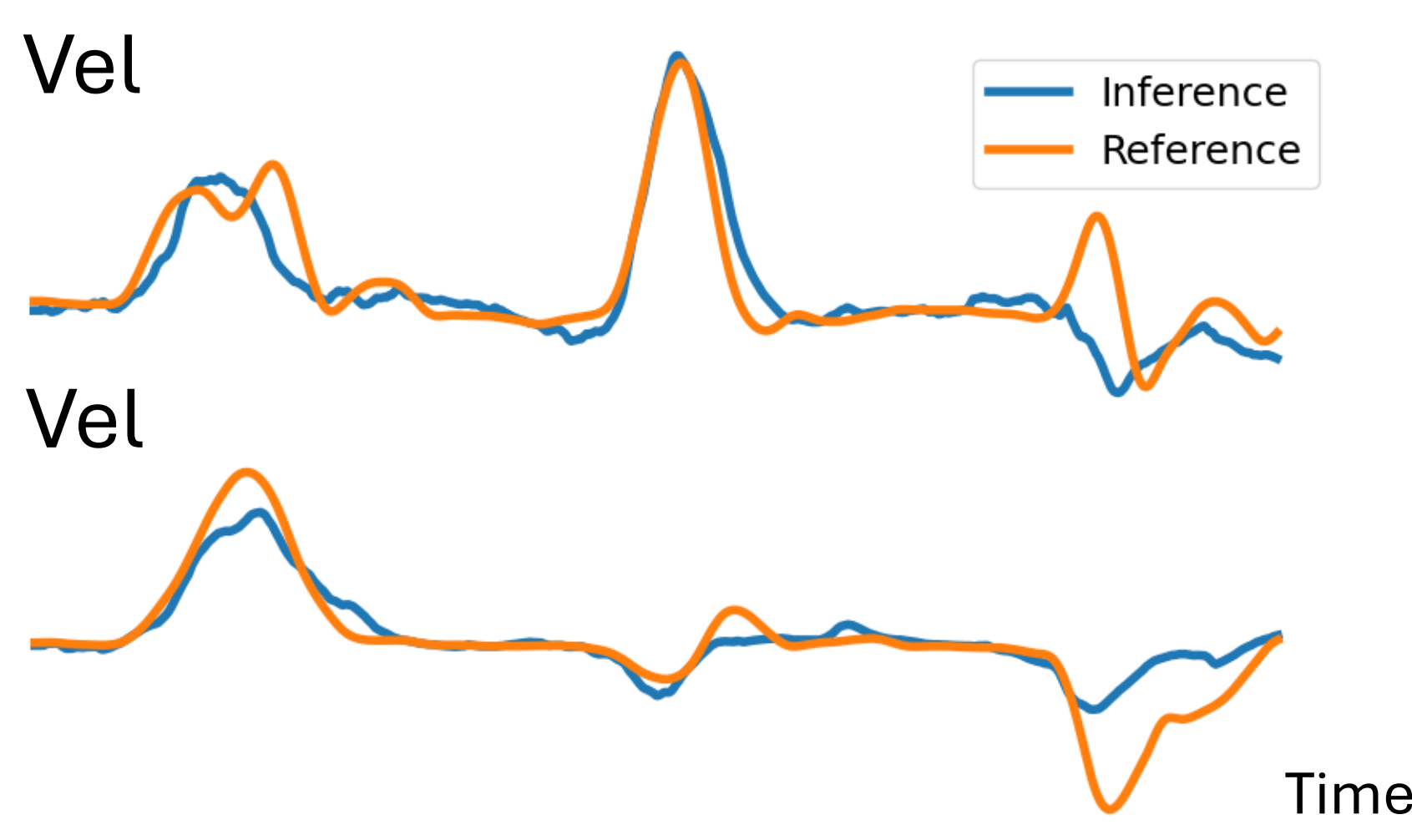
**SNNs** algorithms process spike-encoded events, enabling workload modulation on an as-needed basis and fostering low power consumption.



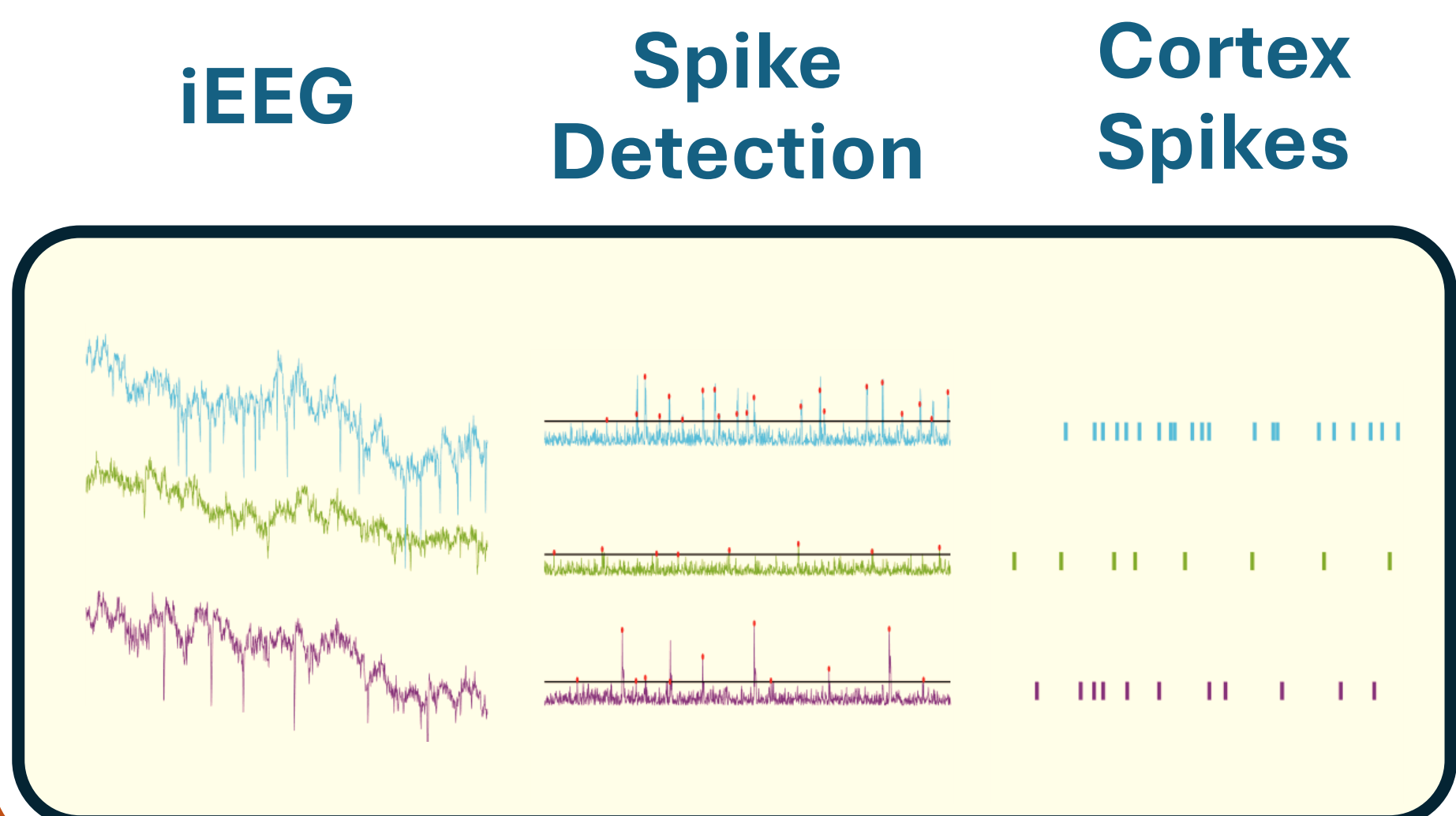
**ARCHITECTURE.** We propose a configurable architecture that can be implemented on top of Lattice ICE40UP5K FPGA for low-power applications, or on XILINX Artix-7/Zynq FPGAs for high-performance and/or high-resolution tasks. The system has proved to be extremely low-power and versatile, operating across various use cases by adapting its encoding and decoding slots. It demonstrates SoA power consumption and accuracy, when the application allows the use of lightweight SNN models.



**iEEG Hand Motion Tracking.** During a reach task, the hand movements and the neural activity of a macaque monkey were recorded [1].



**Encoding.** The raw 96-channel neural signal is filtered, rectified, and compared to a mean-based adaptive threshold to detect spikes in the motor cortex.



**Training.** SNNs consisting of dense layers of LIF neurons were trained using the MSE between the potential of the last layer neurons and the target variables as loss function.

INPUT	L1	L2	L3	L4
96	64	128	64	5
LEARNING RATE		BATCH		
1e-3		1		
SPARSITY		PLATFORM		
82%		SLAYER		

**Scaling on**

	96	128	1k	2k	4k
<b>INPUT</b>	96	128	1k	2k	4k
<b>LUT</b>	4.5k	15k	21k	28k	42k
<b>REG</b>	4.5k	16k	22k	29k	43k
<b>DSP</b>	2	28	77	133	240
<b>BRAM</b>	24	23	48	76	133

**Other applications**

“sEMG-based Gesture Recognition with Spiking Neural Networks on Low-power FPGA”, DASIP 2024.

“On-FPGA Spiking Neural Networks for Integrated Near-Sensor ECG Analysis”, DATE 2024.

**SoA Comparison**

Work	Model	Device	Acc	Power
<b>Our</b>	SNN	Lattice	0.84	<b>8 mw</b>
<b>Our [2]</b>	SNN	Xilinx	0.84	56 mw
[3]	QRNN	PC	0.84	N/A
[4]	RNN	PC	0.91	N/A

[1] Brochier, Thomas, et al. "Massively parallel recordings in macaque motor cortex during an instructed delayed reach-to-grasp task." Scientific data 5.1 (2018): 1-23.  
 [2] Leone, Gianluca, et al. "On-FPGA Spiking Neural Networks for Multi-variable End-to-End Neural Decoding." International Symposium on Applied Reconfigurable Computing. Cham: Springer Nature Switzerland, 2023.  
 [3] Nur Ahmadi, Timothy G Constantinou, and Christos-Savvas Bouganis. "Robust and accurate decoding of hand kinematics from entire spiking activity using deep learning". In: Journal of Neural Engineering 18.2 (2021), p. 026011.  
 [4] Shih-Hung Yang, Jyun-We Huang, Chun-Jui Huang, Po-Hsiung Chiu, Hsinyi Lai, and You-Yin Chen. "Selection of essential neural activity timesteps for intracortical brain-computer interface based on recurrent neural network". In: Sensors 21.19 (2021), p. 6372.